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W83L784R/W83L784G
Winbond H/W
Monitoring IC

Publication Release Date: Jan. 2005

W83L784R
Data Sheet Revision History

	PAGES	DATES	VERSION	VERSION ON WEB	MAIN CONTENTS
1	n.a.			n.a.	All the versions before 0.50 are for internal use.
2	n.a.	4/99	0.5	n.a.	First publication.
3	P.56-57	6/99	0.52	n.a.	Schematics updated
4	P.56	6/99	0.53	n.a.	Corrected the length (D) from 10.2mm to 7.2mm in the package outline table.
5	P.57	9/99	0.54	n.a.	Updated V0.5 schematics adding pull-high resistors for RESET# (pin15)
6	P.36 P. 9	10/99	0.55	n.a.	This update is for **C version** IC. Update CR [54h] register for PWMOUT function. Change Pin 15 from output to open-drain.
7	n.a.	4/02	1.0	1.0	Change version and version on web site to 1.0
8	n.a.	4/06	1.1	1.1	Add lead-free package version

LIFE SUPPORT APPLICATIONS

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Table of Contents-

1. GENERAL DESCRIPTION

W83L784R/G is an evolving product of W83782D/G --- Winbond's most popular hardware status monitoring IC. Specifically designed for the Notebook system, W83L784R/G can be used to monitor several critical hardware parameters of the system, including power supply voltages, fan speeds, and temperatures, which are very important for a high-end Notebook system to work stably and properly.

An 8-bit analog-to-digital converter (ADC) is built inside W83L784R/G. The W83L784R/G can monitor 4 analog voltage inputs, 2 fan tachometer inputs, one on-chip internal temperature sensor and 2 remote temperature sensors. The remote temperature sensing can be performed by thermistors, or 2N3904 NPN-type transistors, or directly from Intel™ Deschutes CPU thermal diode output. The W83L784R/G provides 2 PWM (pulse width modulation) outputs for the fan speed control to support the **"** Thermal Cruise™ **"** system, which can maintain the CPU or system in the specific programmable temperature under the hardware control. Another Fan speed control mode is **"**Speed Cruise**"** to keep the fan operating in the specific RPM. On the other hand, the W83L784R/G provides low active outputs such as fan fault and Battery low which could issue the hardware warning signals when the fan speed or battery voltage drop out of the preset range. Also the W83L784R/G provides power good reset for 3V and 5V; power down mode for power saving; fault pin for necessary H/W shutdown control; SMI#, OVT#, GPO# signals for system protection events; I^2C™ serial bus interface.

Through the application software or BIOS, the users can read all the monitored parameters of system from time to time. And a pop-up warning can be also activated when the monitored item was out of the proper/preset range. The application software could be Winbond's Hardware Doctor™, or Intel™ LDCM (LanDesk Client Management), or other management application software. Also the users can set up the upper and lower limits (alarm thresholds) of these monitored parameters and to activate one programmable and maskable interrupts. For the spacing saving consideration of the Notebook system, W83L784R/G is in the package of 209mil 20pins-SSOP.

2. FEATURES

2.1 Monitoring Items

- 2 thermal inputs from remote thermistors or 2N3904 NPN-type transistors or Pentium™ II (Deschutes) thermal diode output
- One on-chip temperature detection
- 4 voltage inputs
  --- typical for Vcore, +3.3V, +5V, Battery
- 2 sets of fan speed control and fan speed monitoring input
- WATCHDOG comparison of all monitored values
- Programmable hysteresis and setting points (alarm thresholds) for all monitored items

2.2 Actions Enabling

- Issue fan fault signal as fans are abnomally stopped
- Issue battery low signal as bettery voltage is abnomally out of range
- 2 PWM (pulse width modulation) outputs for fan speed control to support " Thermal Cruise™ " or " Speed Cruise™ "

--- Automatically maintain the CPU or system in the specific temperature or keep the fans in the specific speed under the H/W control

- Issue SMI#, OVT#, GPO to activate system protection
- PWR_DN# setting for the Power down mode
- Warning signal pop-up in application software

2.3 Power Good

- Issue RESET# outputs as the Power Good signal when 3V and 5V rise across a reset threshold.

2.4 General

- I^2C™ serial bus interface
- Intel™ LDCM (DMI driver 2.0) support
- Acer™ ADM (DMI driver 2.0) support
- Winbond hardware monitoring application software (Hardware Doctor™) support, for both Windows 95/98
- Meet WfM 2.0 (Wired for Management) spec.
- 5V Vcc operation

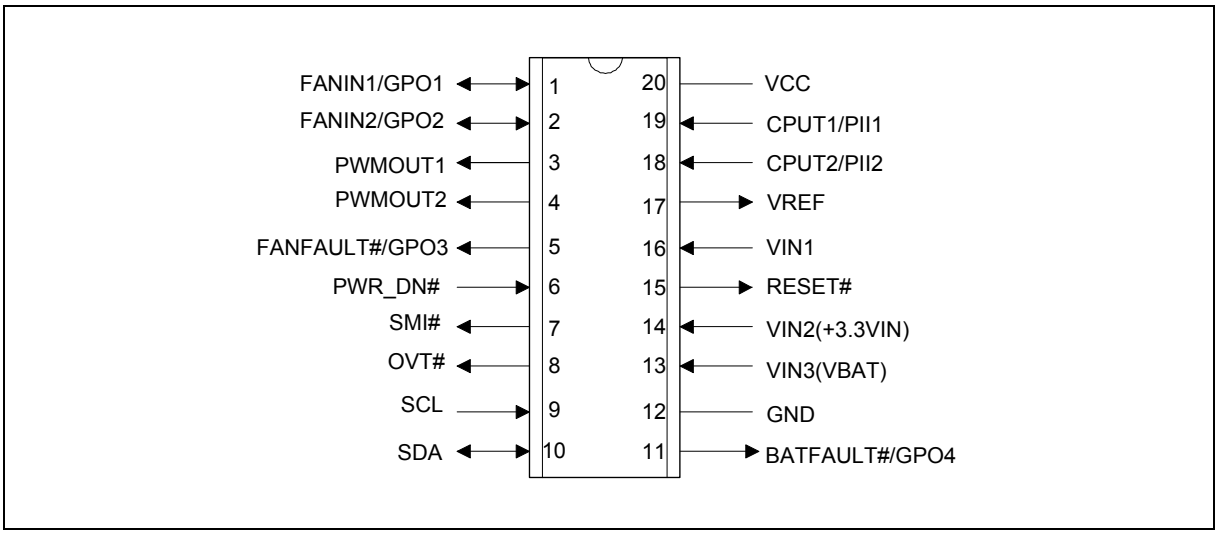
2.5 Package

- 20-pin SSOP (209mil)

3. KEY SPECIFICATIONS

• Voltage monitoring accuracy		±1% (Max)
• Monitoring Temperature Range and Accuracy	- 40°C to +120°C	± 3°C(Max)
• Supply Voltage		5V
• Operating Supply Current		2 mA typ.
• Power Down Suppy Current		0.5 mA typ.
• ADC Resolution		8 Bits

4. PIN CONFIGURATION



5. PIN DESCRIPTION

I/O_{12t} - TTL level bi-directional pin with 12 mA source-sink capability

I/O_{12ts} - TTL level and schmitt trigger

OUT_{12} - Output pin with 12 mA source-sink capability

AOUT - Output pin(Analog)

OD_{12} - Open-drain output pin with 12 mA sink capability

IN_t - TTL level input pin

IN_{ts} - TTL level input pin and schmitt trigger

AIN - Input pin(Analog)

PIN NAME	PIN NO.	TYPE	DESCRIPTION
FANIN1 / GPO1	1	IN_{ts} / OUT_{12}	0V to +5V amplitude fan tachometer input. (Default) / General purpose output. This multi-functional pin is programmable.
FANIN2 / GPO2	2	IN_{ts} / OUT_{12}	0V to +5V amplitude fan tachometer input. (Default) / General purpose output. This multi-functional pin is programmable.
PWMOUT1	3	OD_{12} / OUT_{12}	Fan speed control PWM output. This pin is **default** open-drain. It can be programmed as an output pin which can drive a HIGH or a LOW.
PWMOUT2	4	OD_{12} / OUT_{12}	Fan speed control PWM output. This pin is **default** open-drain. It can be programmed as an output pin which can drive a HIGH or a LOW.
FANFAULT# / GPO3	5	OD_{12}	Active-Low output. This pin will be a logic LOW when fan1 or fan2 is abnormally stopped. (Default) / General purpose output. This multi-functional pin is programmable.
PWR_DN#	6	IN_t	Power down input. When set this pin LOW, all output pins would be tristate except the pin15 RESET# which will keep HIGH.
SMI#	7	OD_{12}	System Management Interrupt.
OVT#	8	OD_{12}	Over temperature Shutdown Output.
SCL	9	IN_{ts}	Serial Bus Clock.
SDA	10	OD_{12}	Serial Bus bi-directional Data.
BATFAULT# / GPO4	11	OD_{12}	Active-Low output. This pin will be a logic LOW when Battery abnormally drops below the low limit or above the high limit. (Default) / General purpose output. This multi-functional pin is programmable.
GND	12	Ground	Ground.
VIN3(VBAT)	13	AIN	0V to 4.096V FSR Analog Inputs. (This pin should be connected to DC BATTERY. If this voltage is above 4.096V, it should be reduced with the external resistors so that the input voltage will be under 4.096V)

PIN DESCRIPTION, continued.

PIN NAME	PIN NO.	TYPE	DESCRIPTION
VIN2(+3.3VIN)	14	AIN	0V to 4.096V FSR Analog Inputs. (This pin should be connected to 3VCC)
RESET#	15	OD_{12}	Active-Low reset output. RESET# remains LOW while the 5VCC and +3.3V are below the reset threshold. It remains LOW for 200ms after the reset condition is terminated.
VIN1(VCORE)	16	AIN	0V to 4.096V FSR Analog Inputs.
VREF	17	AOUT	Reference Voltage.
CPUT2 / PII2	18	AIN	Thermistor terminal input.(Default) / Pentium™ II diode input. This multi-functional pin is programmable.
CPUT1 / PII1	19	AIN	Thermistor terminal input.(Default) / Pentium™ II diode input. This multi-functional pin is programmable.
VCC	20	POWER	+5VCC power supply input.

6. FUNCTIONAL DESCRIPTION

6.1 General Description

The W83L784R/G provides at most 4 analog positive inputs, 2 fan speed monitors, 2 sets for fan PWM (Pulse Width Modulation) Smart Fan Control , 2 remote thermal inputs from remote thermistors or 2N3904 transistors or Pentium™ II (Deschutes) thermal diode outputs and one on-chip thermal detection. W83L784R/G also provides the power good (reset) output for 3V and 5V power detection and two fault output pins issuing hardware warning if battery and fans become abnormal. When starting the monitor function on the chip, the watch dog machine monitor every function and store the value to registers. If the monitor value exceeds the limit value, the interrupt status will be set to 1.

6.2 Access Interface

The W83L784R/G provides I^2C Serial Bus to read/write internal registers. In the W83L784R/G there are three serial bus addresses. The first address defined at CR [4Ah] can read/write all registers excluding CPUT1/CPUT2 temperature sensor registers and its address default value is 0101101. The address for CPUT1 defined at CR [4Bh] bit2-0 only read/write CPUT1 temperature sensor registers and the address default value is 1001001. The address for CPUT2 defined at CR [4Bh] bit2-0 only read/write CPUT1 temperature sensor registers and the address default value is 1001000.

6.2.1 The first serial bus access timing is shown as follows:

(a) Serial bus write to internal address register followed by the data byte

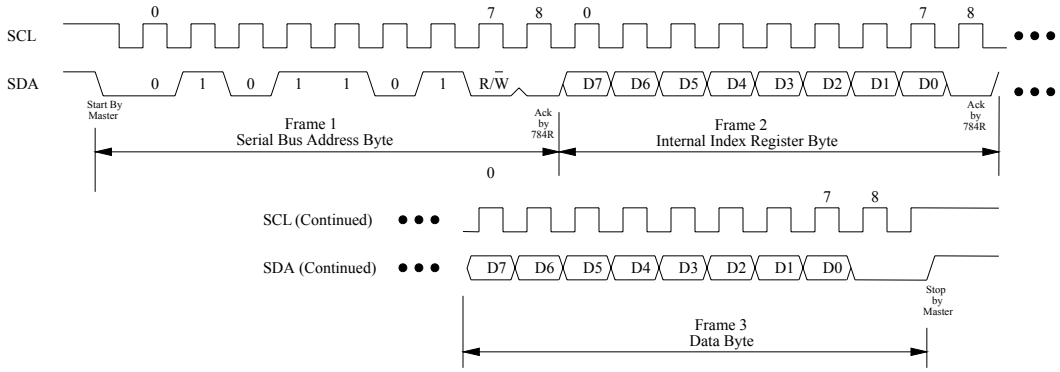


Figure 1. Serial Bus Write to Internal Address Register followed by the Data Byte

(b) Serial bus write to internal address register only

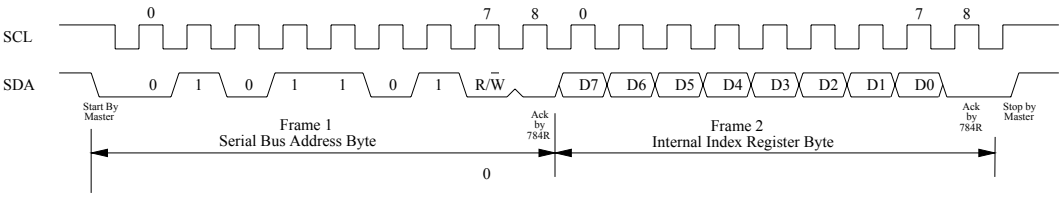


Figure 2. Serial Bus Write to Internal Address Register Only

(c) Serial bus read from a register with the internal address register prefer to desired location

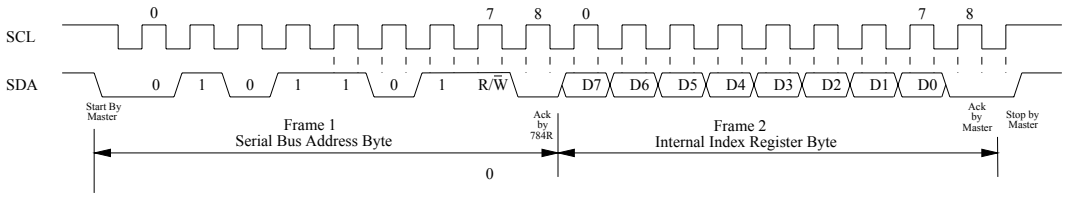


Figure 3. Serial Bus Read from Internal Address Register

6.2.2 The serial bus timing of the temperature CPUT1 and CPUT2 is shown as follow:

(a) Typical 2-byte read from preset pointer location (Temp, T_{OS}, T_{HYST})

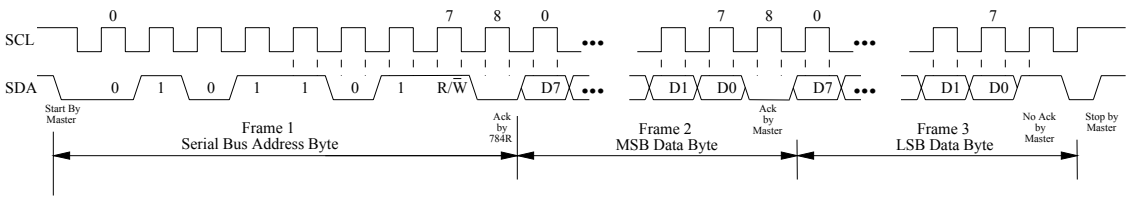


Figure 4. Typical 2-Byte Read From Preset Pointer Location

(b)Typical pointer set followed by immediate read for 2-byte register (Temp, T_{OS}, T_{HYST})

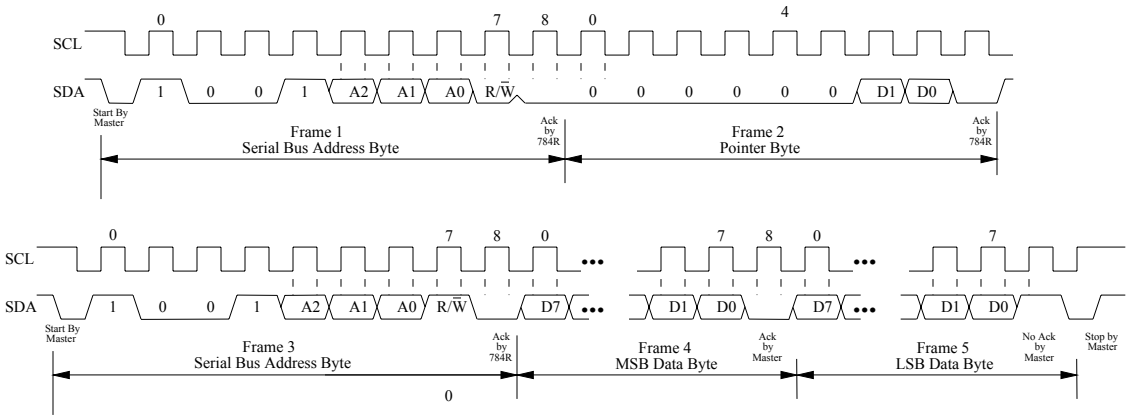


Figure 5. Typical Pointer Set Followed by Immediate Read for 2-Byte Register

(c) Typical read 1-byte from configuration register with preset pointer

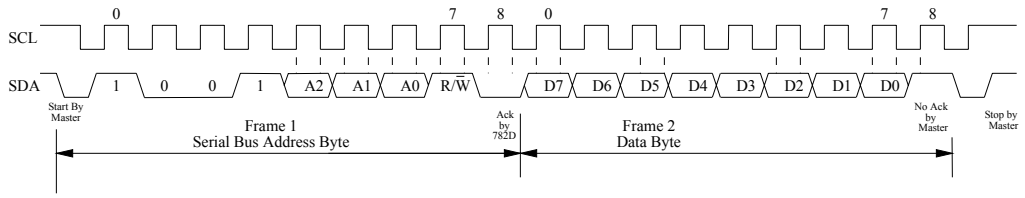


Figure 6. Typical 1-Byte Read From Configuration With Preset Pointer

(d) Typical pointer set followed by immediate read from configuration register

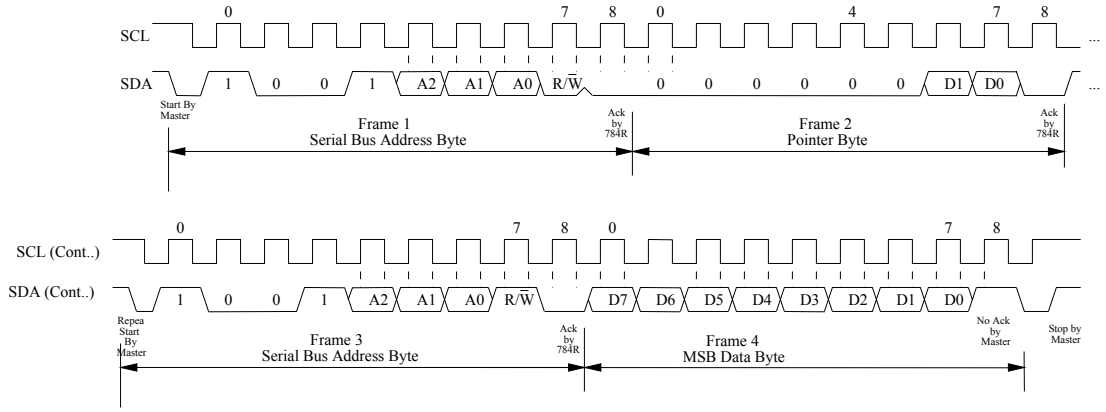


Figure 7. Typical Pointor Set Followed by Immediate Read from Temp 2/3 Configuration Register

(e) Temperature configuration register Write

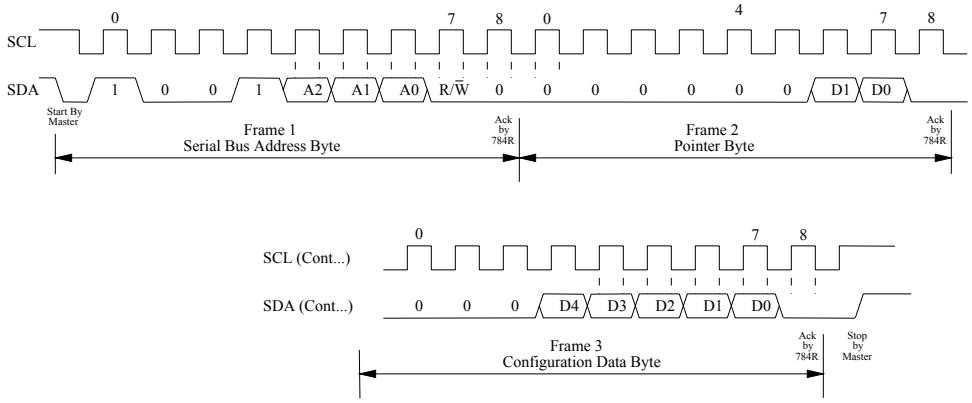


Figure 8. Configuration Register Write

(f) Temperature T_{OS} and T_{HYST} write

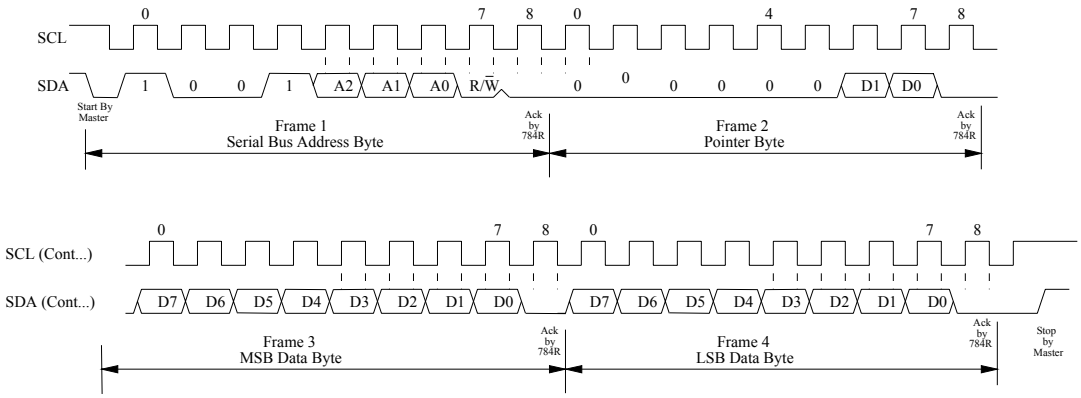


Figure 9. Configuration Register Write

6.3 Analog Inputs

The maximum input voltage of the analog pin is 4.096V because the 8-bit ADC has a 16mv LSB. Really, the application of the PC monitoring would most often be connected to power suppliers. The CPU V-core voltage and +3.3V voltage can directly connected to these analog inputs. The 5VSB and battery inputs should be reduced a factor with external resistors so as to obtain the input range. As Figure 10 shows.

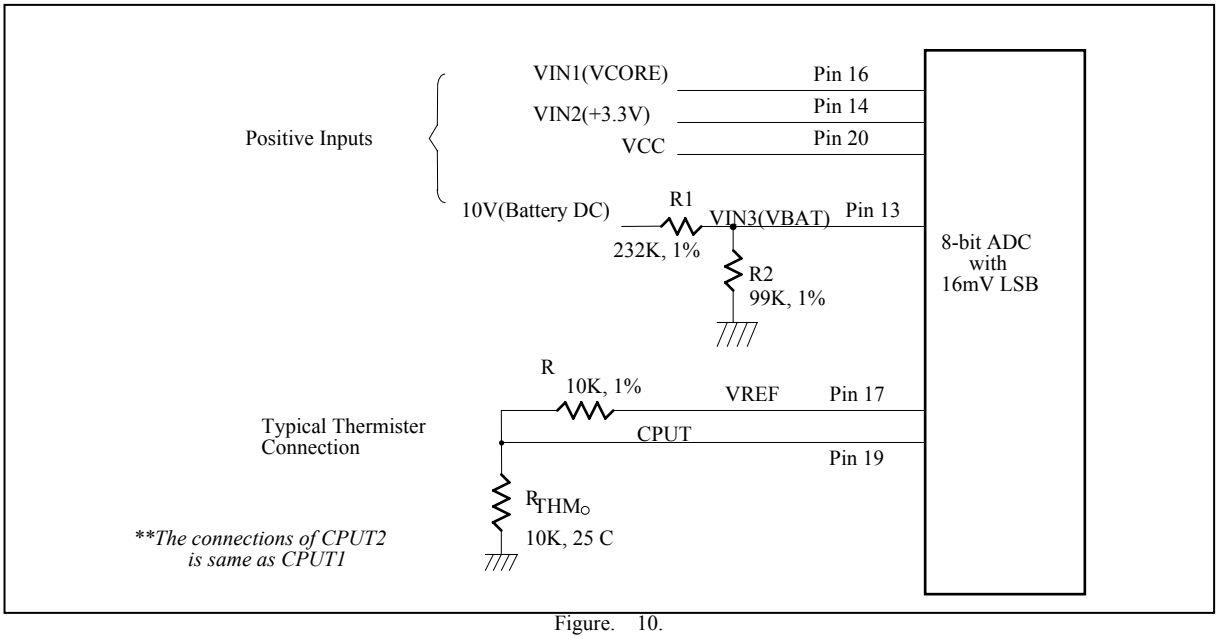


Figure. 10.

6.3.1 Monitor over 4.096V voltage:

The input voltage VIN3 can be expressed as following equation.

$$VIN3 = V_{BAT-DC} \times \frac{R_2}{R_1 + R_2}$$

The value of R1 and R2 can be selected to 232K Ohms and 99K Ohms, respectively, when the input voltage V_{BAT-DC} is 10V. The node voltage of VIN3 can be subject to less than 4.096V for the maximum input range of the 8-bit ADC. The pin 24 is connected to the power supply VCC with +5V. There are two functions in this pin with 5V. The first function is to supply internal analog power in the W83L784R and the second function is that this voltage with 5V is connected to internal serial resistors to monitor the +5V voltage. The values of two serial resistors are 34K ohms and 50K ohms so that input voltage to ADC is 2.98V which is less than 4.096V of ADC maximum input voltage. The express equation can represent as follows.

$$V_{in} = VCC \times \frac{50K\Omega}{50K\Omega + 34K\Omega} \cong 2.98V$$

where VCC is set to 5V

6.3.2 Power good for 3V and 5V

On power up, once VCC (5V) reaches 1V, RESET# will be logic low. As 3V and VCC (5V) rise, RESET# remains asserted. If 3V and VCC (5V) both exceed the reset threshold, RESET becomes logic high after a time equal to the reset pulse width (tRST, typically 200ms). (Figure 11) If a power fail or a brownout happens (i.e. 3V or VCC (5V) drops below the threshold), RESET# output is asserted. As long as the 3V and VCC (5V) remain below the reset threshold, RESET# output remains asserted. Therefore, a brownout condition that interrupts a previously initiated reset pulse causes an additional 200ms delay from the time the latest interruption occurred. On power-on, once 3Vor VCC (5V) drops below the reset threshold, RESET# are guaranteed to be asserted for VCC ≥ 1V.

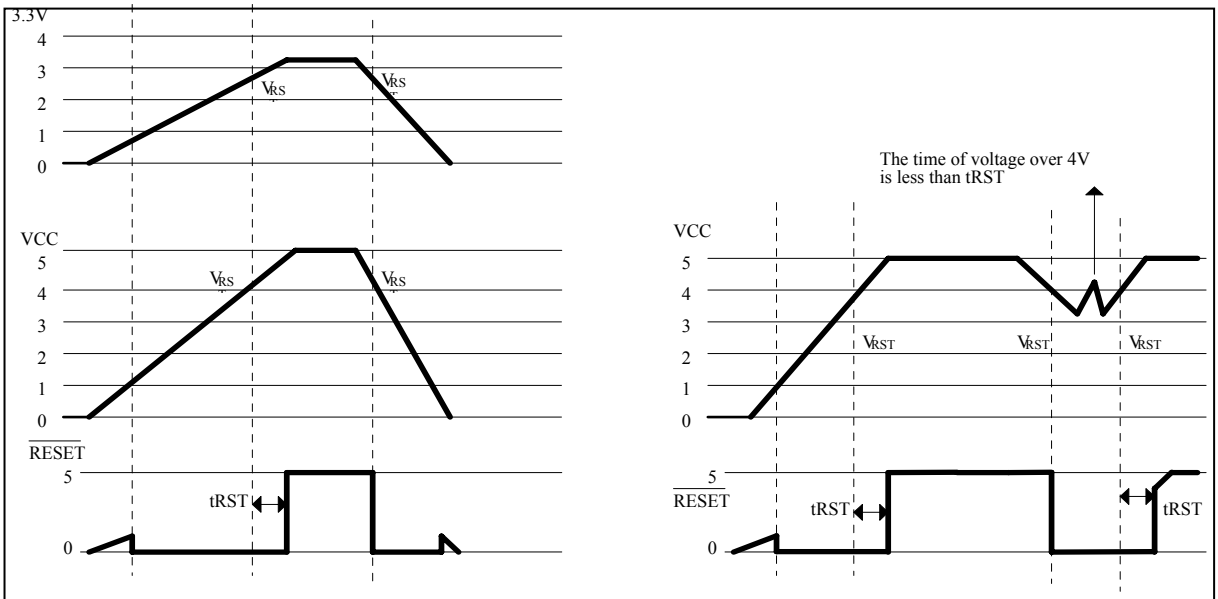


Figure 11

6.3.3 Battery Fault Alarm

W83L784R/G provides a good protection for DC battery. Set VIN3 to monitor DC battery voltage and enable VBAT fault function. When VIN3 (pin13) voltage exceeds high or low limit value, pin BATFAULT# will be asserted.

6.4 Temperature Measurement Machine

The temperature data format is 8-bit two-complement for internal sensor and 9-bit two -complement for sensor CPUT1 and CPUT2. The 8-bit temperature data can be obtained by reading the CR [27h]. The 9-bit temperature data (CPUT1 and CPUT2) can be obtained by reading CR [00h] of its serial bus address. The format of the temperature data is show in Table 1.

Table 1

TEMPERATURE	8-BIT DIGITAL OUTPUT		9-BIT DIGITAL OUTPUT	
	8-BIT BINARY	8-BIT HEX	9-BIT BINARY	9-BIT HEX
+125°C	0111,1101	7Dh	0,1111,1010	0FAh
+25°C	0001,1001	19h	0,0011,0010	032h
+1°C	0000,0001	01h	0,0000,0010	002h
+0.5°C	-	-	0,0000,0001	001h
+0°C	0000,0000	00h	0,0000,0000	000h
-0.5°C	-	-	1,1111,1111	1FFh
-1°C	1111,1111	FFh	1,1111,1110	1FFh
-25°C	1110,0111	E7h	1,1100,1110	1CEh
-55°C	1100,1001	C9h	1,1001,0010	192h

6.4.1 Monitor temperature from thermistor:

The W83L784R/G can connect three thermistors to measure three different envirment temperature. The specification of thermistor should be considered to (1) β value is 3435K, (2) resistor value is 10K ohms at 25°C. In the Figure 10, the themistor is connected by a serial resistor with 10K Ohms, and then connect to VREF (pin 17).

6.4.2 Monitor temperature from Pentium IITM thermal diode or bipolar transistor 2N3904

The W83L784R/G can alternate the thermistor to Pentium II™ (Deschutes) thermal diode interface or transistor 2N3904 and the circuit connection is shown as Figure 12. The pin of Pentium II™ D- is connected to power supply ground (GND) and the pin D+ is connected to pin PIIx in the W83L784R/G. The resistor R=30K ohms should be connected to VREF to supply the diode bias current and the bypass capacitor C=3300pF should be added to filter the high frequency noise. The transistor 2N3904 should be connected to a form with a diode, that is, the Base (B) and Collector (C) in the 2N3904 should be tied together to act as a thermal diode.

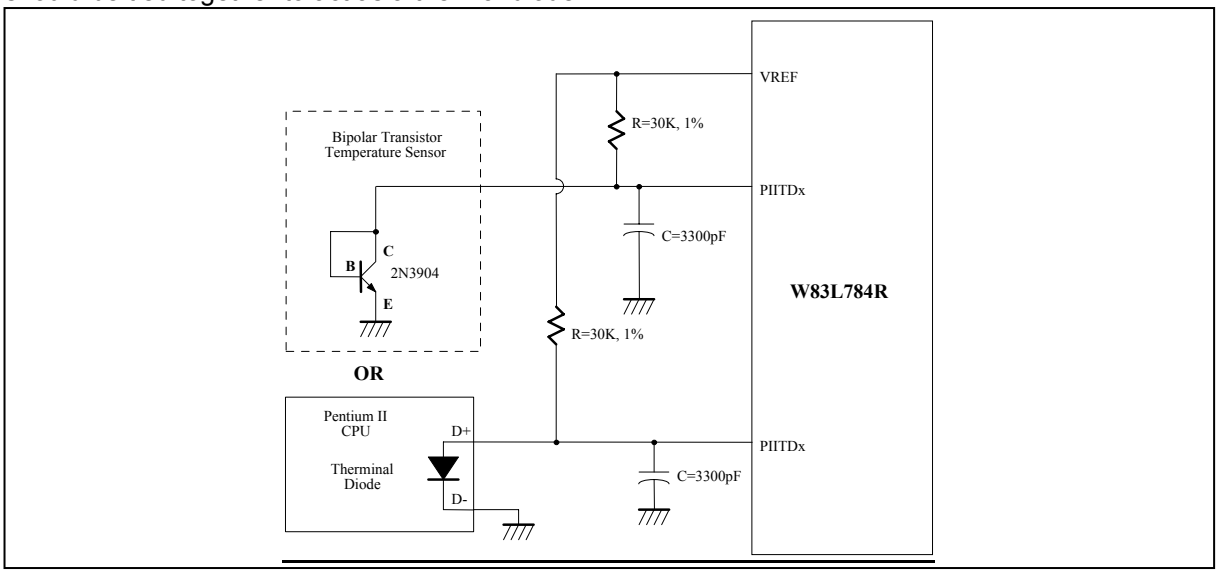


Figure 12

6.4.3 Over Temperature

W83L784R/G provides two external thermal sensors to detect temperature. When detected temperature exceeds the over-temperature value, pin OVT# will be asserted until the temperature goes below the hysteresis temperature. Pin OVT# has 3 operating modes.

6.4.3.1. ACPI Mode

At this mode, temperature exceeding one level of temperature separation, starting from 0 degree, causes the OVT# output activated. OVT# will be activated again once temperature exceeding the next level. OVT# output will act the same manner when temperature goes down. (Figure 13) The

granularity of temperature separation between each OVT# output signal can be programmed at Bank0 CR [4Fh].

The priority of this mode is higher than Comparator mode and Interrupt mode.

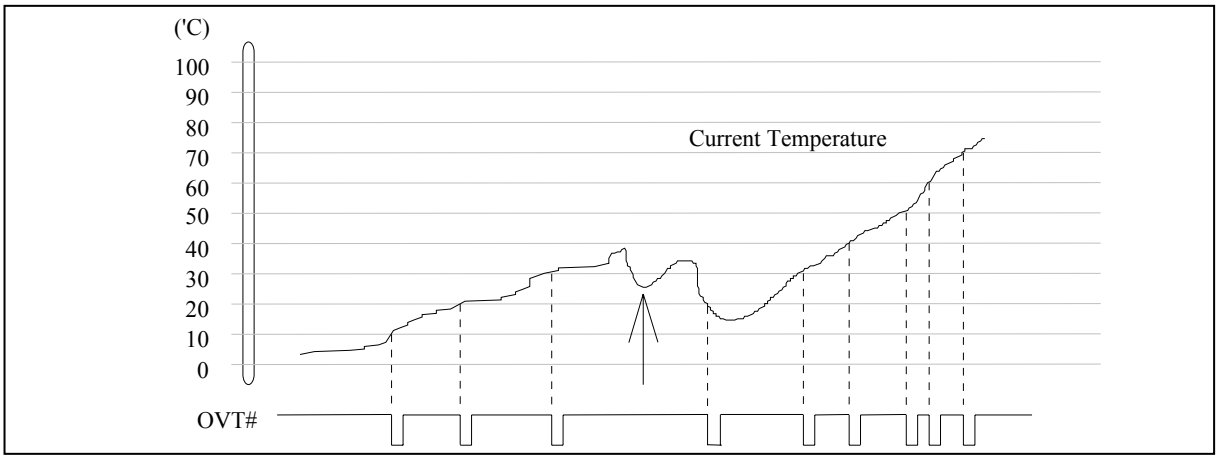


Figure 13

6.4.3.2. Comparator Mode

At this mode, temperature exceeding T_O causes the OVT# output activated until the temperature is less than T_{HYST}. (Figure 14)

6.4.3.3. Interrupt Mode

At this mode, temperature exceeding T_O causes the OVT# output activated indefinitely until reset by reading CPUT1 or CPUT2 registers. Temperature exceeding T_O, then OVT# asserted, and then temperature going below T_{HYST} will also cause the OVT# activated indefinitely until reset by reading temperature sensor2 or sensor 3 registers. Once the OVT# is activated by exceeding T_O, then reset, if the temperature remains above T_{HYST}, the OVT# will not be activated again.(Figure 14)

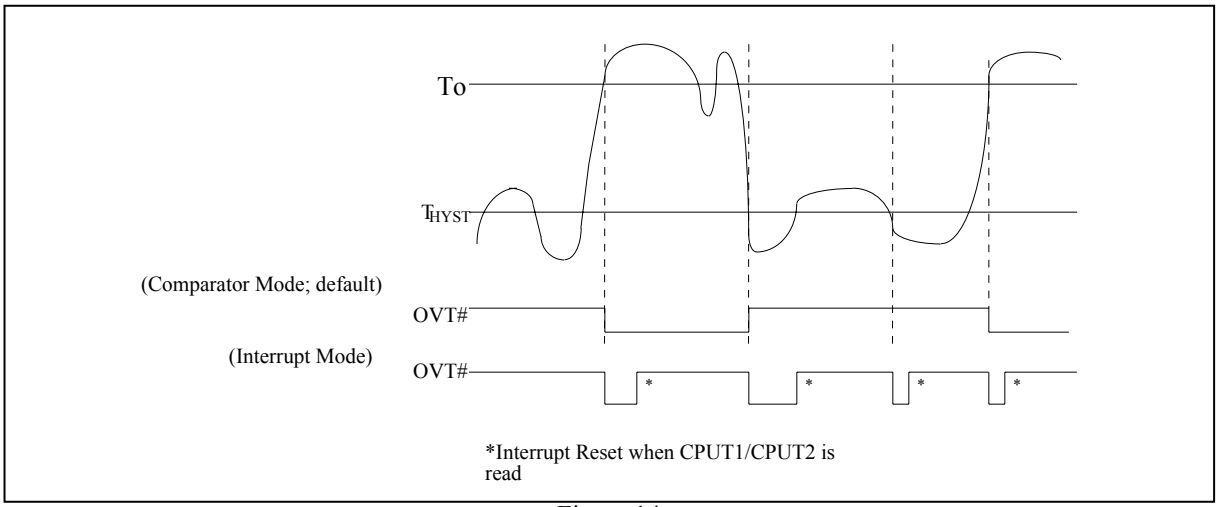


Figure 14

6.5 FAN Speed Count and FAN Speed Control

6.5.1 Fan speed count

Inputs are provides for signals from fans equipped with tachometer outputs. The level of these signals should be set to TTL level, and maximum input voltage can not be over +5.5V. If the input signals from the tachometer outputs are over the VCC, the external trimming circuit should be added to reduce the voltage to obtain the input specification. The normal circuit and trimming circuits are shown as Figure 15.

Determine the fan counter according to:

$$Count = \frac{1.35 \times 10^6}{RPM \times Divisor}$$

In other words, the fan speed counter has been read from register CR28 or CR29 or CR2A, the fan speed can be evaluated by the following equation.

$$RPM = \frac{1.35 \times 10^6}{Count \times Divisor}$$

The default divisor is 2 and defined at CR49.bit0~2, bit4~6 which are three bits for divisor. That provides very low speed fan counter such as power supply fan. The followed table is an example for the relation of divisor, PRM, and count.

Table 2

DIVISOR	NOMINAL PRM	TIME PER REVOLUTION	COUNTS	70% RPM	TIME FOR 70%
1	8800	6.82 ms	*153*	6160	9.74 ms
2 (default)	4400	13.64 ms	*153*	3080	19.48 ms
4	2200	27.27 ms	*153*	1540	38.96 ms
8	1100	54.54 ms	*153*	770	77.92 ms
16	550	109.08 ms	*153*	385	155.84 ms
32	275	218.16 ms	*153*	192	311.68 ms
64	137	436.32 ms	*153*	96	623.36 ms
128	68	872.64 ms	*153*	48	1246.72 ms

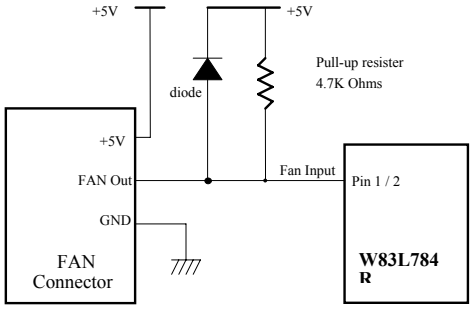


Figure 15-1. Fan with Tach Pull-Up to +5V

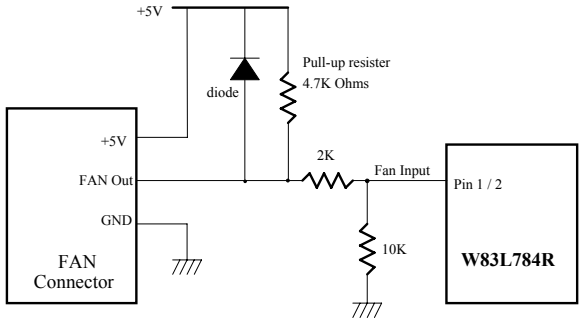


Figure 15-2. Fan with Tach Pull-Up to +5V, or Totem-Pole Output and Register Attenuator

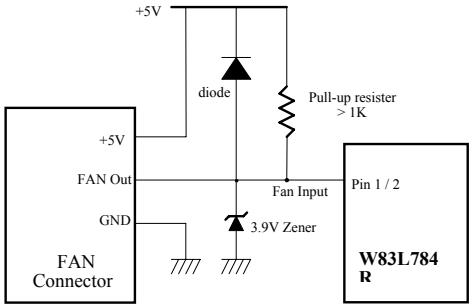


Figure 15-3. Fan with Tach Pull-Up to +5V and Zener Clamp

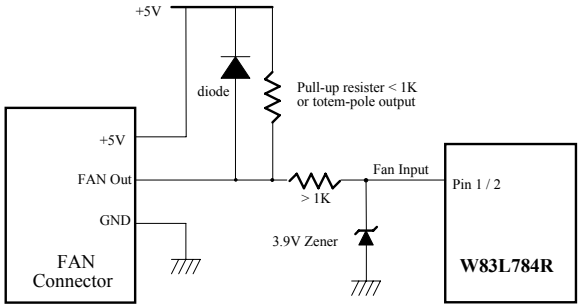


Figure 15-4. Fan with Tach Pull-Up to +5V, or Totem-Pole Putput and Zener Clamp

6.5.2 Fan speed control

The W83L784R/G provides four sets for fan PWM speed control. The duty cycle of PWM can be programmed by an 8-bit register which are defined in the Bank0 CR81h and CR83h. The default duty cycle is set to 100%, that is, the default 8-bit registers is set to FFh. The expression of duty can be represented as follows.

$$\text{Duty} - \text{cycle}(\%) = \frac{\text{Programmed 8 - bit Register Value}}{255} \times 100\%$$

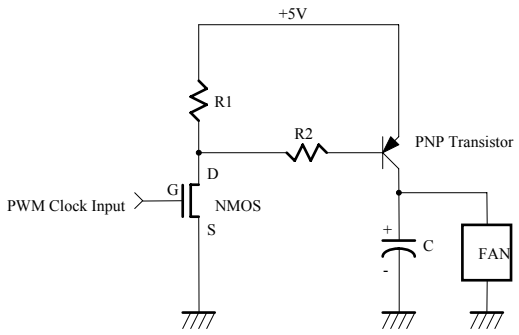


Figure 16

6.5.3 Smart Fan Control

Smart Fan Control provides two mechanisms. One is Thermal Cruise mode and the other is Fan Speed Cruise mode.

6.5.3.1. Thermal Cruise mode

At this mode, W83L784R/G provides the Smart Fan system which can control the fan speed automatically depend on current temperature to keep it with in a specific range. At first a wanted temperature and interval must be set (ex. 55 °C ± 3 °C) by BIOS, as long as the current temperature remains below the setting value, the fan will be off. Once the temperature exceeds the setting high limit temperature (58°C), the fan will be turned on with a specific speed set by BIOS (ex: 80% duty cycle) and automatically controlled its PWM duty cycle with the temperature varying. Three conditions may occur:

(1) If the temperature still exceeds the high limit (ex: 58°C), PWM duty cycle will increase slowly. If the fan has been operating in its fully speed but the temperature still exceeds the high limit (ex: 58°C), a warning message or a fan_fault signal(pin5) will be issued to protect the system.

(2) If the temperature goes below the high limit (ex: 58°C), but above the low limit (ex: 52°C), the fan speed will be fixed at the current speed because the temperature is in the target area (ex: 52 °C ~ 58°C).

(3) If the temperature goes below the low limit (ex: 52°C), PWM duty cycle will decrease slowly to 0 or a preset value until the temperature exceeds the low limit.

Figure 17 gives an illustration for Thermal Cruise Mode.

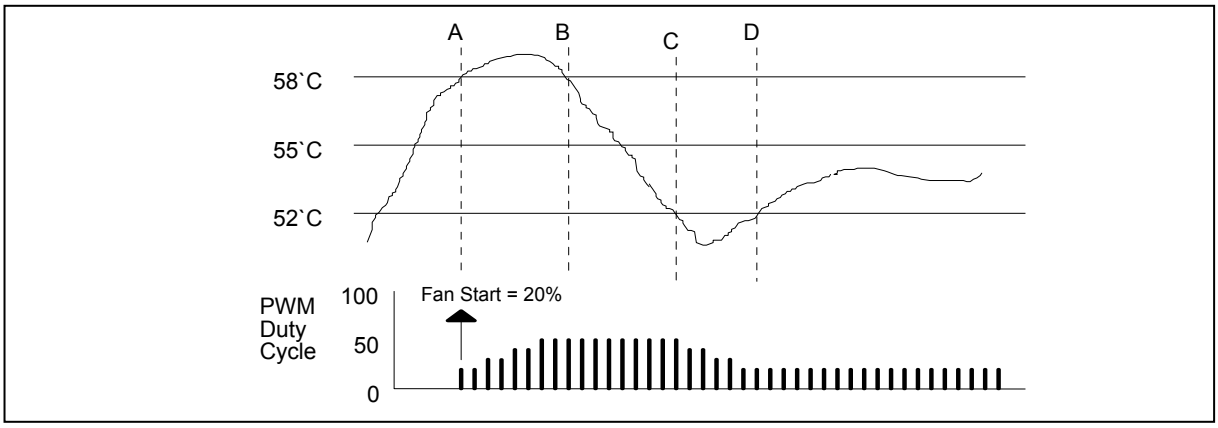


Figure 17-1

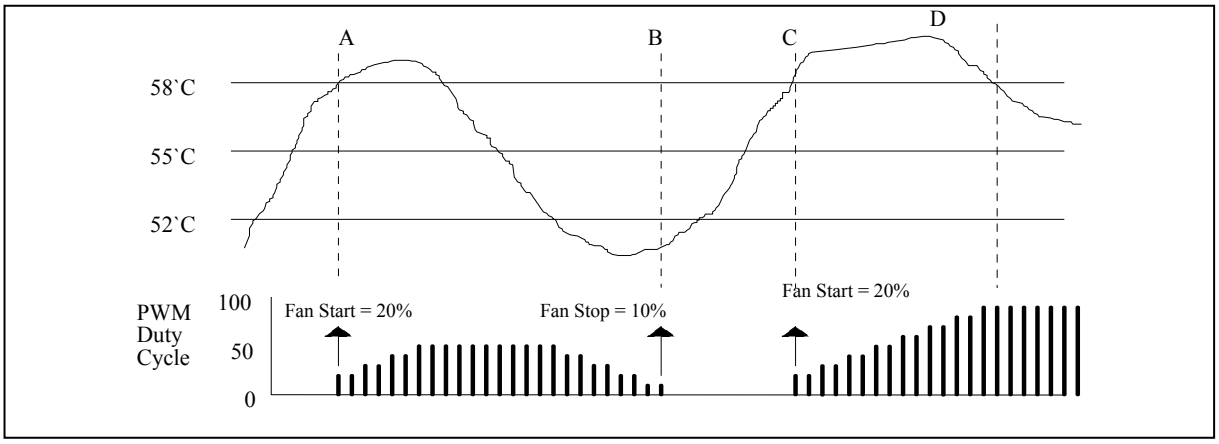


Figure 17-2

6.5.3.2. Fan Speed Cruise mode

At this mode, W83L784R/G provides the Smart Fan system which can control the fan speed automatically depend on current fan speed to keep it with in a specific range. A wanted fan speed count and interval must be set (ex. 160 ± 10) by BIOS. As long as the fan speed count is the specific range, PWM duty will keep the current value. If current fan speed count is higher than the high limit (ex. 160+10), PWM duty will be increased to keep the count less than the high limit. Otherwise, if current fan speed is less than the low limit (ex. 160-10), PWM duty will be decreased to keep the count higher than the low limit. See Figure 18 example.

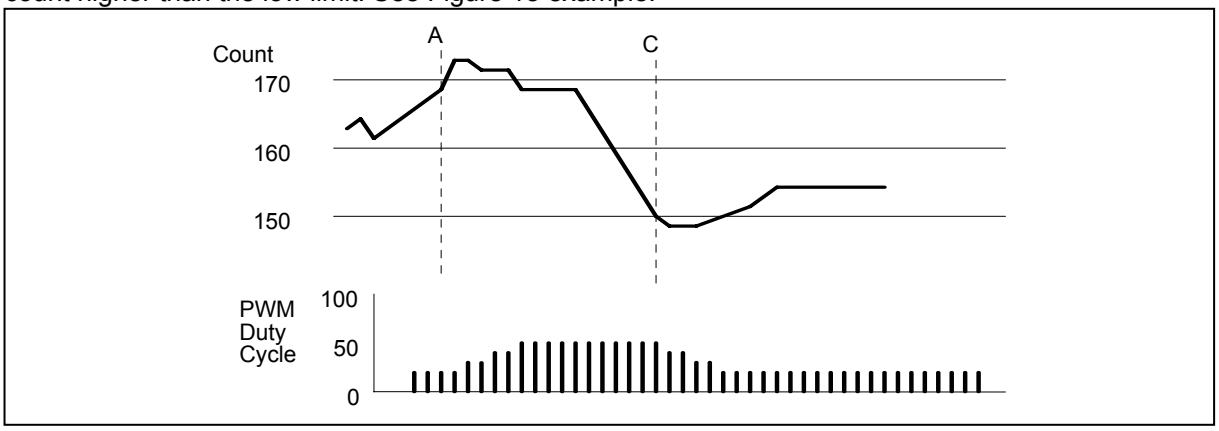


Figure 18

Of course, Smart Fan control system can be disabled and the fan speed control algorithm can be programmed by BIOS or application software.

6.5.4 Fan Fault Alarm

W83L784R/G can monitor fan speed by detecting fan speed counter value. When fan speed count is higher than high limit count value (CR58h) or less than low limit count value (CR59h), pin FANFAULT# is asserted.

6.6 SMI#

6.6.1 Temperature

Pin SMI# for temperature has 3 modes.

6.6.1.1. Comparator Interrupt Mode

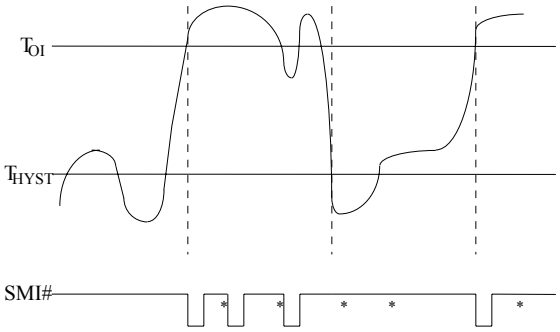
Temperature exceeding T_O causes an interrupt and this interrupt will be reset by reading all the Interrupt Status Registers. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will occur again when the next conversion has completed. If an interrupt event has occurred by exceeding T_O and not reset, the interrupts will not occur again. The interrupts will continue to occur in this manner until the temperature goes below T_{HYST}. (Figure 19-1)

6.6.1.2. Two-Times Interrupt Mode

Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will also cause an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. Once an interrupt event has occurred by exceeding T_O, then reset, if the temperature remains above the T_{HYST}, the interrupt will not occur. (Figure 19-2)

6.6.1.3. One-Time Interrupt Mode

Temperature exceeding T_O causes an interrupt and then temperature going below T_{HYST} will not cause an interrupt. Once an interrupt event has occurred by exceeding T_O, then going below T_{HYST}, an interrupt will not occur again until the temperature exceeding T_O. (Figure 19-3)



*Interrupt Reset when Interrupt Status Registers are read

Figure 19-1. Comparator Interrupt Mode

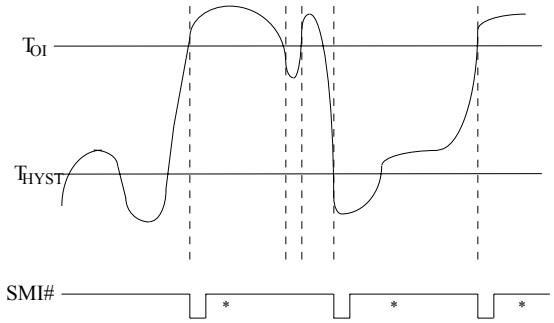
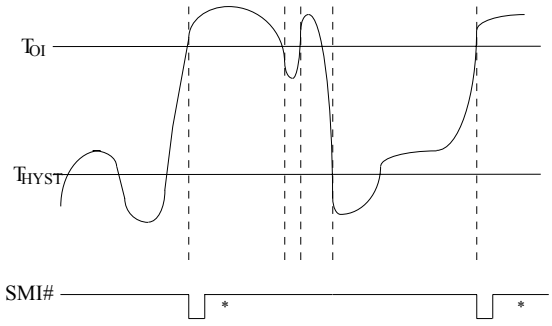


Figure 19-2. Two-Times Interrupt Mode



*Interrupt Reset when Interrupt Status Registers are read

Figure 19-3. One-Time Interrupt Mode

6.6.2 Voltage

SMI# interrupt for voltage is Two-Times Interrupt Mode. Voltage exceeding high limit or going below low limit will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 20-1)

6.6.3 Fan

SMI# interrupt for fan is Two-Times Interrupt Mode. Fan count exceeding the limit, or exceeding and then going below the limit (set at value ram index 3Bh and 3Ch) , will causes an interrupt if the previous interrupt has been reset by reading all the interrupt Status Register. (Figure 20-2)

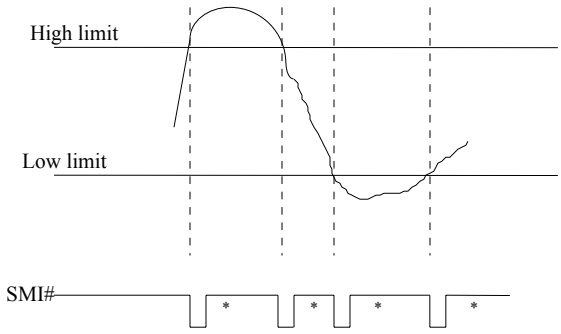


Figure 20-1. Voltage SMI# Mode

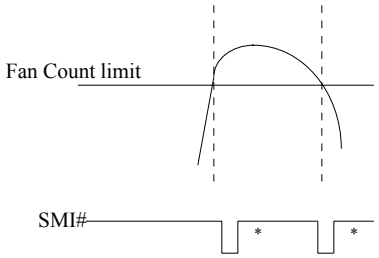


Figure 20-2. Fan SMI# Mode

*Interrupt Reset when Interrupt Status Registers are read