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Winbond
Mobile Keyboard and
Embedded Controller

W83L951DG
W83L951FG

Date: August/2006 Revision: 1.00

W83L951DG/W83L951FG Data Sheet Revision History

	PAGES	DATES	VERSION	WEB VERSION	MAIN CONTENTS
1	n.a.	8/7/2006	1.0	1.0	First Release
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winbond

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1. GENERAL DESCRIPTION

The Winbond mobile keyboard and embedded controller W83L951DG/FG architecture consists of a Turbo-8051 core logic controller and surrounded by various components, 2K+256 bytes of RAM, 64K on-chip FLASH, LPC host interface, 13 general purpose I/O port with 24 external interrupt source, 4 timers, 1 serial port, 2 SMBus interface for master mode, 3 PS/2 port, 2 PWM channels with 8-bits and 2 PWM channels with 16-bits, 2 D-A and 8 A-D converters, 1 Consumer Infrared Communications Receiver, 2 Fan Tachometer , 1 Real Time Clock Generator, and Matrix Interface. The part number with an affix of “G” is the Lead-free package product.

2. PRODUCT FEATURES

- Core logic

  8-bit Turbo 8052 Microprocessor Code based, Speed up to 24MHz

  256 bytes Internal RAM

  64K bytes Embedded Programmable Flash Memory

  2K bytes External SRAM

- Host interface

  Software Optional with LPC Interface

  Primary Programmable I/O Address Communication Port in LPC Mode

  Support SERIRQ in LPC Interface

  Support Hardware Fast Gate A20 and KBRST

  Support Port 92h

- SMBus

  Support 2 SMBus Interface support Master Mode.

- Timers

  Support Four Timer Signal with Three Pre-scalars

  Timer 1 and 2 Shard the Same Pre-scalar and are Free-Running Only.

  Timer X and Y Have Individual Pre-scalar and Support up to Four Control Modes, Free Running, Pulse Output, Event Counter and Pulse Width Measurement

- PWM

  Support Four PWM Channels

  PWM 0 and 1 are 8-bits and Programmable Frequency from 62Hz to 7.5 KHz

  PWM 2 and 3 are 16-bits and Programmable Frequency from 6Hz to 3MHz

- Fan Tachometer

  Support two Fan Tachometer Inputs

- A/D Converter

  Firmware Programmable Optional with 10-bite or 8-bit Resolution

  Support Eight Channels

- D/A Converter
  8-bit Resolution
  Support Two Channels

- PS2
  Support Three Hardware PS2 Channels
  Optional PS2 Clock Inhibit by Hardware or Firmware

- Keyboard Controller
  Support 16*8 Keyboard Matrix-scan, Expanding to 18*8 and 20*8

- GPIO
  Support 104 Useful GPIO Pins Totally and Bit–addressable to Facility Firmware Coding

- FLASH
  Support External On-Board 64K Flash via Matrix Interface (GP0, 1, 3)

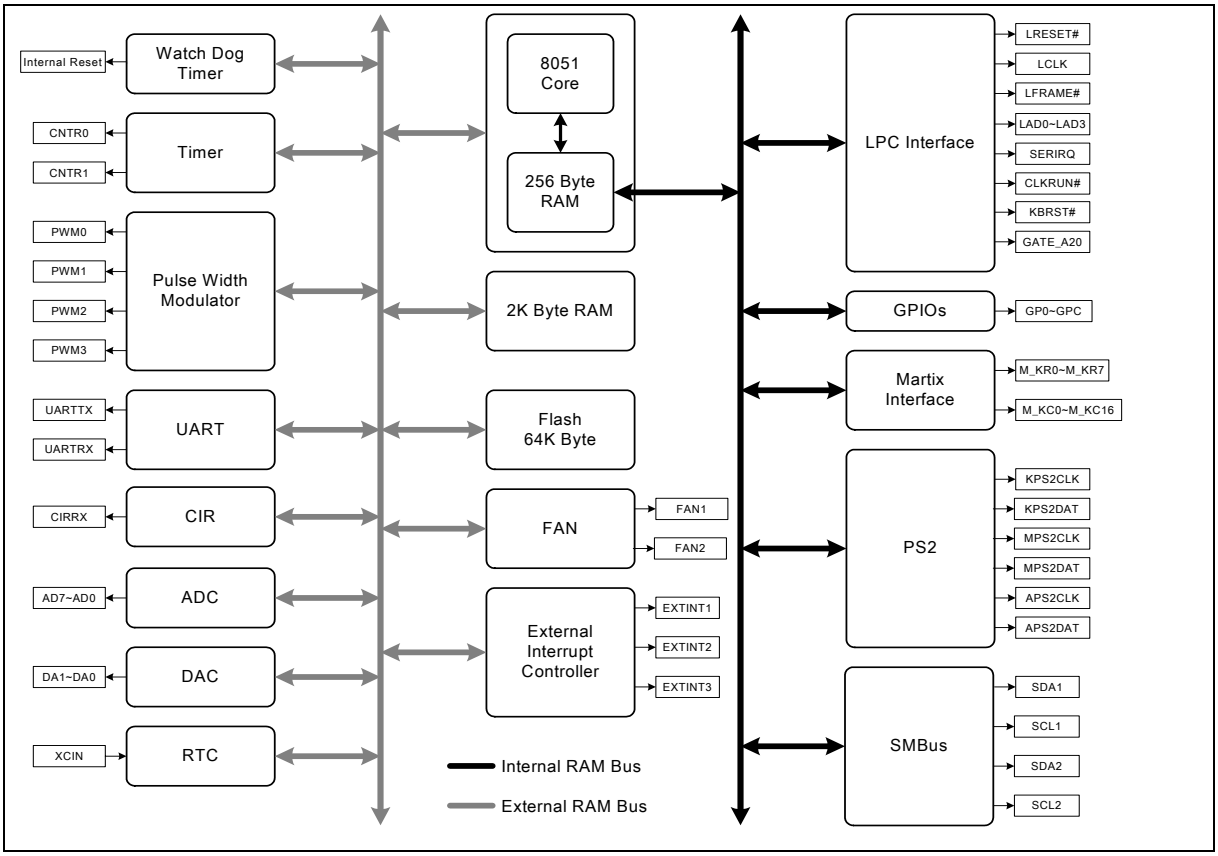
- CIR
  Support Decoding for the NEC Consumer IR Remote Control Format

- RTC
  Real Time Clock Generator with 32.768 KHz Input

- ACPI
  Support ACPI Appliance
  Secondary Programmable I/O Address Communication Port in LPC Mode

- Package
  -Pin QFP and 128-Pin LQFP Leadfree Package Options, in compliance with the RoHS (Restriction on Hazardous Substances)

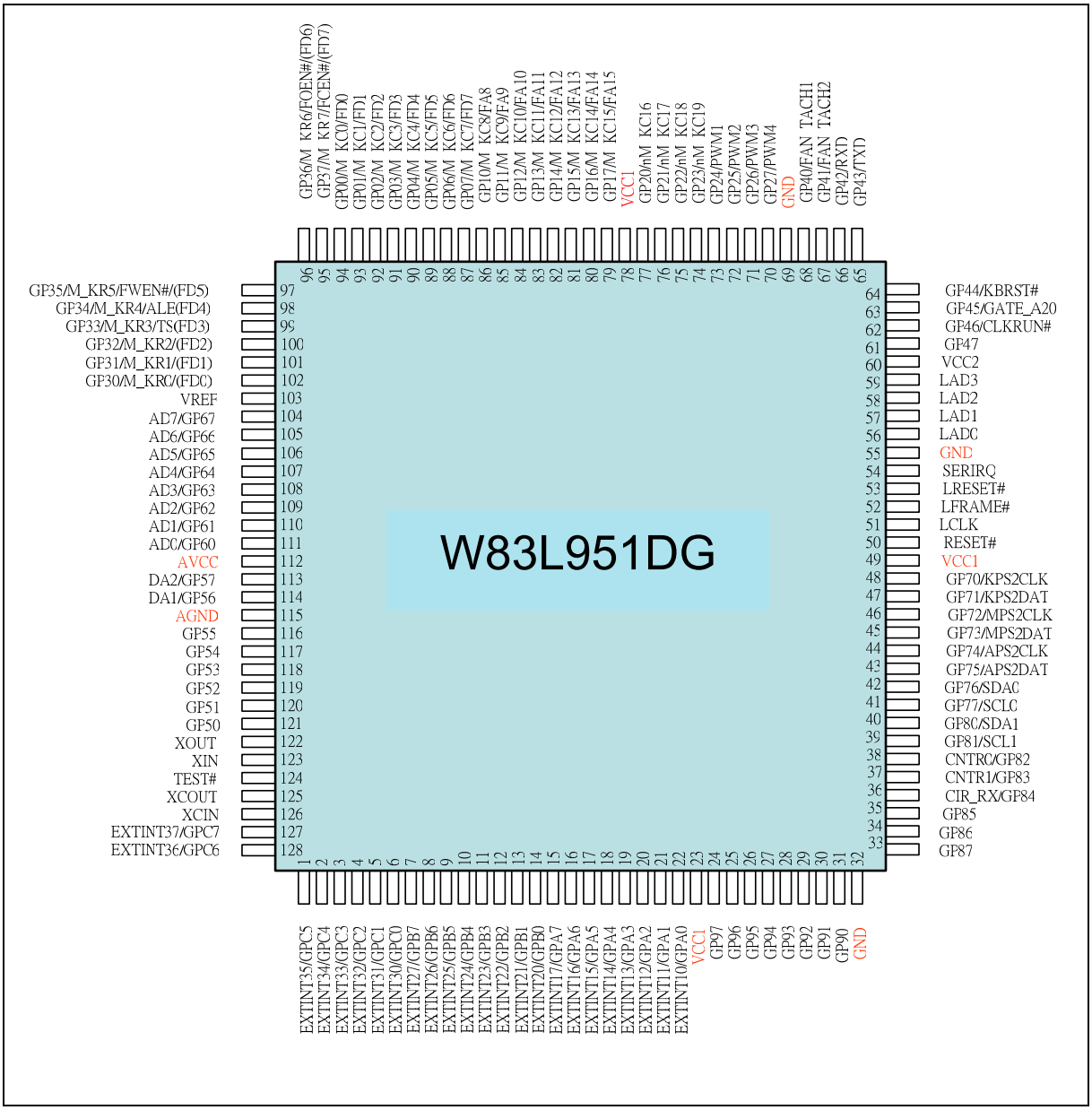
3. BLOCK DIAGRAM



Note: This Block Diagram should not used for pin count.

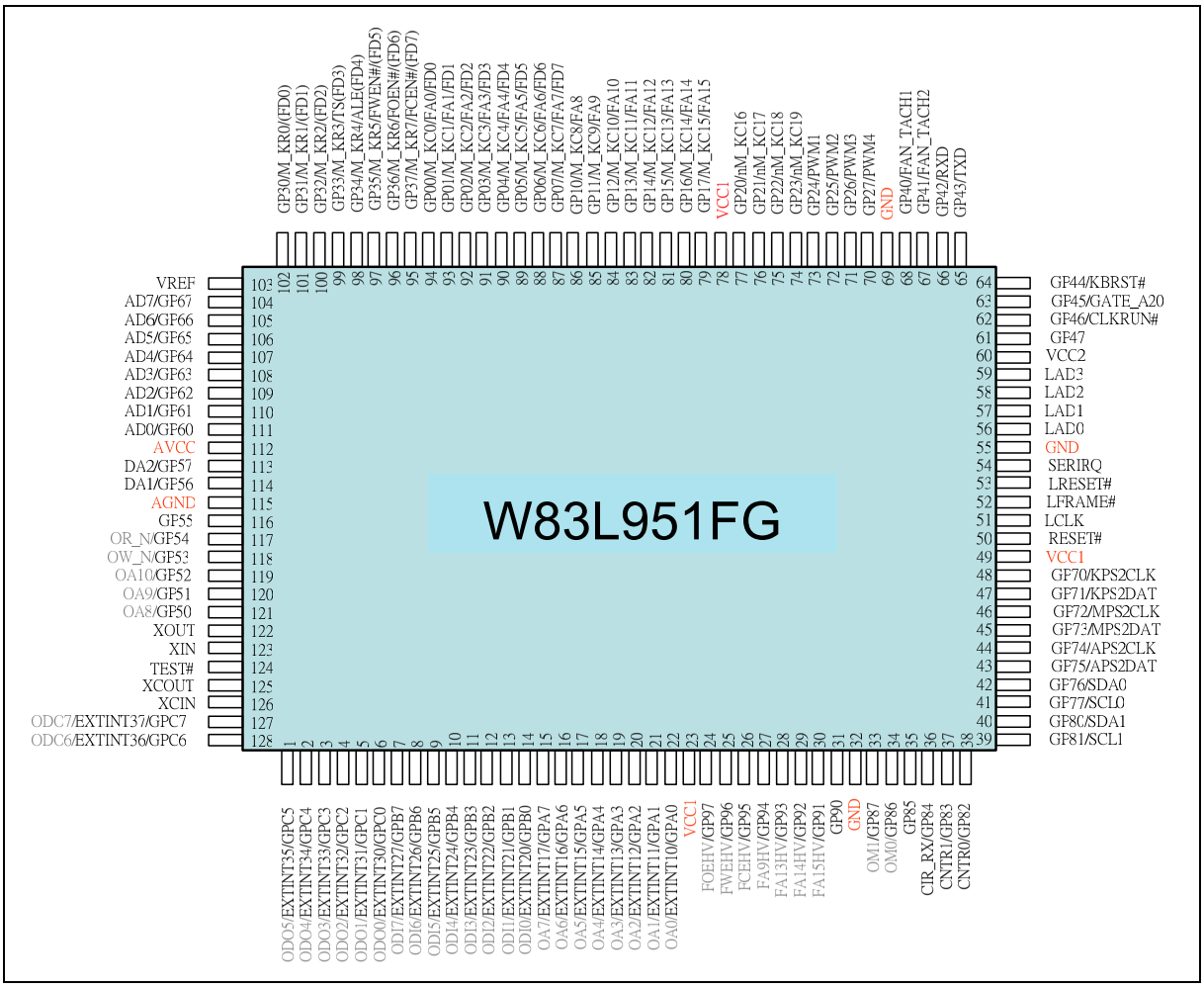
4. PIN CONFIGURATION FOR W83L951DG/W83L951FG

128-Pin Low Profile Quad Flat Pack (LQFP)



Note: The Pin Configuration is only for 128-pin LQFP Package.

128-Pin Quad Flat Pack (QFP)



Note: The Pin Configuration is only for 128-pin QFP Package.

5. PIN DESCRIPTION

Table 5-1 Pin Type Description

TYPE	DESCRIPTION
I/O_{12tsm}	Bi-directional pin, TTL level, Schmitt-trigger input, selectable 250uA/12mA sink capability, 12mA select source capability
I/O_{12tsai}	Bi-directional pin, TTL level, Schmitt-trigger input, Analog Input, 12mA source-sink capability
I/O_{12tsao}	Bi-directional pin, TTL level, Schmitt-trigger input, Analog Output, 12mA source-sink capability
I/O_{16tsh}	Bi-directional pin, TTL level, Schmitt-trigger input, 5V Tolerant, 16mA source-sink capability
I/O_{24ts}	Bi-directional pin, Schmitt-trigger input, 24mA source-sink capability
I_{ts}	TTL level, Schmitt-trigger input
I_c, O_c	Clock Input, Clock Out
I_{vdd}	Voltage Input
I_{vss}	Ground Input

Note: t – TTL level, s – Schmitt-trigger, m – matrix keyboard, ai – analog input, ao – analog output, h – 5V Tolerant, c – clock.

5.1 Pin configuration table

Table 5-2 Pin configuration table

SYMBOL	PIN	I/O	FUNCTION
GPC5 EXTINT35	1	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPC4 EXTINT34	2	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPC3 EXTINT33	3	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPC2 EXTINT32	4	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPC1 EXTINT31	5	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPC0 EXTINT30	6	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPB7 EXTINT27	7	I/O16tsh	General Purpose I/O Function External Interrupt Input

Pin configuration table, continued.

SYMBOL	PIN	I/O	FUNCTION
GPB6 EXTINT26	8	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPB5 EXTINT25	9	I/O16tsh	General Purpose I/O Function External Interrupt Input
SYMBOL	PIN	I/O	FUNCTION
GPB4 EXTINT24	10	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPB3 EXTINT23	11	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPB2 EXTINT22	12	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPB1 EXTINT21	13	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPB0 EXTINT20	14	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPA7 EXTINT17	15	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPA6 EXTINT16	16	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPA5 EXTINT15	17	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPA4 EXTINT14	18	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPA3 EXTINT13	19	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPA2 EXTINT12	20	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPA1 EXTINT11	21	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPA0 EXTINT10	22	I/O16tsh	General Purpose I/O Function External Interrupt Input
VCC1	23	Ivdd	Normal Power Input, +3.3V
GP97	24	I/O16tsh	General Purpose I/O Function

Pin configuration table, continued.

SYMBOL	PIN	I/O	FUNCTION
GP96	25	I/O16tsh	General Purpose I/O Function
GP95	26	I/O16tsh	General Purpose I/O Function
GP94	27	I/O16tsh	General Purpose I/O Function
GP93	28	I/O16tsh	General Purpose I/O Function
GP92	29	I/O16tsh	General Purpose I/O Function
GP91	30	I/O16tsh	General Purpose I/O Function
GP90	31	I/O16tsh	General Purpose I/O Function
GND	32	Ivss	Normal GND
GP87	33	I/O16tsh	General Purpose I/O Function
GP86	34	I/O16tsh	General Purpose I/O Function
GP85	35	I/O16tsh	General Purpose I/O Function
GP84 CIR_RX	36	I/O16tsh	General Purpose I/O Function Consumer Infrared Communication Receiver Function
GP83 CNTR1	37	I/O16tsh	General Purpose I/O Function Timer Y Signal
GP82 CNTR0	38	I/O16tsh	General Purpose I/O Function Timer X Signal
GP81 SCL2	39	I/O16tsh	General Purpose I/O Function SMBus 2 Clock Signal
SYMBOL	PIN	I/O	FUNCTION
GP80 SDA2	40	I/O16tsh	General Purpose I/O Function SMBus 2 Data Signal
GP77 SCL1	41	I/O16tsh	General Purpose I/O Function SMBus 1 Clock Signal
GP76 SDA1	42	I/O16tsh	General Purpose I/O Function SMBus 1 Data Signal
GP75 APS2_DAT	43	I/O16tsh	General Purpose I/O Function Auxiliary PS2 Data Signal
GP74 APS2_CLK	44	I/O16tsh	General Purpose I/O Function Auxiliary PS2 Clock Signal
GP73 MPS2_DAT	45	I/O16tsh	General Purpose I/O Function Mouse PS2 Data Signal

Pin configuration table, continued.

SYMBOL	PIN	I/O	FUNCTION
GP72 MPS2_CLK	46	I/O16tsh	General Purpose I/O Function Mouse PS2 Clock Signal
GP71 KPS2_DAT	47	I/O16tsh	General Purpose I/O Function Keyboard PS2 Data Signal
GP70 KPS2_CLK	48	I/O16tsh	General Purpose I/O Function Keyboard PS2 Clock Signal
VCC1	49	Ivdd	Normal Power Input, +3.3V
RESET#	50	I_{ts}	System Reset.
LCLK	51	Its	PCI clock input. Same 33MHz clock as PCI clock on the host. Same clock phase with typical PCI skew.
LFRAME#	52	Its	Indicates start of a new cycle or termination of a broken cycle.
LRESET#	53	Its	Reset signal. It can connect to PCIRST# signal on the host.
SERIRQ	54	I/O24ts	Serial IRQ input/Output.
GND	55	Ivss	Normal GND
LAD0	56	I/O24ts	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD1	57	I/O24ts	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD2	58	I/O24ts	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD3	59	I/O24ts	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LPWRSTS	60	Its	Power status. Indicates current power status of LPC interface.
GP47	61	I/O16tsh	General Purpose I/O Function
GP46 CLKRUN#	62	I/O16tsh	General Purpose I/O Function Advance LPC function: It is used to request starting the clock
GP45 GATE_A20	63	I/O16tsh	General Purpose I/O Function Gate A20 output
GP44 KBRST#	64	I/O16tsh	General Purpose I/O Function CPU reset output

Pin configuration table, continued.

SYMBOL	PIN	I/O	FUNCTION
GP43 TXD	65	I/O16tsh	General Purpose I/O Function UART TX output
GP42 RXD	66	I/O16tsh	General Purpose I/O Function UART RX Input
GP41 FAN_TACH1	67	I/O16tsh	General Purpose I/O Function Fan tachometer 1
GP40 FAN_TACH0	68	I/O16tsh	General Purpose I/O Function Fan tachometer 0
SYMBOL	PIN	I/O	FUNCTION
GND	69	Ivss	Normal GND
GP27 PWM3	70	I/O16tsh	General Purpose I/O Function Pulse Width Modulator Output
GP26 PWM2	71	I/O16tsh	General Purpose I/O Function Pulse Width Modulator Output
GP25 PWM1	72	I/O16tsh	General Purpose I/O Function Pulse Width Modulator Output
GP24 PWM0	73	I/O16tsh	General Purpose I/O Function Pulse Width Modulator Output
GP23 KC19	74	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output
GP22 KC18	75	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output
GP21 KC17	76	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output
GP20 KC16	77	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output
VCC1	78	Ivdd	Normal Power Input, +3.3V
GP17 KC15 FA15	79	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address

Pin configuration table, continued.

SYMBOL	PIN	I/O	FUNCTION
GP16 KC14 FA14	80	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP15 KC13 FA13	81	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP14 KC12 FA12	82	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP13 KC11 FA11	83	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP12 KC10 FA10	84	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP11 KC9 FA9	85	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP10 KC8 FA8	86	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP07 KC7 FA7/FD7	87	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP06 KC6 FA6/FD6	88	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
SYMBOL	PIN	I/O	FUNCTION
GP05 KC5 FA5/FD5	89	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data

Pin configuration table, continued.

SYMBOL	PIN	I/O	FUNCTION
GP04 KC4 FA4/FD4	90	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP03 KC3 FA3/FD3	91	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP02 KC2 FA2/FD2	92	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP01 KC1 FA1/FD1	93	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP00 KC0 FA0/FD0	94	I/O12tsm	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP37 KR7 CE#	95	I/O16tsh	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Flash chip select enable
GP36 KR6 OE#	96	I/O16tsh	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Flash output enable
GP35 KR5 WE#	97	I/O16tsh	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Flash write enable
GP34 KR4 ALE	98	I/O16tsh	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Address latch enable
GP33 KR3	99	I/O16tsh	General Purpose I/O Function Keyboard Matrix Row Input
GP32 KR2	100	I/O16tsh	General Purpose I/O Function Keyboard Matrix Row Input

Pin configuration table, continued.

SYMBOL	PIN	I/O	FUNCTION
GP31 KR1	101	I/O16tsh	General Purpose I/O Function Keyboard Matrix Row Input
GP30 KR0	102	I/O16tsh	General Purpose I/O Function Keyboard Matrix Row Input
VREF	103	Ivdd	Analog Reference Voltage Input
GP67 AD7	104	I/O12tsao	General Purpose I/O Function A/D Converter Input Signal
GP66 AD6	105	I/O12tsao	General Purpose I/O Function A/D Converter Input Signal
GP65 AD5	106	I/O12tsao	General Purpose I/O Function A/D Converter Input Signal
GP64 AD4	107	I/O12tsao	General Purpose I/O Function A/D Converter Input Signal
SYMBOL	PIN	I/O	FUNCTION
GP63 AD3	108	I/O12tsao	General Purpose I/O Function A/D Converter Input Signal
GP62 AD2	109	I/O12tsao	General Purpose I/O Function A/D Converter Input Signal
GP61 AD1	110	I/O12tsao	General Purpose I/O Function A/D Converter Input Signal
GP60 AD0	111	I/O12tsao	General Purpose I/O Function A/D Converter Input Signal
AVCC	112	Ivdd	Analog Power Input, +3.3V
GP57 DA2	113	I/O12tsai	General Purpose I/O Function DA Converter Output
GP56 DA1	114	I/O12tsai	General Purpose I/O Function DA Converter Output
AGND	115	Ivss	Analog GND
GP55	116	I/O16tsh	General Purpose I/O Function
GP54	117	I/O16tsh	General Purpose I/O Function
GP53	118	I/O16tsh	General Purpose I/O Function
GP52	119	I/O16tsh	General Purpose I/O Function

Pin configuration table, continued.

SYMBOL	PIN	I/O	FUNCTION
GP51	120	I/O16tsh	General Purpose I/O Function
GP50	121	I/O16tsh	General Purpose I/O Function
XOUT	122	Oc	24MHz/12MHz System Clock Output
XIN	123	Ic	24MHz/12MHz System Clock Input
TEST#	124	I_{ts}	Test pin to provide different operation.
XCOUT	125	Oc	32.768 KHz Clock Output
XCIN	126	Ic	32.768 KHz Clock Input
GPC7 EXTINT37	127	I/O16tsh	General Purpose I/O Function External Interrupt Input
GPC6 EXTINT36	128	I/O16tsh	General Purpose I/O Function External Interrupt Input

5.2 RESET# & TEST# Part

Table 5-3 RESET# & TEST# pin configuration table

SYMBOL	PIN	I/O	FUNCTION
RESET#	50	I_{ts}	System Reset.
TEST#	124	I_{ts}	Test pin to provide different operation.

In W83L951DG/FG, RESET# Pin and TEST# Pin decide the status of W83L951DG/FG to provide 4 operations.

TEST#	RESET#	CHIP CURRENT STATUS
0	0	Internal Flash Access Interface Enable
0	1	Reserved
1	0	Normal Reset
1	1	Normal Operation

5.3 LPC Interface Part

LPC Interface is formed by LAD0~LAD3, SERIRQ, LRESET#, LFRAME#, LCLK and VCC2. These pins are defined by LPC interface Spec except VCC2. Below are descriptions about all LPC pins:

Table 5-4 LPC interface pin configuration table

SYMBOL	PIN	I/O	FUNCTION
LCLK	51	I_{ts}	PCI clock input. Same 33MHz clock as PCI clock on the host. Same clock phase with typical PCI skew.
LFRAME#	52	I_{ts}	Indicates start of a new cycle or termination of a broken cycle.
LRESET#	53	I_{ts}	Reset signal. It can connect to PCIRST# signal on the host.
SERIRQ	54	I/O_{24ts}	Serial IRQ input/Output.
LAD0	56	I/O_{24ts}	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD1	57	I/O_{24ts}	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD2	58	I/O_{24ts}	LAD[3..0] are multiplexed address, control, and data in LPC bus.
LAD3	59	I/O_{24ts}	LAD[3..0] are multiplexed address, control, and data in LPC bus.

Note: Other pins about LPC interface, CLKRUN#: Please see “GP4” part.VCC2: Please see “power & clock” part.

5.4 GPIO0 Part

This part contains:

General Purpose I/O Function

Default is General Purpose I/O. Change the value of GPIO0 and GPIOD0 register to determine 8 input/output.

Keyboard Matrix Column Output

Use Chipctrl2 register bit 3 to enable {GP0, GP1, GP20~23} keyboard scan and GP3 key wakeup interrupt function.

Internal Flash Access Interface

When TEST# and RESET# are both low, Internal Flash Access Interface is enabled and other functions are disabled.

Table 5-5 GPIO0 pin configuration table

SYMBOL	PIN	I/O	FUNCTION
GP07 KC7 FA7/FD7	87	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP06 KC6 FA6/FD6	88	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP05 KC5 FA5/FD5	89	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP04 KC4 FA4/FD4	90	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP03 KC3 FA3/FD3	91	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP02 KC2 FA2/FD2	92	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP01 KC1 FA1/FD1	93	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data
GP00 KC0 FA0/FD0	94	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address/ Internal Flash Data

5.5 GPIO1 Part

This part contains:

General Purpose I/O Function

Default is General Purpose I/O. Change the value of GPIO1 and GPIOD1 register to determine 8 input/output.

Keyboard Matrix Column Output

Use Chipctrl2 register bit 3 to enable {GP0, GP1, GP20~23} keyboard scan and GP3 key wakeup interrupt function.

Internal Flash Access Interface

When TEST# and RESET# are both low, Internal Flash Access Interface is enabled and other functions are disabled.

Table 5-6 GPIO1 pin configuration table

SYMBOL	PIN	I/O	FUNCTION
GP17 KC15 FA15	79	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP16 KC14 FA14	80	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP15 KC13 FA13	81	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP14 KC12 FA12	82	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP13 KC11 FA11	83	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP12 KC10 FA10	84	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP11 KC9 FA9	85	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address
GP10 KC8 FA8	86	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output Internal Flash Address

5.6 GPIO2 Part

This part contains:

General Purpose I/O Function

Default is General Purpose I/O. Change the value of GPIO2 and GPIOD2 register to determine 8 input/output.

Pulse Width Modulator Output

Use Pulse Width Modulator Registers to control 4 Pulse Width Modulator Output.

Keyboard Matrix Column Output

Change the value of chip control 2 register bit 3 (Keyboard Scan Function Enable) to enable {GP0, GP1, GP20~23} keyboard scan function and GP3 key wakeup interrupt function.

Table 5-7 GPIO2 pin configuration table

SYMBOL	PIN	I/O	FUNCTION
GP27 PWM3	70	I/O_{16tsh}	General Purpose I/O Function Pulse Width Modulator Output
GP26 PWM2	71	I/O_{16tsh}	General Purpose I/O Function Pulse Width Modulator Output
GP25 PWM1	72	I/O_{16tsh}	General Purpose I/O Function Pulse Width Modulator Output
GP24 PWM0	73	I/O_{16tsh}	General Purpose I/O Function Pulse Width Modulator Output
GP23 KC19	74	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output
GP22 KC18	75	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output
GP21 KC17	76	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output
GP20 KC16	77	I/O_{12tsm}	General Purpose I/O Function Keyboard Matrix Column Output

5.7 GPIO3 Part

This part contains General Purpose I/O function, external flash interface, and keyboard matrix row input. Default function is General Purpose I/O function.

General Purpose I/O Function

Change the value of GPIO 3 data register (GPIO3) and GPIO 3 direction register (GPIOD3) to determine 8 input/output.

Keyboard Matrix Row Input

Change the value of chip control 2 register bit 3 (Keyboard Scan Function Enable) to enable GP3 key wakeup interrupt function.

Note: GPIO3 must be set as input when this function is enabled

The sample frequency about KEY Interrupt Mode is a system cycle, trigger for ' Low ' of input of GP3 and only take a sample once (unless input of GP3 return 'High', then enter 'low'). If signal debounce, then interrupt may request again.

Internal Flash Access Interface

GPIO30~33: Reserved (Must assign low)

Table 5-8 GPIO3 pin configuration table

SYMBOL	PIN	I/O	FUNCTION
GP37 KR7 CE#	95	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Flash chip select enable
GP36 KR6 OE#	96	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Flash output enable
GP35 KR5 WE#	97	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Flash write enable
GP34 KR4 ALE	98	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input Internal Flash Access Interface: Address latch enable
GP33 KR3	99	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input
GP32 KR2	100	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input
GP31 KR1	101	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input
GP30 KR0	102	I/O_{16tsh}	General Purpose I/O Function Keyboard Matrix Row Input

5.8 GPIO4 Part

General Purpose I/O Function

Change the value of GPIO 4 data register (GPIO4) and GPIO 4 direction register (GPIOD4) to determine 8 input/output.

Universal Asynchronous Serial I/O Function

Change the value of chip control 1 register bit 3 (UART Function Enable) to enable Universal Asynchronous Serial I/O Function.

Hardware Keyboard Reset Function

Change the value of keyboard control register bit4 (Port 92 Enable) and bit3 (Hardware Keyboard Reset Control Enable) to enable Hardware Keyboard Reset Function.

Hardware Gate A20 Function

Change the value of keyboard control register bit4 (Port 92 Enable) and bit2 (Hardware Gate A20 Control Enable) to enable Hardware Gate A20 Function.

Table 5-9 GPIO4 pin configuration table

SYMBOL	PIN	I/O	FUNCTION
GP47	61	I/O_{16tsh}	General Purpose I/O Function
GP46 CLKRUN#	62	I/O_{16tsh}	General Purpose I/O Function Advance LPC function: It is used to request starting the clock
GP45 GATE_A20	63	I/O_{16tsh}	General Purpose I/O Function Gate A20 output
GP44 KBRST#	64	I/O_{16tsh}	General Purpose I/O Function CPU reset output
GP43 TXD	65	I/O_{16tsh}	General Purpose I/O Function UART TX output
GP42 RXD	66	I/O_{16tsh}	General Purpose I/O Function UART RX Input
GP41 FAN_TACH1	67	I/O_{16tsh}	General Purpose I/O Function Fan tachometer 1
GP40 FAN_TACH0	68	I/O_{16tsh}	General Purpose I/O Function Fan tachometer 0