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W90N740CD/W90N740CDG
DATA SHEET

WINBOND

32-BIT ARM7TDMI-BASED MICRO-CONTROLLER

Winbond is providing this document only for reference purposes of W90N740-based system design. Winbond assumes no responsibility for errors or omissions.

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Publication Release Date: Aug. 18, 2005

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1. GENERAL DESCRIPTION

The **W90N740** micro-controller is 16/32 bit, **ARM7TDMI based RISC** micro-controller for **network** as well as **embedded** applications. An integrated dual Ethernet MAC, the W90N740, is designed for use in broadband routers, wireless access points, residential gateways and LAN camera.

The W90N740N is built around The ARM7TDMI CPU core designed by Advanced RISC Machines, Ltd. And achieves **80MHz** under **worse conditions**. Its small size, fully static design is particularly suitable for cost-sensitive and power-sensitive applications. It designs as Harvard architecture by offering an **8K-byte I-cache/SRAM and an 2K-byte D-cache/SRAM** with flexible configuration and two way set associative structure to balance data movement between CPU and external memory. Four stages **write buffer** also improves latency for write operations.

The **external bus interface (EBI)** controller provides single bus architecture, 8/16/32 bit data width to access external SDRAM, ROM/SRAM, flash memory and I/O devices. It achieves same frequency as CPU core to minimize latency if internal cache misses. Memory controller supports different kinds of SDRAM types and configurations to ease system design. The System Manager includes an internal 32-bit system bus arbiter and a PLL clock controller. Generic I/O bus is easily served as PCMCIA-like interface for 802.11b wireless LAN connection.

Two 10/100Mb MACs of Ethernet controller is built in to reduce total system cost and increase performance between WAN and LAN port. Either **MII or RMII** of MAC is selected for external 10/100 PHY chip to design for varieties of applications. A powerful **NAT accelerator** (**Patent Pending**) between LAN and WAN reduces the software loading of CPU and speeds up performance between LAN and WAN.

W90N740 integrates **root hub of USB 1.1 host controller with one port transceiver** and uses additional port with external transceiver if necessary, which can add valuable functions like flash disk, printer server, Bluetooth device via USB port. The important peripheral functions include **one full wired high speed UART** channel, **2-Channel GDMA**, **one watch-dog timer**, **two 24-bit timers** with 8-bit pre-scale, **20 programmable I/O ports**, and **an advanced interrupt controller**.

2. FEATURES

Architecture

- Highly-integrated system for embedded Ethernet applications
- Powerful ARM7TDMI core and fully 16/32-bit RISC architecture
- Big /Little-Endian mode supported
- Cost-effective JTAG-based debug solution

System Manager

- System memory map & on-chip peripherals memory map
- The data bus width of external memory address & data bus connection with external memory
- Bus arbitration supports the Fixed Priority Mode & Rotate Priority Mode
- Power-On setting
- On-Chip PLL module control & Clock select control

External Bus Interface (EBI)

- External I/O Control with 8/16/32 bit external data bus
- Cost-effective memory-to-peripheral DMA interface
- SDRAM Controller supports up to 2 external SDRAM & the maximum size of each device is 32MB
- ROM/FLASH & External I/O interface
- Support for PCMCIA 16-bit PC Card devices

On-Chip Instruction and Data Cache

- Two-way, Set-associative, 8K-byte I-cache and 2K-byte D-cache
- Support for LRU (Least Recently Used) Protocol
- Cache can be configured as an internal SRAM
- Support Cache Lock function

Ethernet MAC Controller (EMC)

- IEEE 802.3 protocol engine with programmable MII or RMII interface for 10/100 Mbits/s
- DMA engine with burst mode
- 256 bytes transmit & 256 bytes receive FIFO for MAC protocol engine and DMA access
- Built-in 16 entry CAM Address Register
- Support long frame (more than 1518 bytes) and short frame (less than 64 bytes)
- Re-transmit (during collision) the frame without DMA access
- Half or full duplex function option
- Support Station Management for external PHY
- On-Chip Pad generation

NAT Accelerator (Patent Pending)

- Hardware acceleration on IP address / port number look up and replacement for network address translation, including MAC address translation
- Provide 64 entries of translation table
- Support TCP / UDP packets

GDMA Controller

- 2 Channel GDMA for memory-to-memory data transfers without CPU intervention
- Increase or decrease source / destination address in 8-bit, 16-bit, or 32-bit data transfers
- Supports 4-data burst mode to boost performance
- Support external GDMA request

USB Host Controller

- USB 1.1 compatible
- Open Host Controller Interface (OHCI) 1.1 compatible.
- Supports both low-speed (1.5 Mbps) and full-speed (12Mbps) USB devices.
- Built-in DMA for real-time data transfer

UART

- One UART (serial I/O) blocks with interrupt-based operation
- Full set of MODEM control functions (CTS, RTS, DSR, DTR, RI and DCD)
- Fully programmable serial-interface characteristics:
- Break generation and detection
- False start bit detection
- Parity, overrun, and framing error detection
- Full prioritized interrupt system controls

Timers

- Two programmable 24-bit timers with 8-bit pre-scalar
- One programmable 24-bit Watch-Dog timer
- One-short mode, period mode or toggle mode operation

Programmable I/Os

- 21 programmable I/O ports
- I/O ports Configurable for Multiple functions

Advanced Interrupt Controller (AIC)

- 18 interrupt sources, including 4 external interrupt sources
- Programmable normal or fast interrupt mode (IRQ, FIQ)
- Programmable as either edge-triggered or level-sensitive for 4 external interrupt sources
- Programmable as either low-active or high-active for 4 external interrupt sources
- Priority methodology is encoded to allow for interrupt daisy-chaining
- Automatically mask out the lower priority interrupt during interrupt nesting

GPIO Controller

- Programmable as an input or output pin

On-Chip PLL

- One PLL for both CPU and USB host controller
- The external clock can be multiplied by on-chip PLL to provide high frequency system clock
- Programmable clock frequency, and the input frequency range is 3-30MHz; 15MHz is preferred.

Operation Voltage Range

- 2.7 – 3.6 V for IO Buffer
- 1.62 – 1.98 V for Core Logic

Operation Temperature Range

- 0 – 70 Degree C

Operating Frequency

- 80 MHz (default)

Package Type

- 176-pin LQFP

3. BLOCK DIAGRAM

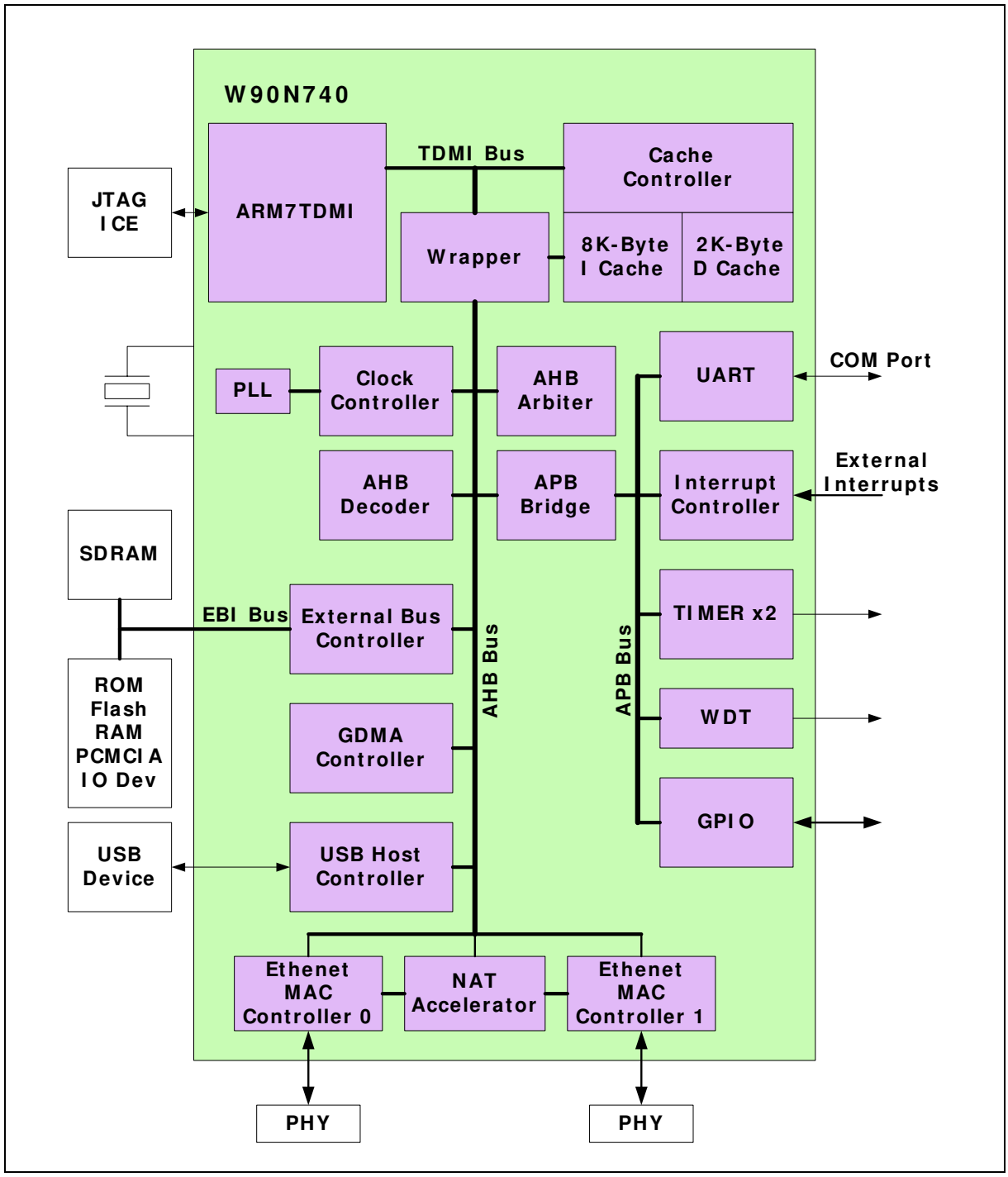

Fig 3.1 W90N740 Functional Block Diagram

4. PIN CONFIGURATION

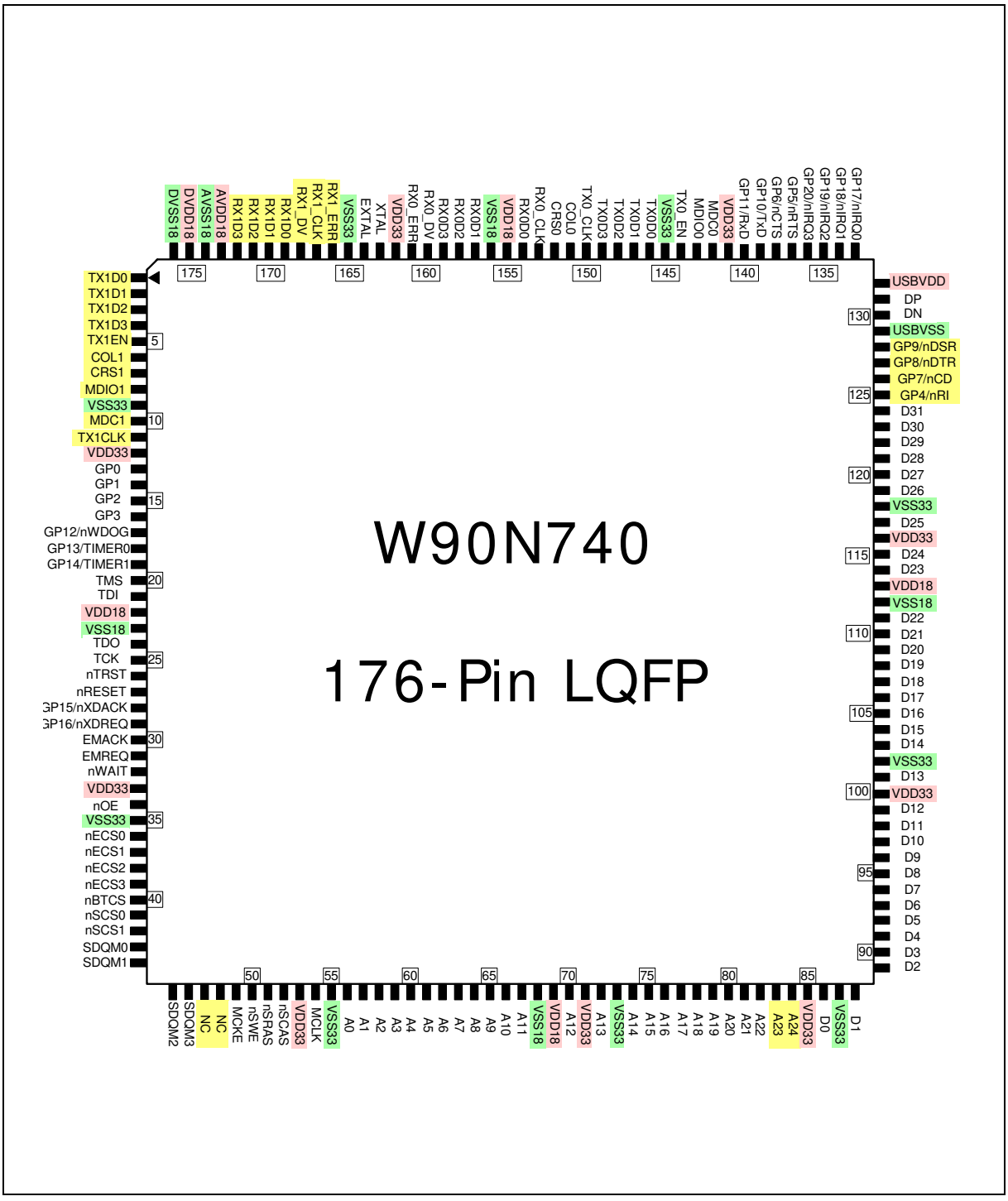

Fig 4.1 176-Pin LQFP Pin Diagram

5. PIN ASSIGNMENT

Table 4 W90N740 Pins Assignment

PIN NAME	176-PIN LQFP	
Clock & Reset	**(4 pins)**	
EXTAL	●	164
XTAL	●	163
MCLK	●	54
nRESET	●	27
TAP Interface	**(5 pins)**	
TCK	●	25
TMS	●	20
TDI	●	21
TDO	●	24
nTRST	●	26
External Bus Interface	**(78 pins)**	
A [24:22]	●	84-82
A [21:0]	●	81-74, 72, 70,67-56
D [31:16]	●	124-119, 117, 115-114, 111-105
D [15:0]	●	104-103, 101, 99-88, 86
nWBE [3:0]/ SDQM [3:0]	●	46-43
nSCS[1:0]	●	42, 41
NSRAS	●	51
NSCAS	●	52
NSWE	●	50
MCKE	●	49
NC	●	48
NC	●	47
EMREQ	●	31
EMACK	●	30
nWAIT	●	32
NBTCS	●	40
nECS[3:0]	●	39-36
NOE	●	34

Table 4 W90N740 Pins Assignment, continued

PIN NAME	176-PIN LQFP	
Ethernet Interface (0)	**(17 pins)**	
MDC0	●	142
MDIO0	●	143
COL0 /	●	151
CRS0 / R1B_CRSDV	●	152
TX0_CLK	●	150
TX0D [3:0] / R1B_TXD [1:0], R0_TXD [1:0]	●	149-146
TX0_EN / R0_TXEN	●	144
RX0_CLK / R0_REFCLK	●	153
RX0D [3:0] / R1B_RXD [1:0], R0_RXD [1:0]	●	159-157, 154
RX0_DV / R0_CRSDV	●	160
RX0_ERR	●	161
Ethernet Interface (1)	**(17 pins)**	
MDC1	●	10
MDIO1	●	8
COL1	●	6
CRS1	●	7
TX1_CLK	●	11
TX1D [3:0] / R1A_TX [1:0]	●	4-1
TX1_EN /R1A_TXEN	●	5
RX1_CLK / R1A_REFCLK	●	167
RX1D [3:0] / R1A_RXD [1:0]	●	172-169
RX1_DV / R1A_CRSDV	●	168
RX1_ERR / R1A_RXERR	●	166

Table 4 W90N740 Pins Assignment, continued

NAME	176-PIN LQFP	
USB Interface	**(2 pins)**	
DP	●	131
DN	●	130
Miscellaneous	**(21 pins)**	
GP [20:17] / nIRQ [3:0]	●	136-133
GP16 / nXDREQ	●	29
GP15 /nXDACK	●	28
GP14 / TIMER1/ SPEED	●	19
GP13 / TIMER0/ STDBY	●	18
GP12 /nWDOG	●	17
GP11 /RxD	●	140
GP10 /TxD	●	139
GP9/nDSR/nTOE	●	128
GP8 /nDTR/FSE0	●	127
GP7 /nCD / VO	●	126
GP6 /nCTS/ VM	●	138
GP5 /nRTS/ VP	●	137
GP4 /nRI / RCV	●	125
GP [3:0]	●	16-13
Power/Ground	**(32 pins)**	
VDD18	●	22, 69, 113, 155
VSS18	●	23, 68, 112, 156
VDD33	●	12, 33, 53, 71, 85, 100, 116, 141, 162
VSS33	●	9, 35, 55, 73, 87, 102, 118, 145, 165
USBVDD	●	132
USBVSS	●	129
DVDD18	●	175
DVSS18	●	176
AVDD18	●	173
AVSS18	●	174

6. PIN DESCRIPTION

Table 6.1 W90N740 Pins Description

PIN NAME	IO TYPE	PAD TYPE	DESCRIPTION
System Clock & Reset			
EXTAL	I	-	External Clock / Crystal Input
XTAL	O	-	Crystal Output
MCLK	O	-	System Master Clock Out, SDRAM clock
nRESET	I	-	System Reset, active-low
TAP Interface			
TCK	ID	internal pull-down	JTAG Test Clock,
TMS	IU	internal pull-up	JTAG Test Mode Select,
TDI	IU	internal pull-up	JTAG Test Data in,
TDO	O	-	JTAG Test Data out
nTRST	IU	internal pull-up	JTAG Reset, active-low,
External Bus Interface			
A [24:22]	O	-	Address Bus (MSB) of external memory and IO devices
A [21:0]	IO	-	Address Bus of external memory and IO devices
D [31:16]	IO	-	Data Bus (MSB) of external memory and IO device,
D [15:0]	IO	-	Data Bus (LSB) of external memory and IO device
nWBE [3:0]/ SDQM [3:0]	IO	-	Write Byte Enable for specific device(nECS[3:0]), Data input/output Mask signal for SDRAM (nSCS[1:0]), active-low These pins are always Output in normal mode, and Input type in internal SRAM test mode.
nSCS [1:0]	O	-	SDRAM chip select for two external banks, active-low.
nSRAS	O	-	Row Address Strobe for SDRAM, active-low
nSCAS	O	-	Column Address Strobe for SDRAM, active-low
nSWE	O	-	SDRAM Write Enable, active-low
MCKE	O	-	SDRAM Clock Enable, active-high
EMREQ	ID	internal pull-down	External Master Bus Request This is used to request external bus. When EMACK active, indicates the bus grants the bus, chip drives all the output pins of the external bus to high impedance.
EMACK	O	-	External Bus Acknowledge
nWAIT	IU	internal pull-up	External Wait, active-low
nBTCS	O	-	ROM/Flash Chip Select, active-low
nECS [3:0]	IO	-	External I/O Chip Select, active-low.
nOE	O	-	ROM/Flash, External Memory Output Enable, active-low

Pins Description, continued

PIN NAME	IO TYPE	PAD TYPE	DESCRIPTION
Ethernet Interface (0)			
MDC0	O	-	MII Management Data Clock for Ethernet 0. It is the reference clock of MDIO0. Each MDIO0 data will be latched at the rising edge of MDC0 clock.
MDIO0	IO	-	MII Management Data I/O for Ethernet 0. It is used to transfer MII control and status information between PHY and MAC.
COL0	I	-	Collision Detect for Ethernet 0 in MII mode. This shall be asserted by PHY upon detecting a collision happened over the medium. It will be asserted and lasted until collision condition vanishes.
CRS0	I	-	Carrier Sense for Ethernet 0 in MII mode. In RMII mode, external pull-up is necessary.
TX0_CLK	I	-	Transmit Data Clock for Ethernet 0 in MII mode. TX0_CLK is driven by PHY and provides the timing reference for TX0_EN and TX0D. The clock will be 25MHz or 2.5 MHz.
TX0D [3:0]/ --, R0_TXD [1:0]	O	-	Transmit Data bus (4-bit) for Ethernet 0 in MII mode. The nibble transmit data bus is synchronized with TX0_CLK. It should be latched by PHY at the rising edge of TX0_CLK. In RMII mode, TX0D [1:0] are used as R0_TXD [1:0], 2-bit Transmit Data bus for Ethernet 0;
TX0_EN / R0_TXEN	O	-	Transmit Enable for Ethernet 0 in MII. It indicates the transmit activity to external PHY. It will be synchronized with TX0_CLK. In RMII mode, R0_TXEN shall be asserted synchronously with the first nibble of the preamble and shall remain asserted while all di-bits to be transmitted are presented. Of course, it is synchronized with R0_REFCLK.
RX0_CLK / R0_REFCLK	I	-	Receive Data Clock for Ethernet 0 in MII mode When it is used as a received clock pin, it is from PHY. The clock will be either 25 MHz or 2.5 MHz. The minimum duty cycle at its high or low state should be 35% of the nominal period for all conditions. In RMII mode, this pin is used as R0_REFCLK, Reference Clock; The clock shall be 50MHz +/- 50 ppm with minimum 35% duty cycle at high or low state.
RX0D [3:0] / --, R0_RXD [1:0]	I	-	Receive Data bus (4-bit) for Ethernet 0 in MII mode. They are driven by external PHY, and should be synchronized with RX0_CLK and valid only when RX0_DV is valid. In RMII mode, RX0D [1:0] are used as R0_RXD [1:0], 2-bit Receive Data bus for Ethernet 0;
RX0_DV / R0_CRSDV	I	-	Receive Data Valid for Ethernet 0 in MII mode. It will be asserted when received data is coming and present, and de-asserted at the end of the frame. In RMII mode, this pin is used as the R0_CRSDV, Carrier Sense / Receive Data Valid for Ethernet 0. The R0_CRSDV shall be asserted by PHY when the receive medium is non-idle. Loss of carrier shall result in the de-assertion of R0_CRSDV synchronous to the cycle of R0_REFCLK, and only on nibble boundaries.
RX0_ERR	I	-	Receive Data Error for Ethernet 0 in MII mode. It indicates a data error detected by PHY. The assertion should be lasted for longer than a period of RX0_CLK. When RX0_ERR is asserted, the MAC will report a CRC error.

Pins Description, continued

PIN NAME	IO TYPE	PAD TYPE	DESCRIPTION
Ethernet Interface (1)			
MDC1	O	-	MII Management Data Clock for Ethernet 1. It is the reference clock of MDIO1. Each MDIO1 data will be latched at the rising edge of MDC1 clock.
MDIO1	IO	-	MII Management Data I/O for Ethernet 1. It is used to transfer MII control and status information between PHY and MAC.
COL1	I	-	Collision Detect for Ethernet 1 in MII mode. This shall be asserted by PHY upon detecting a collision happened over the medium. It will be asserted and lasted until collision condition vanishes. External pull-up is necessary in RMII mode.
CRS1	I	-	Carrier Sense for Ethernet 1 in MII mode. External pull-up is necessary in RMII mode.
TX1_CLK	I	-	Transmit Data Clock for Ethernet 1 in MII mode, TX1_CLK is driven by PHY and provides the timing reference for TX1_EN and TX1D. The clock will be 25MHz or 2.5 MHz. External pull-up will be necessary in RMII mode.
TX1D [3:0] / --,R1A_TXD [1:0]	O	-	Transmit Data bus (4-bit) for Ethernet 1 in MII mode. The nibble transmit data bus is synchronized with TX1_CLK. It should be latched by PHY at the rising edge of TX1_CLK. In RMII mode, TX1D [1:0] are used as R1A_TXD [1:0], 2-bit Transmit Data bus for Ethernet 1
TX1_EN/ R1A_TXEN/R1B_ TXEN	O	-	Transmit Enable for Ethernet 1 in MII and RMII mode. It indicates the transmit activity to external PHY. It will be synchronized with TX1_CLK in MII mode.
RX1_CLK / R1A_REFCLK	I	-	Receive Data Clock for Ethernet 1 in MII mode. When it is used as a received clock pin, it is from PHY. The clock will be either 25 MHz or 2.5 MHz. The minimum duty cycle at its high or low state should be 35% of the nominal period for all conditions. In RMII mode, this pin is used as R1A_REFCLK, Reference Clock and only available for 176-pin package. The clock shall be 50MHz +/-50 ppm with minimum 35% duty cycle at high or low state.
RX1D [3:0] / --, R1A_RXD[1:0]	I	-	Receive Data bus (4-bit) for Ethernet 1 in MII mode. They are driven by external PHY, and should be synchronized with RX1_CLK and valid only when RX1_DV is valid. In RMII mode, RX1D [1:0] are used as R1A_RXD [1:0], 2-bit Receive Data bus for Ethernet 1.
RX1_DV/ R1A_CRSDV	I	-	Receive Data Valid for Ethernet 1 in MII mode. It will be asserted when received data is coming and present, and de-asserted at the end of the frame. In RMII mode, this pin is used as the R1A_CRSDV, Carrier Sense / Receive Data Valid for Ethernet 1 and only available for 176-pin package. The R1A_CRSDV shall be asserted by PHY when the receive medium is non-idle. Loss of carrier shall result in the de-assertion of R1A_CRSDV synchronous to the cycle of R1A_REFCLK, and only on nibble boundaries.
RX1_ERR / R1A_RXERR	I	-	Receive Data Error for Ethernet 1 in MII and RMII mode. It indicates a data error detected by PHY. The assertion should be lasted for longer than a period of RX0_CLK. When RX0_ERR is asserted, the MAC will report a CRC error.

Pins Description, continued

NAME	IO TYPE	PAD TYPE	DESCRIPTION
USB Interface			
DP	IO	-	Differential Positive USB IO signal
DN	IO	-	Differential Negative (Minus) USB IO signal
Miscellaneous			
GP[20:17] / nIRQ[3:0]	IO	-	External Interrupt Request or General Purpose I/O
GP16 / nXDREQ	IO	-	External DMA Request or General Purpose I/O
GP15 /nXDACK	IO	-	External DMA Acknowledge or General Purpose I/O
GP14 / TIMER1/SPEED	IO	-	Timer 1 or General Purpose I/O. This pin is also used as SPEED, Speed mode control for external USB transceiver
GP13 / TIMER0/STDBY	IO	-	Timer 0 or General Purpose I/O. This pin is also used as STDBY, StandBy control for external USB transceiver
GP12 /nWDOG	IO	-	Watchdog Timer Timeout Flag (active-low) or General Purpose I/O
GP11 /RxD	IO	-	UART Receive Data or General Purpose I/O
GP10 /TxD	IO	-	UART Transmit Data or General Purpose I/O
GP9/nDSR/nTOE	IO	-	UART Receive Clock or General Purpose I/O. This pin is also used as nTOE, Output Enable control (active-low) for external USB transceiver.
GP8 /nDTR/FSE0	IO	-	UART Transmit Clock or General Purpose I/O. This pin is also used as SE0, Differential Data Transceiver Output for external USB transceiver. T
GP7 /nCD /VO	IO	-	UART Carrier Detector or General Purpose I/O. This pin is also used as VO, Data Output for external USB transceiver.
GP6 /nCTS/ VM	IO	-	UART Clear to Send or General Purpose I/O. This pin is also used as VM, Data Negative (Minus) Input for external USB receiver.
GP5 /nRTS/ VP	IO	-	UART Ready to Send or General Purpose I/O. This pin is also used as VP, Data Positive Input for external USB receiver.
GP4 /nRI /RCV	IO	-	UART Ring Indicator or General Purpose I/O. This pin is also used as RCV, Difference Receiver Input.
GP[3:0]	IO	-	General Purpose I/O.
Power/Ground			
VDD18	P	-	Core Logic power (1.8V)
VSS18	G	-	Core Logic ground (0V)
VDD33	P	-	IO Buffer power (3.3V)
VSS33	G	-	IO Buffer ground (0V)
USBVDD	P	-	USB power (3.3V)
USBVSS	G	-	USB ground (0V)
DVDD18	P	-	PLL Digital power (1.8V)
DVSS18	G	-	PLL Digital ground (0V)
AVDD18	P	-	PLL Analog power (1.8V)
AVSS18	G	-	PLL Analog ground (0V)

7. FUNCTIONAL DESCRIPTION

7.1 ARM7TDMI CPU Core

The ARM7TDMI CPU core is a member of the ARM family of general-purpose 32-bit microprocessors, which offer high performance for very low power consumption. The architecture is based on Reduced Instruction Set Computer (RISC) principles, and the instruction set and related decode mechanism are much simpler than those of micro-programmed Complex Instruction Set Computer (CISC) systems. Pipelining is employed so that all parts of the processing and memory systems can operate continuously. The high instruction throughput and impressive real-time interrupt response are the major benefits.

The ARM7TDMI core can execute two instruction sets:

(1) The standard 32-bit ARM instruction set

(2) The 16-bit THUMB instruction set

The THUMB set's 16-bit instruction length allows it to approach twice the density of standard ARM core while retaining most of the ARM's performance advantage over a traditional 16-bit processor using 16-bit registers. THUMB instructions operate with the standard ARM register configuration, allowing excellent interoperability between ARM and THUMB states. Each 16-bit THUMB instruction has a corresponding 32-bit ARM instruction with the same effect on the processor model. In the other words, the THUMB architecture give 16-bit systems a way to access the 32-bit performance of the ARM Core without requiring the full overhead of 32-bit processing.

ARM7TDMI CPU core has 31 x 32-bit registers. At any one time, 16 set are visible; the other registers are used to speed up exception processing. All the register specifies in ARM instructions can address any of the 16 registers. The CPU also supports 5 types of exception, such as two levels of interrupt, memory aborts, attempted execution of an undefined instruction and software interrupts.

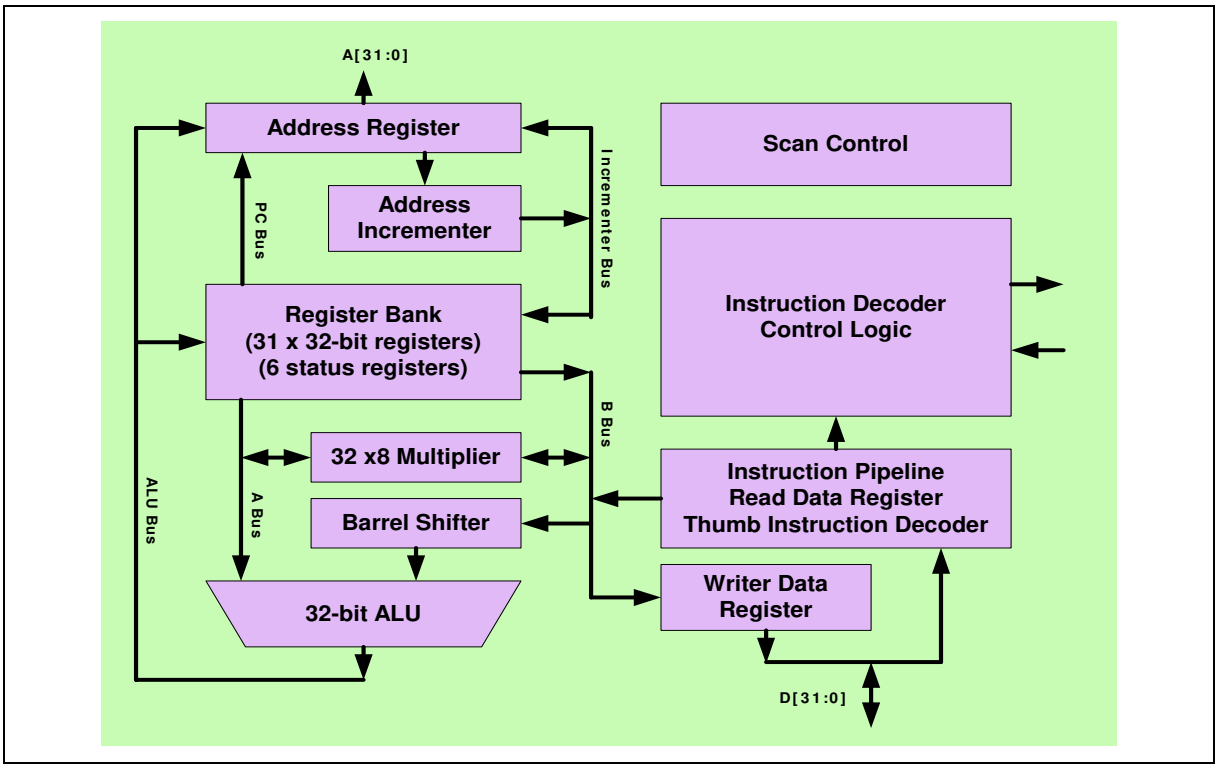

Fig 7.1 ARM7TDMI CPU Core Block Diagram

7.2 System Manager

7.2.1 Overview

The functions of the System Manager:

- System memory map & on-chip peripherals memory map
- The data bus width of external memory address & data bus connection with external memory
- Bus arbitration supports the Fixed Priority Mode & Rotate Priority Mode
- Power-On setting
- On-Chip PLL module control & Clock select control

7.2.2 System Memory Map

W90N740 provides 2G bytes cacheable address space and the other 2G bytes are non-cacheable. The On-Chip Peripherals bank is on 1M bytes top of the space (0xFFF0.0000 – 0xFFFF.FFFF) and the On-Chip RAM bank's start address is 0xFFE0.0000, the other banks can be located anywhere (cacheable space: 0x0~0x7FDF.FFFF if Cache ON; non-cacheable space: 0x8000.0000 ~ 0xFFDF.FFFF).

The size and location of each bank is determined by the register settings for "current bank base address pointer" and "current bank size". (*Note: The address boundaries of consecutive banks must not overlap, when setting the bank control registers.)

The start address of each memory bank is not fixed, except On-Chip Peripherals and On-Chip RAM. You can use bank control registers to assign a specific bank start address by setting the bank's base pointer (13 bits). The address resolution is 256K bytes. The bank's start address is defined as "base pointer << 18" and the bank's size is "current bank size".

In the event of an access request to an address outside any programmed bank size, an abort signal is generated. The maximum accessible memory size of each external IO bank is 32M bytes, and 64M bytes on SDRAM banks.

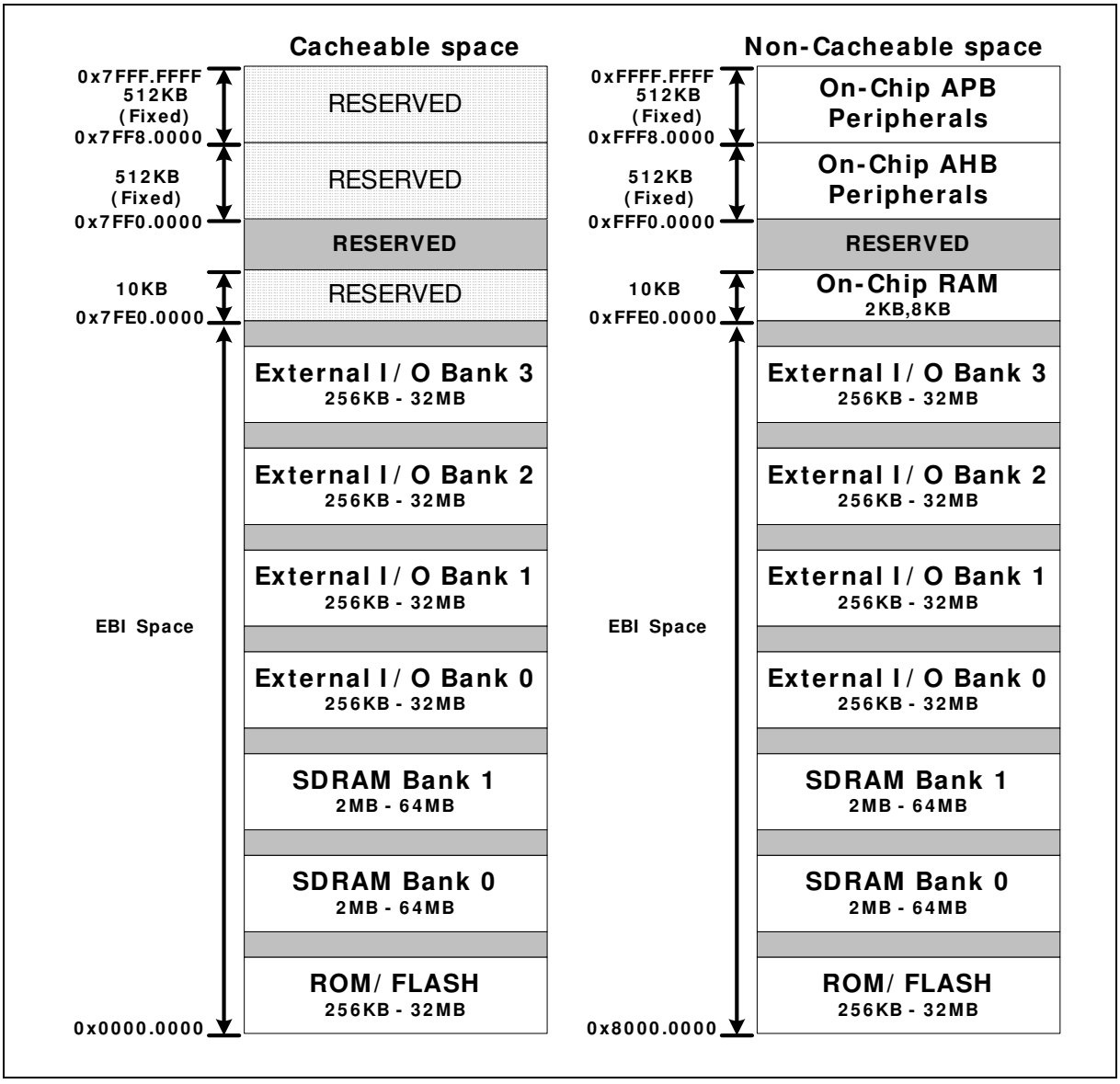

Fig7.2.1 System Memory Map

Table 7.2.1 On-Chip Peripherals Memory Map

BASE ADDRESS	DESCRIPTION
AHB PERIPHERALS	
0xFFF0.0000	Product Identifier Register (PDID)
0xFFF0.0004	Arbitration Control Register (ARBCON)
0xFFF0.0008	PLL Control Register (PLLCON)
0xFFF0.000C	Clock Select Register (CLKSEL)
0xFFF0.1000	EBI Control Register (EBICON)
0xFFF0.1004	ROM/FLASH (ROMCON)
0xFFF0.1008	SDRAM bank 0 - 1
0xFFF0.1018	External I/O 0 - 3
0xFFF0.2000	Cache Controller
0xFFF0.3000	Ethernet MAC Controller 0 - 1
0xFFF0.4000	GDMA 0 - 1
0xFFF0.5000	USB (Host)
0xFFF0.6000	NAT Accelerator
0xFFF6.0000	Reserved
0xFFF7.0000	Reserved
APB Peripherals	
0xFFF8.0000	UART
0xFFF8.1000	Timer 0 - 1, WDOG Timer
0xFFF8.2000	Interrupt Controller
0xFFF8.3000	GPIO

7.2.3 Address Bus Generation

The W90N740 address bus generation is depended on the required data bus width of each memory bank. The data bus width is determined by **DBWD** bits in each bank's control register.

The maximum accessible memory size of each external IO bank is 32M bytes .

Table 7.2.2 Address Bus Generation Guidelines

DATA BUS	EXTERNAL ADDRESS PINS			MAXIMUM ACCESSIBLE
WIDTH	**A [22:0]**	**A23**	**A24**	**MEMORY SIZE**
8-BIT	A22 – A0 (Internal)	A23 (Internal)	A24 (Internal)	32M bytes
16-BIT	A23 – A1 (Internal)	A24 (Internal)	NA	16M half-words
32-BIT	A24 – A2 (Internal)	NA	NA	8M words

7.2.4 Data Bus Connection with External Memory

7.2.4.1. Memory formats

The internal architecture is big endian. The little endian mode only support for external memory. The W90N740 can be configured as big endian or little endian mode by pull up or down the data D14 pin. If D14 is pull-up then it is a little endian mode, otherwise, it is a big endian mode.

Big Endian

In Big endian format, the W90N740 stores the most significant byte of a word at the lowest numbered byte, and the least significant byte at the highest-numbered byte. So the byte at address 0 of the memory system connects to data lines 31 through 24.

For a word aligned address A, Fig7.2.2 shows how the word at address A, the half-word at addresses A and A+2, and the bytes at addresses A, A+1, A+2, and A+3 map on to each other when the **LITTLE** pin is Low.

<table>
<tr><td colspan="32">31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td></tr>
<tr><td colspan="32">Word at address A</td></tr>
<tr><td colspan="16">Half-word at address A</td><td colspan="16">Half-word at address A+2</td></tr>
<tr><td colspan="8">Byte at address A</td><td colspan="8">Byte at address A+1</td><td colspan="8">Byte at address A+2</td><td colspan="8">Byte at address A+3</td></tr>
</table>

Fig. 7.2.2 Big endian addresses of bytes and half-words within words

Little Endian

In Little endian format, the lowest addressed byte in a word is considered the least significant byte of the word and the highest addressed bye is the most significant. So the byte at address 0 of the memory system connects to data lines 7 through 0.

For a word aligned address A, Fig7.2.3 shows how the word at address A, the half-word at addresses A and A+2, and the bytes at addresses A, A+1, A+2, and A+3 map on to each other when **LITTLE** pin is High.

<table>
<tr><td colspan="32">31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</td></tr>
<tr><td colspan="32">Word at address A</td></tr>
<tr><td colspan="16">Half-word at address A+2</td><td colspan="16">Half-word at address A</td></tr>
<tr><td colspan="8">Byte at address A+3</td><td colspan="8">Byte at address A+2</td><td colspan="8">Byte at address A+1</td><td colspan="8">Byte at address A</td></tr>
</table>

Fig. 7.2.3 Little endian addresses of bytes and half-words within words

7.2.4.2. Connection of External Memory with Various Data Width

The system diagram for W90N740 connecting with the external memory is shown in Fig. 7.2.4. Below tables (Table7.2.3 – Table7.2.14) show the program/data path between CPU register and the external memory using little / big endian and word/half-word/byte access.

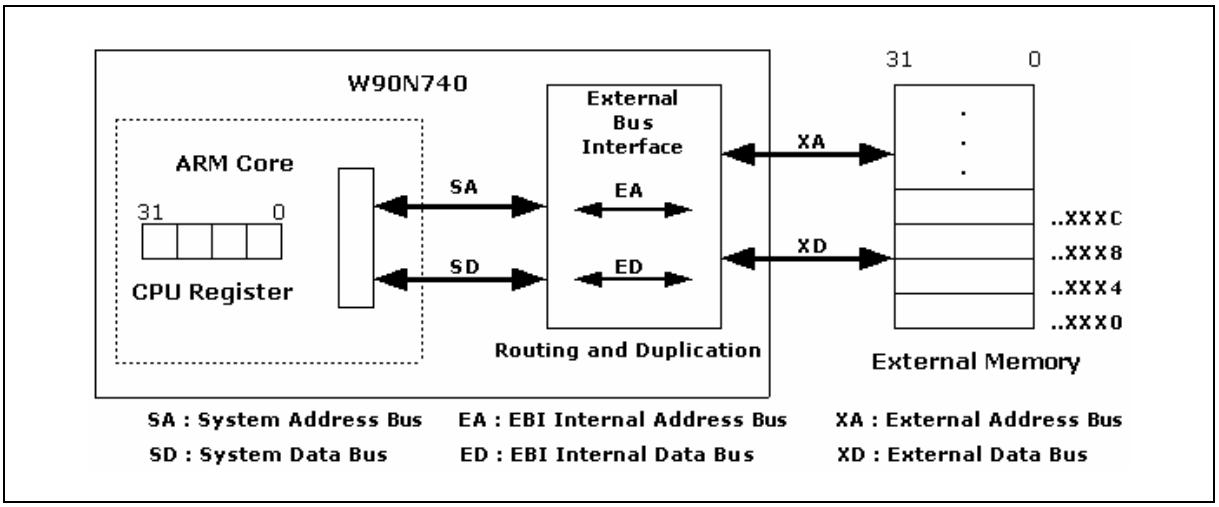

Fig. 7.2.4 Address/Data bus connection with external memory

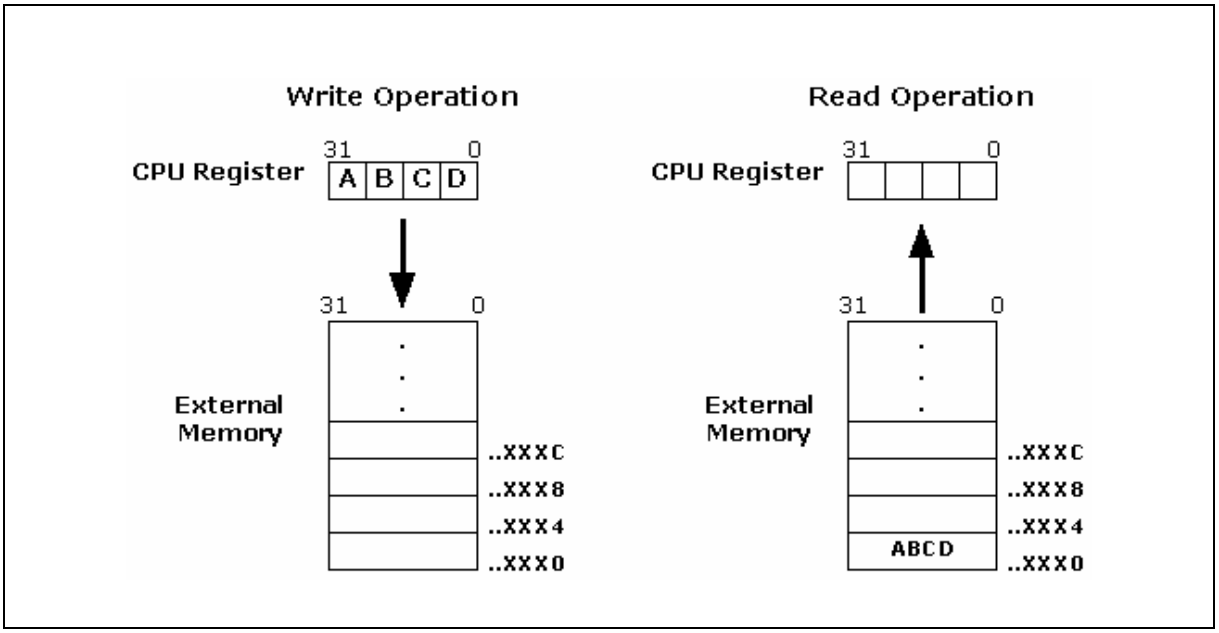

Fig. 7.2.5 CPU register Read/Write with external memory

Table 7.2.3 and Table 7.2.4

Using big-endian and word access, Program/Data path between register and external memory

WA = Address whose LSB is 0, 4, 8, C X = Don't care

nWBE [3-0] / SDQM [3-0] = A means active and U means inactive

Table7.2.3 Word access write operation with Big Endian

ACCESS OPERATION	WRITE OPERATION (CPU REGISTER ➔ EXTERNAL MEMORY)						
XD WIDTH	WORD	HALF WORD		BYTE			
BIT NUMBER CPU REG DATA	31 0 ABCD	31 0 ABCD		31 0 ABCD			
SA	WA	WA		WA			
BIT NUMBER SD	31 0 ABCD	31 0 AB CD		31 0 A B C D			
BIT NUMBER ED	31 0 ABCD	15 0 AB	15 0 CD	7 0 A	7 0 B	7 0 C	7 0 D
XA	WA	WA	WA+2	WA	WA+1	WA+2	WA+3
NWBE [3-0] / SDQM [3-0]	AAAA	XXAA	XXAA	XXXA	XXXA	XXXA	XXXA
BIT NUMBER XD	31 0 ABCD	15 0 AB	15 0 CD	7 0 A	7 0 B	7 0 C	7 0 D
BIT NUMBER EXT. MEM DATA	31 0 ABCD	15 0 AB	15 0 CD	7 0 A	7 0 B	7 0 C	7 0 D
TIMING SEQUENCE		1st write	2nd write	1st write	2nd write	3rd write	4th write

Table7.2.4 Word access read operation with Big Endian

ACCESS OPERATION	READ OPERATION (CPU REGISTER ← EXTERNAL MEMORY)						
XD WIDTH	WORD	HALF WORD		BYTE			
Bit Number CPU Reg Data	31 0 ABCD	31 0 CDAB		31 0 DCBA			
SA	WA	WA		WA			
Bit Number SD	31 0 ABCD	31 0 CD AB		31 0 D C B A			
Bit Number ED	31 0 ABCD	31 0 CD XX	31 0 CD AB	31 0 D X X X	31 0 D C X X	31 0 D C B X	31 0 D C B A
XA	WA	WA	WA+2	WA	WA+1	WA+2	WA+3
SDQM [3-0]	AAAA	XXAA	XXAA	XXXA	XXXA	XXXA	XXXA
Bit Number XD	31 0 ABCD	15 0 CD	15 0 AB	7 0 D	7 0 C	7 0 B	7 0 A
Bit Number Ext. Mem Data	31 0 ABCD	15 0 CD	15 0 AB	7 0 D	7 0 C	7 0 B	7 0 A
Timing Sequence		1st read	2nd read	1st read	2nd read	3rd read	4th read

Table 7.2.5 and Table 7.2.6

Using big-endian and half-word access, Program/Data path between register and external memory.

HA = Address whose LSB is 0, 2, 4, 6, 8, A, C, E HAL = Address whose LSB is 0, 4, 8, C

HAU = Address whose LSB is 2, 6, A, E X = Don't care

nWBE [3-0] / SDQM [3-0] = A means active and U means inactive

Table7.2.5 Half-word access write operation with Big Endian

ACCESS OPERATION	WRITE OPERATION (CPU REGISTER → EXTERNAL MEMORY)				
XD WIDTH	WORD		HALF WORD	BYTE	
BIT NUMBER CPU REG DATA	31 0 ABCD		31 0 ABCD	31 0 ABCD	
SA	HAL	HAU	HA	HA	
BIT NUMBER SD	31 0 CD CD	31 0 CD CD	31 0 CD CD	31 0 CD CD	31 0 CD CD
BIT NUMBER ED	31 0 CD CD	31 0 CD CD	31 0 CD CD	7 0 C	7 0 D
XA	HAL	HAL	HA	HA	HA+1
NWBE [3-0] / SDQM [3-0]	AAUU	UUAA	XXAA	XXXA	XXXA
BIT NUMBER XD	31 0 CD CD	31 0 CD CD	15 0 CD	7 0 C	7 0 D
BIT NUMBER EXT. MEM DATA	31 16 CD	15 0 CD	15 0 CD	7 0 C	7 0 D
TIMING SEQUENCE				1st write	2nd write

Table7.2.6 Half-word access read operation with Big Endian

ACCESS OPERATION	READ OPERATION (CPU REGISTER ← EXTERNAL MEMORY)				
XD WIDTH	WORD		HALF WORD	BYTE	
BIT NUMBER CPU REG DATA	15 0 AB	15 0 CD	15 0 CD	15 0 DC	
SA	HAL	HAU	HA	HA	
BIT NUMBER SD	15 0 AB	15 0 CD	15 0 CD	15 0 DC	
BIT NUMBER ED	15 0 AB	15 0 CD	15 0 CD	15 0 DX	15 0 DC
XA	HAL	HAL	HA	HA	HA+1
SDQM [3-0]	AAUU	UUAA	XXAA	XXXA	XXXA
BIT NUMBER XD	31 0 AB CD	31 0 AB CD	15 0 CD	7 0 D	7 0 C
BIT NUMBER EXT. MEM DATA	31 0 ABCD		15 0 CD	7 0 D	7 0 C
TIMING SEQUENCE				1st read	2nd read