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8-BIT CID MICROCONTROLLER

Table of Contents-

1. GENERAL DESCRIPTION

The W925E/C240 is an all in one single 8-bit micro-controller with widely used Calling Identity Delivery (CID) function. The 8-bit CPU core is based on the 8051 family; therefore, all the instructions are compatible to the Turbo 8051 series. The CID part consisted of FSK decoder, DTMF receiver, CPE* Alert Signal (CAS) detector and Ring detector. Also built-in DTMF generator and FSK generator with baud rate 1200 bps (bits/sec). Using W925E/C240 can easily implement the CID adjunct box and the feature phone or Short Message Service (SMS) phone with CID function. The main features are listed in the next section.

2. FEATURES

- **APPLICATION**: The ***SMS*** phone with CID function and CID adjunct box.
- **CPU**: 8-bit micro-controller is similar to the 8051 family.
  - – EEPROM type(E version) operating voltage:
    μC: Depend on the operating vol. option. Either 2.4 to 3.6V or 3.0 to 5.5V for operating. If 2.4 to 3.6V be selected, the μC operating range is from 2.4 to 3.6V, else if 3.0 to 5.5V be selected, the μC operating range is from 3.0 to 5.5V.

    CID: 3.0 to 5.5V.
  - – MASK type(C version) operating voltage:
    μC: 2.2 to 5.5V.

    CID: 3.0 to 5.5V.
- **Dual-clock operation:**
  - – Main oscillator: 3.58MHz crystal for CID and DTMF function. And built-in RC oscillator.
  - – Sub oscillator: 32768Hz crystal.
  - – Main and sub oscillators are enable/disable by bit control individually.
- **ROM**: 256K bytes internal flash EEPROM/MASK ROM type.
  - – Up 128K bytes for program ROM.
  - – Total 256K bytes for look-up table ROM.
  - – Separate 256K into 4 pages, each page is 64K addressable.
- **RAM**:
  - – 256 bytes on chip scratch-pad RAM.
  - – 8K bytes on chip RAM for MOVX instruction.
- **CID**
  - – Compatible with Bellcore TR-NWT-000030 & SR-TSV-002476, British Telecom(BT) SIN227, U.K. Cable Communication Association(CCA) specification.
  - – FSK modulator/demodulator: for Bell 202 and ITU-T V.23 FSK with 1200-baud rate.
  - – CAS detector: for dual tones of Bellcore CAS and BT Idle State and Loop State Dual Tone Alert Signal (DTAS).
  - – DTMF generator/receiver;
  - – Ring detector: for line reversal for BT, ring burst for CCA or ring signal for Bellcore.
  - – Two independent OP amps with adjustable gain for Tip/Ring and Telephone Hybrid connections.

- **I/O**: 40 I/O pins.
  - P0: Bit and byte addressable. I/O mode can be bit controlled. Open drain type.
  - P1~P3: Bit and byte addressable. Pull high and I/O mode can be bit controlled.
  - P4: Byte addressable. Pull high and I/O mode can be bit controlled.

    Note: "CPE*" Customer Premises Equipment
- **Power mode**:
  - **Dual-clock slow operation mode**: System is operated by the sub-oscillator (Fosc=Fs and Fm is stopped)
  - **Idle mode**: CPU hold. The clock to the CPU is halted, but the interrupt, timer and watchdog timer block work normally but CID function is disabled.
  - **Power down mode**: All activity is completely stopped and power consumption is less than 1 μA.
- **Timer**: 2 13/16-bit timers, or 8-bit auto-reload timers, that are Timer0 and Timer1.
- **Watchdog timer**: WDT can be programmed by the user to serve as a system monitor.
- **Interrupt:** 11 interrupt sources with two levels of priority.
  - 4 interrupts from INT0, INT1, INT2 and INT3.
  - 2 interrupts from Timer0, Timer1.
  - 1 interrupt from Serial port.
  - 1 interrupt from CID.
  - 1 interrupt from 13/14-bit Divider.
  - 1 interrupt from Comparator.
  - 1 interrupt from Watch Dog Timer.
- **Divider:** 13/14 bit divider, clock source from sub-oscillator, therefore, DIVF set every 0.25/0.5 second.
- **Comparator:**
  - Comparator: 1 analog inputs from VNEG pin, 2 reference input pins, one is from VPOS pin and another is from internal regulator output.
- **Serial port:**
  - An 8-bit serial transceiver with SCLK and SDATA.
- **Package:**
  - 100pin LQFP: The part numbers are W925E240 & W925C240
  - Lead free 100pin LQFP: The part numbers are W925E240FG & W925G240

3. PIN CONFIGURATION

Figure 3-1 shows the pin assignment. The package type is 100pin QFP.

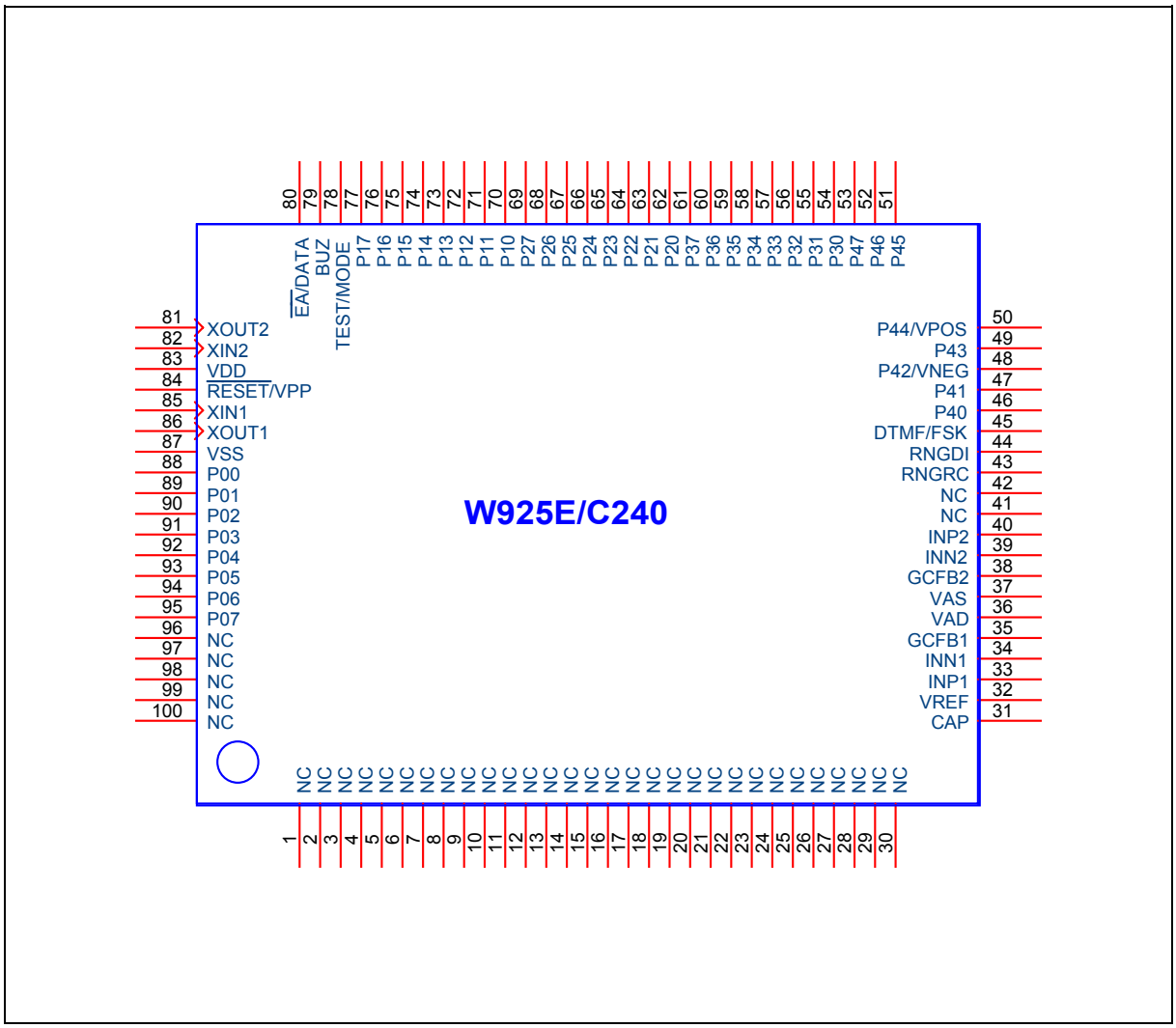


Figure 3-1 W925E/C240 Pin Configuration

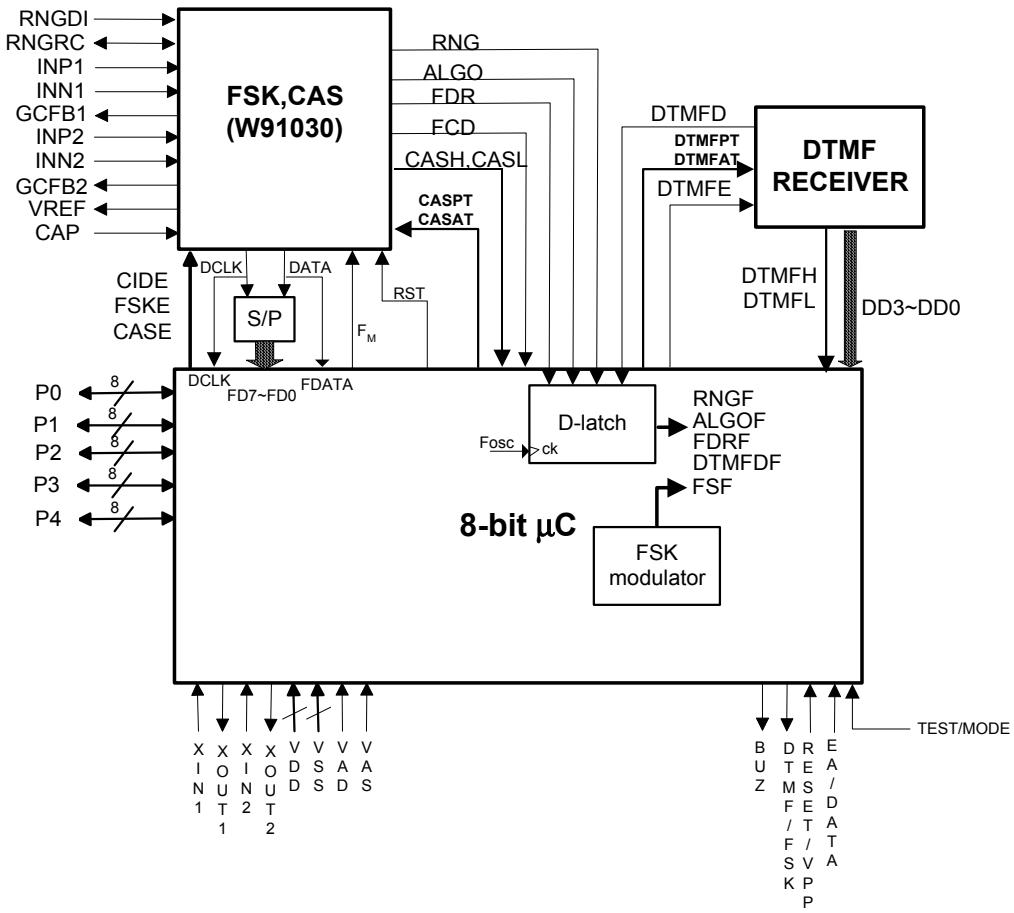
4. PIN DESCRIPTION

NAME	I/O	DESCRIPTION
TEST/MODE	I/O	TEST pin. In E version (EEPROM type), it works as a Mode pin to select programming mode. In C version (Mask type), this pin with internal pull-low resistor.
$\overline{EA}$ /DATA	I, I/O	Set high for normal function. In E version, it works as a Data pin. In C version, this pin with internal pull-high resistor.
$\overline{RESET}$ /VPP	I	RESET pin. A low pulse causes the whole chip reset. In E version, this pin works as a VPP pin, which is a supply programming voltage. In C version, this pin with internal pull-high resistor.
RNGDI	I	Ring Detect Input (Schmitt trigger input). Used for ring detection and line reversal detection. Must maintain a voltage between VAD and VAS.
RNGRC	O	Ring RC (Open drain output and Schmitt trigger input). Used to set the time interval from the end of RNGDI pin to the inactive condition of the RNGON pin. An external resistor must connected to VAD and a capacitor connected to V_{SS}, the time interval is the RC time constant.
CAP	O	Must be connected 0.1μF capacitor to V_{SS}.
VREF	O	Reference Voltage. Nominally, VDD/2 is used to bias the input of the gain control op-amp.
GCFB1	O	Op-amp1 Feed-back Gain Control signal. Select the input gain by connecting this pin and the INN1 pin with feedback resistor. It is recommended that the op-amp1 be set to unity gain.
INN1	I	Inverting Input of the gain control op-amp1.
INP1	I	Non-inverting Input of the gain control op-amp1.
GCFB2	O	Op-amp2 Feed-back Gain Control signal. Select the input gain by connecting this pin and the INN2 pin with feedback resistor. It is recommended that the op-amp2 be set to unity gain.
INN2	I	Inverting Input of the gain control op-amp2.
INP2	I	Non-inverting Input of the gain control op-amp2.
VAD	I	Analog voltage supply.
VAS	I	Analog ground.
V_{DD}	I	Digital voltage supply.
V_{SS}	I	Digital ground.
XOUT1	O	Output pin for main-oscillator. Connected to 3.58MHz crystal for CID function.
XIN1	I	Input pin for main-oscillator. Connected to 3.58MHz crystal for CID function.

Pin Description, continued

NAME	I/O	DESCRIPTION
XOUT2	O	Output pin for sub-oscillator. Connected to 32.768KHz crystal only. Suggest to add an external capacitor about 10~30pF to ground(VSS) for the accuracy of the oscillator.
XIN2	I	Input pin for sub-oscillator. Connected to 32.768KHz crystal only. Suggest to add an external capacitor about 10~30pF to ground(VSS) for the accuracy of the oscillator.
DTMF/FSK	O	FTE=0, Dual-Tone Multi-Frequency(DTMF) signal output FTE=1, FSK signal output
BUZ	O	Buzzer output pin. If buzzer function is disabled, BUZ pin is in floating state.
P00-P07	I/O	Input/output port0. Port0 data can be bit controlled. The I/O mode is controlled by P0IO register. Port0 is open drain type when it is configured as output mode.
P10-P17	I/O	Input/output port1 with pull high resistors. Port1 data can be bit controlled. The I/O mode is controlled by P1IO register. The P10-P13 and P14-P17 indicate the external interrupt pins(INT2 and INT3)
P20-P27	I/O	Input/output port2 with pull high resistors. Port2 data can be bit controlled. The I/O mode is controlled by P2IO register.
P30-P37	I/O	Input/output port3 with pull high resistors. Port3 data can be bit controlled. The I/O mode is controlled by P3IO register. The special function of port3 is referred to the description of P3 register.
P40-P47	I/O	Contents are byte controlled. Pull high and I/O mode can be bit controlled. The special function of P4 is referred to the description of P4 register.
VPOS, VNEG	I	The comparator V+, V- analog input pins. Share pin with P4.2 and P4.4

5. BLOCK DIAGRAM



6. FUNCTIONAL DESCRIPTION

The W925E/C240 is an 8-bit micro-controller with CID function. The 8-bit micro-control has the same instruction set as the 8051 family, with one addition: DEC DPTR (op-code A5H, the DPTR is decreased by 1). In addition, the W925E/C240 contains on-chip 8K bytes MOVX RAM.

ROM

There are 256K bytes EEPROM/MASK ROM. Only 128K bytes EEPROM/MASK ROM is used for program code. The completely 256K bytes EEPROM/MASK ROM can be used for the look-up table memory.

On-chip Data RAM

The W925E/C240 has 8K normal RAM which address is from 0000H to 1FFFH. It only can be accessed by MOVX instruction; this on-chip RAM is optional under software control. The on-chip data RAM is not used for executable program memory. There is no conflict or overlap among the 256 bytes scratchpad RAM and the 8K Bytes MOVX RAM as they use different addressing modes and separate instructions.

CID

The CID functions include the FSK decoder, CAS detector, and DTMF decoder and ring detector.

FSK Modulator

Support ITU-T V.23 and Bellcore 202 FSK transmit modulated signal.

DTMF Modulator

The W925E/C240 built-in dual tone multi-frequency generator.

I/O Ports:

The W925E/C240 has five 8-bit I/O ports giving 40 lines. Port0 to Port3 can be used as an 8-bit general I/O port with bit-addressable. The I/O mode of each port is controlled by PxIO registers. Port1 to Port4 have internal pull high resistors enabled/disabled by PxH registers. Port0 is open-drain type in output mode.

Serial I/O Port

The serial port, through P4.0 (SCLK) and P4.1 (SDATA), is an 8-bit synchronous serial I/O interface.

Timers

The W925E/C240 has two 13/16-bit timers or an 8 bits auto-reload timers. An independent watchdog timer is used as a system monitor or as a very long time period timer. A divider can produce the divider interrupt in every period of 0.5S or 0.25S.

Comparator

The W925E/C240 has an internal comparator with one external analog signal input path VNEG and an external path VPOS or a regulator voltage for the reference input REF1.

Interrupts

The W925E/C240 provides 11 interrupt resources with two priority level, including 4 external interrupt sources, 2 timer interrupts, 1 CID interrupt, 1 divider interrupt, 1 serial port interrupt, 1 comparator interrupt and 1 watchdog timer interrupt.

Power Management

The W925E/C240 has IDLE and POWER DOWN modes of operation. In the IDLE mode, the clock to the CPU core is stopped however the functions of the timers, divider, CID and interrupts are active continuously. In the POWER DOWN mode, both of the system clock stop oscillating and the chip operation is completely stopped. POWER DOWN mode is the state of the lowest power consumption.

6.1 Memory Organization

The W925E/C240 separates the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes and look-up table data, while the Data Memory is used to store data or for memory mapped devices.

Program Memory

The Program Memory on the W925E/C240 can be up to 256K bytes that are divided into 4 pages, each page has the size of 64K bytes. The upper 128K bytes are used to store the op-codes and the whole 256K can be used to store look-up table data. Because the op-code is 64K addressable, a PG bit in PAGE register decides which ROM page between page0, page1 is enabled, and the ALU fetches the op-code from the selected ROM page. If PG=0, ALU fetches the op-code from page0. If PG=1, ALU fetches the op-code from page1. When MOVC instruction is executed, ALU fetches the look-up table data according the indication of LT1 and LT0 bits. The value of LT1 and LT0 indicates which ROM page is active for look-up table instruction.

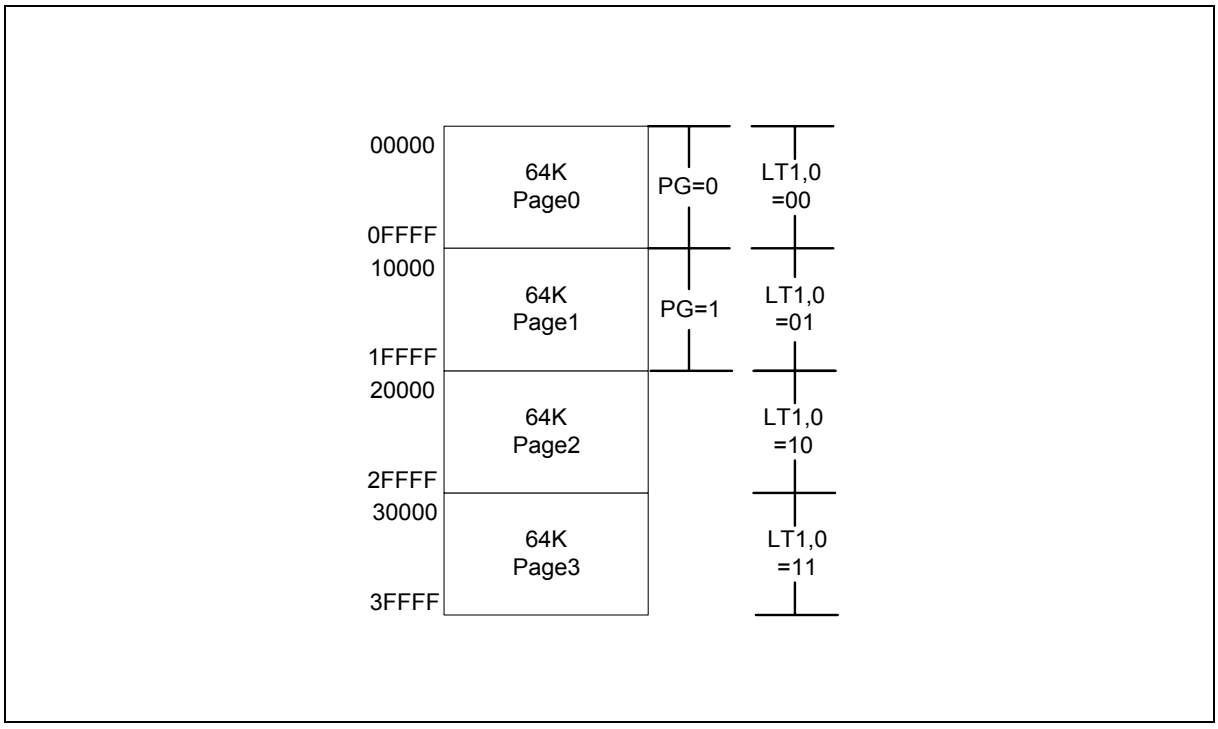


Figure 6-1 Program Memory Map

Data Memory

The W925E/C240 contains on-chip 8K MOVX RAM of Data Memory, which can only be accessed by MOVX instructions from the address 0000H to 1FFFH. In addition, the W925E/C240 has 256 bytes of on-chip scratchpad RAM. This can be accessed either by direct addressing or by indirect addressing. There are also Special Function Registers (SFRs), which can only be accessed by direct addressing. Since the scratchpad RAM is only 256 bytes, it can be used only when data contents are small. In the event that larger data contents are present, the only one selection is on-chip MOVX RAM. The on-chip MOVX RAM can only be accessed by a MOVX instruction. However, the on-chip RAM has the fastest access times. The memory map is shown Figure 6-2 and Figure 6-3 shows the scratched-pad RAM/register addressing.

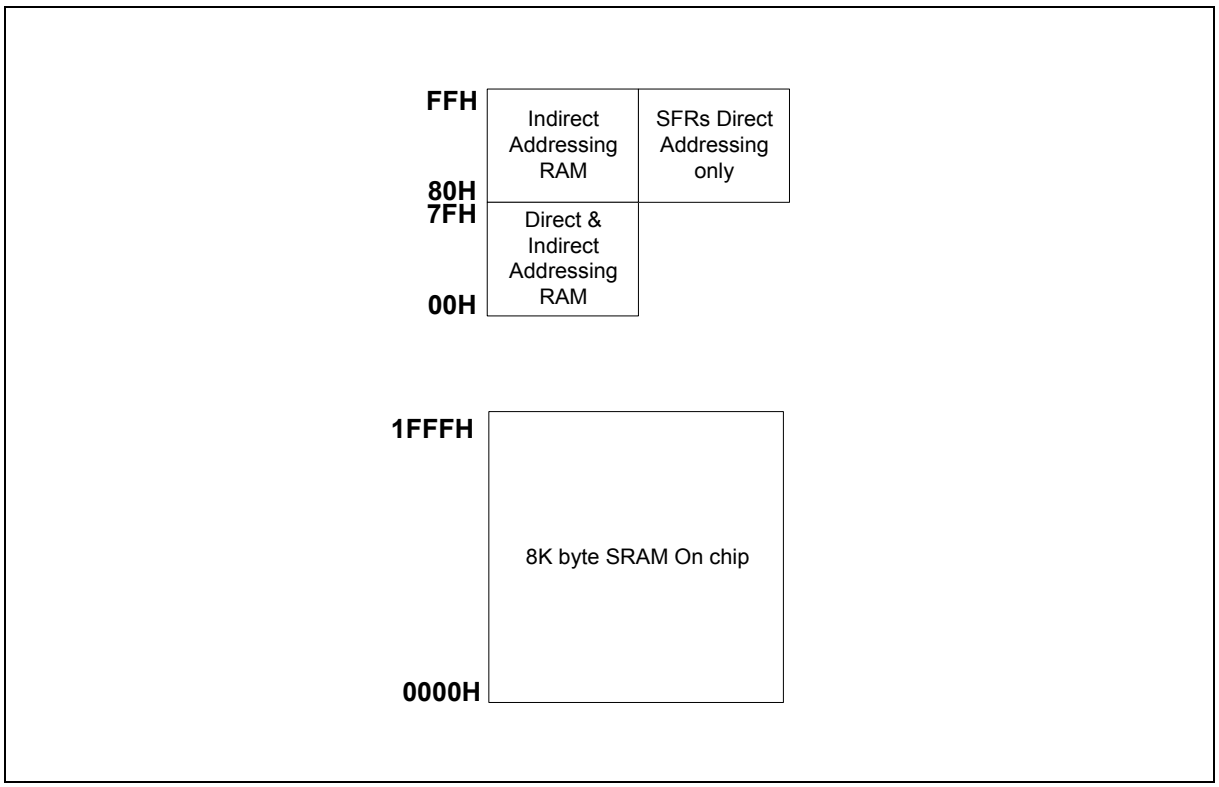


Figure 6-2 memory map

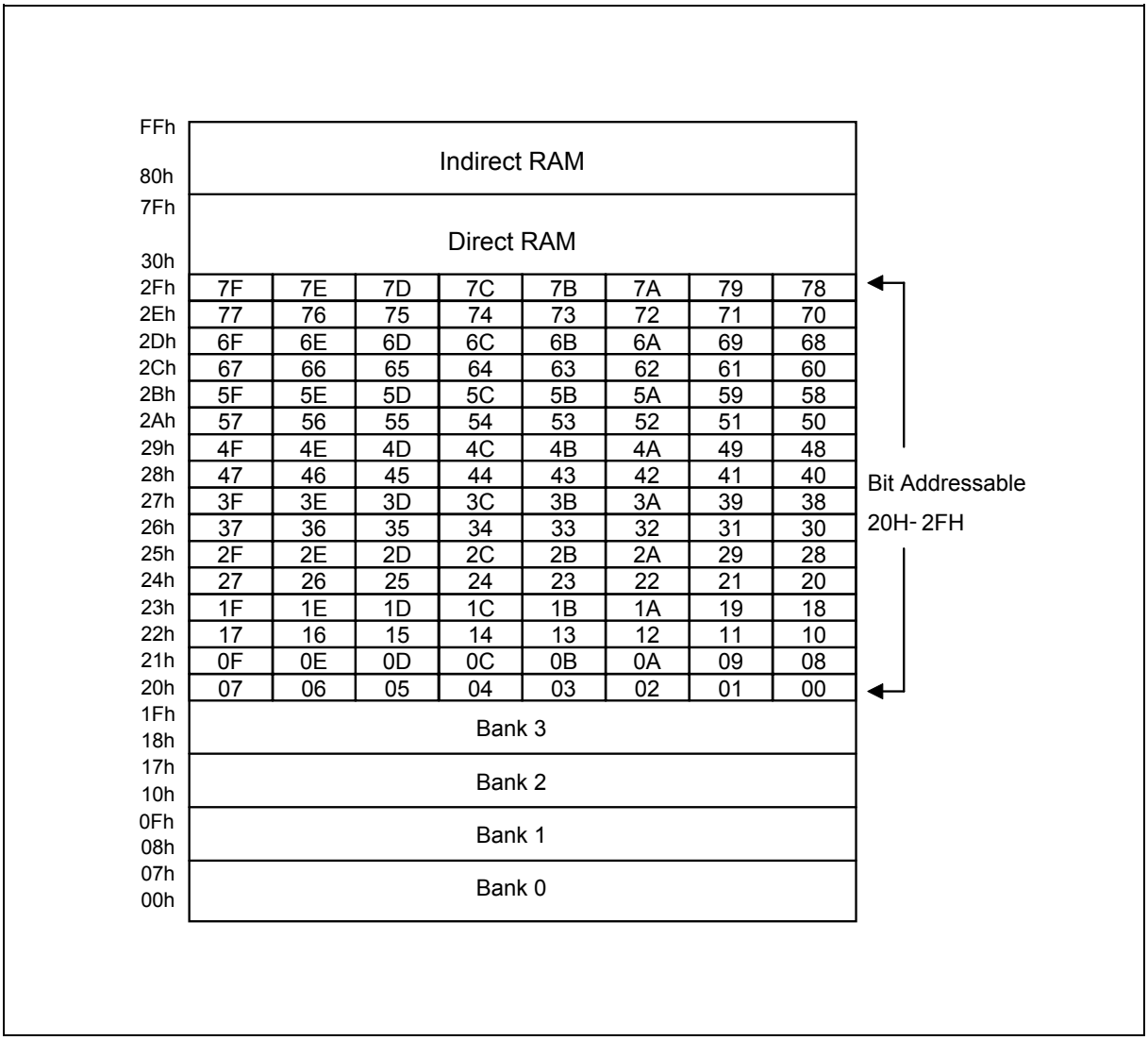


Figure 6-3 Scratchpad RAM/Register Addressing

6.2 Special Function Registers

The W925E/C240 uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes.

The SFRs reside in the register locations 80-FFh and accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where one wishes to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. The list of SFRs is as follows. The table is condensed with eight locations per row. Empty locations indicate that there are no registers at these addresses. The content of reserved bits or registers is not guaranteed.

Table 1 Special Function Register Location Table

F8	EIP	CIDGD	CIDGA					
F0	B							
E8	EIE							
E0	ACC							
D8	WDCON							
D0	PSW							
C8	DIVC							
C0	SCON1	SBUF1	REGVC		PMR	STATUS	FSKTC	FSKTB
B8	IP		DTMFG	COMPR	IRC1	IRC2	CASPT	CASAT
B0	P3	CIDR	CIDFG	CIDPCR	FSKDR	DTMFDR	DTMFPT	DTMFAT
A8	IE						P4IO	
A0	P2	HB	P4H				P4	
98				P1EF		P1H	P2H	P3H
90	P1	EXIF	RPAGE	P1SR	P0IO	P1IO	P2IO	P3IO
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON1	CKCON2
80	P0	SP	DPL	DPH	DPL1	DPH1	DPS	PCON

Note: The SFRs in the column with dark borders are bit-addressable.

A brief description of the SFRs now follows.

PORT 0 (initial=FFh, input mode)

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

P0: P0 can be selected as input or output mode by the P0IO register. At initial reset, P0IO is set to FFH, P0 is used as input mode. When P0IO is set to 0, the P0 is used as CMOS open drain mode.

STACK POINTER (initial=07H)

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

SP: The Stack Pointer stores the scratchpad RAM address where the stack begins. In other words, it always points to the top of the stack.

DATA POINTER LOW (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

DPL: This is the low byte of the standard 8052 16-bit data pointer.

DATA POINTER HIGH (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

DPH: This is the high byte of the standard 8052 16-bit data pointer.

DATA POINTER LOW1 (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	DPL1.7	DPL1.6	DPL1.5	DPL1.4	DPL1.3	DPL1.2	DPL1.1	DPL1.0

Mnemonic: DPL1 Address: 84h

DPL1: This is the low byte of the new additional 16-bit data pointer. That has been added to the W925E/C240. The user can switch between DPL, DPH and DPL1, DPH1 simply by setting register DPS.0 = 1. The instructions that use DPTR will now access DPL1 and DPH1 in place of DPL and DPH. If they are not required, they can be used as conventional register locations by the user.

DATA POINTER HIGH1 (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	DPH1.7	DPH1.6	DPH1.5	DPH1.4	DPH1.3	DPH1.2	DPH1.1	DPH1.0

Mnemonic: DPH1 Address: 85h

DPH1: This is the high byte of the new additional 16-bit data pointer. That has been added to the W925E/C240. The user can switch between DPL, DPH and DPL1, DPH1 simply by setting register DPS = 1. The instructions that use DPTR will now access DPL1 and DPH1 in place of DPL and DPH. If they are not required, they can be used as conventional register locations by the user.

DATA POINTER SELECT (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	DPS.0

Mnemonic: DPS Address: 86h

DPS.0: This bit is used to select either the DPL,DPH pair or the DPL1,DPH1 pair as the active Data Pointer. When set to 1, DPL1,DPH1 will be selected, otherwise DPL,DPH will be selected.

DPS.1-7: These bits are reserved, but will read 0.

POWER CONTROL (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	-	-	-	IDLT	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

IDLT: This bit controls the idle mode type. In idle mode when idle mode is released by any interrupt, if IDLT=1 it will not jump to the corresponding interrupt; if IDLT=0 it will jump to the corresponding interrupt.

GF1-0: These two bits are general-purpose user flags.

PD: Setting this bit causes the W925E/C240 to go into the POWER DOWN mode. In this mode, all the clocks are stopped and program execution is frozen. Power down mode can be released by INT0~INT3 and ring detection of CID interrupt.

IDL: Setting this bit causes the W925E/C240 to go into the IDLE mode. The type of idle mode is selected by IDLT. In this mode the clocks to the CPU are stopped, so program execution is frozen. However, the clock path to the timers blocks and interrupt blocks is not stopped, and these blocks continue operating.

TIMER CONTROL (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

TF1: Timer 1 overflows flag. This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.

TR1: Timer 1 runs control. This bit is set or cleared by software to turn timer on or off.

TF0: Timer 0 overflows flag. This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.

TR0: Timer 0 runs control. This bit is set or cleared by software to turn timer on or off.

IE1: Interrupt 1 edge detects: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise, it follows the pin.

IT1: Interrupt 1 type control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

IE0: Interrupt 0 edge detects: Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise, it follows the pin.

IT0: Interrupt 0 type control. Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0

Mnemonic: TMOD Address: 89h

Bit7~4 control timer 1, bit3~0 control timer0

GATE: Gating control. When this bit is set, Timer x is enabled only while $\overline{INTx}$ pin is high and TRx control bit is set. When cleared, Timer x is enabled whenever TRx control bit is set.

C/$\overline{T}$: Timer or Counter Select. When cleared, the timer is incremented by internal clocks. When set, the timer counts high-to-low edges of the Tx pin.

Note: X is either 0 or 1.

M1, M0: Mode Select bits:

M1	M0	Mode
0	0	Mode 0: 13-bits timer
0	1	Mode 1: 16-bits timer
1	0	Mode 2: 8-bits with auto-reload from Thx
1	1	Reserved

TIMER 0 LOW BYTE (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

TL0.7-0: Timer 0 low byte register.

TIMER 1 LOW BYTE (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

TL1.7-0: Timer 1 low byte register.

TIMER 0 HIGH BYTE (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

TH0.7-0: Timer 0 high byte register.

TIMER 1 HIGH BYTE (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

TH1.7-0: Timer 1 high byte register.

CLOCK CONTROL1 (initial=00H)

Bit:	7	6	5	4	3	2	1	0
	WD1	WD0	T1S1	T1S0	T0S1	T0S0	DIVS	$\overline{M}$/S

Mnemonic: CKCON1 Address: 8Eh

WD1-0: Watchdog timer mode select bits: These bits determine the time-out period for the watchdog timer. In all four time-out options the reset time-out is 512 clocks more than the interrupt time-out period.

WD1	WD0	Interrupt time-out	Reset time-out
0	0	Fosc/2^{12}	Fosc/2^{12} + 512
0	1	Fosc/2^{15}	Fosc/2^{15} + 512
1	0	Fosc/2^{18}	Fosc/2^{18} + 512
1	1	Fosc/2^{21}	Fosc/2^{21} + 512

T0S0-1&T1S0-1: Timer0 & Timer1 clock source mode select bits. These bits determine the timer0 & timer1 clock source.

T0S1 (T1S1)	T0S0 (T1S0)	Prescale Clock Source
0	0	Fosc/2^{2}
0	1	Fosc/2^{6}
1	0	Fosc/2^{10}
1	1	Fs

DIVS: Divider clock source control bit 1:

DIVS = 0 : Fs/2^{13}

DIVS= 1 : Fs/2^{14}

$\overline{M}$/S: System clock source control bit: $\overline{M}$/S = 0 : Fosc = XIN1 (F_M)
$\overline{M}$/S = 1 : Fosc = XIN2 (Fs)

CLOCK CONTROL2 (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	ENBUZ	BUZSL	KT1	KT0	-	-	-	-

Mnemonic: CKCON2 Address: 8Fh

ENBUZ: When ENBUZ=1 the BUZ pin works as buzzer output, otherwise BUZ pin is in floating state.

BUZSL: Buzzer output selection. When BUZSL=0 BUZ is the output of octave tone. When BUZZL=1, BUZ is the output of key tone.

KT1-0: Key tone frequency sources from divider. When divider is enable, KT1 and KT0 determines the key tone frequency.

KT1	KT0	Key tone frequency
0	0	Low
0	1	512Hz
1	0	1024Hz
1	1	2048Hz

PORT 1 (initial=FFH,input mode)

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7-0: P1 can be selected as input or output mode by the P1IO register, at initial reset, P1IO is set to 1, so P1 is used as input mode. When P1IO is set to 0, the P1 is used as CMOS output mode. When P1EF are set and P1IO are set as input mode P1 can be used as external interrupt source. The functions are listed below.

P1.0 : INT2.0 External Interrupt 2
P1.1 : INT2.1 External Interrupt 2
P1.2 : INT2.2 External Interrupt 2
P1.3 : INT2.3 External Interrupt 2
P1.4 : INT3.0 External Interrupt 3
P1.5 : INT3.1 External Interrupt 3
P1.6 : INT3.2 External Interrupt 3
P1.7 : INT3.3 External Interrupt 3

EXTERNAL INTERRUPT FLAG (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	-	-	-	COMPF	DIVF	CIDF	IE3	IE2

Mnemonic: EXIF Address: 91h

COMPF: Comparator flag. Set by hardware when RESC bit is from low to high.

DIVF: Divider overflow flag.

CIDF: CID interrupt flag. Set by hardware when at least one of CID flags is set.

IE3: External Interrupt 3 flag. Set by hardware when a falling edge is detected on INT3.

IE2: External Interrupt 2 flag. Set by hardware when a falling edge is detected on INT2.

ROM PAGE POINTER (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	-	-	LT1	LT0	-	-	-	PG

Mnemonic: RPAGE Address: 92h

LT1 and LT0 determine the ROM page of the instruction MOVC reading the content from ROM.

	ROM PAGE	**Rom address**
(LT1, LT0) = (0, 0)	Page 0	00000H-0FFFFH
(LT1, LT0) = (0, 1)	Page 1	10000H-1FFFFH
(LT1, LT0) = (1, 0)	Page 2	20000H-2FFFFH
(LT1, LT0) = (1, 1)	Page 3	30000H-3FFFFH

PG = 0 indicates the executing program is in page 0, from 00000H-0FFFFH

PG = 1 indicates the executing program is in page 1, from 10000H-1FFFFH

P1 PINS STATUS (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	P1.7SR	P1.6SR	P1.5SR	P1.4SR	P1.3SR	P1.2SR	P1.1SR	P1.0SR

Mnemonic: P1SR Address: 93h

P1SR: Set when a falling edge is detected on the corresponding P1 pin, clear by software.

P0 I/O PORT CONTROL (initial = FFH)

Bit:	7	6	5	4	3	2	1	0
	P0.7IO	P0.6IO	P0.5IO	P0.4IO	P0.3IO	P0.2IO	P0.1IO	P0.0IO

Mnemonic: P0IO Address: 94h

P0IO: P0 pins I/O control.

1: input mode

0: output mode

P1 I/O PORT CONTROL (initial = FFH)

Bit:	7	6	5	4	3	2	1	0
	P1.7IO	P1.6IO	P1.5IO	P1.4IO	P1.3IO	P1.2IO	P1.1IO	P1.0IO

Mnemonic: P1IO Address: 95h

P1IO: P1 pins I/O control.
1: input mode
0: output mode

P2 I/O PORT CONTROL (initial = FFH)

Bit:	7	6	5	4	3	2	1	0
	P2.7IO	P2.6IO	P2.5IO	P2.4IO	P2.3IO	P2.2IO	P2.1IO	P2.0IO

Mnemonic: P2IO Address: 96h

P2IO: P2 pins I/O control.
1: input mode
0: output mode

P3 I/O PORT CONTROL (initial = FFH)

Bit:	7	6	5	4	3	2	1	0
	P3.7IO	P3.6IO	P3.5IO	P3.4IO	P3.3IO	P3.2IO	P3.1IO	P3.0IO

Mnemonic: P3IO Address: 97h

P3IO: P3 pins I/O control.
1: input mode
0: output mode

P1 PINS INTERRUPT EABLE (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	P1.7EF	P1.6EF	P1.5EF	P1.4EF	P1.3EF	P1.2EF	P1.1EF	P1.0EF

Mnemonic: P1EF Address: 9Bh

P1EF: P1 pins interrupt function enabled/disabled register
0: disable
1: enable

P1 PULL-HIGH CONTROL (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	P1.7H	P1.6H	P1.5H	P1.4H	P1.3H	P1.2H	P1.1H	P1.0H

Mnemonic: P1H Address: 9Dh

P1H: Port1 pins pull-high resistor enable/disable

1: enable

0: disable

P2 PULL-HIGH CONTROL (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	P2.7H	P2.6H	P2.5H	P2.4H	P2.3H	P2.2H	P2.1H	P2.0H

Mnemonic: P2H Address: 9Eh

P2H: Port1 pins pull-high resistor enable/disable

1: enable

0: disable

P3 PULL-HIGH CONTROL (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	P3.7H	P3.6H	P3.5H	P3.4H	P3.3H	P3.2H	P3.1H	P3.0H

Mnemonic: P3H Address: 9Fh

P3H: Port1 pins pull-high resistor enable/disable

1: enable

0: disable

PORT 2 (initial = FFH,input mode)

Bit:	7	6	5	4	3	2	1	0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

Mnemonic: P2 Address: A0h

P2.7-0: Port 2 is an I/O port with internal pull-high resistor. P2 can be selected as input or output mode by the P2IO register. At initial reset, P2 is used as input mode. When P2IO is set to 0, P2 is used as CMOS output mode.

HIGH BYTE REGISTER (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	HB.7	HB.6	HB.5	HB.4	HB.3	HB.2	HB.1	HB.0

Mnemonic: HB Address: A1h

This register contains the high byte address during execution of " MOVX @Ri, " instructions.

P4 PULL-HIGH CONTROL (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	P4.7H	P4.6H	P4.5H	P4.4H	P4.3H	P4.2H	P4.1H	P4.0H

Mnemonic: P4H Address: A2h

P4H: Port4 pins pull-high resistor enable/disable

1: enable

0: disable

PORT 4 (initial = FFH,input mode)

Bit:	7	6	5	4	3	2	1	0
	P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0

Mnemonic: P4 Address: A6h

P4.7-0: Port 4 is an I/O port with internal pull-high resistor. P4 can be selected as input or output mode by the P4IO register. At initial reset, P4IO is set to 0FFh, P4 is used as input mode. When P4IO is set to 00h, P4 is used as CMOS output mode. Special function of P4 is described below.

P4.4	VPOS	Positive input of the comparator
P4.2	VNEG	Negative input of the comparator
P4.1	SDATA	Serial port data I/O
P4.0	SCLK	Serial port clock I/O with Smith trigger in input path

INTERRUPT ENABLE (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	EA	ES1	-	-	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

EA: Global enable. Enable/disable all interrupts.

ES1: Enable Serial port interrupt

ET1: Enable Timer 1 interrupt

EX1: Enable external interrupt 1

ET0: Enable Timer 0 interrupt

EX0: Enable external interrupt 0

P4 I/O PORT CONTROL (initial = FFH)

Bit:	7	6	5	4	3	2	1	0
	P4.7IO	P4.6IO	P4.5IO	P4.4IO	P4.3IO	P4.2IO	P4.1IO	P4.0IO

Mnemonic: P4IO Address: AEh

P4IO: P4 pins I/O control.

1: input mode

0: output mode

PORT 3 (initial = FFH,input mode)

Bit:	7	6	5	4	3	2	1	0
	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0

Mnemonic: P3 Address: B0h

P3.7-0: P3 can be selected as input or output mode by the P3IO register, at initial reset, P3IO is set to 0FFH, P3 is used as input mode. When P3IO is set to 00h, the P3 is used as CMOS output mode. Special function of P3 is described below.

P3.5	T1	Timer/Counter 1 external count input
P3.4	T0	Timer/Counter 0 external count input
P3.3	$\overline{INT1}$	External interrupt 1
P3.2	$\overline{INT0}$	External interrupt 0

CID REGISTER (initial = 00H,**read only**)

Bit:	7	6	5	4	3	2	1	0
	-	FCLK	FDATA	FCD	DTMFD	FDR	ALGO	RNG

Mnemonic: CIDR Address: B1h

This SFR indicates the CID signal immediately. Register data is set or cleared by hardware only.

FCLK: FSK serial clock with the baud rate of 1200Hz.

FDATA: FSK serial bit data.

FCD: Set when FSK carrier is detected. Cleared when FSK carrier is disappeared.

DTMFD: Set when DTMF decoded data is ready. Cleared when DTMF signal ends.

FDR: Set when FSK 8 bits data is ready. Cleared before next FSK start bit comes

ALGO: Dual tone Alert signal Guard time detect signal. Set when a guard time qualified dual tone alert signal has been detected. Cleared when the guard time qualified dual tone alert signal is absent.

RNG: Ring detection bit. High to indicate the detection of line reversal and/or ringing.

CID FLAG GENERATOR (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	-	-	-	FSF	DTMFDF	FDRF	ALGOF	RNGF

Mnemonic: CIDFG Address: B2h

FSF: Set when FSK Latch clock low to high. Cleared by software

DTMFDF: Set when DTMFD low to high. Cleared by software

FDRF: Set when FDR low to high. Cleared by software.

ALGOF: Set when ALGO low to high. Cleared by software.

RNGF: Set when RNG low to high. Cleared by software.

CID POWER CONTROL REGISTER (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	-	-	-	CIDE	-	FSKE	CASE	DTMFE

Mnemonic: CIDPCR Address: B3h

CIDE: Global enable CID function. Low to disable all functions of CID parts.

FSKE: Enable FSK demodulation circuit.

CASE: Enable Dual Tone Alert Signal detection circuit.

DTMFE: Enable DTMF demodulation circuit.

FSK DATA REGISTER (initial = XXH)

Bit:	7	6	5	4	3	2	1	0
	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0

Mnemonic: FSKDR Address: B4h

FD7-0: 8 bits FSK demodulated data.

DTMF DATA REGISTER (initial = XXH)

Bit:	7	6	5	4	3	2	1	0
	CASH	CASL	DTMFH	DTMFL	DD3	DD2	DD1	DD0

Mnemonic: DTMFDR Address: B5h

CASH: Set when Dual Tone Alert Signal high tone is detected.

CASL: Set when Dual Tone Alert Signal low tone is detected.

DTMFH: Set when DTMF high tone is detected.

DTMFL: Set when DTMF low tone is detected.

DD3-0: 4 bits DTMF demodulated data.

DTMF PRESENT TIME REGISTER (initial = 19H)

Bit:	7	6	5	4	3	2	1	0
	DPT7	DPT6	DPT5	DPT4	DPT3	DPT2	DPT1	DPT0

Mnemonic: DTMFPT Address: B6h

The clock period of guard-time timer is 0.8582mS. The default DTMF present time is 21.45mS.

DPT7-0: The pre-set data register for counting DTMF present time. When DTMF is detected(Est, low to high), the guard timer starts to up-count from 00H. As the guard timer is equal to the value of DTMFPT, the exist of the DTMF is accepted. Est changes to low state to stop and reset the counter.

DTMF ABSENT TIME REGISTER (initial = 19H)

Bit:	7	6	5	4	3	2	1	0
	DAT7	DAT6	DAT5	DAT4	DAT3	DAT2	DAT1	DAT0

Mnemonic: DTMFAT Address: B7h

The clock period of guard-time timer is 0.8582mS. The default DTMF absent time is 21.45mS.

DAT7-0: The pre-set data register for counting DTMF absent time. When DTMF is absent(Est, high to low), the guard timer starts to up-count from 00H. As the guard timer is equal to the value of DTMFAT, the finish of DTMF is recognized. Est changes to low state to stop and reset the counter.

INTERRUPT PRIORITY (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	-	PS1	-	-	PT1	PX1	PT0	PX0

Mnemonic: IP Address: B8h

IP.7: This bit is un-implemented and will read high.

PS1: This bit defines the Serial port interrupt priority. PS1 = 1 sets it to higher priority level

PT1: This bit defines the Timer 1 interrupt priority. PT1 = 1 sets it to higher priority level.

PX1: This bit defines the External interrupt 1 priority. PX1 = 1 sets it to higher priority level.

PT0: This bit defines the Timer 0 interrupt priority. PT0 = 1 sets it to higher priority level.

PX0: This bit defines the External interrupt 0 priority. PX0 = 1 sets it to higher priority level.

DTMF GENERATOR REGISTER (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	-	DTGE	HE	LE	L1	L0	H1	H0

Mnemonic: DTMFG Address: BAh

L1	L0	H1	H0	Selected tone
x	x	0	0	1209Hz
x	x	0	1	1336Hz
x	x	1	0	1477Hz
x	x	1	1	1633Hz
0	0	x	x	697Hz
0	1	x	x	770Hz
1	0	x	x	852Hz
1	1	x	x	941Hz

LE: Enable low group frequency output.

HE: Enable high group frequency output.

DTGE: Enable dual tone output to DTMF pin.

COMPARATOR REGISTER (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	RESC	REF	-	COMPEN

Mnemonic: COMPR Address: BBh

RESC: Result of the comparator. Set when positive analog input voltage is(VPOS or 1.0v internal regular output) higher than negative analog input voltage(VNEG) RESC is a read only bit.

REF: REF = 0 reference input from analog input voltage(VPOS/P4.4) pin.

REF = 1 reference input from the internal regulator output.

COMPEN: COMPEN = 0 Disable comparator

COMPEN = 1 Enable comparator

IDLE RELEASED CONDITION REGISTER 1 (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	-	IRCS1	-	-	IRCT1	IRCX1	IRCT0	IRCX0

Mnemonic: IRC1 Address: BCh

One of the bits of IRC1 and IRC2 will be set by hardware to record the idle released condition when the idle mode is released. IRC1 and IRC2 can be set by hardware and can be R/W by software.

IRCS1: Idle mode released by Serial port interrupt flag.

IRCT1: Idle mode released by Timer 1 interrupt flag.

IRCX1: Idle mode released by external interrupt 1 flag.

IRCT0: Idle mode released by Timer 0 interrupt flag.

IRCX0: Idle mode released by external interrupt 0 flag.

IDLE RELEASED CONDITION REGISTER 2 (initial = 00H)

Bit:	7	6	5	4	3	2	1	0
	-	-	IRCWDI	IRCCOMP	IRCDIV	IRCCID	IRCX3	IRCX2

Mnemonic: IRC2 Address: BDh

One of the bits of IRC1 and IRC2 will be set by hardware to record the idle released condition when the idle mode is released. IRC1 and IRC2 can be set by hardware and can be R/W by software.

IRCWDI: Idle mode released by Watchdog timer interrupt flag.

IRCCOMP: Idle mode released by comparator interrupt flag.

IRCDIV: Idle mode released by Divider interrupt flag.

IRCCID: Idle mode released by CID interrupt flag.

IRCX3: Idle mode released by External Interrupt 3 flag.

IRCX2: Idle mode released by External Interrupt 2 flag.