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1. GENERAL DESCRIPTION

W947D6HB / W947D2HB is a high-speed Low Power double data rate synchronous dynamic random access memory (LPDDR SDRAM), An access to the LPDDR SDRAM is burst oriented. Consecutive memory location in one page can be accessed at a burst length of 2, 4, 8 and 16 when a bank and row is selected by an ACTIVE command. Column addresses are automatically generated by the LPDDR SDRAM internal counter in burst operation. Random column read is also possible by providing its address at each clock cycle. The multiple bank nature enables interleaving among internal banks to hide the pre-charging time. By setting programmable Mode Registers, the system can change burst length, latency cycle, interleave or sequential burst to maximize its performance. The device supports special low power functions such as Partial Array Self Refresh (PASR) and Automatic Temperature Compensated Self Refresh (ATCSR).

2. FEATURES

- VDD = 1.7~1.95V
- VDDQ = 1.7~1.95V;
- Data width: x16 / x32
- Clock rate: 200MHz(-5),166MHz(-6),133MHz(-75)
- Partial Array Self-Refresh(PASR)
- Auto Temperature Compensated Self-Refresh(ATCSR)
- Power Down Mode
- Deep Power Down Mode (DPD Mode)
- Programmable output buffer driver strength
- Four internal banks for concurrent operation
- Data mask (DM) for write data
- Clock Stop capability during idle periods
- Auto Pre-charge option for each burst access
- Double data rate for data output
- Differential clock inputs (CK and $\overline{CK}$)
- Bidirectional, data strobe (DQS)
- $\overline{CAS}$ Latency: 2 and 3
- Burst Length: 2, 4, 8 and 16
- Burst Type: Sequential or Interleave
- 64 ms Refresh period
- Interface: LVCMOS compatible
- Support package:
  60 balls BGA (x16)
  90 balls BGA (x32)
- Operating Temperature Range :
  Extended (-25°C ~ +85°C)
  Industrial (-40°C ~ +85°C)

3. PIN CONFIGURATION

3.1 Ball Assignment: LPDDR X16

60 BALL VFBGA									
	1	2	3	4	5	6	7	8	9
A	VSS	DQ15	VSSQ				VDDQ	DQ0	VDD
B	VDDQ	DQ13	DQ14				DQ1	DQ2	VSSQ
C	VSSQ	DQ11	DQ12				DQ3	DQ4	VDDQ
D	VDDQ	DQ9	DQ10				DQ5	DQ6	VSSQ
E	VSSQ	UDQS	DQ8				DQ7	LDQS	VDDQ
F	VSS	UDM	NC				NC	LDM	VDD
G	CKE	CK	$\overline{CK}$				$\overline{WE}$	$\overline{CAS}$	$\overline{RAS}$
H	A9	A11	NC				$\overline{CS}$	BA0	BA1
J	A6	A7	A8				A10/AP	A0	A1
K	VSS	A4	A5				A2	A3	VDD

(Top View) Pin Configuration

3.2 Ball Assignment: LPDDR X32

90 BALL VFBGA									
	1	2	3	4	5	6	7	8	9
A	VSS	DQ31	VSSQ				VDDQ	DQ16	VDD
B	VDDQ	DQ29	DQ30				DQ17	DQ18	VSSQ
C	VSSQ	DQ27	DQ28				DQ19	DQ20	VDDQ
D	VDDQ	DQ25	DQ26				DQ21	DQ22	VSSQ
E	VSSQ	DQS3	DQ24				DQ23	DQS2	VDDQ
F	VDD	DM3	NC				NC	DM2	VSS
G	CKE	CK	$\overline{CK}$				$\overline{WE}$	$\overline{CAS}$	$\overline{RAS}$
H	A9	A11	NC				$\overline{CS}$	BA0	BA1
J	A6	A7	A8				A10/AP	A0	A1
K	A4	DM1	A5				A2	DM0	A3
L	VSSQ	DQS1	DQ8				DQ7	DQS0	VDDQ
M	VDDQ	DQ9	DQ10				DQ5	DQ6	VSSQ
N	VSSQ	DQ11	DQ12				DQ3	DQ4	VDDQ
P	VDDQ	DQ13	DQ14				DQ1	DQ2	VSSQ
R	VSS	DQ15	VSSQ				VDDQ	DQ0	VDD

(Top View) Pin Configuration

4. PIN DESCRIPTION

4.1 Signal Descriptions

SIGNAL NAME	TYPE	FUNCTION	DESCRIPTION
A [n : 0]	Input	Address	Provide the row address for ACTIVE commands, and the column address and AUTO PRECHARGE bit for READ/WRITE commands, to select one location out of the memory array in the respective bank. The address inputs also provide the opcode during a MODE REGISTER SET command. A10 is used for Auto Pre-charge Select.
BA0, BA1	Input	Bank Select	Define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
DQ0~DQ15 (×16) DQ0~DQ31 (×32)	I/O	Data Input/ Output	Data bus: Input / Output.
$\overline{CS}$	Input	Chip Select	$\overline{CS}$ enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$	Input	Row Address Strobe	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
$\overline{CAS}$	Input	Column Address Strobe	Referred to $\overline{RAS}$
$\overline{WE}$	Input	Write Enable	Referred to $\overline{RAS}$
UDM / LDM(x16); DM0 to DM3 (x32)	Input	Input Mask	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading matches the DQ and DQS loading. x16: LDM: DQ0 - DQ7, UDM: DQ8 – DQ15 x32: DM0: DQ0 - DQ7, DM1: DQ8 – DQ15, DM2: DQ16 – DQ23, DM3: DQ24 – DQ31
CK / $\overline{CK}$	Input	Clock Inputs	CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$ .Input and output data is referenced to the crossing of CK and $\overline{CK}$ (both directions of crossing). Internal clock signals are derived from CK/ $\overline{CK}$.

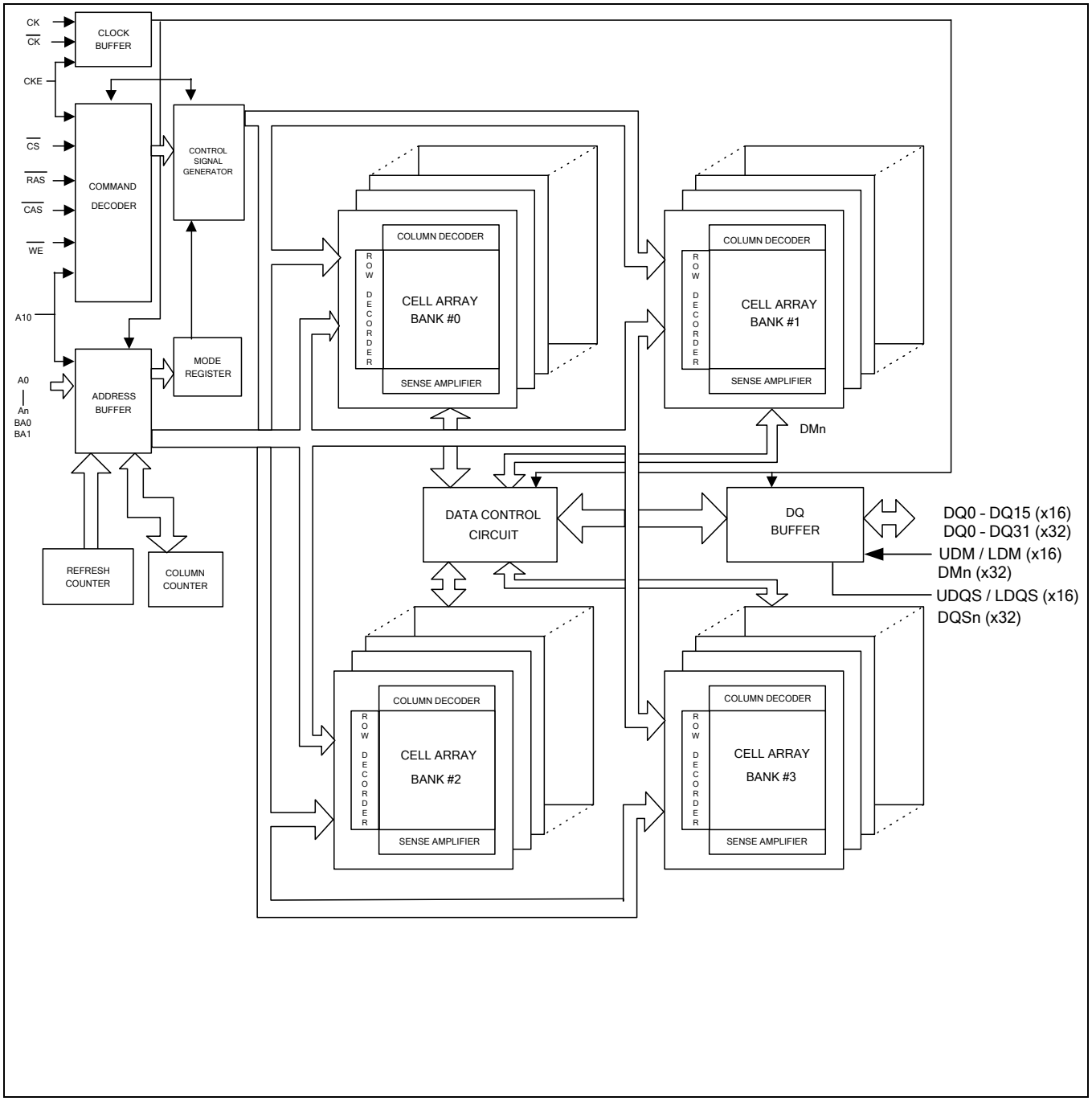
SIGNAL NAME	TYPE	FUNCTION	DESCRIPTION
CKE	Input	Clock Enable	CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE, POWER DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for SELF REFRESH EXIT, which is achieved asynchronously. Input buffers, excluding CK, $\overline{CK}$ and CKE, are disabled during power down and self refresh mode which are contrived for low standby power consumption.
LDQS, UDQS (x16); DQS0~DQS3 (x32)	I/O	Data Strobe	Output with read data, input with write data. Edge-aligned with read data, centered with write data. Used to capture write data. x16: LDQS: DQ0~DQ7; UDQS: DQ8~DQ15. x32: DQS0: DQ0~DQ7; DQS1: DQ8~DQ15; DQS2: DQ16~DQ23; DQS3: DQ24~DQ31.
VDD	Supply	Power	Power supply for input buffers and internal circuit.
VSS	Supply	Ground	Ground for input buffers and internal circuit.
VDDQ	Supply	Power for I/O Buffer	Power supply separated from VDD, used for output drivers to improve noise.
VSSQ	Supply	Ground for I/O Buffer	Ground for output drivers.
NC	-	No Connect	Non connection pin.

4.2 Addressing Table

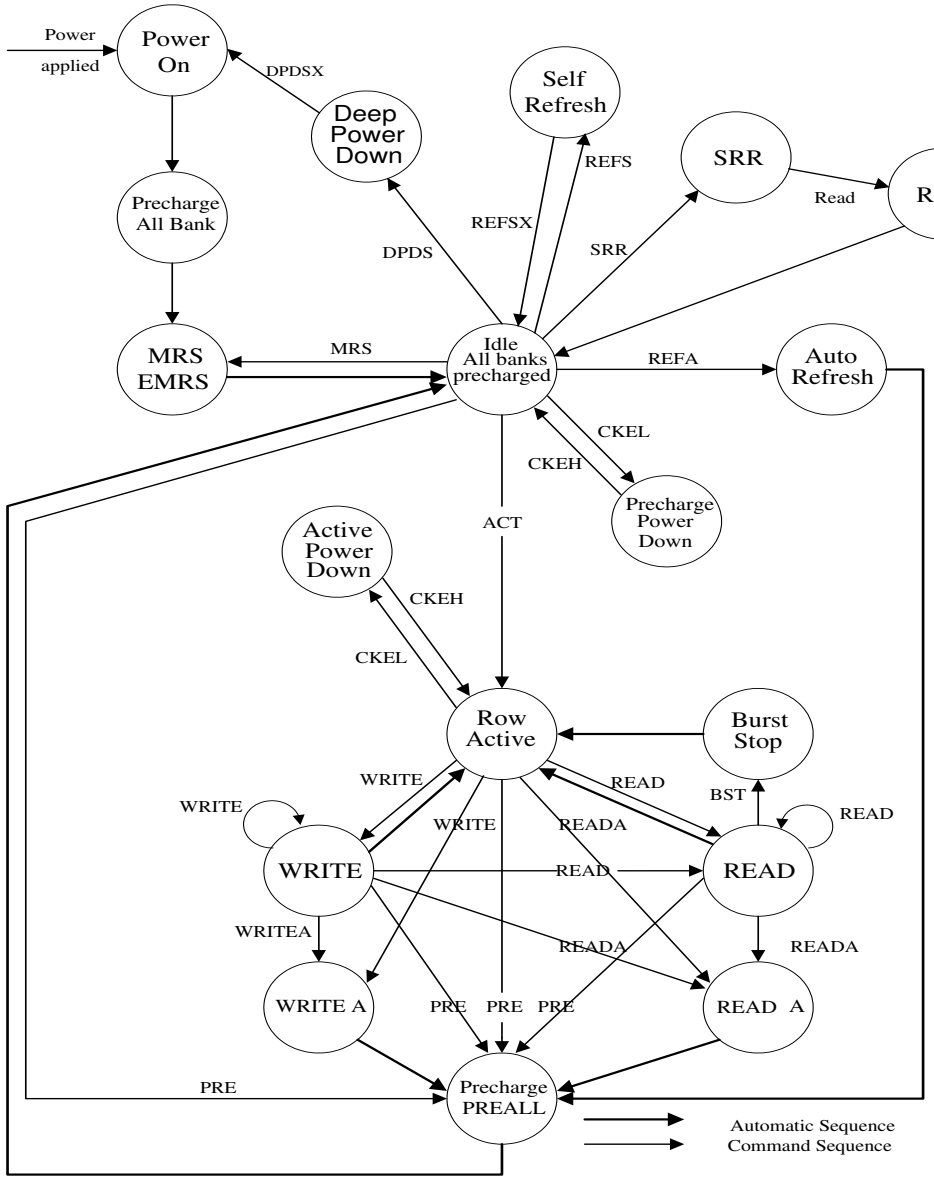
ITEM		128Mb
Number of banks		4
Bank address pins		BA0,BA1
Auto precharge pin		A10/AP
X16	Row addresses	A0-A11
	Column addresses	A0-A8
	tREFI (µs)	15.6
x32	Row addresses	A0-A11
	Column addresses	A0-A7
	tREFI (µs)	15.6

5. BLOCK DIAGRAM

5.1 Block Diagram



5.2 Simplified State Diagram



ACT = Active
BST = Burst Terminate
CKEL= Enter Power-Down
CKEH=Exit Power - Down
DPDS= Enter Deep Power Down
DPDSX=Exit Deep Power Down
MRS = Ext . Mode Reg . Set
MRS = Mode Register Set
PRE = Precharge
PREALL= Precharge All Bank
REFA = Auto Refresh
REFS = Enter Self Refresh
REFSX= Exit Self Refresh
READ = Read w/o Auto Precharge
READA = Read with Auto Precharge
WRITE = Write w/o Auto Precharge
WRITEA = Write with Auto Precharge
SRR = Status Register Read

Note: Use caution with this diagram . It is indented to provide a floorplan of the possible state transitions and commands to control them , not all details.In particular situations involving more than one bank are not captured in full detail.

6. FUNCTION DESCRIPTION

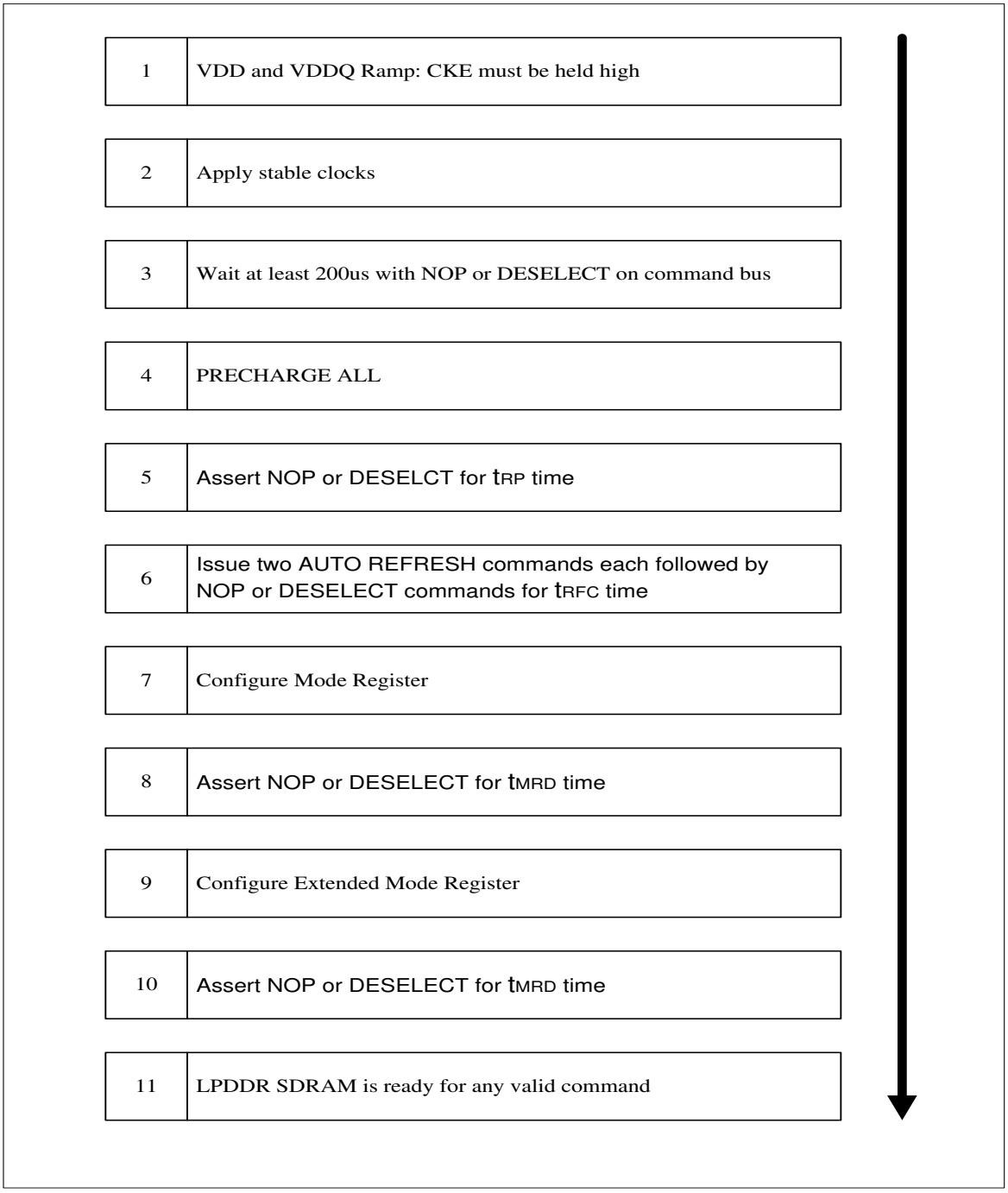
6.1 Initialization

LPDDR SDRAM must be powered up and initialized in a predefined manner. Operations procedures other than those specified may result in undefined operation. If there is any interruption to the device power, the initialization routine should be followed. The steps to be followed for device initialization are listed below.

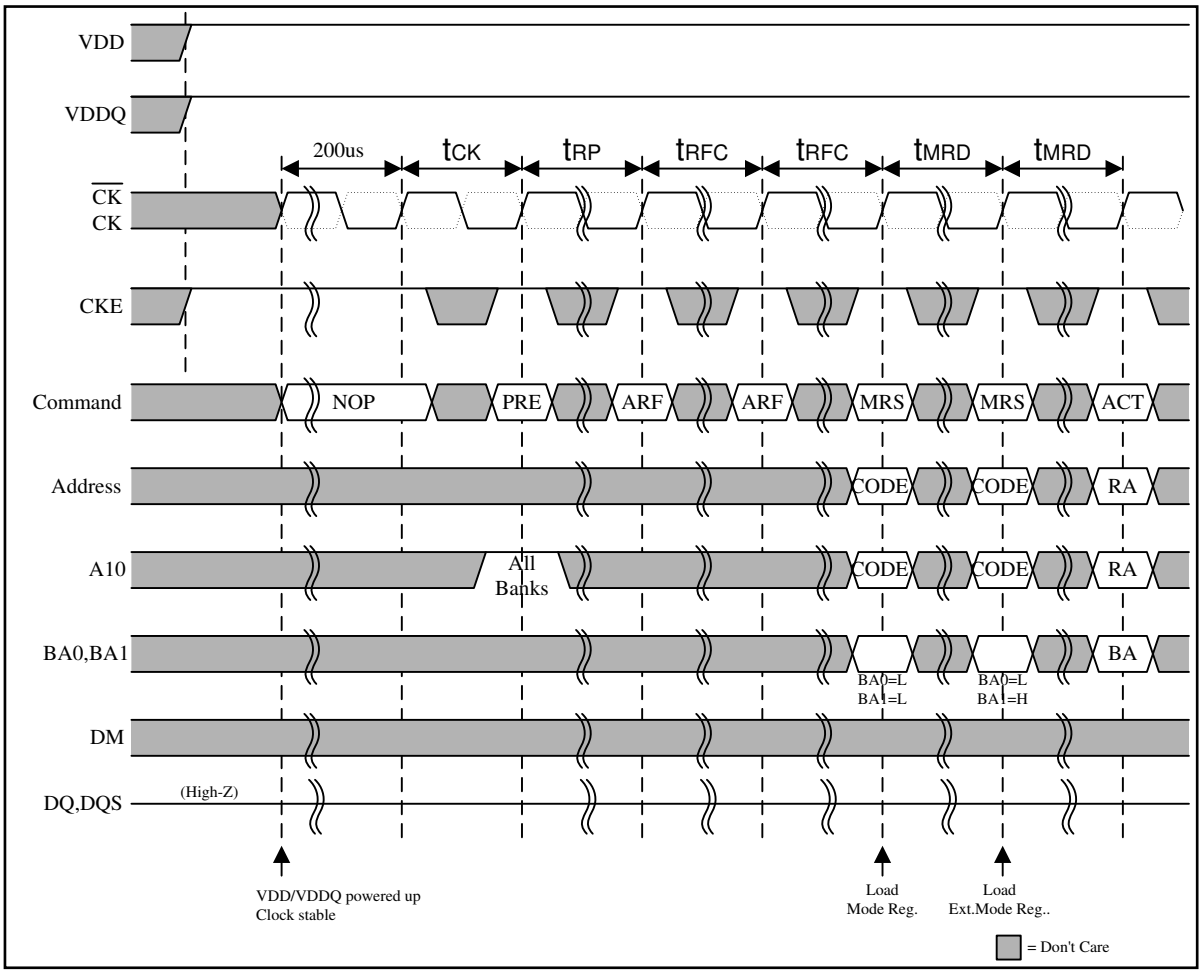
The Mode Register and Extended Mode Register do not have default values. If they are not programmed during the initialization sequence, it may lead to unspecified operation. The clock stop feature is not available until the device has been properly initialized from Step 1 through 11.

- Step 1: Provide power, the device core power (VDD) and the device I/O power (VDDQ) must be brought up simultaneously to prevent device latch-up. Although not required, it is recommended that VDD and VDDQ are from the same power source. Also Assert and hold Clock Enable (CKE) to a LVCMOS logic high level
- Step 2: Once the system has established consistent device power and CKE is driven high, it is safe to apply stable clock.
- Step 3: There must be at least 200µs of valid clocks before any command may be given to the DRAM. During this time NOP or DESELECT commands must be issued on the command bus.
- Step 4: Issue a PRECHARGE ALL command.
- Step 5: Provide NOPs or DESELECT commands for at least tRP time.
- Step 6: Issue an AUTO REFRESH command followed by NOPs or DESELECT command for at least tRFC time. Issue the second AUTO REFRESH command followed by NOPs or DESELECT command for at least tRFC time. Note as part of the initialization sequence there must be two Auto Refresh commands issued. The typical flow is to issue them at Step 6, but they may also be issued between steps 10 and 11.
- Step 7: Using the MRS command, program the base mode register. Set the desired operation modes.
- Step 8: Provide NOPs or DESELECT commands for at least tMRD time.
- Step 9: Using the MRS command, program the extended mode register for the desired operating modes. Note the order of the base and extended mode register programmed is not important.
- Step 10: Provide NOP or DESELECT commands for at least tMRD time.
- Step 11: The DRAM has been properly initialized and is ready for any valid command.

6.1.1 Initialization Flow Diagram



6.1.2 Initialization Waveform Sequence



6.2 Register Definition

6.2.1 Mode Register Set Operation

The Mode Register is used to define the specific mode of operation of the LPDDR SDRAM. This definition includes the definition of a burst length, a burst type, a CAS latency as shown in the following figure.

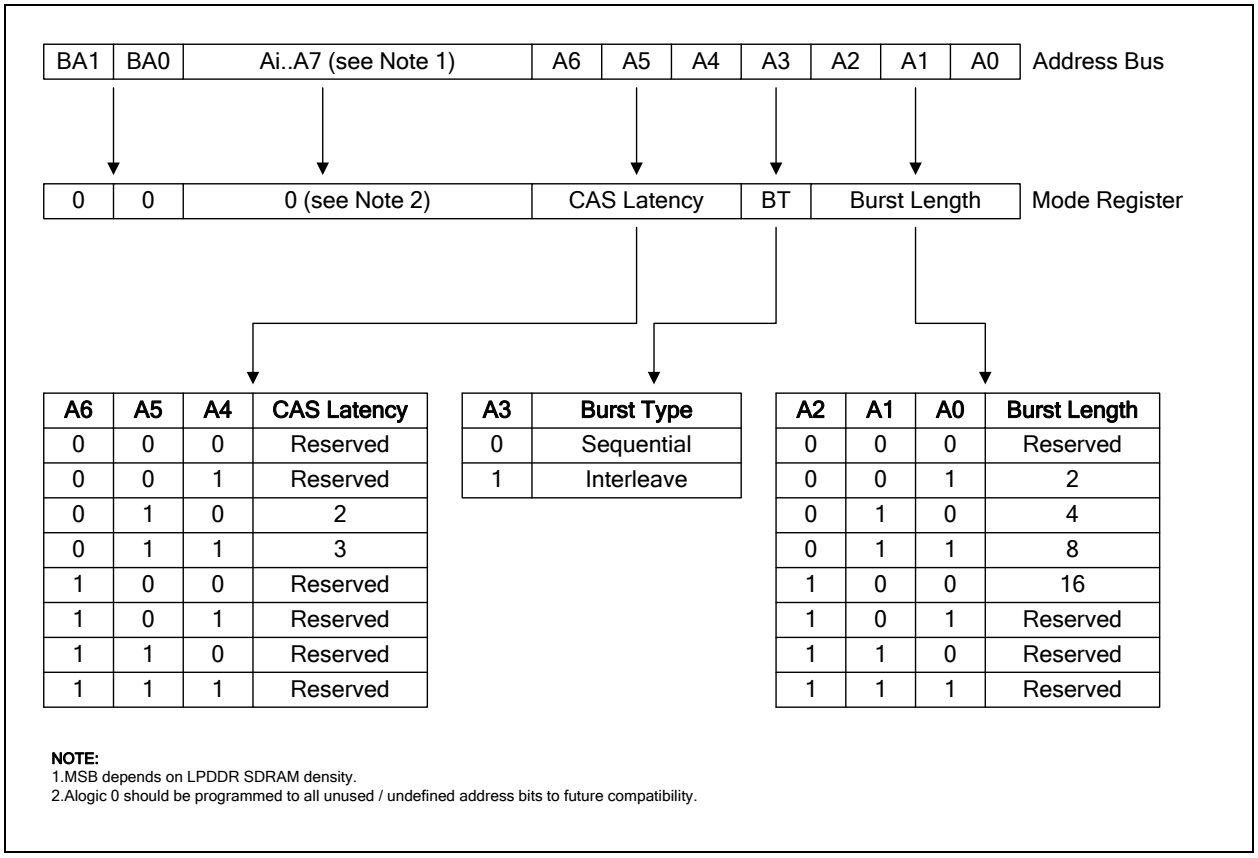
The Mode Register is programmed via the MODE REGISTER SET command (with BA0=0 and BA1=0) and will retain the stored information until it is reprogrammed, the device goes into Deep Power Down mode, or the device loses power.

Mode Register bits A0-A2 specify the burst length, A3 the type of burst (sequential or interleave), A4-A6 the CAS latency. A logic 0 should be programmed to all the undefined addresses bits to ensure future compatibility.

The Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time tMRD before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

6.2.2 Mode Register Definition



A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	Burst Length
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

NOTE:
1.MSB depends on LPDDR SDRAM density.
2.Alogic 0 should be programmed to all unused / undefined address bits to future compatibility.

6.2.3. Burst Length

Read and write accesses to the LPDDR SDRAM are burst oriented, with the burst length and burst type being programmable.
The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. Burst lengths of 2, 4, or 8 locations are available for both the sequential and the interleaved burst types.
When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within the block, meaning that the burst will wrap within the block if a boundary is reached.
The block is uniquely selected by A1−An when the burst length is set to two, by A2−An when the burst length is set to 4, by A3−An when the burst length is set to 8 (where An is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

6.3 Burst Definition

BURST LENGTH	STARTING COLUMN ADDRESS				ORDER OF ACCESSES WITHIN A BURST (HEXADECIMAL NOTATION)	
	A3	A2	A1	A0	SEQUENTIAL	INTERLEAVED
2				0	0 – 1	0 – 1
				1	1 – 0	1 – 0
4			0	0	0 – 1 – 2 – 3	0 – 1 – 2 – 3
			0	1	1 – 2 – 3 – 0	1 – 0 – 3 – 2
			1	0	2 – 3 – 0 – 1	2 – 3 – 0 – 1
			1	1	3 – 0 – 1 – 2	3 – 2 – 1 – 0
8		0	0	0	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7	0 – 1 – 2 – 3 – 4 – 5 – 6 – 7
		0	0	1	1 – 2 – 3 – 4 – 5 – 6 – 7 – 0	1 – 0 – 3 – 2 – 5 – 4 – 7 – 6
		0	1	0	2 – 3 – 4 – 5 – 6 – 7 – 0 – 1	2 – 3 – 0 – 1 – 6 – 7 – 4 – 5
		0	1	1	3 – 4 – 5 – 6 – 7 – 0 – 1 – 2	3 – 2 – 1 – 0 – 7 – 6 – 5 – 4
		1	0	0	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3	4 – 5 – 6 – 7 – 0 – 1 – 2 – 3
		1	0	1	5 – 6 – 7 – 0 – 1 – 2 – 3 – 4	5 – 4 – 7 – 6 – 1 – 0 – 3 – 2
		1	1	0	6 – 7 – 0 – 1 – 2 – 3 – 4 – 5	6 – 7 – 4 – 5 – 2 – 3 – 0 – 1
		1	1	1	7 – 0 – 1 – 2 – 3 – 4 – 5 – 6	7 – 6 – 5 – 4 – 3 – 2 – 1 – 0
16	0	0	0	0	0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F	0-1-2-3-4-5-6-7-8-9-A-B-C-D-E-F
	0	0	0	1	1-2-3-4-5-6-7-8-9-A-B-C-D-E-F-0	1-0-3-2-5-4-7-6-9-8-B-A-D-C-F-E
	0	0	1	0	2-3-4-5-6-7-8-9-A-B-C-D-E-F-0-1	2-3-0-1-6-7-4-5-A-B-8-9-E-F-C-D
	0	0	1	1	3-4-5-6-7-8-9-A-B-C-D-E-F-0-1-2	3-2-1-0-7-6-5-4-B-A-9-8-F-E-D-C
	0	1	0	0	4-5-6-7-8-9-A-B-C-D-E-F-0-1-2-3	4-5-6-7-0-1-2-3-C-D-E-F-8-9-A-B
	0	1	0	1	5-6-7-8-9-A-B-C-D-E-F-0-1-2-3-4	5-4-7-6-1-0-3-2-D-C-F-E-9-8-B-A
	0	1	1	0	6-7-8-9-A-B-C-D-E-F-0-1-2-3-4-5	6-7-4-5-2-3-0-1-E-F-C-D-A-B-8-9
	0	1	1	1	7-8-9-A-B-C-D-E-F-0-1-2-3-4-5-6	7-6-5-4-3-2-1-0-F-E-D-C-B-A-9-8
	1	0	0	0	8-9-A-B-C-D-E-F-0-1-2-3-4-5-6-7	8-9-A-B-C-D-E-F-0-1-2-3-4-5-6-7
	1	0	0	1	9-A-B-C-D-E-F-0-1-2-3-4-5-6-7-8	9-8-B-A-D-C-F-E-1-0-3-2-5-4-7-6
	1	0	1	0	A-B-C-D-E-F-0-1-2-3-4-5-6-7-8-9	A-B-8-9-E-F-C-D-2-3-0-1-6-7-4-5
	1	0	1	1	B-C-D-E-F-0-1-2-3-4-5-6-7-8-9-A	B-A-9-8-F-E-D-C-3-2-1-0-7-6-5-4
	1	1	0	0	C-D-E-F-0-1-2-3-4-5-6-7-8-9-A-B	C-D-E-F-8-9-A-B-4-5-6-7-0-1-2-3
	1	1	0	1	D-E-F-0-1-2-3-4-5-6-7-8-9-A-B-C	D-C-F-E-9-8-B-A-5-4-7-6-1-0-3-2
	1	1	1	0	E-F-0-1-2-3-4-5-6-7-8-9-A-B-C-D	E-F-C-D-A-B-8-9-6-7-4-5-2-3-0-1
	1	1	1	1	F-0-1-2-3-4-5-6-7-8-9-A-B-C-D-E	F-E-D-C-B-A-9-8-7-6-5-4-3-2-1-0

Notes:

1. For a burst length of two, A1-An selects the two data element block; A0 selects the first access within the block.
2. For a burst length of four, A2-An selects the four data element block; A0-A1 selects the first access within the block.
3. For a burst length of eight, A3-An selects the eight data element block; A0-A2 selects the first access within the block.
4. For the optional burst length of sixteen, A4-An selects the sixteen data element block; A0-A3 selects the first access within the block.
5. Whenever a boundary of the block is reached within a given sequence, the following access wraps within the block.

   When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within the block, meaning that the burst will wrap within the block if a boundary is reached.

   The block is uniquely selected by A1-An when the burst length is set to two, by A2-An when the burst length is set to 4, by A3-An when the burst length is set to 8 and A4-An when the burst length is set to 16(where An is the most significant column address bit for a given configuration). The remaining (least significant) address bit(s) is (are) used to select the starting location within the block. The programmed burst length applies to both read and write bursts.

6.4 Burst Type

Accesses within a given burst may be programmed to be either sequential or interleaved; this is referred to as the burst type and is selected via bit A3. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in the previous table.

6.5 Read Latency

The READ latency is the delay between the registration of a READ command and the availability of the first piece of output data. The latency should be set to 2 or 3 clocks.
If a READ command is registered at a clock edge n and the latency is 3 clocks, the first data element will be valid at n + 2 tCK + tAC. If a READ command is registered at a clock edge n and the latency is 2 clocks, the first data element will be valid at n + tCK + tAC.

6.6 Extended Mode Register Description

The Extended Mode Register controls functions beyond those controlled by the Mode Register; these additional functions include output drive strength selection and Partial Array Self Refresh (PASR). PASR is effective in Self Refresh mode only.

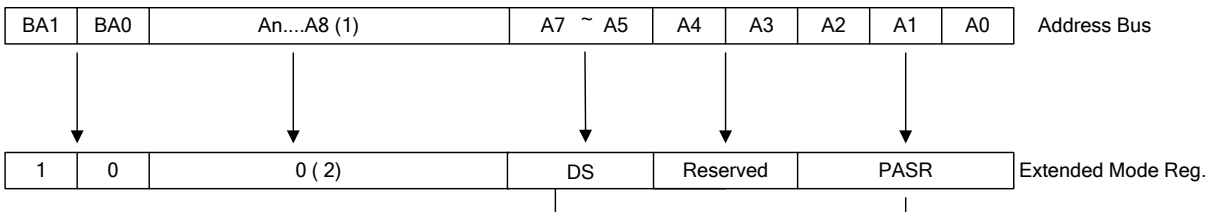
The Extended Mode Register is programmed via the MODE REGISTER SET command (with BA1=1 and BA0=0) and will retain the stored information until it is reprogrammed, the device is put in Deep Power Down mode, or the device loses power.

The Extended Mode Register must be loaded when all banks are idle and no bursts are in progress, and the controller must wait the specified time tMRD before initiating any subsequent operation. Violating either of these requirements will result in unspecified operation.

Address bits A0-A2 specify PASR, A5-A7 the Driver Strength. A logic 0 should be programmed to all the undefined addresses bits to ensure future compatibility.

Reserved states should not be used, as unknown operation or incompatibility with future versions may result.

6.6.1 Extended Mode Register Definition



A7	A6	A5	Drive Strength
0	0	0	Full Strength Driver
0	0	1	Half Strength Drive
0	1	0	Quarter Strength Driver
0	1	1	Octant Strength Driver
1	0	0	Three-Quarters Strength Driver

A2	A1	A0	PASR
0	0	0	All banks
0	0	1	1/2 array (BA1=0)
0	1	0	1/4 array (BA1=BA0=0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

NOTES:
1.MSB depends on mobile DDR SDRAM density.
2.A logic 0 should be programmed to all unused / undefined bits to ensure future compatibility.

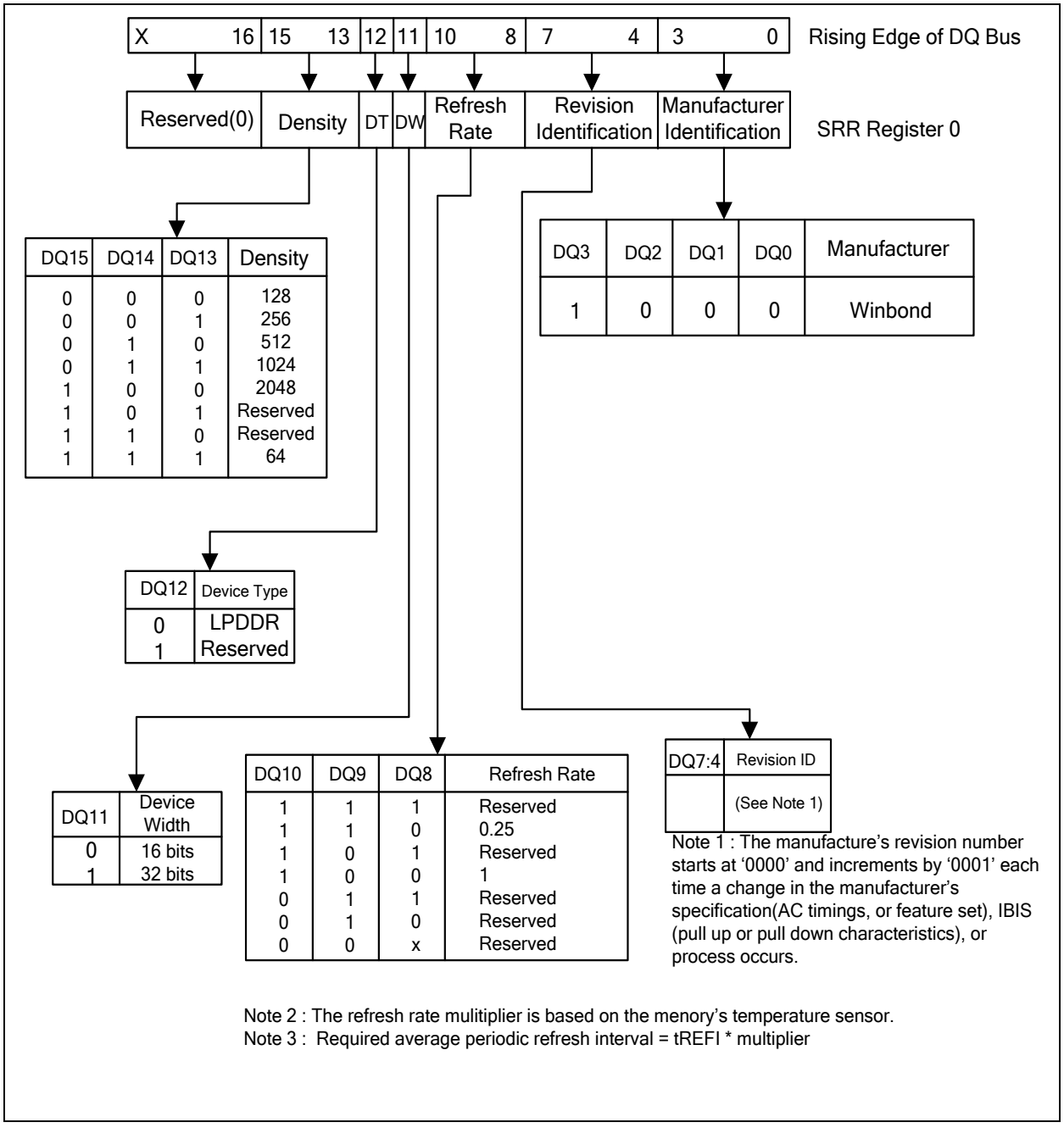
6.7 Status Register Read

Status Register Read (SRR) is an optional feature in JEDEC, and it is implemented in this device. With SRR, a method is defined to read registers from the device. The encoding for an SRR command is the same as a MRS with BA[1:0]="01". The address pins (A[n:0]) encode which register is to be read. Currently only one register is defined at A[n:0]=0. The sequence to perform an SRR command is as follows:

- All reads/writes must be completed
- All banks must be closed
- MRS with BA=01 is issued (SRR)
- Wait tSRR
- Read issued to any bank/page
- CAS latency cycles later the device returns the registers data as it would a normal read
- The next command to the device can be issued tSRC after the Read command was issued.

The burst length for the SRR read is always fixed to length 2.

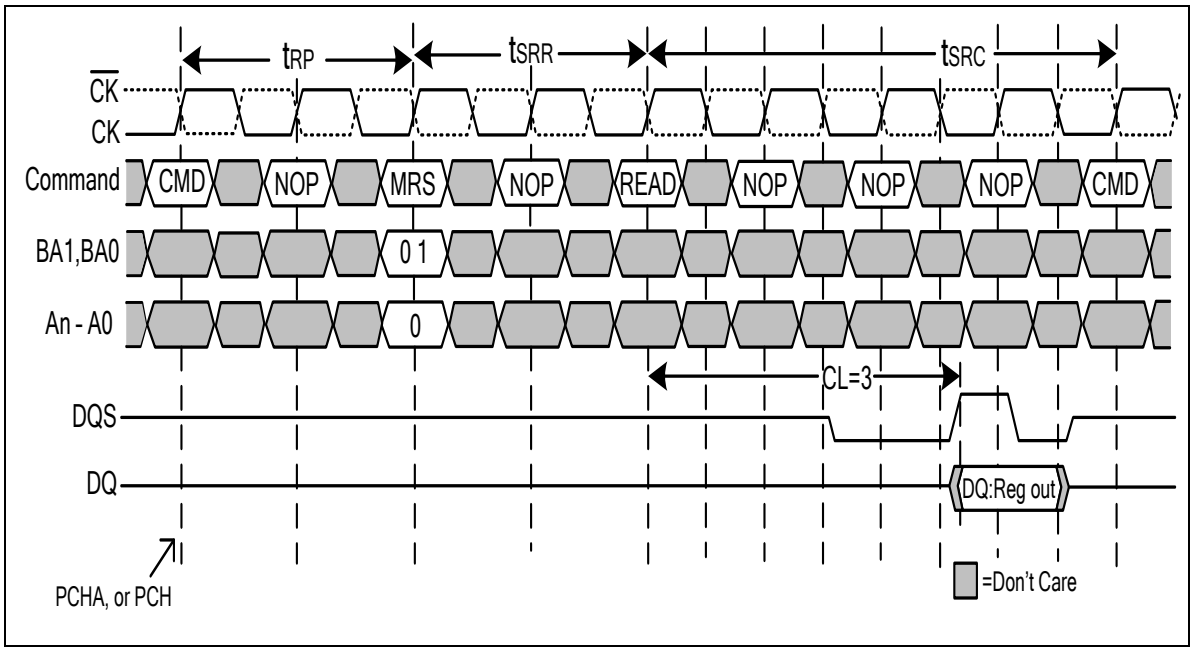
6.7.1 SRR Register (A[n:0] = 0)



Note 1 : The manufacture's revision number starts at '0000' and increments by '0001' each time a change in the manufacturer's specification(AC timings, or feature set), IBIS (pull up or pull down characteristics), or process occurs.

Note 2 : The refresh rate mulitiplier is based on the menory's temperature sensor.
Note 3 : Required average periodic refresh interval = tREFI * multiplier

6.7.2 Status Register Read Timing Diagram



Notes :

1. SRR can only be issued after power-up sequence is complete.
2. SRR can only be issued with all banks precharged.
3. SRR CL is unchanged from value in the mode register.
4. SRR BL is fixed at 2.
5. tSRR = 2 (min).
6. tSRC = CL + 1; (min time between read to next valid command)
7. No commands other than NOP and DES are allowed between the SRR and the READ.

6.8 Partial Array Self Refresh

With partial array self refresh (PASR), the self refresh may be restricted to a variable portion of the total array. The whole array (default), 1/2 array, or 1/4 array could be selected. Data outside the defined area will be lost. Address bits A0 to A2 are used to set PASR.

6.9 Automatic Temperature Compensated Self Refresh

The device has an Automatic Temperature Compensated Self Refresh feature. It automatically adjusts the refresh rate based on the device temperature without any register update needed. To maintain backward compatibility, this device which have Automatic TCSR, ignore (don't care) the inputs to address bits A3 and A4 during EMRS programming.

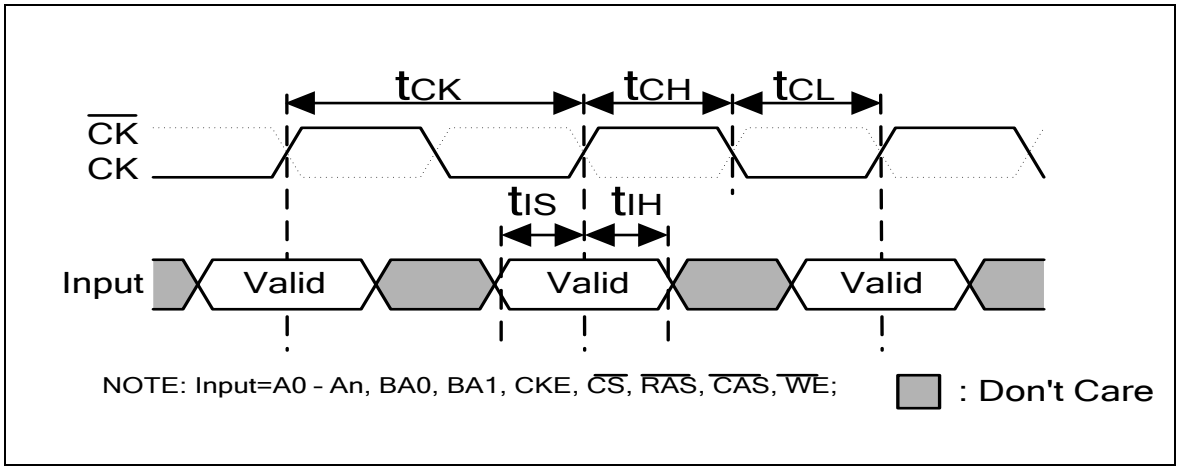
6.10 Output Drive Strength

The drive strength could be set to full, half or three-quarter strength via address bits A5 and A6. The half drive strength option is intended for lighter loads or point-to-point environments.

6.11 Commands

All commands (address and control signals) are registered on the positive edge of clock (crossing of CK going high and $\overline{CK}$ going low).

6.11.1 Basic Timing Parameters for Commands



6.11.2 Truth Table - Commands

NAME (FUNCTION)	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	BA	A10/AP	ADDR	NOTES
DESELECT (NOP)	H	X	X	X	X	X	X	2
NO OPERATION (NOP)	L	H	H	H	X	X	X	2
ACTIVE (Select Bank and activate row)	L	L	H	H	Valid	Row	Row	
READ (Select bank and column and start read burst)	L	H	L	H	Valid	L	Col	
READ with AP (Read Burst with Auto Precharge)	L	H	L	H	Valid	H	Col	3
WRITE (Select bank and column and start write burst)	L	H	L	L	Valid	L	Col	
WRITE with AP (Write Burst with Auto Precharge)	L	H	L	L	Valid	H	Col	3
BURST TERMINATE or enter DEEP POWER DOWN	L	H	H	L	X	X	X	4, 5
PRECHARGE (Deactivate Row in selected bank)	L	L	H	L	Valid	L	X	6
PRECHARGE ALL (Deactivate rows in all banks)	L	L	H	L	X	H	X	6
AUTO REFRESH or enter SELF REFRESH	L	L	L	H	X	X	X	7, 8, 9
MODE REGISTER SET	L	L	L	L	Valid	Op-code		10

Notes:

1. All states and sequences not shown are illegal or reserved.
2. DESELECT and NOP are functionally interchangeable.
3. Auto precharge is non-persistent. A10 High enables Auto precharge, while A10 Low disables Auto precharge.
4. Burst Terminate applies to only Read bursts with Autoprecharge disabled. This command is undefined and should not be used for Read with Auto precharge enabled, and for Write bursts.
5. This command is BURST TERMINATE if CKE is High and DEEP POWER DOWN entry if CKE is Low.
6. If A10 is low, bank address determines which bank is to be precharged. If A10 is high, all banks are precharged and BA0~BA1 are don't care.
7. This command is AUTO REFRESH if CKE is High and SELF REFRESH if CKE is low.
8. All address inputs and I/O are 'don't care' except for CKE. Internal refresh counters control bank and row addressing.
9. All banks must be precharged before issuing an AUTO-REFRESH or SELF REFRESH command.
10. BA0 and BA1 value select between MRS and EMRS.
11. CKE is HIGH for all commands shown except SELF REFRESH and DEEP POWER-DOWN.

6.11.3 Truth Table - DM Operations

FUNCTION	DM	DQ	NOTES
Write Enable	L	Valid	1
Write Inhibit	H	X	1

Notes:

1. Used to mask write data, provided coincident with the corresponding data.

6.11.4 Truth Table - CKE

CKEn-1	CKEn	CURRENT STATE	COMMANDn	ACTIONn	NOTES
L	L	Power Down	X	Maintain Power Down	
L	L	Self Refresh	X	Maintain Self Refresh	
L	L	Deep Power Down	X	Maintain Deep Power Down	
L	H	Power Down	NOP or DESELECT	Exit Power Down	5, 6, 9
L	H	Self Refresh	NOP or DESELECT	Exit Self Refresh	5, 7, 10
L	H	Deep Power Down	NOP or DESELECT	Exit Deep Power Down	5, 8
H	L	All Banks Idle	NOP or DESELECT	Precharge Power Down Entry	5
H	L	Bank(s) Active	NOP or DESELECT	Active Power Down Entry	5
H	L	All Banks Idle	AUTO REFRESH	Self Refresh Entry	
H	L	All Banks Idle	BURST TERMINATE	Enter Deep Power Down	
H	H	See the other Truth Tables			

Notes:

1. CKEn is the logic state of CKE at clock edge n; CKEn-1 was the state of CKE at the previous clock edge.
2. Current state is the state of LPDDR immediately prior to clock edge n.
3. COMMANDn is the command registered at clock edge n, and ACTIONn is the result of COMMANDn.
4. All states and sequences not shown are illegal or reserved.
5. DESELECT and NOP are functionally interchangeable.
6. Power Down exit time (tXP) should elapse before a command other than NOP or DESELECT is issued.
7. SELF REFRESH exit time (tXSR) should elapse before a command other than NOP or DESELECT is issued.
8. The Deep Power-Down exit procedure must be followed as discussed in the Deep Power-Down section of the Functional Description.
9. The clock must toggle at least once during the tXP period.
10. The clock must toggle at least once during the tXSR time.

6.11.5 Truth Table - Current State BANKn - Command to BANKn

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND	ACTION	NOTES
Any	H	X	X	X	DESELECT	NOP or Continue previous operation	
	L	H	H	H	No Operation	NOP or Continue previous operation	
Idle	L	L	H	H	ACTIVE	Select and activate row	
	L	L	L	H	AUTO REFRESH	Auto refresh	10
	L	L	L	L	MRS	Mode register set	10
Row Active	L	H	L	H	READ	Select column & start read burst	
	L	H	L	L	WRITE	Select column & start write burst	
	L	L	H	L	PRECHARGE	Deactivate row in bank (or banks)	4
Read (Auto precharge Disabled)	L	H	L	H	READ	Select column & start new read burst	5, 6
	L	H	L	L	WRITE	Select column & start write burst	5, 6, 13
	L	L	H	L	PRECHARGE	Truncate read burst, start precharge	
	L	H	H	L	BURST TERMINATE	Burst terminate	11
Write (Auto precharge Disabled)	L	H	L	H	READ	Select column & start read burst	5, 6, 12
	L	H	L	L	WRITE	Select column & start new write burst	5, 6
	L	L	H	L	PRECHARGE	Truncate write burst & start precharge	12

Notes:

1. The table applies when both CKEn-1 and CKEn are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. This command may or may not be bank specific. If all banks are being precharged, they must be in a valid state for precharging.
5. A command other than NOP should not be issued to the same bank while a READ or WRITE burst with Auto Precharge is enabled.
6. The new Read or Write command could be Auto Prechrge enabled or Auto Precharge disabled.
7. Current State Definitions:
   Idle: The bank has been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Write: A WRITE burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
8. The following states must not be interrupted by a command issued to the same bank. DESEDECT or NOP commands or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and this table, and according to next table.
   Precharging: Starts with the registration of a PRECHARGE command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.
   Row Activating: Starts with registration of an ACTIVE command and ends when tRCD is met. Once tRCD is met, the bank will be in the 'row active' state.
   Read with AP Enabled: Starts with the registration of the READ command with Auto Precharge enabled and ends when tRP has been met. Once tRP has been met, the bank will be in the idle state.
   Write with AP Enabled: Starts with registration of a WRITE command with Auto Precharge enabled and ends when tRP has been met. Once tRP is met, the bank will be in the idle state.
9. The following states must not be interrupted by any executable command; DESEDECT or NOP commands must be applied to each positive clock edge during these states.
   Refreshing: Starts with registration of an AUTO REFRESH command and ends when tRFC is met. Once tRFC is met, the LPDDR will be in an 'all banks idle' state.

Accessing Mode Register: Starts with registration of a MODE REGISTER SET command and ends when tMRD has been met. Once tMRD is met, the LPDDR will be in an 'all banks idle' state.
Precharging All: Starts with the registration of a PRECHARGE ALL command and ends when tRP is met. Once tRP is met, the bank will be in the idle state.

10. Not bank-specific; requires that all banks are idle and no bursts are in progress.
11. Not bank-specific. BURST TERMINATE affects the most recent READ burst, regardless of bank.
12. Requires appropriate DM masking.
13. A WRITE command may be applied after the completion of the READ burst; otherwise, a BURST TERMINATE must be used to end the READ prior to asserting a WRITE command.

6.11.6 Truth Table - Current State BANKn, Command to BANKn

CURRENT STATE	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	COMMAND	ACTION	NOTES
Any	H	X	X	X	DESELECT	NOP or Continue previous Operation	
	L	H	H	H	NOP	NOP or Continue previous Operation	
Idle	X	X	X	X	ANY	Any command allowed to bank m	
Row Activating, Active, or Precharging	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start read burst	8
	L	H	L	L	WRITE	Select column & start write burst	8
	L	L	H	L	PRECHARGE	Precharge	
Read with Auto Precharge disabled	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start new read burst	8
	L	H	L	L	WRITE	Select column & start write burst	8,10
	L	L	H	L	PRECHARGE	Precharge	
Write with Auto Precharge disabled	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start read burst	8, 9
	L	H	L	L	WRITE	Select column & start new write burst	8
	L	L	H	L	PRECHARGE	Precharge	
Read with Auto Precharge	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start new read burst	5, 8
	L	H	L	L	WRITE	Select column & start write burst	5, 8, 10
	L	L	H	L	PRECHARGE	Precharge	
Write with Auto Precharge	L	L	H	H	ACTIVE	Select and activate row	
	L	H	L	H	READ	Select column & start read burst	5, 8
	L	H	L	L	WRITE	Select column & start new write burst	5, 8
	L	L	H	L	PRECHARGE	Precharge	

Notes:
1. The table applies when both CKEn-1 and CKEn are HIGH, and after tXSR or tXP has been met if the previous state was Self Refresh or Power Down.
2. DESELECT and NOP are functionally interchangeable.
3. All states and sequences not shown are illegal or reserved.
4. Current State Definitions:
   Idle: The bank has been precharged, and tRP has been met.
   Row Active: A row in the bank has been activated, and tRCD has been met. No data bursts/accesses and no register accesses are in progress.
   Read: A READ burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
   Write: A Write burst has been initiated, with Auto Precharge disabled, and has not yet terminated or been terminated.
5. Read with AP enabled and Write with AP enabled: The read with Auto Precharge enabled or Write with Auto Precharge enabled states can be broken into two parts: the access period and the precharge period. For Read with AP, the precharge period is defined as if the same burst was executed with Auto Precharge disabled and then followed with the earliest possible PRECHARGE command that still accesses all the data in the burst. For Write with Auto precharge, the precharge period begins when tWR ends, with tWR measured as if Auto Precharge was disabled. The access period starts with registration of the command and ends where the precharge period (or tRP) begins. During the precharge period, of the Read with Auto Precharge enabled or Write with Auto Precharge enabled states, ACTIVE, PRECHARGE, READ, and WRITE commands to the other bank may be applied; during the access period, only ACTIVE and PRECHARGE commands to the other banks may be applied. In either case, all other related limitations apply (e.g. contention between READ data and WRITE data must be avoided).
6. AUTO REFRESH, SELF REFRESH, and MODE REGISTER SET commands may only be issued when all bank are idle.
7. A BURST TERMINATE command cannot be issued to another bank; it applies to the bank represented by the current state only.
8. READs or WRITEs listed in the Command column include READs and WRITEs with Auto Precharge enabled and READs and WRITEs with Auto Precharge disabled.
9. Requires appropriate DM masking.
10. A WRITE command may be applied after the completion of data output, otherwise a BURST TERMINATE command must be issued to end the READ prior to asserting a WRITE command.

7. OPERATION

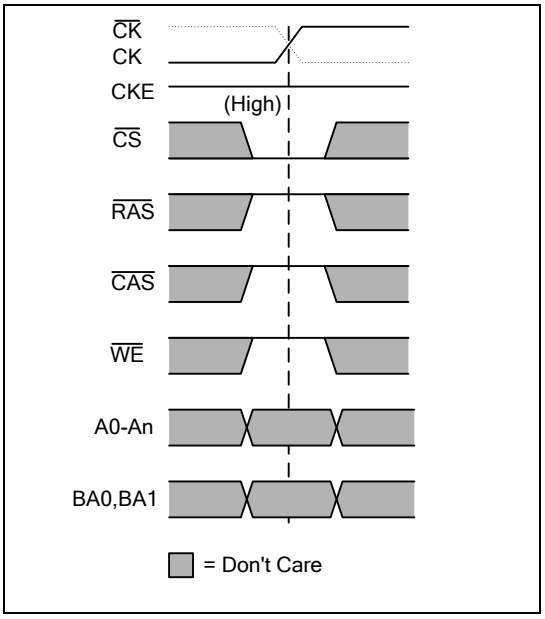
7.1. Deselect

The DESELECT function ($\overline{CS}$ = high) prevents new commands from being executed by the LPDDR SDRAM. The LPDDR SDRAM is effectively deselected. Operations already in progress are not affected.

7.2. No Operation

The NO OPERATION (NOP) command is used to perform a NOP to a LPDDR SDRAM that is selected ($\overline{CS}$ =Low). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

7.2.1 NOP Command



7.3 Mode Register Set

The Mode Register and the Extended Mode Register are loaded via the address inputs. The MODE REGISTER SET command can only be issued when all banks are idle and no bursts are in progress, and a subsequent executable command cannot be issued until tMRD is met.

7.3.1 Mode Register Set Command