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winbond

8M × 8 BANKS × 16 BIT DDR2 SDRAM

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1. GENERAL DESCRIPTION

The W971GG6KB is a 1G bits DDR2 SDRAM, organized as 8,388,608 words × 8 banks × 16 bits. This device achieves high speed transfer rates up to 1066Mb/sec/pin (DDR2-1066) for various applications. W971GG6KB is sorted into the following grade parts: -18, -25, 25I and -3. The -18 grade parts is compliant to the DDR2-1066 (7-7-7) specification. The -25 and 25I grade parts are compliant to the DDR2-800 (5-5-5) or DDR2-800 (6-6-6) specification (the 25I industrial grade which is guaranteed to support -40°C ≤ T_{CASE} ≤ 95°C). The -3 grade parts is compliant to the DDR2-667 (5-5-5) specification.

All of the control and address inputs are synchronized with a pair of externally supplied differential clocks. Inputs are latched at the cross point of differential clocks (CLK rising and $\overline{CLK}$ falling). All I/Os are synchronized with a single ended DQS or differential DQS- $\overline{DQS}$ pair in a source synchronous fashion.

2. FEATURES

- Power Supply: V_{DD}, V_{DDQ} = 1.8 V ± 0.1 V
- Double Data Rate architecture: two data transfers per clock cycle
- CAS Latency: 3, 4, 5, 6 and 7
- Burst Length: 4 and 8
- Bi-directional, differential data strobes (DQS and $\overline{DQS}$) are transmitted / received with data
- Edge-aligned with Read data and center-aligned with Write data
- DLL aligns DQ and DQS transitions with clock
- Differential clock inputs (CLK and $\overline{CLK}$)
- Data masks (DM) for write data
- Commands entered on each positive CLK edge, data and data mask are referenced to both edges of DQS
- Posted $\overline{CAS}$ programmable additive latency supported to make command and data bus efficiency
- Read Latency = Additive Latency plus CAS Latency (RL = AL + CL)
- Off-Chip-Driver impedance adjustment (OCD) and On-Die-Termination (ODT) for better signal quality
- Auto-precharge operation for read and write bursts
- Auto Refresh and Self Refresh modes
- Precharged Power Down and Active Power Down
- Write Data Mask
- Write Latency = Read Latency - 1 (WL = RL - 1)
- Interface: SSTL_18
- Packaged in WBGA 84 Ball (8X12.5 mm^2), using Lead free materials with RoHS compliant

3. ORDER INFORMATION

PART NUMBER	SPEED GRADE	OPERATING TEMPERATURE
W971GG6KB-18	DDR2-1066 (7-7-7)	0°C ≤ T_{CASE} ≤ 85°C
W971GG6KB-25	DDR2-800 (5-5-5) or DDR2-800 (6-6-6)	0°C ≤ T_{CASE} ≤ 85°C
W971GG6KB25I	DDR2-800 (5-5-5) or DDR2-800 (6-6-6)	-40°C ≤ T_{CASE} ≤ 95°C
W971GG6KB-3	DDR2-667 (5-5-5)	0°C ≤ T_{CASE} ≤ 85°C

4. KEY PARAMETERS

SYM.	SPEED GRADE			DDR2-1066	DDR2-800	DDR2-667
	Bin(CL-tRCD-tRP)			7-7-7	5-5-5/6-6-6	5-5-5
	Part Number Extension			-18	-25/25I	-3
tCK(avg)	Average clock period	@CL = 7	Min.	1.875 nS	–	–
			Max.	7.5 nS	–	–
		@CL = 6	Min.	2.5 nS	2.5 nS	–
			Max.	7.5 nS	8 nS	–
		@CL = 5	Min.	3 nS	2.5 nS	3 nS
			Max.	7.5 nS	8 nS	8 nS
		@CL = 4	Min.	3.75 nS	3.75 nS	3.75 nS
			Max.	7.5 nS	8 nS	8 nS
		@CL = 3	Min.	–	5 nS	5 nS
			Max.	–	8 nS	8 nS
tRCD	Active to Read/Write Command Delay Time		Min.	13.125 nS	12.5 nS	15 nS
tRP	Precharge to Active Command Period		Min.	13.125 nS	12.5 nS	15 nS
tRC	Active to Ref/Active Command Period		Min.	58.125 nS	57.5 nS	60 nS
tRAS	Active to Precharge Command Period		Min.	45 nS	45 nS	45 nS
IDD0	Operating one bank active-precharge current		Max.	75 mA	70 mA	65 mA
IDD1	Operating one bank active-read-precharge current		Max.	90 mA	85 mA	80 mA
IDD4R	Operating burst read current		Max.	145 mA	120 mA	105 mA
IDD4W	Operating burst write current		Max.	155 mA	130 mA	110 mA
IDD5B	Burst refresh current		Max.	145 mA	130 mA	120 mA
IDD6	Self refresh current ($T_{CASE} \leq 85°C$)		Max.	8 mA	8 mA	8 mA
IDD7	Operating bank interleave read current		Max.	190 mA	185 mA	160 mA

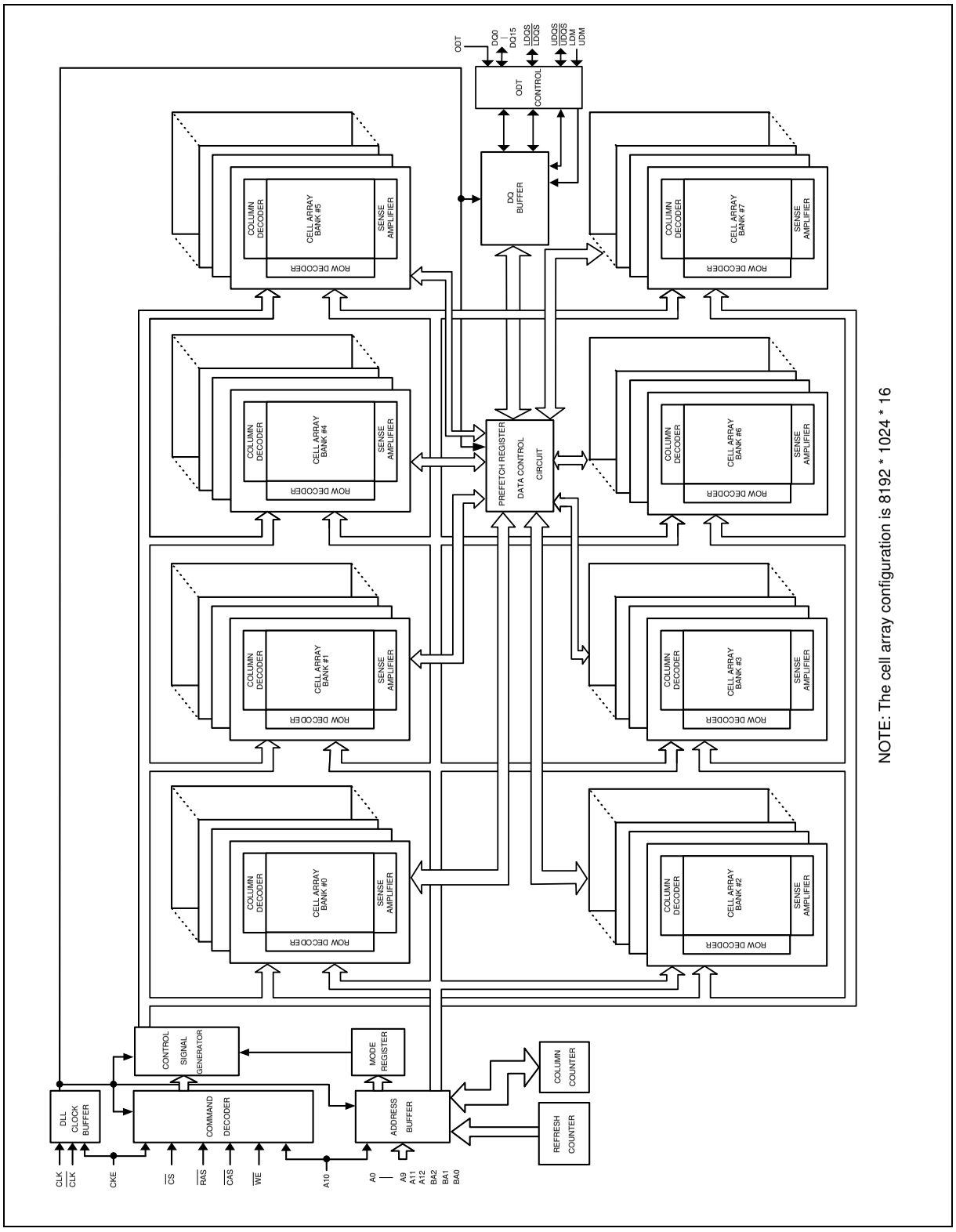
5. BALL CONFIGURATION

1	2	3	4	5	6	7	8	9
VDD	NC	VSS		A		VSSQ	$\overline{\text{UDQS}}$	VDDQ
DQ14	VSSQ	UDM		B		UDQS	VSSQ	DQ15
VDDQ	DQ9	VDDQ		C		VDDQ	DQ8	VDDQ
DQ12	VSSQ	DQ11		D		DQ10	VSSQ	DQ13
VDD	NC	VSS		E		VSSQ	$\overline{\text{LDQS}}$	VDDQ
DQ6	VSSQ	LDM		F		LDQS	VSSQ	DQ7
VDDQ	DQ1	VDDQ		G		VDDQ	DQ0	VDDQ
DQ4	VSSQ	DQ3		H		DQ2	VSSQ	DQ5
VDDL	VREF	VSS		J		VSSDL	CLK	VDD
	CKE	$\overline{\text{WE}}$		K		$\overline{\text{RAS}}$	$\overline{\text{CLK}}$	ODT
BA2	BA0	BA1		L		$\overline{\text{CAS}}$	$\overline{\text{CS}}$	
	A10/AP	A1		M		A2	A0	VDD
VSS	A3	A5		N		A6	A4	
	A7	A9		P		A11	A8	VSS
VDD	A12	NC		R		NC	NC	

6. BALL DESCRIPTION

BALL NUMBER	SYMBOL	FUNCTION	DESCRIPTION
M8,M3,M7,N2,N8,N3,N7,P2,P8,P3,M2,P7,R2	A0−A12	Address	Provide the row address for active commands, and the column address and Auto-precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. Row address: A0−A12. Column address: A0−A9. (A10 is used for Auto-precharge)
L2,L3,L1	BA0−BA2	Bank Select	BA0−BA2 define to which bank an ACTIVE, READ, WRITE or PRECHARGE command is being applied.
G8,G2,H7,H3,H1,H9,F1,F9,C8,C2,D7,D3,D1,D9,B1,B9	DQ0−DQ15	Data Input / Output	Bi-directional data bus.
K9	ODT	On Die Termination Control	ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM.
F7,E8	LDQS, $\overline{\text{LDQS}}$	LOW Data Strobe	Data Strobe for Lower Byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. LDQS corresponds to the data on DQ0−DQ7. $\overline{\text{LDQS}}$ is only used when differential data strobe mode is enabled via the control bit at EMR (1)[A10 EMRS command].
B7,A8	UDQS, $\overline{\text{UDQS}}$	UP Data Strobe	Data Strobe for Upper Byte: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. UDQS corresponds to the data on DQ8−DQ15. $\overline{\text{UDQS}}$ is only used when differential data strobe mode is enabled via the control bit at EMR (1)[A10 EMRS command].
L8	$\overline{\text{CS}}$	Chip Select	All commands are masked when $\overline{\text{CS}}$ is registered HIGH. $\overline{\text{CS}}$ provides for external rank selection on systems with multiple ranks. $\overline{\text{CS}}$ is considered part of the command code.
K7,L7,K3	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$	Command Inputs	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ (along with $\overline{\text{CS}}$) define the command being entered.
B3,F3	UDM LDM	Input Data Mask	DM is an input mask signal for write data. Input data is masked when DM is sampled high coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
J8,K8	CLK, $\overline{\text{CLK}}$	Differential Clock Inputs	CLK and $\overline{\text{CLK}}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CLK and negative edge of $\overline{\text{CLK}}$. Output (read) data is referenced to the crossings of CLK and $\overline{\text{CLK}}$ (both directions of crossing).
K2	CKE	Clock Enable	CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM.
J2	V_{REF}	Reference Voltage	V_{REF} is reference voltage for inputs.
A1,E1,J9,M9,R1	V_{DD}	Power Supply	Power Supply: 1.8V ± 0.1V.
A3,E3,J3,N1,P9	V_{SS}	Ground	Ground.
A9,C1,C3,C7,C9,E9,G1,G3,G7,G9	V_{DDQ}	DQ Power Supply	DQ Power Supply: 1.8V ± 0.1V.
A7,B2,B8,D2,D8,E7,F2,F8,H2,H8	V_{SSQ}	DQ Ground	DQ Ground. Isolated on the device for improved noise immunity.
A2,E2,R3,R7,R8	NC	No Connection	No connection.
J7	V_{SSDL}	DLL Ground	DLL Ground.
J1	V_{DDL}	DLL Power Supply	DLL Power Supply: 1.8V ± 0.1V.

7. BLOCK DIAGRAM



8. FUNCTIONAL DESCRIPTION

8.1 Power-up and Initialization Sequence

DDR2 SDRAMs must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. The following sequence is required for Power-up and Initialization.

1. Apply power and attempt to maintain CKE below 0.2 × V_{DDQ} and ODT[*1] at a LOW state (all other inputs may be undefined.) Either one of the following sequence is required for Power-up.
   A. The V_{DD} voltage ramp time must be no greater than 200 mS from when V_{DD} ramps from 300 mV to V_{DD} min; and during the V_{DD} voltage ramp, $|V_{DD} - V_{DDQ}| \leq 0.3$ volts.
      - V_{DD}, V_{DDL} and V_{DDQ} are driven from a single power converter output
      - V_{TT} is limited to 0.95V max
      - V_{REF}[*2] tracks $V_{DDQ}/2$
      - $V_{DDQ} \geq V_{REF}$ must be met at all times
   B. Voltage levels at I/Os and outputs must be less than V_{DDQ} during voltage ramp time to avoid DRAM latch-up. During the ramping of the supply voltages, $V_{DD} \geq V_{DDL} \geq V_{DDQ}$ must be maintained and is applicable to both AC and DC levels until the ramping of the supply voltages is complete.
      - Apply V_{DD}/V_{DDL}[*3] before or at the same time as V_{DDQ}
      - Apply V_{DDQ}[*4] before or at the same time as V_{TT}
      - V_{REF}[*2] tracks $V_{DDQ}/2$
      - $V_{DDQ} \geq V_{REF}$ must be met at all times.
      - Apply V_{TT}
      - The V_{TT} voltage ramp time from when V_{DDQ} min is achieved on V_{DDQ} to when V_{TT} min is achieved on V_{TT} must be no greater than 500 mS
2. Start Clock and maintain stable condition for 200 µS (min.).
3. After stable power and clock (CLK, $\overline{CLK}$), apply NOP or Deselect and take CKE HIGH.
4. Wait minimum of 400 nS then issue precharge all command. NOP or Deselect applied during 400 nS period.
5. Issue an EMRS command to EMR (2). (To issue EMRS command to EMR (2), provide LOW to BA0, HIGH to BA1, LOW to BA2.)
6. Issue an EMRS command to EMR (3). (To issue EMRS command to EMR (3), provide HIGH to BA0 and BA1, LOW to BA2.)
7. Issue EMRS to enable DLL. (To issue DLL Enable command, provide LOW to A0, HIGH to BA0 and LOW to BA1, LOW to BA2. And A9=A8=A7=LOW must be used when issuing this command.)
8. Issue a Mode Register Set command for DLL reset. (To issue DLL Reset command, provide HIGH to A8 and LOW to BA0 and BA1 and BA2.)
9. Issue a precharge all command.
10. Issue 2 or more Auto Refresh commands.
11. Issue a MRS command with LOW to A8 to initialize device operation. (i.e. to program operating parameters without resetting the DLL.)
12. At least 200 clocks after step 8, execute OCD Calibration (Off Chip Driver impedance adjustment). If OCD calibration is not used, EMRS to EMR (1) to set OCD Calibration Default (A9=A8=A7=HIGH) followed by EMRS to EMR (1) to exit OCD Calibration Mode (A9=A8=A7=LOW) must be issued with other operating parameters of EMR(1).
13. The DDR2 SDRAM is now ready for normal operation.

Notes:

1. To guarantee ODT off, VREF must be valid and a LOW level must be applied to the ODT pin.
2. VREF must be within ± 300 mV with respect to VDDQ/2 during supply ramp time.
3. VDD/VDDL voltage ramp time must be no greater than 200 mS from when VDD ramps from 300 mV to VDD min.
4. The VDDQ voltage ramp time from when VDD min is achieved on VDD to when VDDQ min is achieved on VDDQ must be no greater than 500 mS.

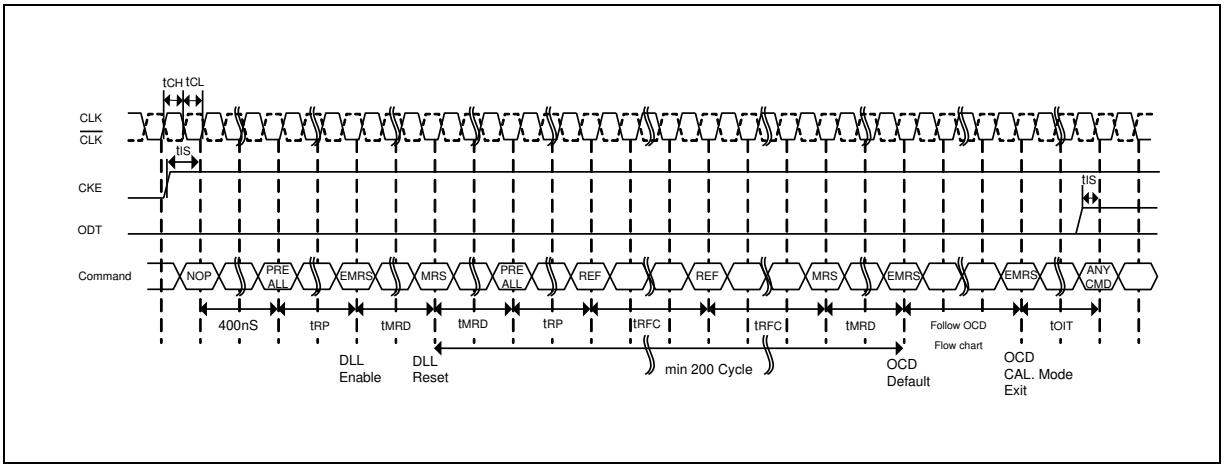


Figure 1 – Initialization sequence after power-up

8.2 Mode Register and Extended Mode Registers Operation

For application flexibility, burst length, burst type, CAS Latency, DLL reset function, write recovery time (WR) are user defined variables and must be programmed with a Mode Register Set (MRS) command. Additionally, DLL disable function, driver impedance, additive CAS Latency, ODT (On Die Termination), single-ended strobe and OCD (off chip driver impedance adjustment) are also user defined variables and must be programmed with an Extended Mode Register Set (EMRS) command. Contents of the Mode Register (MR) or Extended Mode Registers EMR (1), EMR (2) and EMR (3) can be altered by re-executing the MRS or EMRS Commands. Even if the user chooses to modify only a subset of the MR or EMR (1), EMR (2) and EMR (3) variables, all variables within the addressed register must be redefined when the MRS or EMRS commands are issued.

MRS, EMRS and Reset DLL do not affect array contents, which mean re-initialization including those can be executed at any time after power-up without affecting array contents.

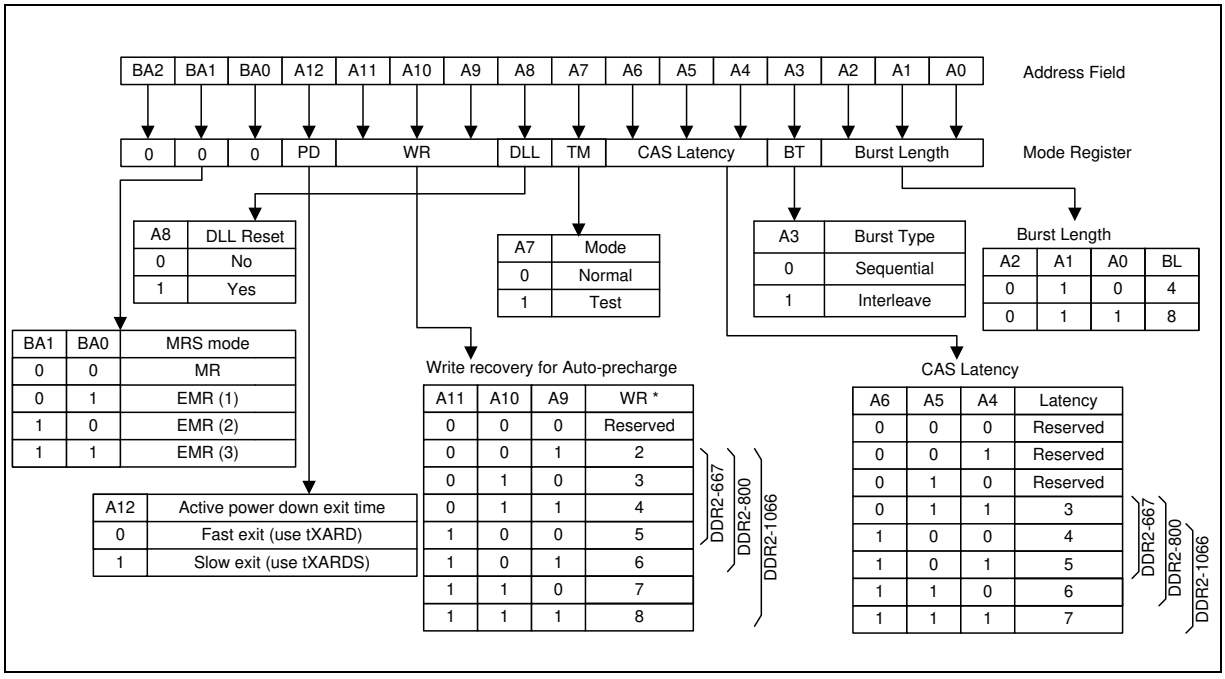
8.2.1 Mode Register Set Command (MRS)

($\overline{CS}$ = "L", $\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BA0 = "L", BA1 = "L", BA2 = "L", A0 to A12 = Register Data)

The mode register stores the data for controlling the various operating modes of DDR2 SDRAM. It programs CAS Latency, burst length, burst sequence, test mode, DLL reset, Write Recovery (WR) and various vendor specific options to make DDR2 SDRAM useful for various applications. The default value in the Mode Register after power-up is not defined, therefore the Mode Register must be programmed during initialization for proper operation.

The DDR2 SDRAM should be in all bank precharge state with CKE already HIGH prior to writing into the mode register. The mode register set command cycle time (tMRD) is required to complete the write operation to the mode register. The mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. The mode register is divided into various fields depending on functionality. Burst length is defined by

A[2:0] with options of 4 and 8 bit burst lengths. The burst length decodes are compatible with DDR SDRAM. Burst address sequence type is defined by A3, CAS Latency is defined by A[6:4]. The DDR2 does not support half clock latency mode. A7 is used for test mode. A8 is used for DLL reset. A7 must be set to LOW for normal MRS operation. Write recovery time WR is defined by A[11:9]. Refer to the table for specific codes.



Note:

1. WR (write recovery for Auto-precharge) min is determined by tCK(avg) max and WR max is determined by tCK(avg) min. WR[cycles] = RU{ tWR[nS] / tCK(avg)[nS] }, where RU stands for round up. The mode register must be programmed to this value. This is also used with tRP to determine tDAL.

Figure 2 – Mode Register Set (MRS)

8.2.2 Extend Mode Register Set Commands (EMRS)

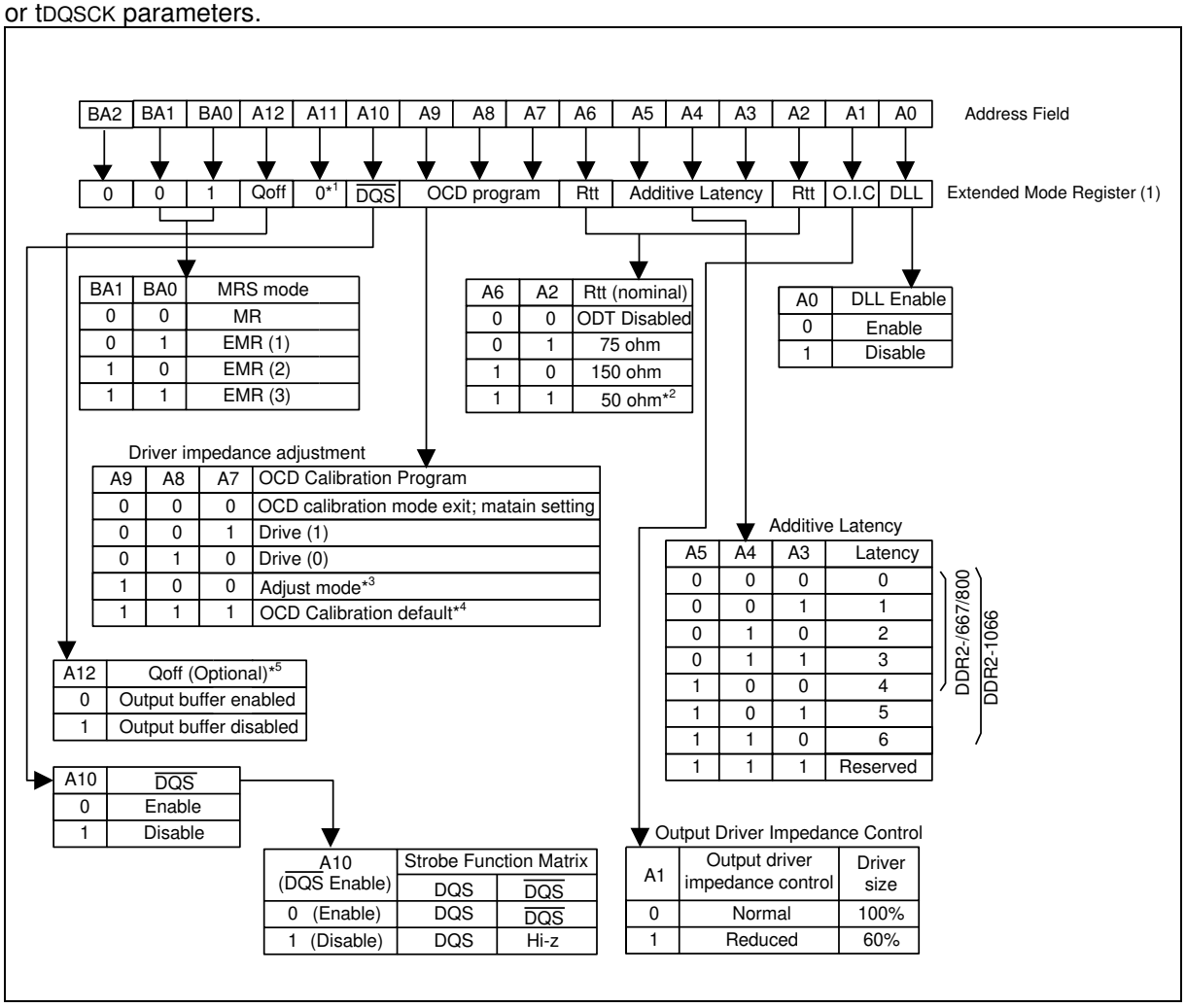
8.2.2.1 Extend Mode Register Set Command (1), EMR (1)

($\overline{CS}$ = "L", $\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BA0 = "H", BA1 = "L, BA2 = "L" A0 to A12 = Register data)

The extended mode register (1) stores the data for enabling or disabling the DLL, output driver strength, additive latency, ODT, $\overline{DQS}$ disable, OCD program. The default value of the extended mode register (1) is not defined, therefore the extended mode register (1) must be programmed during initialization for proper operation. The DDR2 SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register (1). The mode register set command cycle time (tMRD) must be satisfied to complete the write operation to the extended mode register (1). Extended mode register (1) contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state. A0 is used for DLL enable or disable. A1 is used for enabling a reduced strength output driver. A[5:3] determines the additive latency, A[9:7] are used for OCD control, A10 is used for $\overline{DQS}$ disable. A2 and A6 are used for ODT setting.

8.2.2.2 DLL Enable/Disable

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization, and upon returning to normal operation after having the DLL disabled. The DLL is automatically disabled when entering Self Refresh operation and is automatically re-enabled and reset upon exit of Self Refresh operation. Any time the DLL is enabled (and subsequently reset), 200 clock cycles must occur before a Read command can be issued to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in a violation of the t_{AC} or t_{DQSCK} parameters.



Notes:

1. A11 default is "0" RDQS disabled.
2. Optional for DDR2-667, mandatory for DDR2-800 and DDR2-1066.
3. When Adjust mode is issued, AL from previously set value must be applied.
4. After setting to default, OCD calibration mode needs to be exited by setting A9-A7 to 000. Refer to the section 8.2.3 for detailed information.
5. Output disabled - DQs, LDQS, $\overline{\text{LDQS}}$, UDQS, $\overline{\text{UDQS}}$. This feature is used in conjunction with DIMM I_{DD} measurements when I_{DDQ} is not desired to be included.

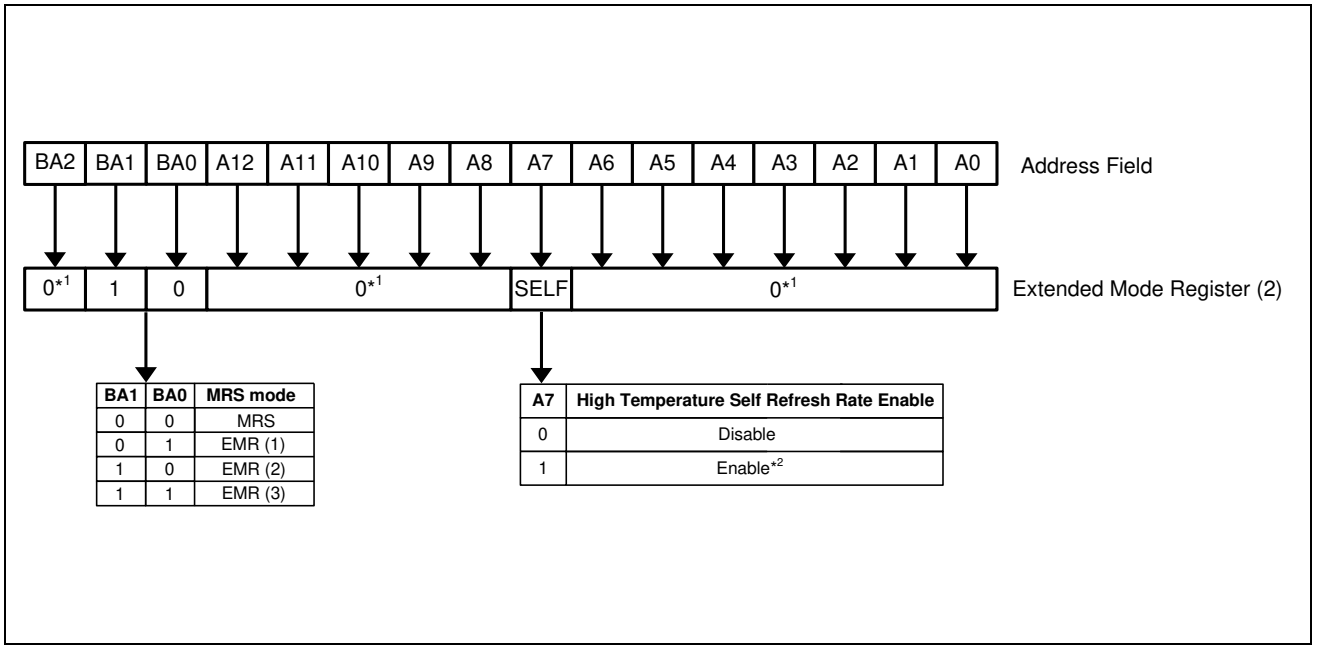
Figure 3 – EMR (1)

8.2.2.3 Extend Mode Register Set Command (2), EMR (2)

($\overline{CS}$ = "L", $\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BA0 = "L", BA1 = "H", BA2 = "L" A0 to A12 = Register data)

The extended mode register (2) controls refresh related features. The default value of the extended mode register (2) is not defined, therefore the extended mode register (2) must be programmed during initialization for proper operation.

The DDR2 SDRAM should be in all bank precharge state with CKE already high prior to writing into the extended mode register (2). The mode register set command cycle time (t_{MRD}) must be satisfied to complete the write operation to the extended mode register (2). Mode register contents can be changed using the same command and clock cycle requirements during normal operation as long as all banks are in the precharge state.



Notes:

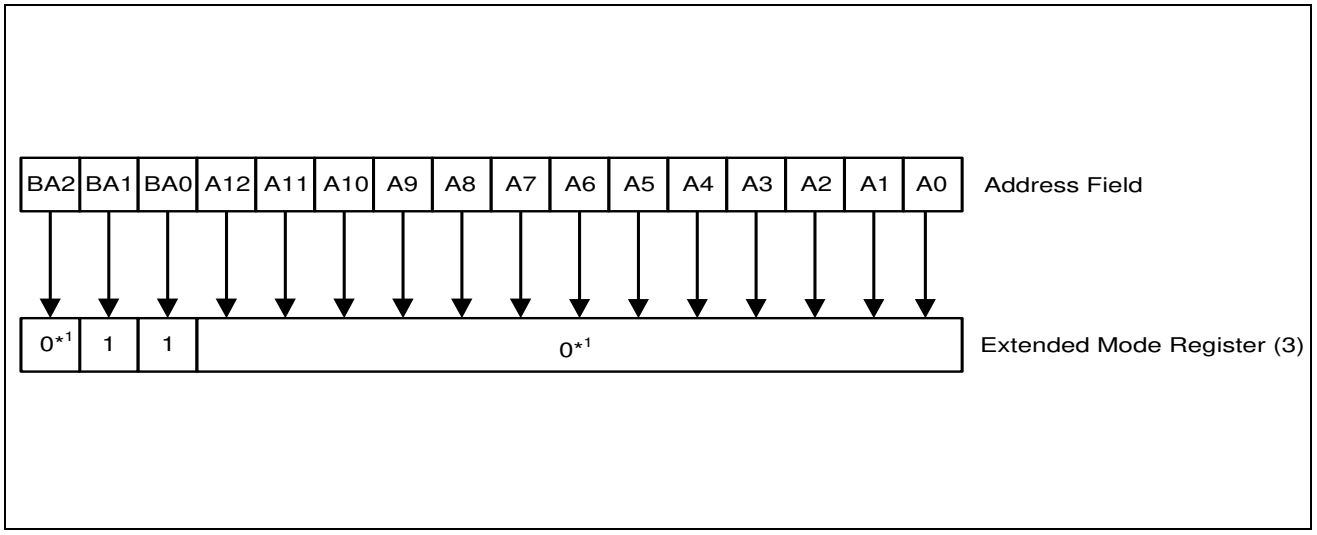
1. The rest bits in EMR (2) is reserved for future use and all bits in EMR (2) except A7, BA0, BA1 and BA2 must be programmed to "0" when setting the extended mode register (2) during initialization.
2. When DRAM is operated at 85°C < T_{CASE} ≤ 95°C the extended Self Refresh rate must be enabled by setting bit A7 to "1" before the Self Refresh mode can be entered.

Figure 4 – EMR (2)

8.2.2.4 Extend Mode Register Set Command (3), EMR (3)

($\overline{CS}$ = "L", $\overline{RAS}$ = "L", $\overline{CAS}$ = "L", $\overline{WE}$ = "L", BA0 = "H", BA1 = "H", BA2 = "L", A0 to A12 = Register data)

No function is defined in extended mode register (3). The default value of the EMR (3) is not defined, therefore the EMR (3) must be programmed during initialization for proper operation.



Note:

1. All bits in EMR(3) except BA0 and BA1 are reserved for future use and must be set to “0” when programming the EMR(3).

Figure 5 – EMR (3)

8.2.3 Off-Chip Driver (OCD) Impedance Adjustment

DDR2 SDRAM supports driver calibration feature and the flow chart in Figure 6 is an example of the sequence. Every calibration mode command should be followed by "OCD calibration mode exit" before any other command being issued. MRS should be set before entering OCD impedance adjustment and On Die Termination (ODT) should be carefully controlled depending on system environment.

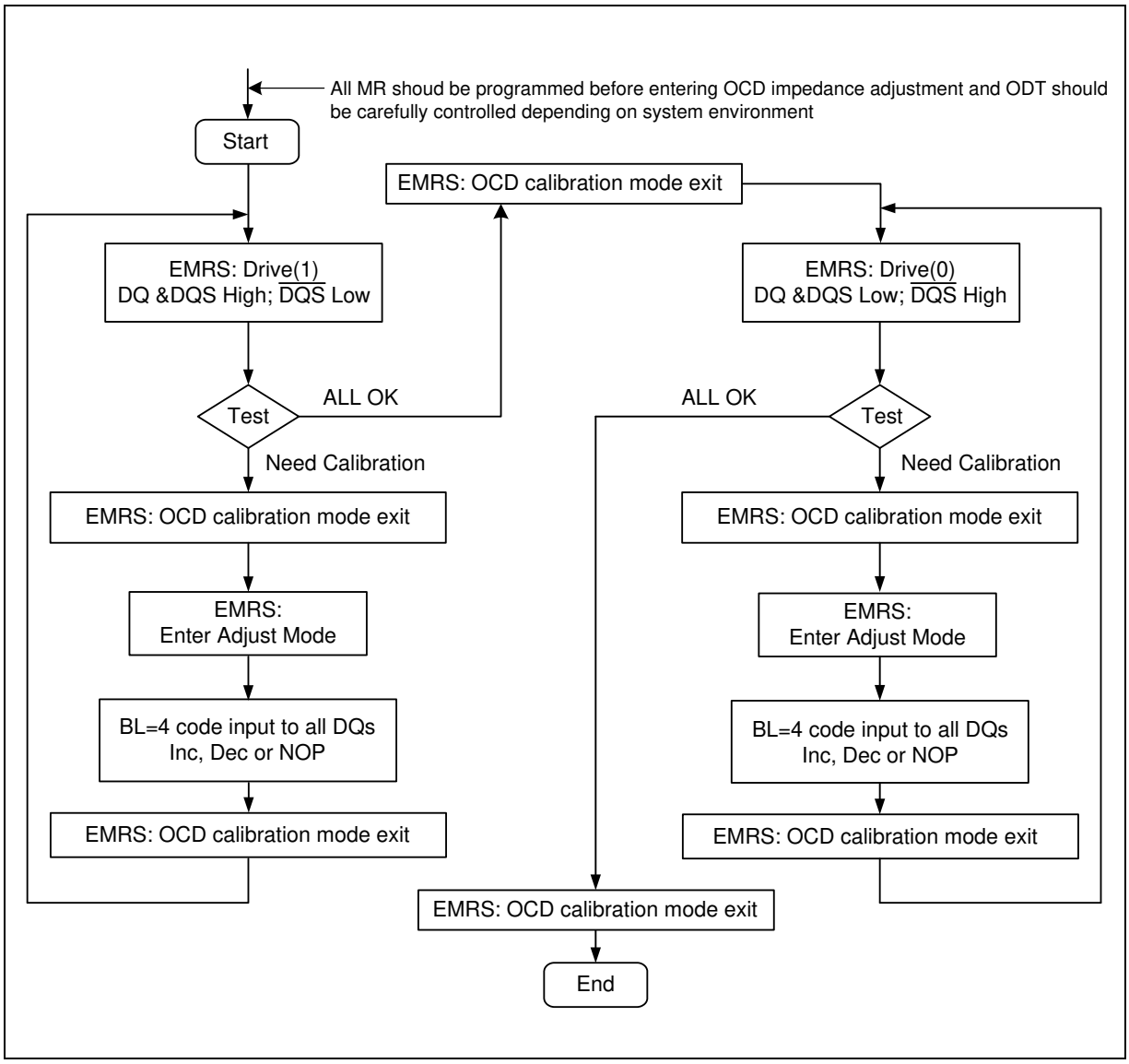


Figure 6 – OCD Impedance Adjustment Flow Chart

8.2.3.1 Extended Mode Register for OCD Impedance Adjustment

OCD impedance adjustment can be done using the following EMRS mode. In drive mode all outputs are driven out by DDR2 SDRAM. In Drive (1) mode, all DQ, DQS signals are driven HIGH and all $\overline{DQS}$ signals are driven LOW. In Drive (0) mode, all DQ, DQS signals are driven LOW and all $\overline{DQS}$ signals are driven HIGH. In adjust mode, BL = 4 of operation code data must be used. In case of OCD calibration default, output driver characteristics have a nominal impedance value of 18 Ohms during nominal temperature and voltage conditions. OCD applies only to normal full strength output drive setting defined by EMR (1) and if reduced strength is set, OCD default driver characteristics are not applicable. When OCD calibration adjust mode is used, OCD default output driver characteristics are not applicable. After OCD calibration is completed or driver strength is set to default, subsequent EMRS commands not intended to adjust OCD characteristics must specify A[9:7] as '000' in order to maintain the default or calibrated value.

Table 1 – OCD Drive Mode Program

A9	A8	A7	Operation
0	0	0	OCD calibration mode exit
0	0	1	Drive (1) DQ, DQS HIGH and $\overline{DQS}$ LOW
0	1	0	Drive (0) DQ, DQS LOW and $\overline{DQS}$ HIGH
1	0	0	Adjust mode
1	1	1	OCD calibration default

8.2.3.2 OCD Impedance Adjust

To adjust output driver impedance, controllers must issue the ADJUST EMRS command along with a 4 bit burst code to DDR2 SDRAM as in table 2. For this operation, Burst Length has to be set to BL = 4 via MRS command before activating OCD and controllers must drive the burst code to all DQs at the same time. DT_0 in table 2 means all DQ bits at bit time 0, DT_1 at bit time 1, and so forth. The driver output impedance is adjusted for all DDR2 SDRAM DQs simultaneously and after OCD calibration, all DQs and DQS's of a given DDR2 SDRAM will be adjusted to the same driver strength setting. The maximum step count for adjustment is 16 and when the limit is reached, further increment or decrement code has no effect. The default setting may be any step within the 16 step range. When Adjust mode command is issued, AL from previously set value must be applied.

Table 2 – OCD Adjust Mode Program

4 bit burst code inputs to all DQs				Operation	
DT_0	DT_1	DT_2	DT_3	**Pull-up driver strength**	**Pull-down driver strength**
0	0	0	0	NOP (No operation)	NOP (No operation)
0	0	0	1	Increase by 1 step	NOP
0	0	1	0	Decrease by 1 step	NOP
0	1	0	0	NOP	Increase by 1 step
1	0	0	0	NOP	Decrease by 1 step
0	1	0	1	Increase by 1 step	Increase by 1 step
0	1	1	0	Decrease by 1 step	Increase by 1 step
1	0	0	1	Increase by 1 step	Decrease by 1 step
1	0	1	0	Decrease by 1 step	Decrease by 1 step
Other Combinations				Reserved	

For proper operation of adjust mode, WL = RL - 1 = AL + CL - 1 clocks and t_{DS}/t_{DH} should be met as shown in Figure 7. For input data pattern for adjustment, D_{T0} - D_{T3} is a fixed order and is not affected by burst type (i.e., sequential or interleave).

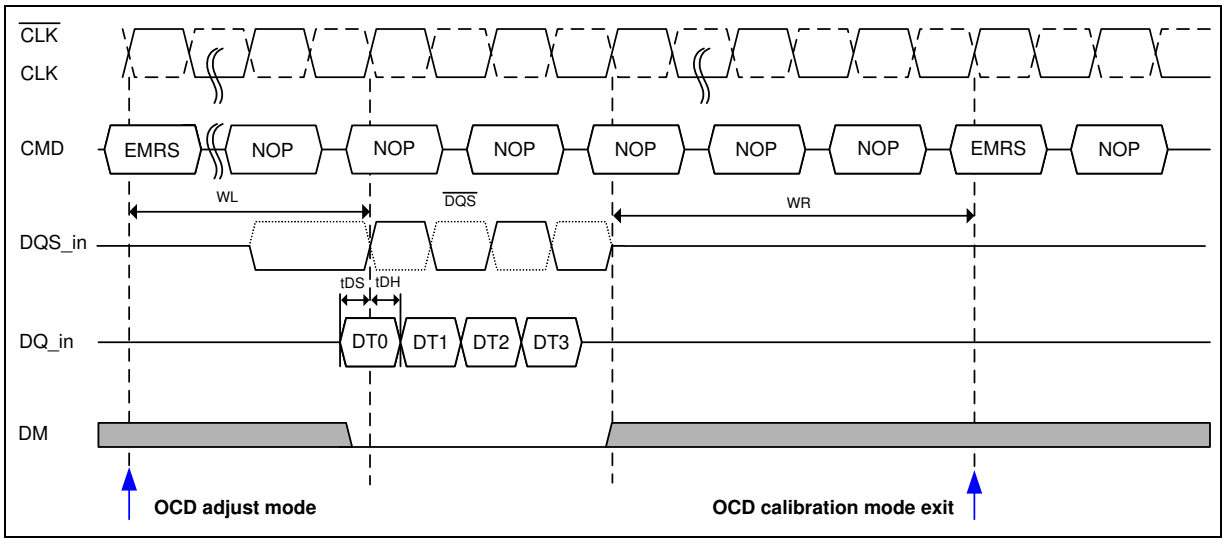


Figure 7 – OCD Adjust Mode

8.2.3.3 Drive Mode

Drive mode, both Drive (1) and Drive (0), is used for controllers to measure DDR2 SDRAM Driver impedance. In this mode, all outputs are driven out t_{OIT} after "enter drive mode" command and all output drivers are turned-off t_{OIT} after "OCD calibration mode exit" command as shown in Figure 8.

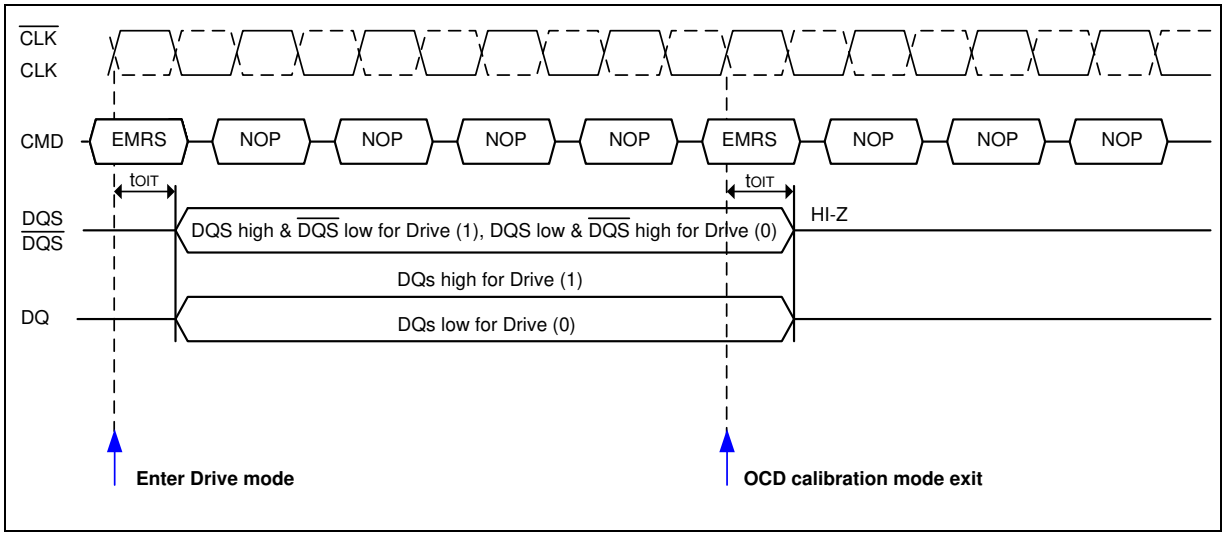
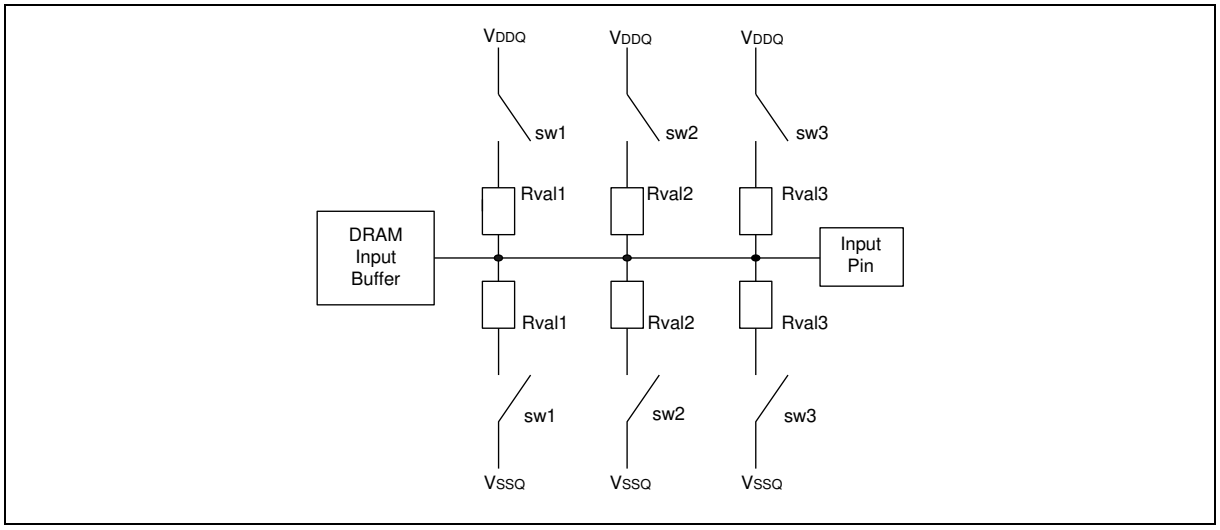


Figure 8 – OCD Drive Mode

8.2.4 On-Die Termination (ODT)

On-Die Termination (ODT) is a new feature on DDR2 components that allows a DRAM to turn on/off termination resistance for each DQ, UDQS/$\overline{\text{UDQS}}$, LDQS/$\overline{\text{LDQS}}$, UDM and LDM signal via the ODT control pin. $\overline{\text{UDQS}}$ and $\overline{\text{LDQS}}$ are terminated only when enabled in the EMR (1) by address bit A10 = 0. The ODT feature is designed to improve signal integrity of the memory channel by allowing the DRAM controller to independently turn on/off termination resistance for any or all DRAM devices.

The ODT function can be used for all active and standby modes. ODT is turned off and not supported in Self Refresh mode. *(Example timing waveforms refer to 11.2, 11.3 ODT Timing for Active/Standby/Power Down Mode and 11.4, 11.5 ODT timing mode switch at entering/exiting power down mode diagram in Chapter 11)*



Switch (sw1, sw2, sw3) is enabled by ODT pin.

Selection among sw1, sw2, and sw3 is determined by "Rtt (nominal)" in EMR (1).

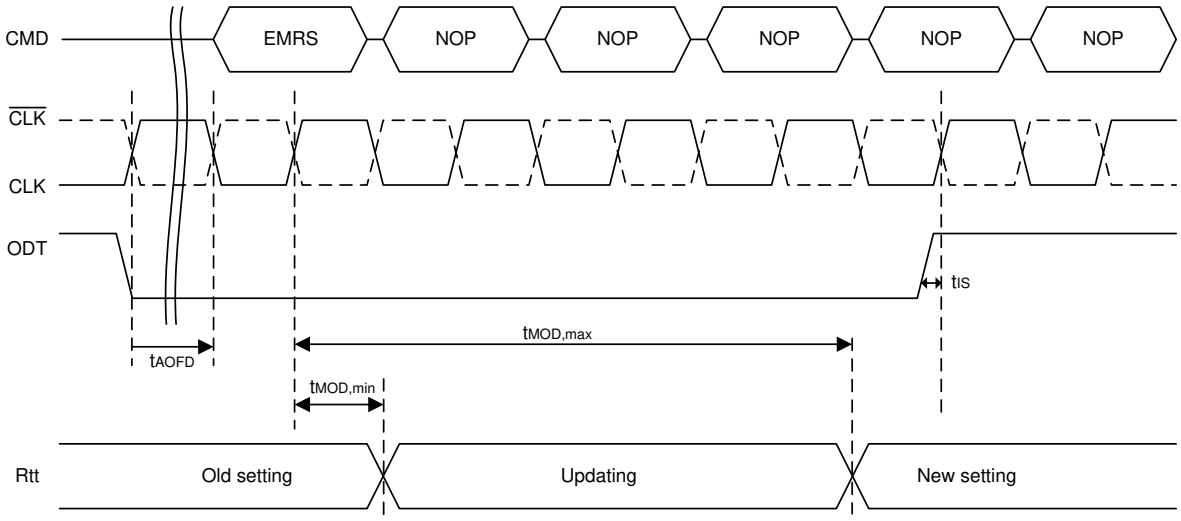
Termination included on all DQs, DM, DQS, $\overline{\text{DQS}}$ pins.

Figure 9 – Functional Representation of ODT

8.2.5 ODT related timings

8.2.5.1 MRS command to ODT update delay

During normal operation the value of the effective termination resistance can be changed with an EMRS command. The update of the Rtt setting is done between t_{MOD},min and t_{MOD},max, and CKE must remain HIGH for the entire duration of t_{MOD} window for proper operation. The timings are shown in the following timing diagram.



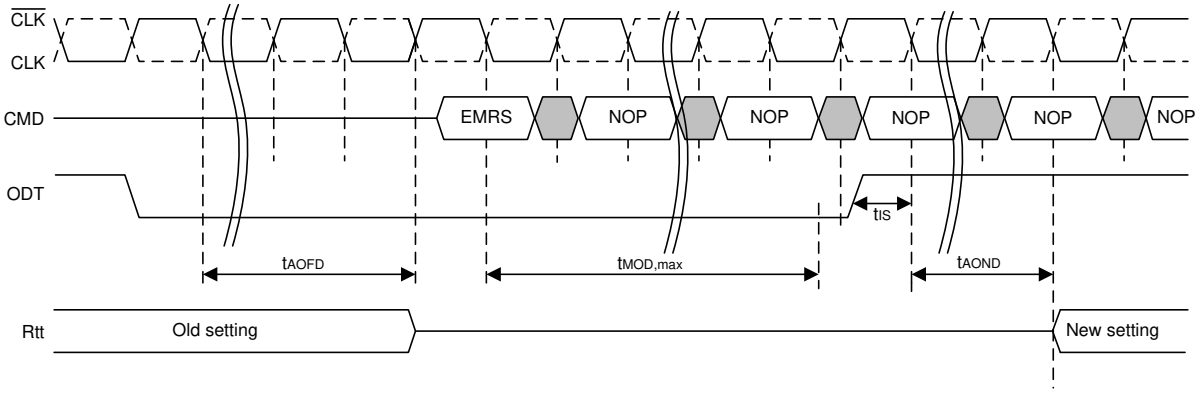
1) EMRS command directed to EMR(1), which updates the information in EMR(1)[A6,A2], i.e. Rtt (Nominal).
2) "setting" in this diagram is the Register and I/O setting, not what is measured from outside.

Figure 10 – ODT update delay timing - tMOD

However, to prevent any impedance glitch on the channel, the following conditions must be met.

- tAOFD must be met before issuing the EMRS command.
- ODT must remain LOW for the entire duration of tMOD window, until tMOD,max is met.

Now the ODT is ready for normal operation with the new setting, and the ODT signal may be raised again to turned on the ODT. Following timing diagram shows the proper Rtt update procedure.



1) EMRS command directed to EMR(1), which updates the information in EMR(1)[A6,A2], i.e. Rtt (Nominal).
2) "setting" in this diagram is what is measured from outside.

Figure 11 – ODT update delay timing - tMOD, as measured from outside

8.3 Command Function

8.3.1 Bank Activate Command

($\overline{CS}$ ="L", $\overline{RAS}$ ="L", $\overline{CAS}$ ="H", $\overline{WE}$ ="H", BA0, BA1, BA2=Bank, A0 to A12 be row address)

The Bank Activate command must be applied before any Read or Write operation can be executed. Immediately after the bank active command, the DDR2 SDRAM can accept a read or write command on the following clock cycle. If a Read/Write command is issued to a bank that has not satisfied the tRCDmin specification, then additive latency must be programmed into the device to delay when the Read/Write command is internally issued to the device. The additive latency value must be chosen to assure tRCDmin is satisfied. Additive latencies of 0, 1, 2, 3, 4, 5 and 6 are supported. Once a bank has been activated it must be precharged before another Bank Activate command can be applied to the same bank. The bank active and precharge times are defined as tRAS and tRP, respectively. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device (tRC). The minimum time interval between Bank Activate commands is tRRD.

In order to ensure that components with 8 internal memory banks do not exceed the instantaneous current supplying capability, certain restrictions on operation of the 8 banks must be observed. There are two rules. One for restricting the number of sequential ACT commands that can be issued and another for allowing more time for RAS precharge for a Precharge All command. The rules are as follows:

- Sequential Bank Activation Restriction: No more than 4 banks may be activated in a rolling tFAW window. Converting to clocks is done by dividing tFAW[nS] by tCK(avg)[ns], and rounding up to next integer value. As an example of the rolling window, if RU{ (tFAW / tCK(avg) } is 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued at or between clock N+1 and N+9.
- Precharge All Allowance: tRP for a Precharge All command is equal to tnRP + 1 x nCK, where tnRP = RU{ tRP / tCK(avg) } and tRP is the value for a single bank precharge.

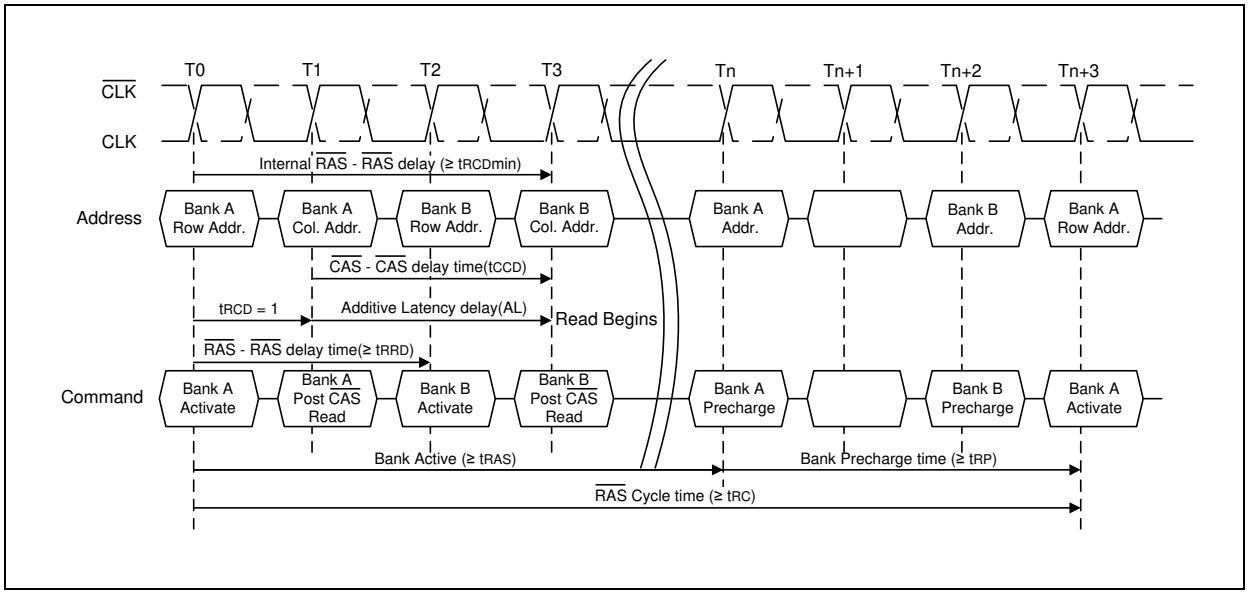


Figure 12 – Bank activate command cycle: tRCD = 3, AL = 2, tRP = 3, tRRD = 2, tCCD = 2

8.3.2 Read Command

($\overline{CS}$ ="L", $\overline{RAS}$ ="H", $\overline{CAS}$ ="L", $\overline{WE}$ ="H", BA0, BA1, BA2=Bank, A10="L", A0 to A9=Column Address)

The READ command is used to initiate a burst read access to an active row. The value on BA0, BA1, BA2 inputs selects the bank, and the A0 to A9 address inputs determine the starting column address. The address input A10 determines whether or not Auto-precharge is used. If Auto-precharge is selected, the row being accessed will be precharged at the end of the READ burst; if Auto-precharge is not selected, the row will remain open for subsequent accesses.

8.3.3 Write Command

($\overline{CS}$ ="L", $\overline{RAS}$ ="H", $\overline{CAS}$ ="L", $\overline{WE}$ ="L", BA0, BA1, BA2=Bank, A10="L", A0 to A9=Column Address)

The WRITE command is used to initiate a burst write access to an active row. The value on BA0, BA1, BA2 inputs selects the bank, and the A0 to A9 address inputs determine the starting column address. The address input A10 determines whether or not Auto-precharge is used. If Auto-precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if Auto-precharge is not selected, the row will remain open for subsequent accesses.

8.3.4 Burst Read with Auto-precharge Command

($\overline{CS}$ ="L", $\overline{RAS}$ ="H", $\overline{CAS}$ ="L", $\overline{WE}$ ="H", BA0, BA1, BA2=Bank, A10="H", A0 to A9=Column Address)

If A10 is HIGH when a Read Command is issued, the Read with Auto-precharge function is engaged. The DDR2 SDRAM starts an Auto-precharge operation on the rising edge which is (AL + BL/2) cycles later than the read with AP command if t_{RAS}(min) and t_{RTP}(min) are satisfied.

8.3.5 Burst Write with Auto-precharge Command

($\overline{CS}$ ="L", $\overline{RAS}$ ="H", $\overline{CAS}$ ="L", $\overline{WE}$ ="L", BA0, BA1, BA2=Bank, A10="H", A0 to A9=Column Address)

If A10 is HIGH when a Write Command is issued, the Write with Auto-precharge function is engaged. The DDR2 SDRAM automatically begins precharge operation after the completion of the burst write plus write recovery time (WR) programmed in the mode register.

8.3.6 Precharge All Command

($\overline{CS}$ ="L", $\overline{RAS}$ ="L", $\overline{CAS}$ ="H", $\overline{WE}$ ="L", BA0, BA1, BA2=Don't Care, A10="H", A0 to A9 and A11 to A12=Don't Care)

The Precharge All command precharge all banks simultaneously. Then all banks are switched to the idle state.

8.3.7 Self Refresh Entry Command

($\overline{CS}$ ="L", $\overline{RAS}$ ="L", $\overline{CAS}$ ="L", $\overline{WE}$ ="H", CKE="L", BA0, BA1, BA2, A0 to A12=Don't Care)

The Self Refresh command can be used to retain data, even if the rest of the system is powered down. When in the Self Refresh mode, the DDR2 SDRAM retains data without external clocking. The DDR2 SDRAM device has a built-in timer to accommodate Self Refresh operation. ODT must be turned off before issuing Self Refresh command, by either driving ODT pin LOW or using an EMRS command. Once the command is registered, CKE must be held LOW to keep the device in Self Refresh mode. The DLL is automatically disabled upon entering Self Refresh and is automatically enabled upon exiting Self Refresh. When the DDR2 SDRAM has entered Self Refresh mode, all of the external signals except CKE, are "Don't Care".

The clock is internally disabled during self refresh operation to save power. The user may change the external clock frequency or halt the external clock one clock after Self Refresh entry is registered; however, the clock must be restarted and stable before the device can exit self refresh operation.

8.3.8 Self Refresh Exit Command

(CKE="H", $\overline{CS}$ ="H" or CKE="H", $\overline{CS}$ ="L", $\overline{RAS}$ ="H", $\overline{CAS}$ ="H", $\overline{WE}$ ="H", BA0, BA1, BA2, A0 to A12=Don't Care)

The procedure for exiting Self Refresh requires a sequence of commands. First, the clock must be stable prior to CKE going back HIGH. Once Self Refresh Exit is registered, a delay of at least tXSNR must be satisfied before a valid command can be issued to the device to allow for any internal refresh in progress. CKE must remain HIGH for the entire Self Refresh exit period tXSRD for proper operation except for self refresh re-entry.

Upon exit from Self Refresh, the DDR2 SDRAM can be put back into Self Refresh mode after waiting at least tXSNR period and issuing one refresh command (refresh period of tRFC). NOP or Deselect commands must be registered on each positive clock edge during the Self Refresh exit interval tXSNR. ODT should be turned off during tXSRD.

The use of Self Refresh mode introduces the possibility that an internally timed refresh event can be missed when CKE is raised for exit from Self Refresh mode. Upon exit from Self Refresh, the DDR2 SDRAM requires a minimum of one extra auto refresh command before it is put back into Self Refresh mode.

8.3.9 Refresh Command

($\overline{CS}$ ="L", $\overline{RAS}$ ="L", $\overline{CAS}$ ="L", $\overline{WE}$ ="H", CKE="H", BA0, BA1, BA2, A0 to A12=Don't Care)

Refresh is used during normal operation of the DDR2 SDRAM. This command is non persistent, so it must be issued each time a refresh is required.

The refresh addressing is generated by the internal refresh controller. This makes the address bits "Don't Care" during an Auto Refresh command. The DDR2 SDRAM requires Auto Refresh cycles at an average periodic interval of tREFI (max.).

When the refresh cycle has completed, all banks of the DDR2 SDRAM will be in the precharged (idle) state. A delay between the auto refresh command (REF) and the next activate command or subsequent auto refresh command must be greater than or equal to the auto refresh cycle time (tRFC).

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute refresh interval is provided. A maximum of eight Refresh commands can be posted to any given DDR2 SDRAM, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 9 x tREFI.

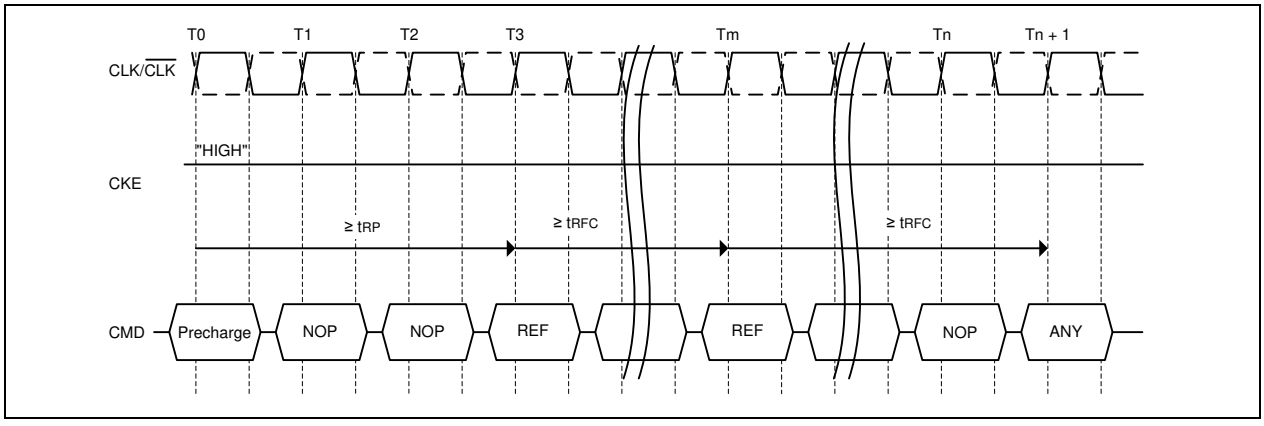


Figure 13 – Refresh command

8.3.10 No-Operation Command

($\overline{CS}$ = "L", $\overline{RAS}$ = "H", $\overline{CAS}$ = "H", $\overline{WE}$ = "H", CKE, BA0, BA1, BA2, A0 to A12 = Don't Care)

The No-Operation command simply performs no operation (same command as Device Deselect).

8.3.11 Device Deselect Command

($\overline{CS}$ = "H", $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE, BA0, BA1, BA2, A0 to A12 = Don't Care)

The Device Deselect command disables the command decoder so that the $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ and Address inputs are ignored. This command is similar to the No-Operation command.

8.4 Read and Write access modes

The DDR2 SDRAM provides a fast column access operation. A single Read or Write Command will initiate a serial read or write operation on successive clock cycles. The boundary of the burst cycle is strictly restricted to specific segments of the page length.

The 8 Mbit x 16 I/O x 8 Bank chip has a page length of 1024 bits (defined by CA0 to CA9)*. The page length of 1024 is divided into 256 or 128 uniquely addressable boundary segments depending on burst length, 256 for 4 bit burst, 128 for 8 bit burst respectively. A 4-bit or 8-bit burst operation will occur entirely within one of the 256 or 128 groups beginning with the column address supplied to the device during the Read or Write Command (CA0 to CA9). The second, third and fourth access will also occur within this group segment. However, the burst order is a function of the starting address, and the burst sequence.

A new burst access must not interrupt the previous 4 bit burst operation in case of BL = 4 setting. However, in case of BL = 8 setting, two cases of interrupt by a new burst access are allowed, one reads interrupted by a read, the other writes interrupted by a write with 4 bit burst boundary respectively. The minimum $\overline{CAS}$ to $\overline{CAS}$ delay is defined by t_{CCD}, and is a minimum of 2 clocks for read or write cycles.

Note: Page length is a function of I/O organization and column addressing

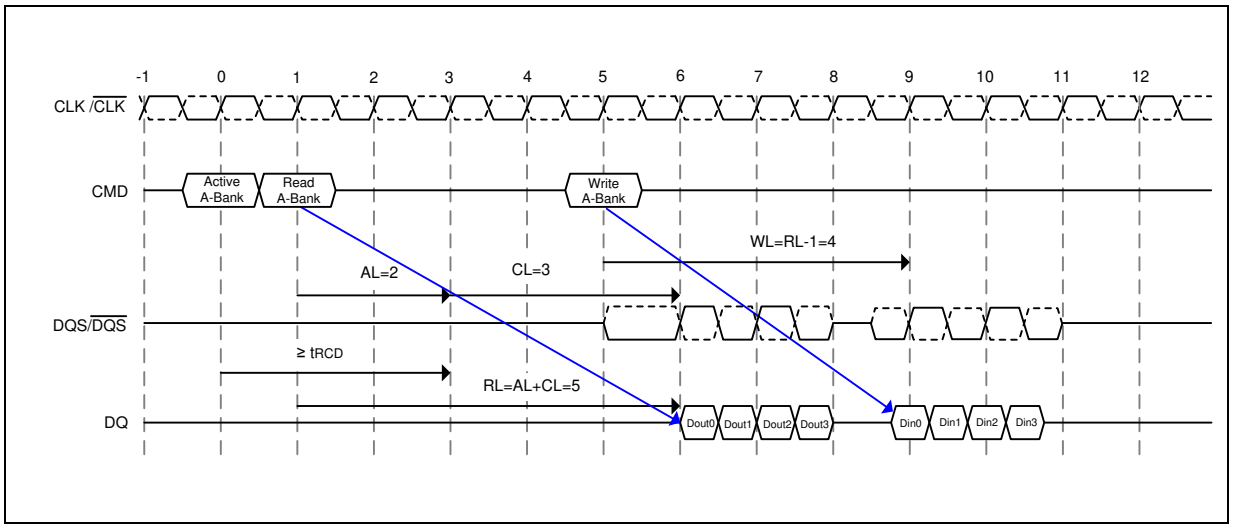
8M bits × 16 organization (CA0 to CA9); Page Length = 1024 bits

8.4.1 Posted $\overline{CAS}$

Posted $\overline{CAS}$ operation is supported to make command and data bus efficient for sustainable bandwidths in DDR2 SDRAM. In this operation, the DDR2 SDRAM allows a $\overline{CAS}$ read or write command to be issued immediately after the $\overline{RAS}$ bank activate command (or any time during the $\overline{RAS}$ - $\overline{CAS}$ -delay time, t_{RCD}, period). The command is held for the time of the Additive Latency (AL) before it is issued inside the device. The Read Latency (RL) is controlled by the sum of AL and the CAS Latency (CL). Therefore if a user chooses to issue a Read/Write command before the t_{RCDmin}, then AL (greater than 0) must be written into the EMR (1). The Write Latency (WL) is always defined as RL -1 (Read Latency -1) where Read Latency is defined as the sum of Additive Latency plus CAS Latency (RL = AL + CL). Read or Write operations using AL allow seamless bursts. *(Example timing waveforms refer to 11.10 and 11.11 seamless burst read/write operation diagram in Chapter 11)*

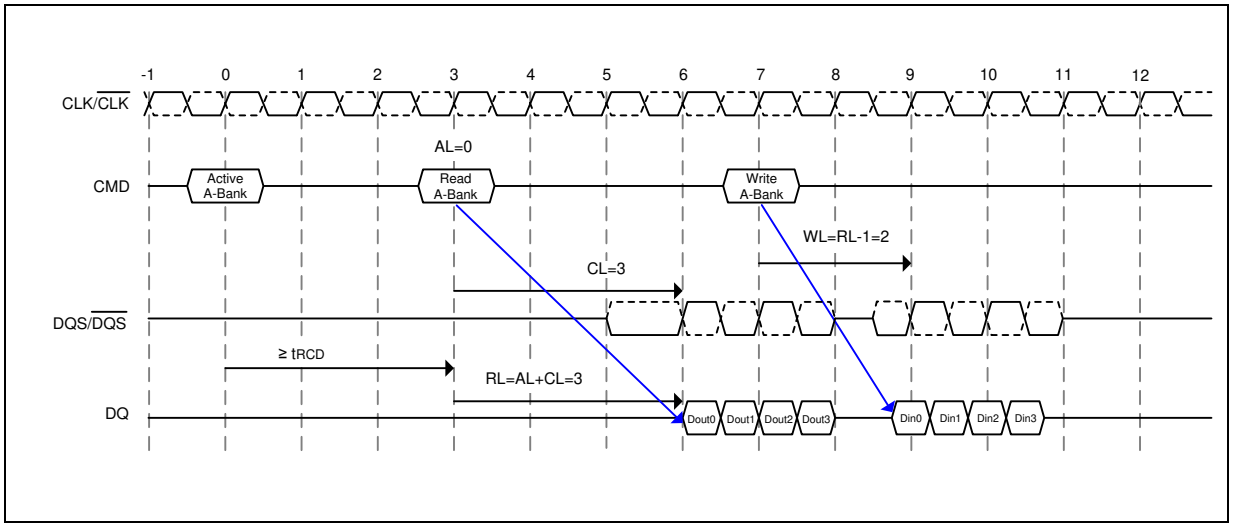
8.4.1.1 Examples of posted $\overline{CAS}$ operation

Examples of a read followed by a write to the same bank where AL = 2 and where AL = 0 are shown in Figures 14 and 15, respectively.



[AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4, BL = 4]

Figure 14 – Example 1: Read followed by a write to the same bank, where AL = 2 and CL = 3, RL = (AL + CL) = 5, WL = (RL - 1) = 4, BL = 4



AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2, BL = 4]

Figure 15 – Example 2: Read followed by a write to the same bank, where AL = 0 and CL = 3, RL = (AL + CL) = 3, WL = (RL - 1) = 2, BL = 4

8.4.2 Burst mode operation

Burst mode operation is used to provide a constant flow of data to memory locations (write cycle), or from memory locations (read cycle). The parameters that define how the burst mode will operate are burst sequence and burst length. The DDR2 SDRAM supports 4 bit and 8 bit burst modes only. For 8 bit burst mode, full interleave address ordering is supported, however, sequential address ordering is nibble based for ease of implementation. The burst length is programmable and defined by MR A[2:0]. The burst type, either sequential or interleaved, is programmable and defined by MR [A3]. Seamless burst read or write operations are supported.

Unlike DDR1 devices, interruption of a burst read or writes cycle during BL = 4 mode operation is prohibited. However in case of BL = 8 mode, interruption of a burst read or write operation is limited to two cases, reads interrupted by a read, or writes interrupted by a write. *(Example timing waveforms refer to 11.12 and 11.13 Burst read and write interrupt timing diagram in Chapter 11)*

Therefore the Burst Stop command is not supported on DDR2 SDRAM devices.

Table 3 – Burst Length and Sequence

Burst Length	Starting Address (A2 A1 A0)	Sequential Addressing (decimal)	Interleave Addressing (decimal)
4	x00	0, 1, 2, 3	0, 1, 2, 3
	x01	1, 2, 3, 0	1, 0, 3, 2
	x10	2, 3, 0, 1	2, 3, 0, 1
	x11	3, 0, 1, 2	3, 2, 1, 0
8	000	0, 1, 2, 3, 4, 5, 6, 7	0, 1, 2, 3, 4, 5, 6, 7
	001	1, 2, 3, 0, 5, 6, 7, 4	1, 0, 3, 2, 5, 4, 7, 6
	010	2, 3, 0, 1, 6, 7, 4, 5	2, 3, 0, 1, 6, 7, 4, 5
	011	3, 0, 1, 2, 7, 4, 5, 6	3, 2, 1, 0, 7, 6, 5, 4
	100	4, 5, 6, 7, 0, 1, 2, 3	4, 5, 6, 7, 0, 1, 2, 3
	101	5, 6, 7, 4, 1, 2, 3, 0	5, 4, 7, 6, 1, 0, 3, 2
	110	6, 7, 4, 5, 2, 3, 0, 1	6, 7, 4, 5, 2, 3, 0, 1
	111	7, 4, 5, 6, 3, 0, 1, 2	7, 6, 5, 4, 3, 2, 1, 0

8.4.3 Burst read mode operation

Burst Read is initiated with a READ command. The address inputs determine the starting column address for the burst. The delay from the start of the command to when the data from the first cell appears on the outputs is equal to the value of the read latency (RL). The data strobe output (DQS) is driven LOW one clock cycle before valid data (DQ) is driven onto the data bus. The first bit of the burst is synchronized with the rising edge of the data strobe (DQS). Each subsequent data-out appears on the DQ pin in phase with the DQS signal in a source synchronous manner. The RL is equal to an additive latency (AL) plus CAS Latency (CL). The CL is defined by the Mode Register Set (MRS). The AL is defined by the Extended Mode Register EMR (1). *(Example timing waveforms refer to 11.6 and 11.7 Data output (read) timing and Burst read operation diagram in Chapter 11)*

8.4.4 Burst write mode operation

Burst Write is initiated with a WRITE command. The address inputs determine the starting column address for the burst. Write Latency (WL) is defined by a Read Latency (RL) minus one and is equal to (AL + CL -1); and is the number of clocks of delay that are required from the time the write command is registered to the clock edge associated to the first DQS strobe. A data strobe signal (DQS) should be driven LOW (preamble) nominally half clock prior to the WL. The first data bit of the burst cycle must be applied to the DQ pins at the first rising edge of the DQS following the preamble. The t_{DQSS} specification must be satisfied for each positive DQS transition to its associated clock edge during write cycles. The subsequent burst bit data are issued on successive edges of the DQS until the burst length is completed, which is 4 or 8 bit burst. When the burst has finished, any additional data supplied to the DQ pins will be ignored. The DQ Signal is ignored after the burst write operation is complete. The time from the completion of the burst write to bank precharge is the write recovery time (WR). *(Example timing waveforms refer to 11.8 and 11.9 Data input (write) timing and Burst write operation diagram in Chapter 11)*