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1. GENERAL DESCRIPTION

LPDDR2 is a high-speed SDRAM device internally configured as a 4-Bank memory. These devices contains 256Mb has 268,435,456 bits.

All LPDDR2 devices use a double data rate architecture on the Command/Address (CA) bus to reduce the number of input pins in the system. The 10-bit CA bus contains command, address, and Bank/Row Buffer information. Each command uses one clock cycle, during which command information is transferred on both the positive and negative edge of the clock.

For LPDDR2 devices, accesses begin with the registration of an Activate command, which is then followed by a Read or Write command. The address and BA bits registered coincident with the Activate command are used to select the row and the Bank to be accessed. The address bits registered coincident with the Read or Write command are used to select the Bank and the starting column location for the burst access.

2. FEATURES

- VDD1 = 1.7~1.95V
- VDD2/VDDCA/VDDQ = 1.14V~1.30V
- Data width: x16 / x32
- Clock rate: up to 533 MHz
- Data rate: up to 1066 Mb/s/pin
- Four-bit prefetch DDR architecture
- Four internal banks
- Programmable READ and WRITE latencies (RL/WL)
- Programmable burst lengths: 4, 8, or 16
- Auto refresh: All bank refresh mode only
- Partial Array Self-Refresh (PASR):

  All bank or per bank, bank mask is supported but segment mask is not supported
- Precharge command: All bank or per bank
- Read with auto-precharge
- Write with auto-precharge
- Deep Power Down Mode (DPD Mode)
- Programmable output buffer driver strength
- Data mask (DM) for write data
- Clock Stop capability during idle periods
- Double data rate for data output
- Differential clock inputs
- Bidirectional differential data strobe
- Interface: HSUL_12
- JEDEC LPDDR2-S4B compliance
- Support package:

  Single channel: 134 VFBGA (10mm x11.5mm)

  Single channel: 168 WFBGA (12mm x12mm)
- Operating Temperature Range:

  -25°C ≤ T_{CASE} ≤ 85°C

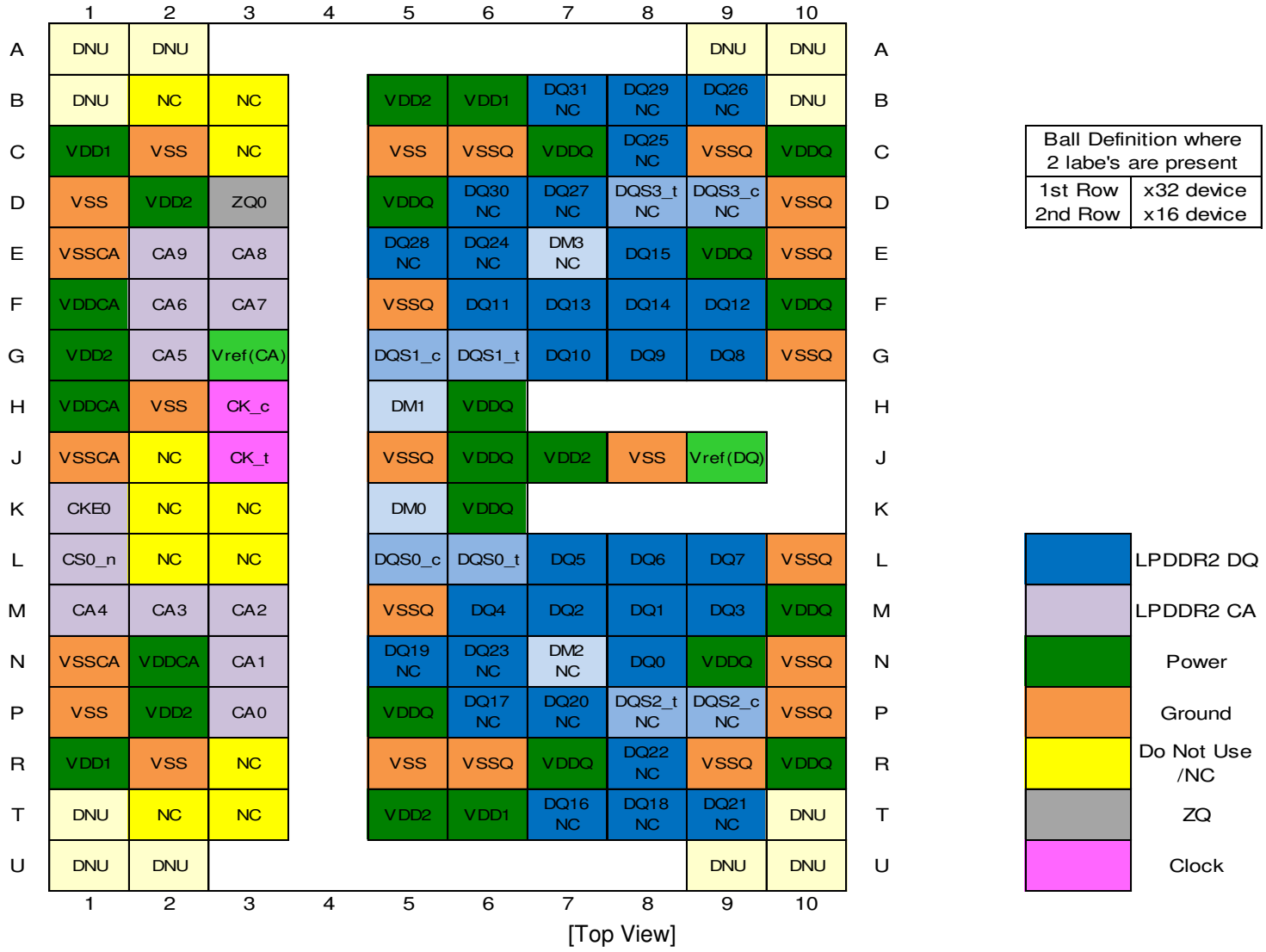
  -40°C ≤ T_{CASE} ≤ 85°C

3. ORDER INFORMATION

Part Number	VDD1/VDD2/VDDQ	I/O Width	Package	Others
W978H6KBQX2I	1.8V/1.2V/1.2V	16	168WFBGA	400MHz, -40°C~85°C
W978H2KBQX2I	1.8V/1.2V/1.2V	32	168WFBGA	400MHz, -40°C~85°C
W978H6KBQX1I	1.8V/1.2V/1.2V	16	168WFBGA	533MHz, -40°C~85°C
W978H2KBQX1I	1.8V/1.2V/1.2V	32	168WFBGA	533MHz, -40°C~85°C
W978H6KBQX2E	1.8V/1.2V/1.2V	16	168WFBGA	400MHz, -25°C~85°C
W978H2KBQX2E	1.8V/1.2V/1.2V	32	168WFBGA	400MHz, -25°C~85°C
W978H6KBQX1E	1.8V/1.2V/1.2V	16	168WFBGA	533MHz, -25°C~85°C
W978H2KBQX1E	1.8V/1.2V/1.2V	32	168WFBGA	533MHz, -25°C~85°C
W978H6KBVX2I	1.8V/1.2V/1.2V	16	134VFBGA	400MHz, -40°C~85°C
W978H2KBVX2I	1.8V/1.2V/1.2V	32	134VFBGA	400MHz, -40°C~85°C
W978H6KBVX1I	1.8V/1.2V/1.2V	16	134VFBGA	533MHz, -40°C~85°C
W978H2KBVX1I	1.8V/1.2V/1.2V	32	134VFBGA	533MHz, -40°C~85°C
W978H6KBVX2E	1.8V/1.2V/1.2V	16	134VFBGA	400MHz, -25°C~85°C
W978H2KBVX2E	1.8V/1.2V/1.2V	32	134VFBGA	400MHz, -25°C~85°C
W978H6KBVX1E	1.8V/1.2V/1.2V	16	134VFBGA	533MHz, -25°C~85°C
W978H2KBVX1E	1.8V/1.2V/1.2V	32	134VFBGA	533MHz, -25°C~85°C

4. PIN CONFIGURATION

4.1 134 Ball VFBGA



4.2 168 Ball WFBGA

168Ball WFBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
A	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	VDD1	VSSQ	DQ30	DQ29	VSSQ	DQ26	DQ25	VSSQ	DQS3_c	VDD1	VSS	NC	NC
B	NC	NC	VDD1	NC	VSS	NC	NC	VSS	NC	VSS	VDD2	DQ31	VDDQ	DQ28	DQ27	VDDQ	DQ24	DQS3_t	VDDQ	DM3	VDD2	NC	NC
C	VSS	VDD2																				DQ15	VSSQ
D	NC	NC																				VDDQ	DQ14
E	NC	NC																				DQ12	DQ13
F	NC	VSS																				DQ11	VSSQ
G	NC	NC																				VDDQ	DQ10
H	NC	NC																				DQ8	DQ9
J	NC	VSS																				DQS1_t	VSSQ
K	NC	NC																				VDDQ	DQS1_c
L	NC	NC																				VDD2	DM1
M	NC	VSS																				Vref(DQ)	VSS
N	NC	VDD1																				VDD1	DM0
P	ZQ	Vref(CA)																				DQS0_c	VSSQ
R	VSS	VDD2																				VDDQ	DQS0_t
T	CA9	CA8																				DQ6	DQ7
U	CA7	VDDCA																				DQ5	VSSQ
V	VSSCA	CA6																				VDDQ	DQ4
W	CA5	VDDCA																				DQ2	DQ3
Y	CK_c	CK_t																				DQ1	VSSQ
AA	VSS	VDD2																				VDDQ	DQ0
AB	NC	NC	CS_n	NC	VDD1	CA1	VSSCA	CA3	CA4	VDD2	VSS	DQ16	VDDQ	DQ18	DQ20	VDDQ	DQ22	DQS2_t	VDDQ	DM2	VDD2	NC	NC
AC	NC	NC	CKE	NC	VSS	CA0	CA2	VDDCA	VSS	NC	NC	VSSQ	DQ17	DQ19	VSSQ	DQ21	DQ23	VSSQ	DQS2_c	VDD1	VSS	NC	NC

[Top View]

Note: x16: DQ16~DQ31,DM2,DM3,DQS2_t,DQS2_c, DQS3_t & DQS3_c is NC.

5. PIN DESCRIPTION

5.1 Basic Functionality

Name	Type	Description
CK_t, CK_c	Input	**Clock:** CK_t and CK_c are differential clock inputs. All Double Data Rate (DDR) CA inputs are sampled on both positive and negative edge of CK_t. Single Data Rate (SDR) inputs, CS_n and CKE, are sampled at the positive Clock edge. Clock is defined as the differential pair, CK_t and CK_c. The positive Clock edge is defined by the crosspoint of a rising CK_t and a falling CK_c. The negative Clock edge is defined by the crosspoint of a falling CK_t and a rising CK_c.
CKE	Input	**Clock Enable:** CKE HIGH activates and CKE LOW deactivates internal clock signals and therefore device input buffers and output drivers. Power savings modes are entered and exited through CKE transitions. CKE is considered part of the command code. See 7.5.1 **"Command Truth Table"** for command code descriptions. CKE is sampled at the positive Clock edge.
CS_n	Input	**Chip Select:** CS_n is considered part of the command code. See 7.5.1 **"Command Truth Table"** for command code descriptions. CS_n is sampled at the positive Clock edge.
CA[n:0]	Input	**DDR Command/Address Inputs:** Uni-directional command/address bus inputs. CA is considered part of the command code. See 7.5.1 **"Command Truth Table"** for command code descriptions.
DQ[n:0]	I/O	**Data Inputs/Output:** Bi-directional data bus. n=15 for 16 bits DQ; n=31 for 32 bits DQ.
DQSn_t, DQSn_c	I/O	**Data Strobe (Bi-directional, Differential):** The data strobe is bi-directional (used for read and write data) and differential (DQS_t and DQS_c). It is output with read data and input with write data. DQS_t is edge-aligned to read data and centered with write data. For x16, DQS0_t and DQS0_c correspond to the data on DQ0-7; DQS1_t and DQS1_c to the data on DQ8-15. For x32 DQS0_t and DQS0_c correspond to the data on DQ0-7; DQS1_t and DQS1_c to the data on DQ8-15; DQS2_t and DQS2_c to the data on DQ16-23; DQS3_t and DQS3_c to the data on DQ24-31.
DMn	Input	**Input Data Mask:** DM is the input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS_t. Although DM is for input only, the DM loading shall match the DQ and DQS (or DQS_c). DM0 is the input data mask signal for the data on DQ0-7. For x16 and x32 devices, DM1 is the input data mask signal for the data on DQ8-15. For x32 devices, DM2 is the input data mask signal for the data on DQ16-23 and DM3 is the input data mask signal for the data on DQ24-31.
V_{DD1}	Supply	**Core Power Supply 1:** Power supply for core.
V_{DD2}	Supply	**Core Power Supply 2:** Power supply for core.
V_{DDCA}	Supply	**Input Receiver Power Supply:** Power supply for CA[n:0], CKE, CS_n, CK_t, and CK_c input buffers.
V_{DDQ}	Supply	**I/O Power Supply:** Power supply for Data input/output buffers.
$V_{REF(CA)}$	Supply	**Reference Voltage for CA Command and Control Input Receiver:** Reference voltage for all CA[n:0], CKE, CS_n, CK_t, and CK_c input buffers.
$V_{REF(DQ)}$	Supply	**Reference Voltage for DQ Input Receiver:** Reference voltage for all Data input buffers.
V_{SS}	Supply	**Ground**
V_{SSCA}	Supply	**Ground for CA Input Receivers**
V_{SSQ}	Supply	**I/O Ground**
ZQ	I/O	**Reference Pin for Output Drive Strength Calibration**

Note: Data includes DQ and DM.

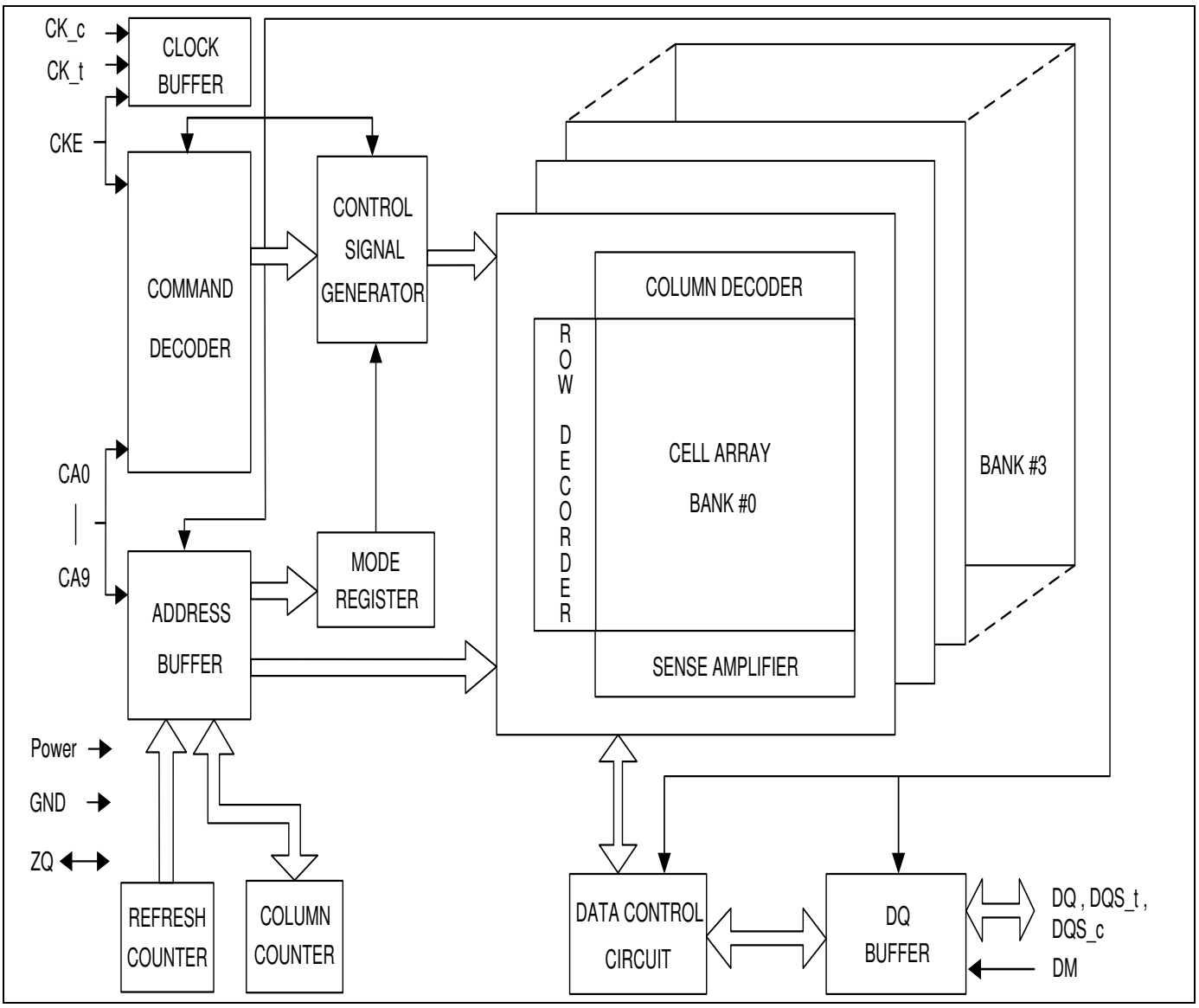
5.2 Addressing Table

Density		256Mb
Number of Banks		4
Bank Addresses		BA0-BA1
tREFI(µS)*2		7.8
x16	Row Addresses	R0-R12
	Column Addresses*1	C0-C8
x32	Row Addresses	R0-R12
	Column Addresses*1	C0-C7

Notes:

1. The least-significant column address C0 is not transmitted on the CA bus, and is implied to be zero.
2. tREFI values for all bank refresh is -40°C ≤ TCASE ≤ 85°C.
3. Row and Column Address values on the CA bus that are not used are “don’t care”.

6. BLOCK DIAGRAM



7. FUNCTIONAL DESCRIPTION

LPDDR2-S4 devices use a double data rate architecture on the DQ pins to achieve high speed operation. The double data rate architecture is essentially a 4n prefetch architecture with an interface designed to transfer two data bits per DQ every clock cycle at the I/O pins. A single read or write access for the LPDDR2-S4 effectively consists of a single 4n-bit-wide, one-clock-cycle data transfer at the internal SDRAM core and four corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

Read and write accesses are burst oriented; accesses start at a selected location and continue for a programmed number of locations in a programmed sequence.

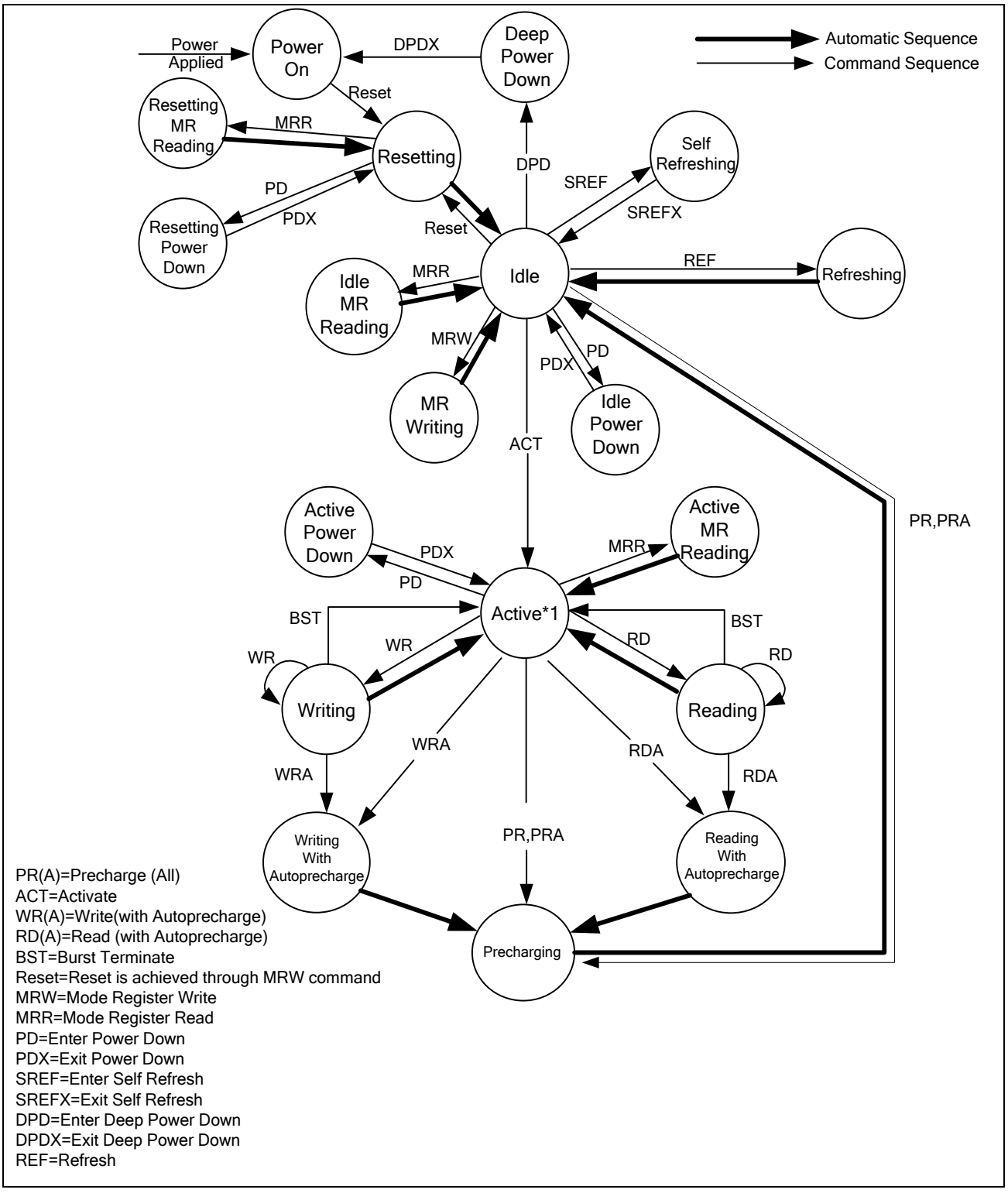
Prior to normal operation, the LPDDR2 device must be initialized. The following section provides detailed information covering device initialization, register definition, command description and device operation.

7.1 Simplified LPDDR2 State Diagram

LPDDR2-SDRAM state diagram provides a simplified illustration of allowed state transitions and the related commands to control them. For a complete definition of the device behavior, the information provided by the state diagram should be integrated with the truth tables and timing specification.

The truth tables provide complementary information to the state diagram, they clarify the device behavior and the applied restrictions when considering the actual state of all the banks.

7.1.1 Simplified LPDDR2 Bus Interface State Diagram



Note: For LPDDR2-SDRAM in the Idle state, all banks are precharged.

7.2 Power-up, Initialization, and Power-Off

The LPDDR2 Devices must be powered up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation.

7.2.1 Power Ramp and Device Initialization

The following sequence shall be used to power up an LPDDR2 device. Unless specified otherwise, these steps are mandatory.

1. Power Ramp

While applying power (after Ta), CKE shall be held at a logic low level (≤ 0.2 x V_{DDCA}), all other inputs shall be between V_{IL}min and V_{IH}max. The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low.

On or before the completion of the power ramp (Tb) CKE must be held low.

DQ, DM, DQS_t and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latchup. CK_t, CK_c, CS_n, and CA input levels must be between V_{SSCA} and V_{DDCA} during voltage ramp to avoid latch-up.

The following conditions apply:

Ta is the point where any power supply first reaches 300mV.

After Ta is reached, V_{DD1} must be greater than V_{DD2} - 200mV.

After Ta is reached, V_{DD1} and V_{DD2} must be greater than V_{DDCA} - 200mV.

After Ta is reached, V_{DD1} and V_{DD2} must be greater than V_{DDQ} - 200mV.

After Ta is reached, V_{REF} must always be less than all other supply voltages.

The voltage difference between any of V_{SS}, V_{SSQ}, and V_{SSCA} pins may not exceed 100mV.

The above conditions apply between Ta and power-off (controlled or uncontrolled).

Tb is the point when all supply voltages are within their respective min/max operating conditions. Reference voltages shall be within their respective min/max operating conditions a minimum of 5 clocks before CKE goes high.

For supply and reference voltage operating conditions, see 8.2.1.1 **"Recommended DC Operating Conditions"** table.

Power ramp duration t_{INIT0} (Tb - Ta) must be no greater than 20 mS.

2. CKE and clock

Beginning at Tb, CKE must remain low for at least t_{INIT1} = 100 nS, after which it may be asserted high. Clock must be stable at least t_{INIT2} = 5 x t_{CK} prior to the first low to high transition of CKE (Tc). CKE, CS_n and CA inputs must observe setup and hold time (t_{IS}, t_{IH}) requirements with respect to the first rising clock edge (as well as to the subsequent falling and rising edges).

The clock period shall be within the range defined for t_{CKb} (18 nS to 100 nS), if any Mode Register Reads are performed. Mode Register Writes can be sent at normal clock operating frequencies so long as all AC Timings are met. Furthermore, some AC parameters (e.g. t_{DQSCK}) may have relaxed timings (e.g. t_{DQSCKb}) before the system is appropriately configured.

While keeping CKE high, issue NOP commands for at least t_{INIT3} = 200 µS. (Td).

3. Reset command

After t_{INIT3} is satisfied, a MRW(Reset) command shall be issued (Td). The memory controller may optionally issue a Precharge-All command prior to the MRW Reset command. Wait for at least t_{INIT4} = 1 µS while keeping CKE asserted and issuing NOP commands.

4. Mode Registers Reads and Device Auto-Initialization (DAI) polling:

After t_{INIT4} is satisfied (Te) only MRR commands and power-down entry/exit commands are allowed. Therefore, after Te, CKE may go low in accordance to Power-Down entry and exit specification (see section 7.4.24 **"Power-Down"**).

The MRR command may be used to poll the DAI-bit to acknowledge when Device Auto-Initialization is complete or the memory controller shall wait a minimum of t_{INIT5} before proceeding.

As the memory output buffers are not properly configured yet, some AC parameters may have relaxed timings before the system is appropriately configured.

After the DAI-bit (MR#0, "DAI") is set to zero "DAI complete" by the memory device, the device is in idle state (Tf). The state of the DAI status bit can be determined by an MRR command to MR#0.

The LPDDR2 SDRAM device will set the DAI-bit no later than t_{INIT5} (10 µS) after the Reset command. The memory controller shall wait a minimum of t_{INIT5} or until the DAI-bit is set before proceeding.

After the DAI-Bit is set, it is recommended to determine the device type and other device characteristics by issuing MRR commands (MR0 "Device Information" etc.).

5. ZQ Calibration:

After t_{INIT5} (Tf), an MRW ZQ Initialization Calibration command may be issued to the memory (MR10). This command is used to calibrate the LPDDR2 output drivers (RON) over process, voltage, and temperature. Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection. In systems in which more than one LPDDR2 device exists on the same bus, the controller must not overlap ZQ Calibration commands. The device is ready for normal operation after t_{ZQINIT}.

6. Normal Operation:

After t_{ZQINIT} (Tg), MRW commands may be used to properly configure the memory, for example the output buffer driver strength, latencies etc. Specifically, MR1, MR2, and MR3 shall be set to configure the memory for the target frequency and memory configuration.

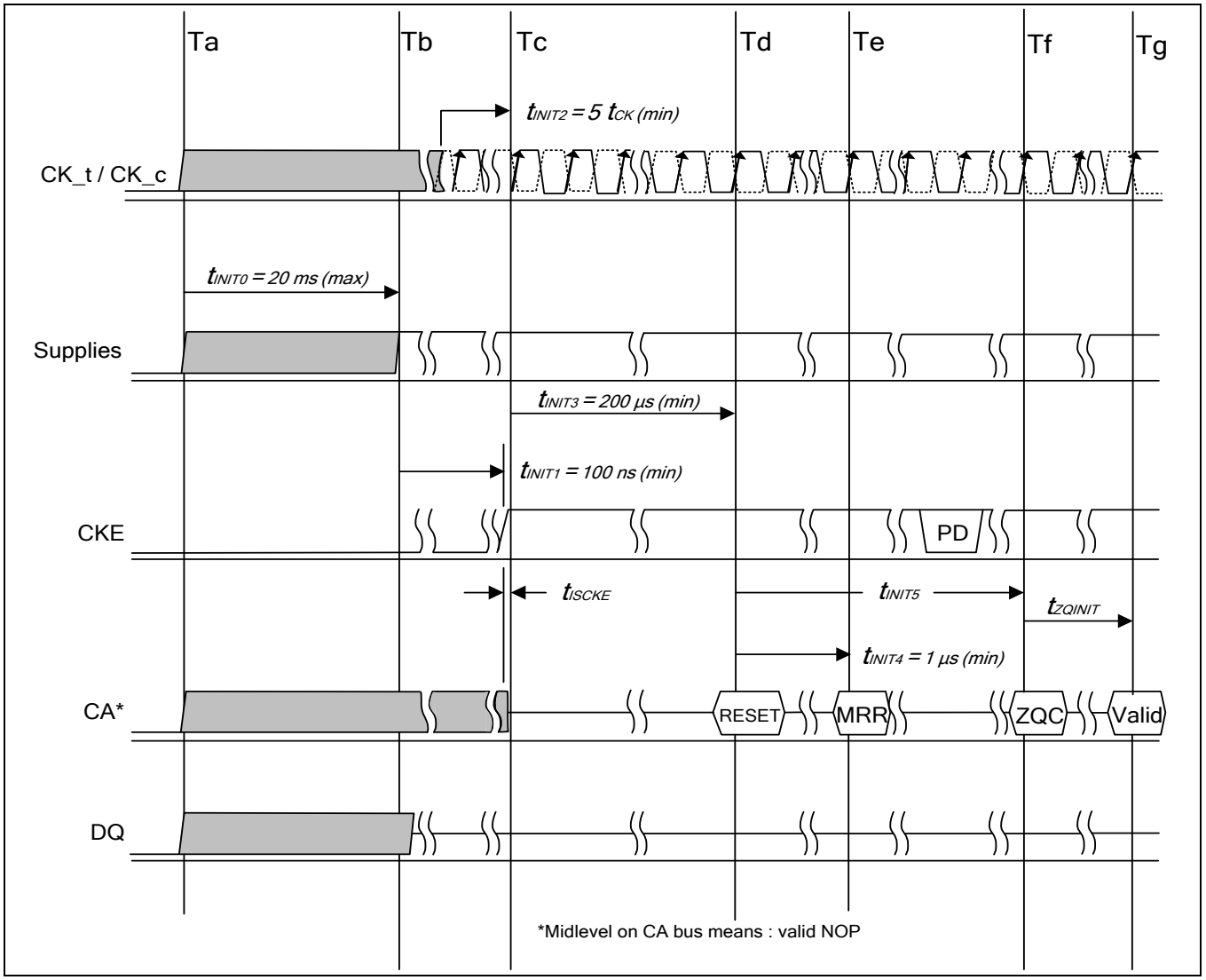
The LPDDR2 device will now be in IDLE state and ready for any valid command.

After Tg, the clock frequency may be changed according to the clock frequency change procedure described in section 7.4.26 **"Input Clock Stop and Frequency Change"**.

7.2.2 Timing Parameters for Initialization

Symbol	Value		Unit	Comment
	min	max		
tINIT0		20	mS	Maximum Power Ramp Time
tINIT1	100		nS	Minimum CKE low time after completion of power ramp
tINIT2	5		tCK	Minimum stable clock before first CKE high
tINIT3	200		µS	Minimum Idle time after first CKE assertion
tINIT4	1		µS	Minimum Idle time after Reset command
tINIT5		10	µS	Maximum duration of Device Auto-Initialization
tZQINIT	1		µS	ZQ Initial Calibration for LPDDR2-S4
tCKb	18	100	nS	Clock cycle time during boot

7.2.3 Power Ramp and Initialization Sequence



7.2.4 Initialization after Reset (without Power ramp)

If the RESET command is issued outside the power up initialization sequence, the reinitialization procedure shall begin with step 3 (Td).

7.2.5 Power-off Sequence

The following sequence shall be used to power off the LPDDR2 device.

While removing power, CKE shall be held at a logic low level (≤ 0.2 x V_{DDCA}), all other inputs shall be between V_{IL}min and V_{IH}max. The LPDDR2 device will only guarantee that outputs are in a high impedance state while CKE is held low.

DQ, DM, DQS_t and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during power off sequence to avoid latch-up. CK_t, CK_c, CS_n and CA input levels must be between V_{SSCA} and V_{DDCA} during power off sequence to avoid latch-up.

Tx is the point where any power supply decreases under its minimum value specified in 8.2.1.1 **"Recommended DC Operating Conditions"** table.

Tz is the point where all power supplies are below 300 mV. After Tz, the device is powered off.

The time between Tx and Tz (t_{POFF}) shall be less than 2s.

The following conditions apply:
Between Tx and Tz, V_{DD1} must be greater than V_{DD2} - 200 mV.
Between Tx and Tz, V_{DD1} and V_{DD2} must be greater than V_{DDCA} - 200 mV.
Between Tx and Tz, V_{DD1} and V_{DD2} must be greater than V_{DDQ} - 200 mV.
Between Tx and Tz, V_{REF} must always be less than all other supply voltages.
The voltage difference between any of V_{SS}, V_{SSQ}, and V_{SSCA} pins may not exceed 100 mV.
For supply and reference voltage operating conditions, see 8.2.1.1 **"Recommended DC Operating Conditions"** table.

7.2.6 Timing Parameters Power-Off

Symbol	Value		Unit	Comment
	min	max		
t_{POFF}	-	2	s	Maximum Power-Off Ramp Time

7.2.7 Uncontrolled Power-Off Sequence

The following sequence shall be used to power off the LPDDR2 device under uncontrolled condition.

Tx is the point where any power supply decreases under its minimum value specified in the DC operating condition table. After turning off all power supplies, any power supply current capacity must be zero, except for any static charge remaining in the system.

Tz is the point where all power supply first reaches 300 mV. After Tz, the device is powered off.
The time between Tx and Tz (t_{POFF}) shall be less than 2s. The relative levels between supply voltages are uncontrolled during this period.

V_{DD1} and V_{DD2} shall decrease with a slope lower than 0.5 V/µS between Tx and Tz.

Uncontrolled power off sequence can be applied only up to 400 times in the life of the device.

7.3 Mode Register Definition

7.3.1 Mode Register Assignment and Definition

Each register is denoted as “R” if it can be read but not written, “W” if it can be written but not read, and “R/W” if it can be read and written.

Mode Register Read command shall be used to read a register. Mode Register Write command shall be used to write a register.

7.3.1.1 Mode Register Assignment

MR#	MA[7:0]	Function	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	00H	Device Info.	R	(RFU)			RZQI		DNVI	DI	DAI
1	01H	Device Feature 1	W	nWR (for AP)			WC	BT	BL		
2	02H	Device Feature 2	W	(RFU)					RL & WL		
3	03H	I/O Config-1	W	(RFU)					DS		
4	04H	Refresh Rate	R	TUF	(RFU)				Refresh Rate		
5	05H	Basic Config-1	R	LPDDR2 Manufacturer ID							
6	06H	Basic Config-2	R	Revision ID1							
7	07H	Basic Config-3	R	Revision ID2							
8	08H	Basic Config-4	R	I/O width		Density				Type	
9	09H	Test Mode	W	Vendor-Specific Test Mode							
10	0AH	I/O Calibration	W	Calibration Code							
11-15	0BH~0FH	(reserved)	-	(RFU)							
16	10H	PASR_Bank	W	Bank Mask							
17	11H	(Reserved)	W	(RFU)							
18-19	12H~13H	(Reserved)	-	(RFU)							
20-31	14h – 1Fh	Reserved for NVM									
32	20H	DQ Calibration Pattern A	R	See 7.4.20.2 **“DQ Calibration”**							
33-39	21H~27H	(Do Not Use)	-								
40	28H	DQ Calibration Pattern B	R	See 7.4.20.2 **“DQ Calibration”**							
41-47	29H~2FH	(Do Not Use)	-								
48-62	30H~3EH	(Reserved)	-	(RFU)							
63	3FH	Reset	W	X							
64-126	40H~7EH	(Reserved)	-	(RFU)							
127	7FH	(Do Not Use)	-								
128-190	80H~BEH	(Reserved for Vendor Use)	-	(RFU)							
191	BFH	(Do Not Use)	-								
192-254	C0H~FEH	(Reserved for Vendor Use)	-	(RFU)							
255	FFH	(Do Not Use)	-								

Notes:

1. RFU bits shall be set to ‘0’ during Mode Register writes.
2. RFU bits shall be read as ‘0’ during Mode Register reads.
3. All Mode Registers that are specified as RFU or write-only shall return undefined data when read and DQS shall be toggled.
4. All Mode Registers that are specified as RFU shall not be written.
5. Writes to read-only registers shall have no impact on the functionality of the device.

7.3.2 MR0_Device Information (MA[7:0] = 00H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)			RZQI		DNVI	DI	DAI

DAI (Device Auto-Initialization Status)	Read-only	OP0	**0_b:** DAI complete **1_b:** DAI still in progress
DI (Device Information)	Read-only	OP1	**0_b:** S4 SDRAM
DNVI (Data Not Valid Information)	Read-only	OP2	**0_b:** LPDDR2 SDRAM will not implement DNV functionalit
RZQI (Built in Self Test for RZQ Information)	Read-only	OP[4:3]	**00b:** RZQ self test not executed. **01b:** ZQ-pin may connect to VDDCA or float **10b:** ZQ-pin may short to GND **11b:** ZQ-pin self test completed, no error condition detected (ZQ-pin may not connect to VDDCA or float nor short to GND)

Notes:
1. RZQI will be set upon completion of the MRW ZQ Initialization Calibration command.
2. If ZQ is connected to VDDCA to set default calibration by user, OP[4:3] shall be read as 01. If user does not want to connect ZQ pin to VDDCA, but OP[4:3] is read as 01 or 10, it might indicate a ZQ-pin assembly error. It is recommended that the assembly error being corrected first.
3. In the case of possible assembly error (either OP[4:3]=01 or OP[4:3]=10 as defined above), the LPDDR2 device will default to factory trim settings for RON, and will ignore ZQ calibration commands. In either case, the system may not function as intended.
4. In the case of the ZQ self-test returning a value of 11b, this result indicates that the device has detected a resistor connection to the ZQ pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e., 240 Ohm ± 1%).

7.3.3 MR1_Device Feature 1 (MA[7:0] = 01H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
nWR (for AP)			WC	BT	BL		

BL	Write-only	OP[2:0]	**010_b:** BL4 (default) **011_b:** BL8 **100_b:** BL16 **All others:** reserved	
BT	Write-only	OP3	**0_b:** Sequential (default) **1_b:** Interleaved	
WC	Write-only	OP4	**0_b:** Wrap (default) **1 b:** No wrap (allowed for SDRAM BL4 only)	
nWR	Write-only	OP[7:5]	**001_b:** nWR=3 (default) **010_b:** nWR=4 **011b:** nWR=5 **100_b:** nWR=6 **101_b:** nWR=7 **110_b:** nWR=8 **All others:** reserved	1

Note:
1. Programmed value in nWR register is the number of clock cycles which determines when to start internal precharge operation for a write burst with AP enabled. It is determined by RU(tWR/tCK).

7.3.3.1 Burst Sequence by Burst Length (BL), Burst Type (BT), and Warp Control (WC)

C3	C2	C1	C0	WC	BT	BL	Burst Cycle Number and Burst Address Sequence															
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
X	X	0b	0b	wrap	any	4	0	1	2	3												
X	X	1b	0b				2	3	0	1												
X	X	X	0b	nw	any		y	y+1	y+2	y+3												
X	0b	0b	0b	wrap	seq	8	0	1	2	3	4	5	6	7								
X	0b	1b	0b				2	3	4	5	6	7	0	1								
X	1b	0b	0b				4	5	6	7	0	1	2	3								
X	1b	1b	0b				6	7	0	1	2	3	4	5								
X	0b	0b	0b		int		0	1	2	3	4	5	6	7								
X	0b	1b	0b				2	3	0	1	6	7	4	5								
X	1b	0b	0b				4	5	6	7	0	1	2	3								
X	1b	1b	0b				6	7	4	5	2	3	0	1								
X	X	X	0b	nw	any		**illegal (not allowed)**															
0b	0b	0b	0b	wrap	seq	16	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0b	0b	1b	0b				2	3	4	5	6	7	8	9	A	B	C	D	E	F	0	1
0b	1b	0b	0b				4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
0b	1b	1b	0b				6	7	8	9	A	B	C	D	E	F	0	1	2	3	4	5
1b	0b	0b	0b				8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
1b	0b	1b	0b				A	B	C	D	E	F	0	1	2	3	4	5	6	7	8	9
1b	1b	0b	0b				C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B
1b	1b	1b	0b				E	F	0	1	2	3	4	5	6	7	8	9	A	B	C	D
X	X	X	0b		int		**illegal (not allowed)**															
X	X	X	0b	nw	any		**illegal (not allowed)**															

Notes:

1. C0 input is not present on CA bus. It is implied zero.
2. For BL=4, the burst address represents C[1: 0].
3. For BL=8, the burst address represents C[2:0].
4. For BL=16, the burst address represents C[3:0].
5. For no-wrap (nw), BL4, the burst shall not cross the page boundary and shall not cross sub-page boundary. The variable y may start at any address with C0 equal to 0 and may not start at any address shown in table below.

7.3.3.2 Non Wrap Restrictions

Bus Width	256Mb
Not across full page boundary	
x16	1FE, 1FF, 000, 001
x32	FE, FF, 00, 01
Not across sub page boundary	
x16	0FE, 0FF, 100, 101
x32	None

Note: Non-wrap BL=4 data-orders shown above are prohibited.

7.3.4 MR2_Device Feature 2 (MA[7:0] = 02H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				RL & WL			

RL & WL	Write-only	OP[3:0]	**0001b:** RL = 3 / WL = 1 (default) **0010b:** RL = 4 / WL = 2 **0011b:** RL = 5 / WL = 2 **0100b:** RL = 6 / WL = 3 **0101b:** RL = 7 / WL = 4 **0110b:** RL = 8 / WL = 4 **All others:** reserved

7.3.5 MR3_I/O Configuration 1 (MA[7:0] = 03H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
(RFU)				DS			

DS	Write-only	OP[3:0]	**0000_b:** reserved **0001_b:** 34.3-ohm typical **0010_b:** 40-ohm typical (default) **0011_b:** 48-ohm typical **0100_b:** 60-ohm typical **0101_b:** reserved **0110_b:** 80-ohm typical **0111_b:** 120-ohm typical **All others:** reserved

7.3.6 MR4_Device Temperature (MA[7:0] = 04H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
TUF	(RFU)				SDRAM Refresh Rate		

SDRAM Refresh Rate	Read-only	OP[2:0]	**000_b:** SDRAM Low temperature operating limit exceeded **001b:** 4x tREFI, 4x tREFW **010_b:** 2x tREFI, 2x tREFW **011_b:** 1x tREFI, 1x tREFW (≤ 85°C) **100_b:** Reserved **101_b:** 0.25x tREFI, 0.25x tREFW, do not de-rate SDRAM AC timing **110_b:** 0.25x tREFI, 0.25x tREFW, de-rate SDRAM AC timing **111_b:** SDRAM High temperature operating limit exceeded
Temperature Update Flag (TUF)	Read-only	OP7	**0_b:** OP[2:0] value has not changed since last read of MR4. **1_b:** OP[2:0] value has changed since last read of MR4.

Notes:

1. A Mode Register Read from MR4 will reset OP7 to '0'.
2. OP7 is reset to '0' at power-up.
3. If OP2 equals '1', the device temperature is greater than 85°C.
4. OP7 is set to '1' if OP2:OP0 has changed at any time since the last read of MR4.
5. LPDDR2 might not operate properly when OP[2:0] = 000b or 111b.
6. For specified operating temperature range and maximum operating temperature, refer to **"Operating Temperature Conditions"** table.
7. LPDDR2 devices must be derated by adding 1.875 nS to the following core timing parameters: tRCD, tRC, tRAS, tRP, and tRRD. tDQSCK shall be de-rated according to the tDQSCK de-rating value in **"LPDDR2 AC Timing"** table. Prevailing clock frequency spec and related setup and hold timings shall remain unchanged.
8. The recommended frequency for reading MR4 is provided in **"Temperature Sensor"** section.

7.3.7 MR5_Basic Configuration 1 (MA[7:0] = 05H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
LPDDR2 Manufacturer ID							

LPDDR2 Manufacturer ID	Read-only	OP[7:0]	0000 1000b: Winbond

7.3.8 MR6_Basic Configuration 2 (MA[7:0] = 06H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID1							

Revision ID1	Read-only	OP[7:0]	00000000b: A-version

Note: MR6 is Vendor Specific.

7.3.9 MR7_Basic Configuration 3 (MA[7:0] = 07H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Revision ID2							

Revision ID2	Read-only	OP[7:0]	00000000b: A-version

Note: MR7 is Vendor Specific.

7.3.10 MR8_Basic Configuration 4 (MA[7:0] = 08H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
I/O width		Density				Type	

Type	Read-only	OP[1:0]	**00b:** S4 SDRAM
Density	Read-only	OP[5:2]	**0010b:** 256Mb
I/O width	Read-only	OP[7:6]	**00b:** x32 **01b:** x16

7.3.11 MR9_Test Mode (MA[7:0] = 09H)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Vendor-specific Test Mode							

7.3.12 MR10_Calibration (MA[7:0] = 0AH)

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
Calibration Code							

Calibration Code	Write-only	OP[7:0]	**0xFF:** Calibration command after initialization **0xAB:** Long calibration **0x56:** Short calibration **0xC3:** ZQ Reset **others:** Reserved

Notes:

1. Host processor shall not write MR10 with "Reserved" values.
2. LPDDR2 devices shall ignore calibration command when a "Reserved" value is written into MR10.
3. See AC timing table for the calibration latency.
4. If ZQ is connected to VSSCA through RZQ, either the ZQ calibration function (see section 7.4.23 **"Mode Register Write ZQ Calibration Command"**) or default calibration (through the ZQreset command) is supported. If ZQ is connected to VDDCA, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.
5. Optionally, the MRW ZQ Initialization Calibration command will update MR0 to indicate RZQ pin connection.

7.3.13 MR16_PASR_Bank Mask (MA[7:0] = 10H)

	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
S4 SDRAM	Reserved				Bank Mask			

Bank [3:0] Mask	Write-only	OP[3:0]	**0b:** self-refresh enable to the bank (=unmasked, default) **1b:** self-refresh blocked (=masked) **OP0:** bank 0 **OP1:** bank 1 **OP2:** bank 2 **OP3:** bank 3
Reserved	Write-only	OP[7:4]	Reserved. Any value written to OP[7:4] are ignored by LPDDR2.

Note: The MR16 is used to control which bank or banks are to be masked or unmasked in self-refresh mode. It has no effect in auto-refresh mode because LPDDR2 256Mb device does not support per-bank refresh in auto-refresh mode.

OP	Bank Mask	4-Bank S4 SDRAM
0	XXXXXXX1	Bank 0
1	XXXXXX1X	Bank 1
2	XXXXX1XX	Bank 2
3	XXXX1XXX	Bank 3
4	-	-
5	-	-
6	-	-
7	-	-

7.3.14 MR32_DQ Calibration Pattern A (MA[7:0] = 20H)

Reads to MR32 return DQ Calibration Pattern "A". See section 7.4.20.2 **"DQ Calibration"**.

7.3.15 MR40_DQ Calibration Pattern B (MA[7:0] = 28H)

Reads to MR40 return DQ Calibration Pattern "B". See section 7.4.20.2 **"DQ Calibration"**.

7.3.16 MR63_Reset (MA[7:0] = 3FH): MRW only

OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
X							

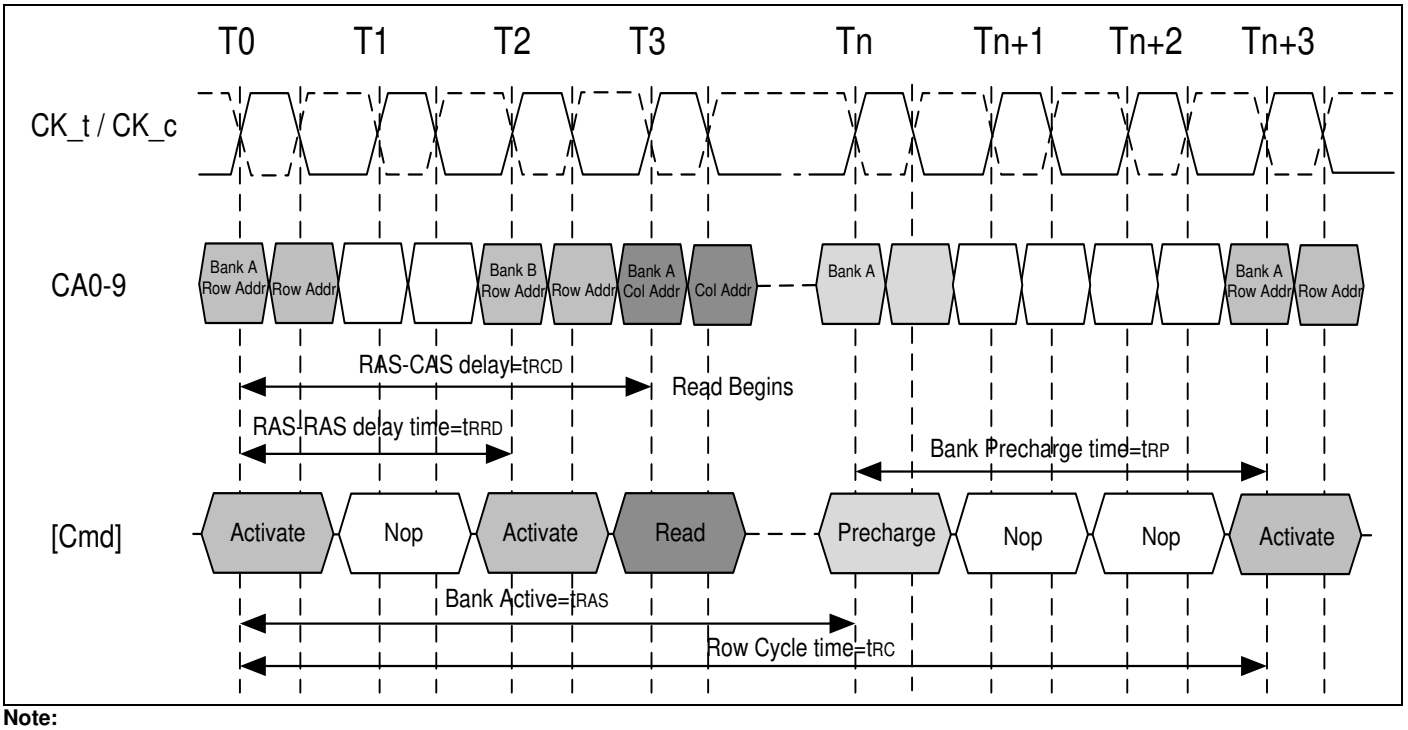
For additonal information on MRW RESET see section 7.4.21 **"Mode Register Write Command"**.

7.4 Command Definitions and Timing Diagrams

7.4.1 Activate Command

The SDRAM Activate command is issued by holding CS_n LOW, CA0 LOW, and CA1 HIGH at the rising edge of the clock. The bank addresses are used to select the desired bank. The row addresses are used to determine which row to activate in the selected bank. The Activate command must be applied before any Read or Write operation can be executed. The LPDDR2 SDRAM can accept a read or write command at time t_{RCD} after the activate command is sent. Once a bank has been activated it must be precharged before another Activate command can be applied to the same bank. The bank active and precharge times are defined as t_{RAS} and t_{RP}, respectively. The minimum time interval between successive Activate commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between Activate commands to different banks is t_{RRD}.

7.4.1.1 Activate Command Cycle: t_{RCD} = 3, t_{RP} = 3, t_{RRD} = 2



Note:

A Precharge-All command uses t_{RPab} timing, while a Single Bank Precharge command uses t_{RPpb} timing. In this figure, t_{RP} is used to denote either an All-bank Precharge or a Single Bank Precharge