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WF111 – 802.11 B/G/N MODULE

DATA SHEET

Monday, 10 June 2013

Version 1.2.2

VERSION HISTORY

Version	Comment
1.0	First public version
1.1	Product codes updated
1.1.1	Added sleep clock specifications
1.1.2	Added frequency variation table
1.1.3	FCC and IC information added
1.1.4	WT111-N layout guide
1.1.5	Some new consumption measurements
1.1.6	Added CE information, corrected supported channels for default FCC version
1.1.7	Different coexistence pad bindings, replaced MIB keys with MIB file names
1.1.8	Listed supported coexistence schemes
1.1.9	Added tape & reel info
1.2.0	Removed unnecessary register information, changes to coexistence description, removed references to engineering sample versions
1.2.1	Repaired broken ToC
1.2.2	MIC Japan and KCC certification info

TABLE OF CONTENTS

1 Product description

DESCRIPTION

WF111 is a fully integrated single 2.4GHz band 802.11 b/g/n module, intended for portable and battery powered applications, where Wi-Fi connectivity is needed. WF111 integrates an IEEE 802.11 b/g/n radio, antenna or U.FL antenna connector and SDIO or CSPI host interfaces.

WF111 provides a low cost and simple Wi-Fi solution for devices that run an operating system and a TCP/IP stack on-board, but still offers the benefits of a module – small form factor, easy integration and certifications. Bluegiga also provides WF111 drivers for the Linux operating system.

TARGET APPLICATIONS:

- PoS terminals
- RFID and laser scanners
- Wi-Fi internet radios and audio streaming products
- Wireless cameras
- Portable navigation devices
- Portable handheld devices
- Wi-Fi medical sensors
- Wireless picture frames

KEY FEATURES:

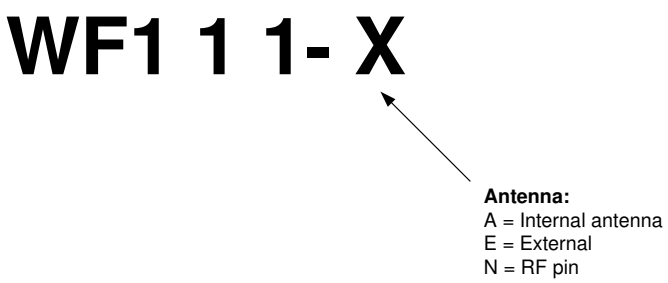
- IEEE 802.11 b/g/n radio
  - Single stream 2.4 GHz band
  - Bit rates up to 72.2Mbps
- Integrated antenna or U.FL connector
- Hardware support for WEP, WPA and WPA2 encryption
- Soft-AP support
- Temperature range: -40°C to +85°C
- SDIO or CSPI host interfaces
- *Fully CE, FCC, IC, Japan and South-Korea certified*
- Operating system drivers for Linux

PHYSICAL OUTLOOK:

Figure 1: WF111-A

2 Ordering Information

WF111 Product Numbering



Confirmed products and codes

Product code	Description
WF111-A	WF111 module with internal chip antenna
WF111-E	WF111 module with U.FL connector for external antenna
WF111-N	WF111 module with 50 RF pin (contact sales@bluegiga.com for availability)
DKWF111	WF111-A SDIO evaluation kit

3 Pinout and terminal descriptions

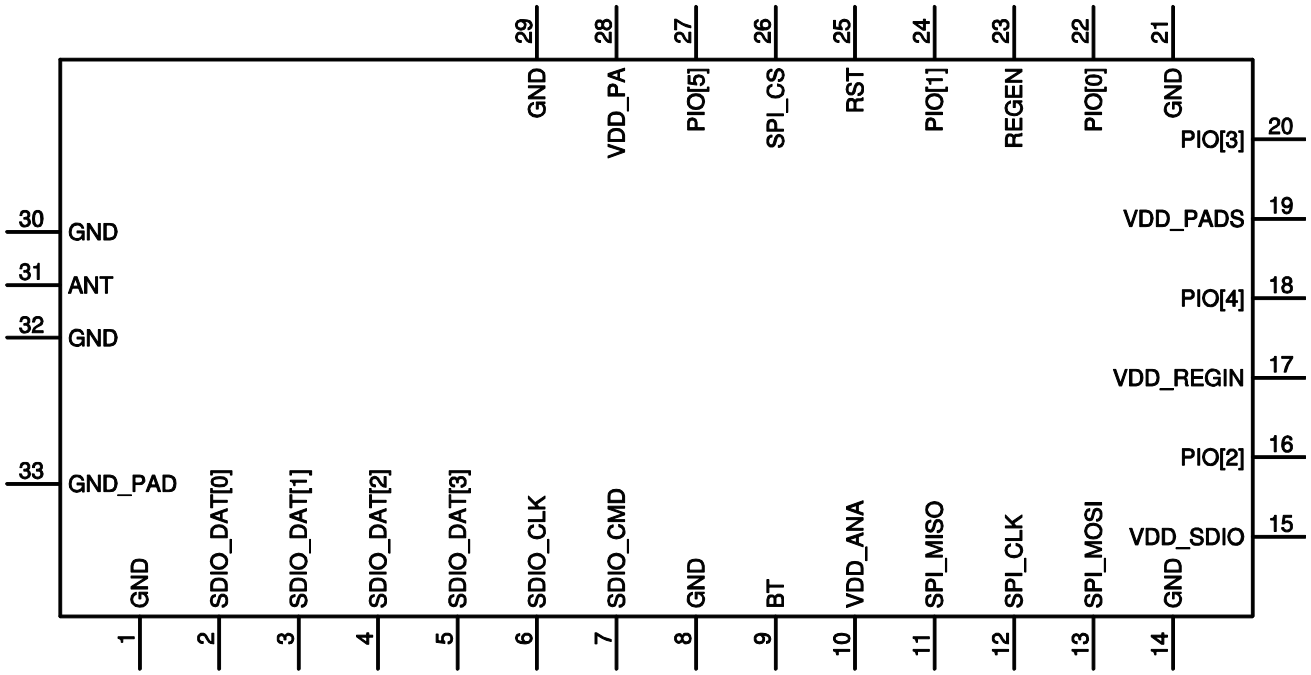


Figure 2: WF111 pinout

POWER SUPPLIES	PIN NUMBER	DESCRIPTION
VDD_REGIN	17	Input for the internal regulators
REGEN	23	Pull high to enable internal voltage regulators (2.0V max)
GND	1, 8, 14, 21, 29, 30, 32	Ground
GND_PAD	33	Thermal pad, on bottom of WF111
VDD_ANA	10	Positive supply for PA control
VDD_PADS	19	Positive supply for the digital interfaces
VDD_SDIO	15	Positive supply for the SDIO interface
VDD_PA	28	Positive supply for the power amplifier

Table 1: Supply Terminal Descriptions

PIO PORT	PIN NUMBER	PAD TYPE	DESCRIPTION
PIO[0]	22	Bi-directional, programmable strength internal pull-down/pull-up	Programmable input/output line. Can be used for *Bluetooth* co-existence.
PIO[1]	24		
PIO[2]	16		
PIO[3]	20		
PIO[4]	18		
PIO[5]	27		

Table 2: GPIO Terminal Descriptions

SDIO/CSPI Interfaces	PIN NUMBER	PAD TYPE	DESCRIPTION
SDIO_DATA[0]	2	Bi-directional, tri-state, weak internal pull-up	Synchronous data input/output
SDIO_SPI_DI			SDIO SPI data output
CSPI_MISO			CSPI data output
SDIO_DATA[1]	3		Synchronous data input/output
SDIO_SPI_INT			SDIO SPI interrupt output
CSPI_INT			CSPI data input
SDIO_DATA[2]	4		Synchronous data input/output
SDIO_DATA[3]	5	Bi-directional, weak/strong internal pull-up	Synchronous data input/output
SDIO_SPI_CS#			SDIO SPI chip select, active low
CSPI_CS#			CSPI chip select, active low
SDIO_CLK	6	Input, weak internal pull-up	SDIO clock
SDIO_SPI_SCLK			SDIO SPI clock
CSPI_CLK			CSPI clock
SDIO_CMD	7	Bi-directional, weak internal pull-up	SDIO data input
SDIO_SPI_MOSI			SDIO SPI data input
CSPI_MOSI			CSPI data input

Table 3: Host Interface Terminal Descriptions

OTHER SIGNALS	PIN NUMBER	PAD TYPE	DESCRIPTION
RST	25	Input, weak internal pull-up, active low	System reset
ANT	31	RF, DC blocked	Antenna output on N variant, on A and E variants not connected
BT	9	RF, DC blocked	Bluetooth antenna sharing RF input

Table 4: Other Terminal Descriptions

DEBUG SPI INTERFACE	PIN NUMBER	PAD TYPE	DESCRIPTION
SPI_MISO	11	Output, tri-state, weak internal pull-down	Synchronous data output
SPI_CLK	12	Input, weak internal pull-down	Synchronous clock input
SPI_MOSI	13		Synchronous data input
SPI_CS	26		Debug SPI Chip select, active low

Table 5: Debug SPI Terminal Descriptions

4 Interfaces

4.1 Host interfaces

WF111 can be interfaced by the host using SDIO in 1bit or 4bit mode, SDIO SPI or CSR proprietary CSPI connection. The host connection buses can be clocked up to 50MHz.

4.1.1 Host selection

WF111 will default to 1-bit SDIO mode. The host interface can be set with 1-bit SDIO or SDIO SPI commands to the required mode. After mode selection, it will then remain in that mode until the module is reset either with the RESET pin or the internal power supply supervisor.

4.1.2 SDIO interface

This is a host interface which allows a Secure Digital Input Output (SDIO) host to gain access to the internals of the chip. All defined slave modes (SPI, SD 1bit, SD 4bit) are provided.

Two functions are supported:

- Function 0 is mandatory function used for SDIO slave configuration. This contains CCCR, FBR and CIS. CCCR registers support sleep and wakeup signaling.
- Function 1 provides access to the IEEE 802.11 functionality. Command IO_RW_DIRECT (CMD52) is used to directly access internal registers. IO_RW_EXTENDED (CMD53) is used for block transfer to/from module MMU buffers.

Command	SD Mode (1/4 bit)	SDIO SPI Mode
GO_IDLE_STATE (CMD0)	Y	Y
SEND_RELATIVE_ADDR (CMD3)	Y	N
IO_SEND_OP_COND (CMD5)	Y	Y
SELECT/DESELECT_CARD (CMD7)	Y	N
GO_INACTIVE_STATE (CMD15)	Y	N
IO_RW_DIRECT (CMD52)	Y	Y
IO_RW_EXTENDED (CMD53)	Y	Y
CRC_ON_OFF (CMD59)	N	Y

Table 6: Supported commands per mode

For more information and detailed descriptions of above functions and commands, see the following specifications:

- SD Specifications Part 1 Physical Layer Specification v.1.10
- SD Specification Part E1 SDIO Specification v.1.10

4.1.3 CSR Serial Peripheral Interface (CSPI)

The CSPI is a host interface which shares pins with the SDIO. It contains a number of modifications on the SDIO SPI specification aimed at increasing the host bus efficiency in hosts supporting SPI but not SDIO. The main advantages compared to SDIO SPI are:

- Burst transfer is continuous instead of blocks with CRC
- Timings are deterministic (fixed number of clocks) reducing the required interaction
- 16 bit registers are transferred as a single command instead of two 8 bit writes

MMU buffers are accessed using burst read/writes. The command and address fields are used to select the correct buffer. The CSPI is able to generate an interrupt to the host when a memory access fails. This interrupt line is shared with the SDIO functions.

The CSPI Interface is an extension of the basic SPI Interface, with the access type determined by the following fields:

- 8-bit command
- 24-bit address
- 16-bit burst length (optional). Only applicable for burst transfers into or out of the MMU

4.1.3.1 CSPI read/write cycles

Register read/write cycles are used to access Function 0, Bluetooth acceleration and MCU registers.

Burst read/write cycles are used to access the MMU.

4.1.3.2 CSPI register write cycle

The command and address are locked into the slave, followed by 16bits of write data. An Error Byte is returned on the MISO signal indicating whether or not the transfer has been successful.

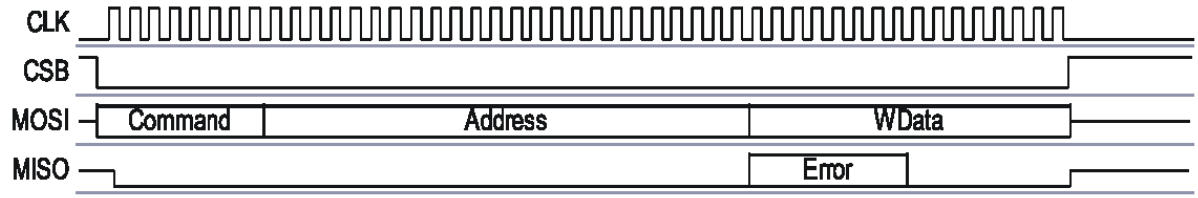


Figure 3: CSPI Register Write Cycle

4.1.3.3 CSPI register read cycle

The command and address field are clocked into the slave, the slave then returns the following:

- Bytes of padding data (MISO held low)
- Error byte
- 16-bits of read data

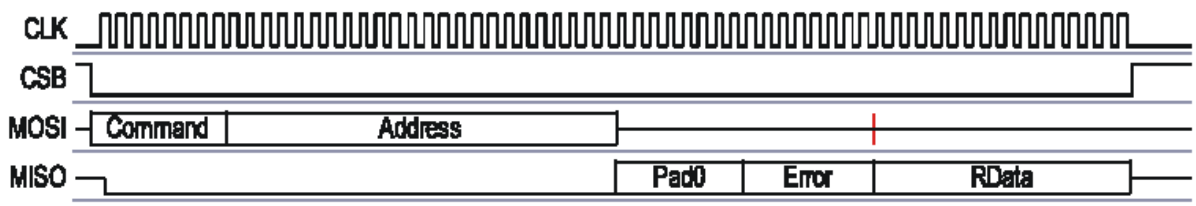


Figure 4: CSPI Register Read Cycle

4.1.3.4 CSPI register burst write cycle

Burst transfers are used to access the MMU buffers. They cannot be used to access registers. Burst read/write cycles are selected by setting the nRegister/Burst bit in the command field to 1.

Burst transfers are byte orientated, have a minimum length of 0 bytes and a maximum length of 64kbytes. Setting the length field to 0 results in no data being transferred to or from the MMU.

As with a register access, the command and address fields are transferred first. There is an optional length field transferred after the address. The use of the length field is controlled by the LengthFieldPresent bit in the Function 0 registers, which is cleared on reset.

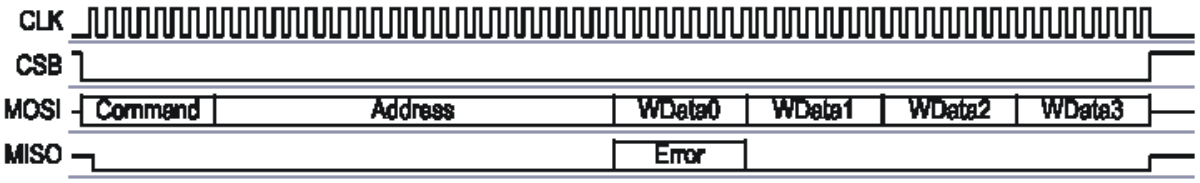


Figure 5: CSPI Burst Write Cycle

4.1.3.5 CSPI register read cycle

Burst reads have a programmable amount of padding data that is returned by the slave. 0-15 bytes are returned as defined in the BurstPadding register. Following this the Error byte is returned followed by the data. Once the transfer has started, no further padding is needed.

A FIFO within SDIO_TOP will pre-fetch the data. The address is not retransmitted, and is auto-updated within the slave.

The length field is transmitted if LengthFieldPresent in the Function 0 registers is set. In the absence of a length field the CSB signal is used to indicate the end of the burst.

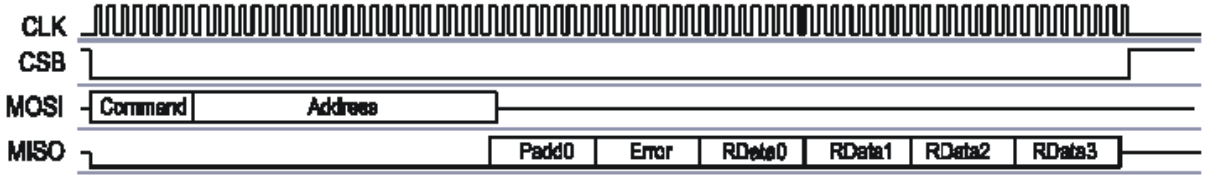


Figure 6: CSPI Burst Read Cycle

4.1.4 SDIO/CSPI deep-sleep control schemes

The module automatically enters deep sleep to minimize power consumption after a while of idling. Deep sleep is the lowest power mode, where the processor, the internal reference (fast) clock, and much of the digital and analogue hardware are shut down. The SDIO communication system however remains on, and is clocked by the host system. During deep sleep only the function 0 is available, while attempts to access Function 1 will likely result in bus timeouts. Function 0 is also available when the Wi-Fi core is physically powered off, as long as the VDD_SDIO supply is present.

Control of when the module is allowed to enter deep sleep is done via Vendor Unique Register in CCCR in function 0. Wake-up is also initiated through this register. The module will initiate an SDIO interrupt when the wake-up is complete.

4.2 Other interfaces

4.2.1 Debug SPI interface

A separate SPI bus is provided at the module pads for device access during testing and uploading settings during application development and manufacturing. This interface cannot be used as a host interface. It is recommended to bring these to a connector or test pads in case RF certification measurements that cannot be made through the host connection are required with the finished design. If it is not expected that certification measurements would be needed, the debug SPI pads should be left unconnected. The pads do not need external pull-ups when unconnected.

The debug SPI bus has logic levels set by the VDD_PADS reference supply line.

4.2.2 *Bluetooth* coexistence

Bluetooth coexistence systems allow co-located Wi-Fi and Bluetooth devices to be aware of each other and to avoid simultaneous transfers that would degrade link performance. WF111 supports a number of different coexistence schemes with up to 6 control lines for hardware communication between the two devices.

For reliable simultaneous communication both stacks need to be able to communicate together, in practice a common driver system needs to be used so the packet priorities can be communicated between the stacks. With separate stacks the only communication channel is the hardware interface and the devices have only high and low priorities in use. As Wi-Fi data will automatically get higher priority than Bluetooth, high data throughput on Wi-Fi may lead to poor Bluetooth operation when used simultaneously.

Wi-Fi and Bluetooth may use separate antennas, or share a single antenna through a switch. With a shared antenna, usually two additional signals are needed to control the front end switch. WF111 contains an internal switch for separating Wi-Fi and Bluetooth transmissions. (**See chapter 7.3.**)

For use with CSR-based Bluetooth (BC4 to BC6 with firmware version 21 or later, BC7 and onwards with all versions), Unity-3e+ is recommended as the coexistence scheme. Unity-3e is an enhanced version of the 3-wire Unity-3 –scheme that uses tighter timings and uses the three control lines also for antenna switch control, removing the need for the two separate switch control lines. Unity-3e+, or Unity-3e with Unity+ adds an additional BT_PERIODIC signal to communicate the need for a periodic transmission from the Bluetooth to the Wi-Fi, allowing a guaranteed low-latency throughput for certain Bluetooth applications despite high Wi-Fi usage. This allows reliable audio connections that would otherwise suffer from the Wi-Fi's higher priority. Use of Unity+ requires the use of a combined stack driver. Without software support, the periodic signaling cannot be initialized.

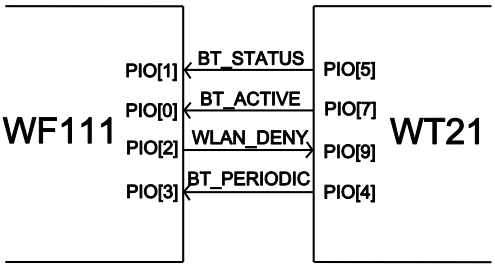


Figure 7: Coexistence signals between WF111 and WT21 Bluetooth module (not showing antenna sharing connection)

Using the Unity-3e+ scheme and the pictured PIO pad bindings, the MIB file *mib111_drv_coex.dat* should be used. If needed, the PIO pads PIO[3], PIO[5], PIO[4] and PIO[2] can also be used for BT_STATUS, BT_ACTIVE, WLAN_DENY and BT_PERIODIC, respectively, in which case the MIB file *mib111_drv_coex_alt.dat* should be chosen.

On the DKWF111 evaluation board, the PIO[5] pad is connected to an activity led, which is supported by the MIB files *mib111_drv_led.dat* and *mib111_drv_coex_led.dat*, the latter of which contains signal bindings for the scheme pictured above.

The PSKEYs for the Unity-3e+ on the WT21 are:

PSKEY_LC_COMBO_DISABLE_PIO_MASK (0x0028) = 0x0200 0x0000 0x0000

PSKEY_LC_COMBO_DOT11_CHANNEL_PIO_BASE (0x002A) = 0x0011

PSKEY_LC_COMBO_DOT11_ESCO_RTX_PRIORITY (0x0050) = 0x0001

PSKEY_LC_COMBO_DOT11_PULL_DISABLE_MASK (0x005A) = 0x0200

PSKEY_LC_COMBO_DOT11_PERIODIC_PIO_MASK (0x005C) = 0x0010 0x0000

PSKEY_LC_COMBO_DOT11_T1 (0x005E) = 0x0043

PSKEY_LC_COMBO_DOT11_T2 (0x005F) = 0x000A

PSKEY_TXRX_PIO_CONTROL (0x0209) = 0x0001

WF111 has hardware support for 3-wire, 4-wire, Unity-3e and Unity+ coexistence schemes. The default MIB files support only Unity-3e with Unity+. For other coexistence schemes a custom MIB is required, for more information please contact Bluegiga technical support.

4.2.3 Configurable I/O pads

A number of programmable bi-directional input/outputs (I/O) are provided. PIO[0:5] logic levels are referred to the VDD_PADS supply line.

PIO lines can be configured through software to implement various automated functions or as generic inputs or outputs. As inputs the lines can be configured to have either weak or strong pull-ups or pull-downs. All PIO lines are configured as inputs with weak pull-downs at reset.

In addition to the coexistence functions, any of the PIO lines can be configured as interrupt request lines, wake-up lines from sleep modes, status led drivers with multiple internally generated modes, general I/O pins controlled by the host, or as a 32.768 kHz sleep clock input.

For further information, please contact Bluegiga technical support.

Note: All unused signals can be left floating. The GPIO lines have internal pull-downs.

5 Power Control and Regulation

5.1 Power Control and Regulation

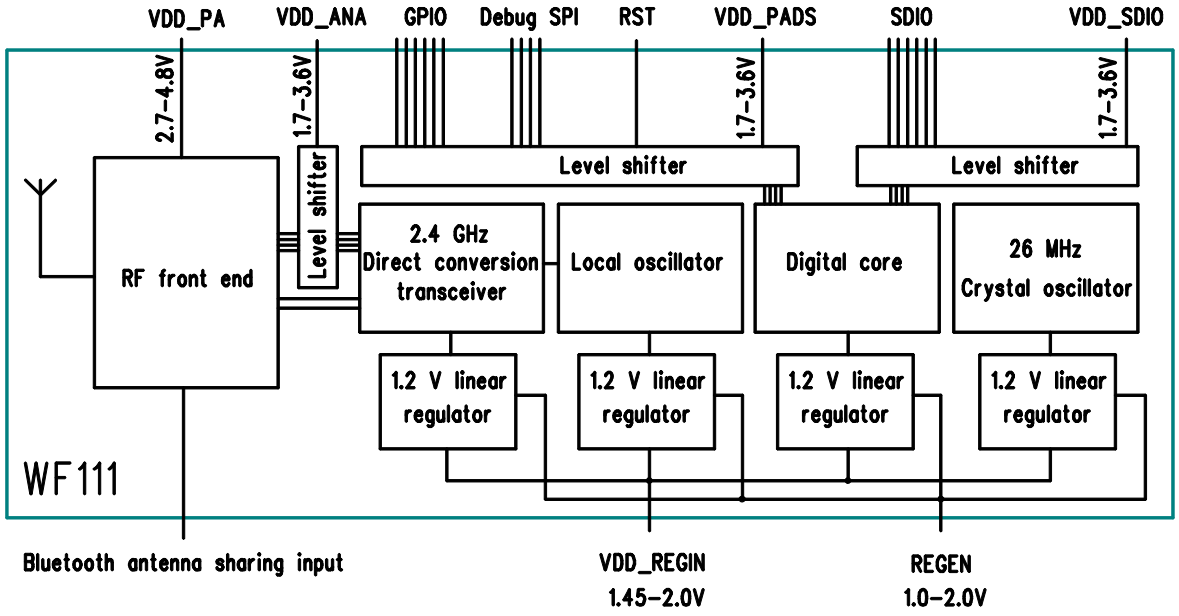


Figure 8: System block diagram

WF111 contains four linear regulators supplying clean voltages for the different parts of the system. All of them produce a 1.2V output voltage, and are fed from a common input, VDD_REGIN. This input can be supplied with a voltage between 1.45-2.0V, typically 1.5V or 1.8V. The VDD_REGIN supply should be relatively clean of ripple and switching spikes in order to avoid degrading the RF performance.

WF111 also needs four other supply lines connected in addition to VDD_REGIN:

- VDD_PADS provides a reference voltage for matching voltage levels of the host system to the GPIO pins used for Bluetooth coexistence and other functions. This can range from 1.7V to 3.6V. The current drawn from this supply is negligible.
- VDD_SDIO provides a reference voltage for matching voltage levels of the host system to the SDIO connection. This can range from 1.7V to 3.6V. The current drawn from this supply depends on bus usage, but with no active data transfer will be negligible.
- VDD_ANA provides a reference voltage for communication between the Wi-Fi chip and the power amplifier. This should be between 1.7V and 3.6V. The current drawn from this supply is negligible.
- VDD_PA is a separate supply voltage for the Wi-Fi power amplifier. This supply will draw considerable currents in pulses. The power traces should be relatively wide. This voltage can range from 2.7V to 4.8V making use directly from a single lithium cell possible. A higher supply voltage will not affect the power amplifiers current draw significantly. The regulator supplying VDD_PA should be capable of reacting to load changes within 5µs. **Note: VDD_PA has an internal 2.2µF ceramic bypass capacitor, it should be made certain the regulator feeding VDD_PA is stable with ceramic load capacitors.**

These voltages are not tied to each other and any combination of supply voltages within the specified limits can be used.

In a 3.3V logic level host system all other supplies would usually be tied to the 3.3V supply, with a separate regulator providing the 1.45-2.0V supply for the Wi-Fi core. A switch mode regulator with 1.5V output is recommended for minimum power consumption. Please see the example schematic in this datasheet.

In a 1.8V logic level host system, all other supplies can be connected to the 1.8V supply rail except VDD_PA which should be connected to a 2.7-4.8V supply.

The higher voltage supplies should be powered before or at the same time as the core supply line, i.e. the **VDD_REGIN should be powered up last**. Powering the core first may lead to the GPIO and SDIO blocks booting into an inaccessible state.

External high frequency bypassing for any the supply lines is not required, all supplies contain internal capacitors. If the VDD_PA line is fed directly from a battery or there are concerns about the speed of the regulator feeding it, a capacitor of around 100µF should be connected close to the module.

Note: All supply voltages and ground lines must be connected.

5.2 REGEN

The regulator enable pin REGEN is used to enable the WF111. REGEN enables the regulators of the digital and analog core supply voltages.

The pin is active high, with a logic threshold of around 1V, and has a weak pull-down. REGEN can tolerate voltages up to 2.0V, and may be connected directly to the internal voltage regulator input (VDD_REGIN) to permanently enable the device. Part of the regulators can also be disabled by firmware in power saving modes. The VDD_REGIN supply can also be externally switched off while leaving the other supply voltages powered.

Cutting power to the core will fully shut down the module internal processors and returning power will cause a power-on reset, requiring a full initialization of the module.

The REGEN pin will not disable system blocks not supplied by the core supply, meaning the coexistence interface and the SDIO Function 0 are available even when the core is powered off.

5.3 RESET

WF111 may be reset from several sources: RESET pin, power-on reset, via software configured watchdog timers as well as through the SDIO/CSPI host interface.

The RESET pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset is performed between 1.5 and 4.0ms following RESET being active. It is recommended that RESET be applied for a period greater than 5ms.

The power-on reset occurs when the core supply (generated by the internal 1.2V linear regulator) falls below typically 1.05V and is released when core voltage rises above typically 1.10V. At reset regardless of the source the digital I/O pins are set to a high impedance state with weak pull-downs, except RESET and DEBUG_SPI_CS# which have a weak pull-up. The host connection interface is only reset by the RESET pin or a power-on reset.

A power-on reset can be achieved through powering down the digital core by either externally cutting the VDD_REGIN supply or giving a low pulse to the REGEN-pad. If REGEN is connected to the host system for powering down the module, or a separate core power switch is implemented, the RESET pin can be tied permanently to a supply voltage line.

Following a reset, WF111 automatically generates internally the clocks needed for safe boot-up of the internal processors. The crystal oscillator is then configured by software with the correct input frequency.

Note: holding the RESET line low will not drive the module into a low power consumption mode, it can't be used as a power-off signal

6 Example Application Schematic

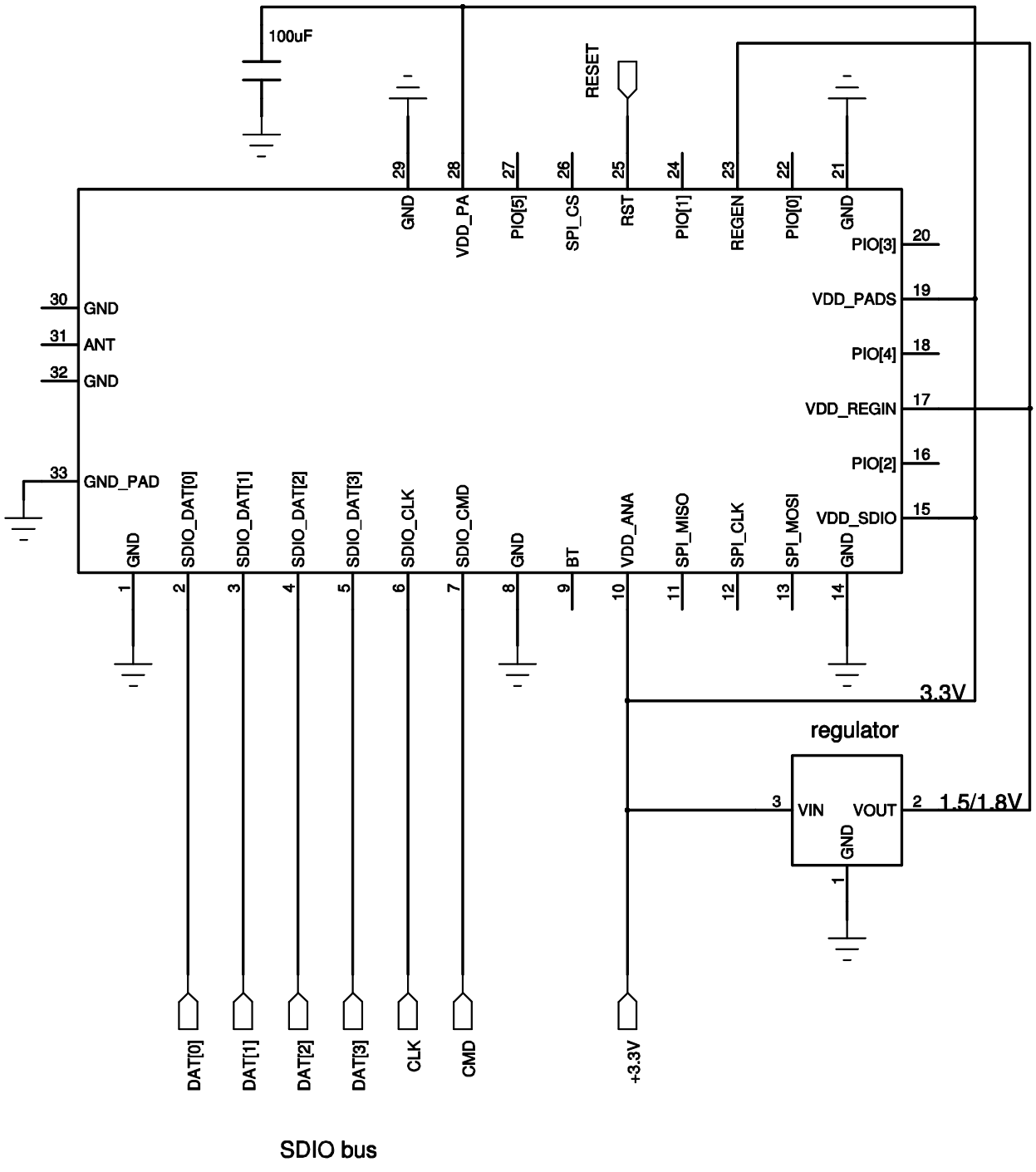


Figure 9: An example application circuit with SDIO host connection, 3.3V level host logic and 1.5/1.8V core supply, REGEN hard wired to the core supply and RST pad used to reset the module (Note: with N-variant ANT-pad and associated grounds would also be connected)

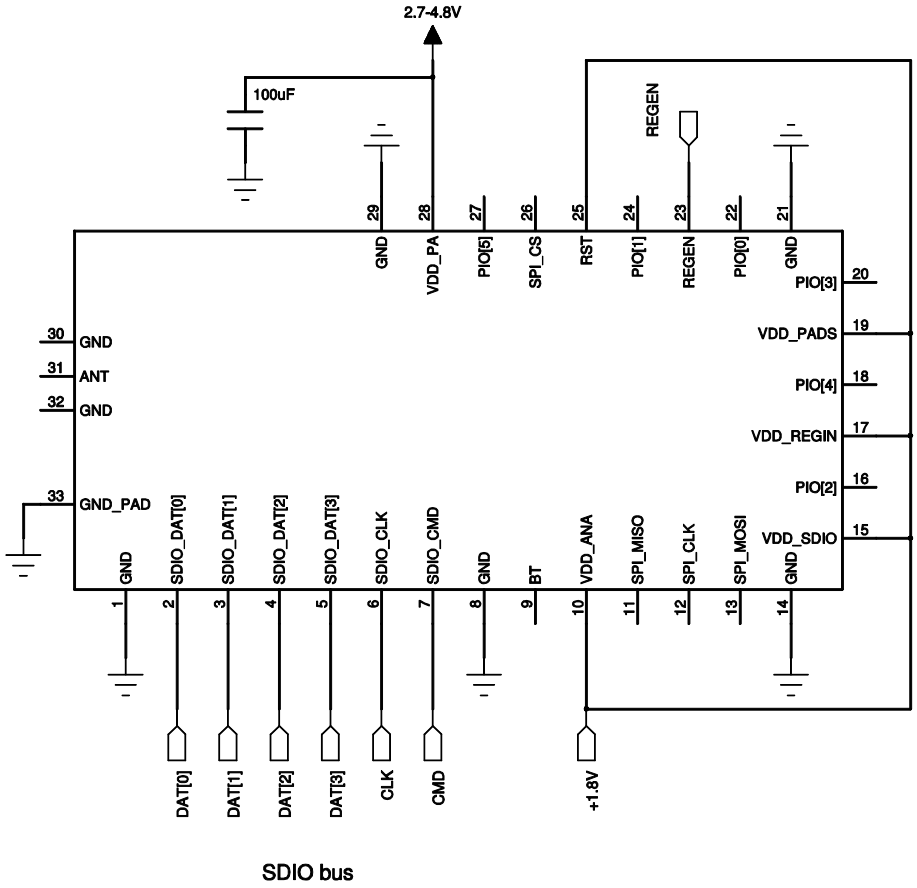


Figure 10: An example application circuit with SDIO host connection, 1.8V level host logic and a separate power amplifier supply, RST hard wired to the core supply and REGEN pad used to power off and reset the module (Note: with N-variant ANT-pad and associated grounds would also be connected)

7 Wi-Fi radio

7.1 Wi-Fi receiver

The receiver features direct conversion architecture. Sufficient out-of-band blocking specification at the Low Noise Amplifier (LNA) input allows the receiver to be used in close proximity to Global System for Mobile Communications (GSM) and Wideband Code Division Multiple Access (W-CDMA) cellular phone transmitters without being desensitized. High-order baseband filters ensure good performance against in-band interference.

7.2 Wi-Fi transmitter

The transmitter features a direct IQ modulator. Digital baseband transmit circuitry provides the required spectral shaping and on-chip trims are used to reduce IQ modulator distortion. Transmitter gain can be controlled on a per-packet basis, allowing the optimization of the transmit power as a function of modulation scheme.

The internal Power Amplifier (PA) has a maximum output power of +15dBm for IEEE 802.11g/n and +17dBm for IEEE 802.11b. The module internally compensates for PA gain and reference oscillator frequency drifts with varying temperature and supply voltage.

7.3 Antenna switch for *Bluetooth* coexistence

WF111 supports sharing the integrated antenna or antenna connector with a *Bluetooth* device through the BT_RF pad. The module contains a bypass switch to route the *Bluetooth* signal directly to the antenna, and supports using the internal LNA for *Bluetooth* reception. The switch is controlled through the coexistence interface. Using the switch will require either two extra control lines or support for Unity-3e scheme for both devices.

Antenna sharing will require full re-certification of both modules used for FCC due to the changed antenna path and some radiated emission measurements for CE. Without a combined stack driver, the coexistence system will have reduced performance and antenna sharing will reduce it further during simultaneous communication. The antenna switch will also have some losses which will reduce *Bluetooth* range. For low rate communication or non-simultaneous use the system should function well.

Currently, Bluegiga does not recommend antenna sharing due to the suboptimal performance.

8 Electrical characteristics

8.1 Absolute maximum ratings

Rating	Min	Max	Unit
Storage temperature	-40	85	°C
VDD_PADS, VDD_ANA, VDD_SDIO	-0.4	3.6	V
VDD_REGIN, REGEN	-0.4	2.5	V
VDD_PA	-0.4	6	V
Other terminal voltages	VSS+0.3	VDD+0.3	V

Table 7: Absolute Maximum Ratings

8.2 Recommended Operating Conditions

Rating	Min	Max	Unit
Operating temperature range (a)	-40	85	°C
VDD_PADS, VDD_SDIO, VDD_ANA	1.7	3.6	V
VDD_PA	2.7	4.8	V
VDD_REGIN	1.45	2	V

Table 8: Recommended Operating Conditions

(a) The module will heat up depending on use, at high transmit duty cycles the maximum operating temperature may need to be derated. See chapter 12.4

8.3 Input/Output terminal characteristics

Digital Terminals	Min	Typ	Max	Unit
Input Voltage Levels				
V_{IL} input logic level low 1.7V ≤ VDD ≤ 3.6V	-0.3	-	0.25*Vdd	V
V_{IH} input logic level low 1.7V ≤ VDD ≤ 3.6V	0.625*Vdd	-	VDD+0.3	V
Output Voltage Levels				
V_{OL} output logic level low 1.7V ≤ VDD ≤ 3.6V, (I_o = 4.0 mA)	-	-	0.4	V
V_{OH} output logic level low 1.7V ≤ VDD ≤ 3.6V, (I_o = -4.0 mA)	0.75*Vdd	-	Vdd	V
Input Tri-state Current with:				
Strong pull-up	-150	-40	-10	µA
Strong pull-down	10	40	150	µA
Weak pull-up	-5	-1	-0.33	µA
Weak pull-down	0.33	1	5	µA
I/O pad leakage current	-1	0	1	µA
Pad input capacitance	1	-	5	pF

Table 9: Digital terminal electrical characteristics

9 RF Characteristics

	Min	max	
Channel	1	11 (13)	Support for modules with 13 channels enabled can be by specific order by contacting Bluegiga Sales. MOQ will apply. With 13 channels enabled, the FCC certification will not apply.
Frequency	2412	2462 (2472)	MHz

Table 10: Supported frequencies

Standard	Supported bit rates
802.11b	1, 2, 5.5, 11 Mbps
802.11g	6, 9, 12, 18, 24, 36, 48, 54 Mbps
802.11n, HT, 20MHz, 800ns	6.5, 13, 19.5, 26, 39, 52, 58.5, 65 Mbps
802.11n, HT, 20MHz, 400ns	7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65, 72.2 Mbps

Table 11: Supported modulations

802.11b	Typ	802.11g	Typ	802.11n short GI	Typ	802.11n long GI	Typ
1 Mbps	-97 dBm	6 Mbps	-92 dBm	6.5 Mbps	-91 dBm	7.2 Mbps	-92 dBm
2 Mbps	-95 dBm	9 Mbps	-91 dBm	13 Mbps	-87 dBm	14.4 Mbps	-90 dBm
5.5 Mbps	-93 dBm	12 Mbps	-89 dBm	19.5 Mbps	-85 dBm	21.7 Mbps	-87 dBm
11 Mbps	-89 dBm	18 Mbps	-87 dBm	26 Mbps	-82 dBm	28.9 Mbps	-84 dBm
		24 Mbps	-84 dBm	39 Mbps	-78 dBm	43.3 Mbps	-80 dBm
		36 Mbps	-80 dBm	52 Mbps	-74 dBm	57.8 Mbps	-75 dBm
		48 Mbps	-75 dBm	58.5 Mbps	-71 dBm	65 Mbps	-72 dBm
		54 Mbps	-73 dBm	65 Mbps	-68 dBm	72.2 Mbps	-69 dBm

Table 12: Receiver sensitivity

Modulation type	Min	Typ	Max	
802.11b	+16	+17	+17.6	dBm
802.11g	+14	+15	+15.6	dBm
802.11n	+14	+15	+15.6	dBm

Table 13: Transmitter output power at maximum setting

Operating mode	Min	Typ	Max	
TX loss	-2.5	-3	-3.5	dB
RX gain (using internal LNA)	8	10	12	dB
Internal LNA noise figure		2.0	2.5	dB

Table 14: BT antenna sharing interface properties

	Typ	Max	802.11 limit (total error)	
Variation between individual units	+/-5	+/-10	+/-25	ppm
Variation with temperature	+/-3	+/-10	+/-25	ppm

Table 15: Carrier frequency accuracy