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WizFi210 Datasheet

(Version 1.20)

WizFi220 follows all of information described in this documents

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Certification Information

CE for Class B ITE

INFORMATION TO THE USER
Hereby, WIZnet. Declares that these WizFi210 and WizFi220 are in compliance with the essential requirements
and other relevant provisions of directive 1999/5/EC.

WARNING: These are the class B products. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

FCC for Class B ITE

INFORMATION TO THE USER
These equipments have been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no Guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

WARNING: These equipments may generate or use radio frequency energy. Changes or modifications to this equipment may cause harmful interference unless the modifications are expressly approved in the instruction manual. The user could lose the authority to operate this equipment if an unauthorized change or modification is made.

TELEC

010-100040

Equipment : Wireless Module
Model : WizFi210 UFL antenna type, WizFi210 Chip antenna type
Made in Korea

KCC for Class B ITE

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- Trade Name or Applicant : WIZnet Co., Ltd.
- Equipment Name : Wireless LAN Module
- Model Number : WizFi210 / WizFi220
- Manufacturer / Country of Origin : WIZnet, Co., Ltd. / KOREA
- Certification Number : KCC-CRM-WWW-WIZFI210 / KCC-CRM-WWW-WIZFI220

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Document Revision History

Date	Revision	Changes
2011-03-24	V1.0	Official Release
2011-05-24	V1.01	Changed Power Consumption and RF Output Power Added Auto Reconnect AT Command(AT+XAR) Added Certification Information
2011-09-05	V1.10	Changed Evaluation Board Changed GPIO number(HW Trigger, Button) Changed AT+XEHT Command Added Limited AP Feature Added WizFi220 Specs
2012-01-11	V1.11	Added UART baud rate(460800, 921600bps) Added EXT_nRESET description Added FAQ Added AT+DHCPSRVR Command Added Product contents
2012-10-24	V1.12	Added AT+WAUTO Option(2 for Limited AP mode) Added FAQ(Reducing the disassociation event) Removed unused AT Commands Removed some features for customizing f/w
2013-03-08	V1.13	Added AT+XRESET Command Added max/min power value of AT+WP command
2013-03-12	V1.14	Added explanation of AT+XRESET Command Added FAQ
2013-05-06	V1.2	Divided two documents, Datasheet for Hardware Engineer and Programmers' guide for Software Engineer. More detail information included in datasheet.

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1. Overview

WizFi210/220(hereinafter WizFi210) is a Wi-Fi module that provides the robust and stale Wi-Fi connectivity with low power consumption. WizFi210 performs all functions for Wi-Fi connectivity and TCP/IP processing. All you have to do is just sending commands to the module via serial interface.

- Support 802.11b only
- Serial interface
  - UART(up to 921Kbps baud rate)
  - SPI(up to 2.25MHz clock)
- Support AT commands
- Support to multi sockets up to 16 concurrently
- Plenty of TCP/IP functions
  - TCP, UDP, IP, ICMP,
- Ultra low power
  - Support to Sleep mode and Alarm input for waking up WizFi210 in sleep mode
- Plenty of Security mode
  - WEP, WPA, WPA2PSK, Enterprise mode(example EAP-TLS and so on)
- Support GPIOs
- Hardware accelerator for AES and RC4 encryption/decryption
- Plenty of Operation mode
  - Station mode(infrastructure)
  - Ad-hoc mode
  - Limited AP(Soft AP) mode without ethernet or Wifi interface for uplink

2. Brief Specifications

Specifications	Description
Radio Protocol	IEEE 802.11b/g/n Compatible
Supported Data Rates	11, 5.5, 2, 1 Mbps (IEEE 802.11b)
Modulation	DSSS and CCK
RF Operating Frequency	2.4 - 2.497 GHz
Antenna Options	Chip antenna and U.FL connector for external antenna
Networking Protocols	UDP, TCP/IP (IPv4), DHCP, ARP, DNS, HTTP/HTTPS Client and Server[1]
Power Consumption (Typical)	Standby = 34.0 µA(WizFi210), 35.0 µA(WizFi220) Receive = 125.0 mA(WizFi210), 125.0 mA(WizFi220) Transmit = 135.0 mA(WizFi210), 250.0 mA(WizFi220)
RF Output Power (Typical)	8 ± 1 dBm (WizFi210) 17 ± 1.5 dBm (WizFi220)
Security Protocols	WEP, WPA/WPA2–PSK, Enterprise(EAP-FAST, EAP-TLS, EAP-TTLS, PEAP)[1]
I/O Interface	UART, SPI[1], WAKE, ALARM, GPIOs
Power Source	3.3V
Dimensions	32 x 23.5 x 3 mm

Table 1 Brief Specification

[1] A dedicated SW is for support to this function

3. Block Diagram

WizFi210 and WizFi220 have the same functions and capabilities except their RF Transmission Power.

WizFi220 has extra PA inside for improving its RF Transmission Power.

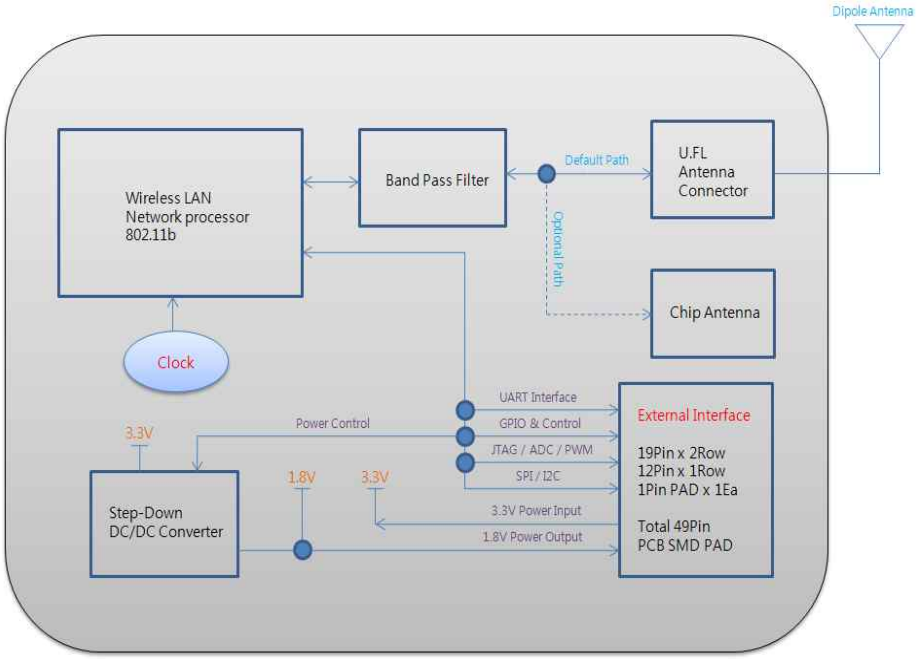

Figure 1 WizFi210 block diagram

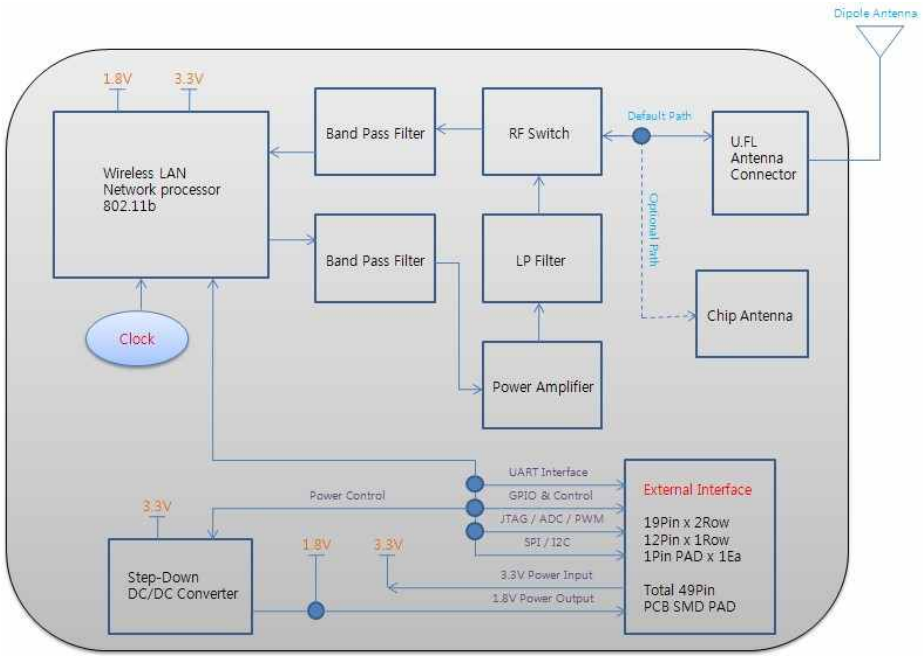

Figure 2 WizFi220 block diagram

4. Pin Description

4.1. Pin Map

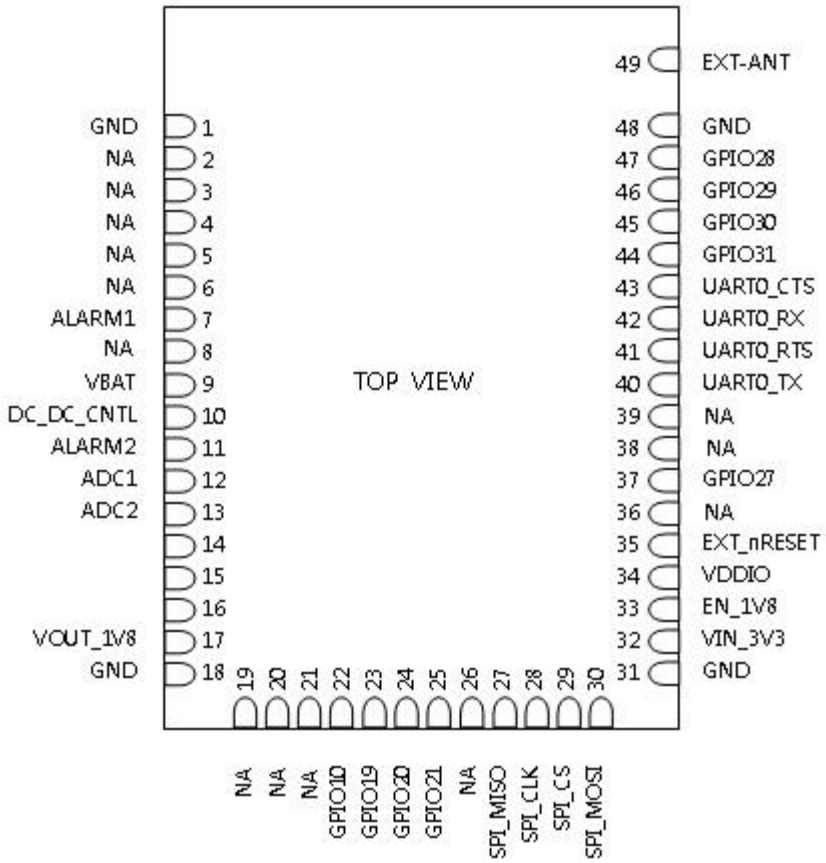

Figure 3 WizFi210 Pin map

4.2. Pin Description

PIN	NAME	I/O	IN BIAS	DESCRIPTION
1	GND	P	NA	Ground
2	NA	I	Pull-up	
3	NA	O	NA	
4	NA	I	NA	
5	NA	I	Pull-up	
6	NA	I	Pull-up	

7	ALARM1	I	NA	Embedded Real Time Clock Wake Up Input 1
8	NA	O	NA	
9	VBAT	P	NA	Embedded Real Time Clock Power Supply
10	DC_DC_CNTL	O	NA	VIN_3V3 Regulator Control Output
11	ALARM2 (*)	I	NA	Embedded Real Time Clock Wake Up Input 2
12	ADC1 (*)	I	NA	General Analog to Digital Converter 1
13	ADC2 (*)	I	NA	General Analog to Digital Converter 2
14	NA	I/O	Pull-down	
15	NA	I/O	Pull-down	
16	NA	I/O	Pull-down	
17	VOUT_1V8 (*)	P	NA	Internal 1.8V Vout
18	GND	P	NA	Ground
19	NA	I/O	Pull-down	
20	NA	I/O	Pull-down	
21	NA	I/O	Pull-down	
22	GPIO10	I/O	Pull-down	General Purpose Input Out-put
23	GPIO19 (*)	I/O	Pull-down	General Purpose Input Output **Data Received Indicator** to Host **while using SPI** **This is OUTPUT, means HOST_WAKEUP, from WizFi210**
24	GPIO20	I	Pull-down	General Purpose Input Output
25	GPIO21	I	Pull-down	Factory Reset(Normal High) Factory mode 1 : Limited AP & Web Server for configuration Factory mode 2 : Ad-hoc mode
26	NA	IO	Pull-down	
27	SPI_MISO (*)	O	Pull-up	SPI Slave Transmit Data Output to the HOST
28	SPI_CLK (*)	I	Pull-up	SPI Slave Clock Input from the HOST

29	SPI_CS (*)	I	Pull-up	SPI Slave Chip Select Input from the HOST
30	SPI_MOSI (*)	I	Pull-down	SPI Slave Receive Data Input from the HOST
31	GND	P	NA	Ground
32	VIN_3V3	P	NA	Single Supply Port
33	EN_1V8	I	NA	Internal 1.8V regulator enable port Active High
34	VDDIO(**)	P	NA	All I/O voltage domain (can be tied to VIN_3V3 or tied to HOST I/O supply)
35	EXT_nRESET	I	Pull-up	Module **Hardware Reset Input**[2]
36	NA	I/O	Pull-down	
37	GPIO27 (*)	O	Pull-down	**Firmware Program Enable** WizFi210/220 operate as firmware download mode, if this is **HIGH** at booting On normal mode, this should be **LOW**
38	NA	I	Pull-down	
39	NA	O	Pull-down	
40	UART0_TX	O	Pull-down	Universal Asynchronous Receiver Transmitter Output
41	UART0_RTS	O	Pull-down	Universal Asynchronous Receiver Transmitter Request to Send Output
42	UART0_RX	I	Pull-down	Universal Asynchronous Receiver Transmitter Input
43	UART0_CTS	I	Pull-down	Universal Asynchronous Receiver Transmitter Clear to Send Input
44	GPIO31 (S_MODE)	O	Pull-down	Data mode / command mode status Indicator You can monitor this pin to know which mode is now. LOW : Data mode HIGH : Command mode
45	GPIO30 (S_RX)	O	Pull-down	Serial Data Received
46	GPIO29 (C_MODE)	I	Pull-down	Switch of Command mode or Data mode You can control this pin to switch some mode

[2] In case of WizFi220, after HW reset on EXT_nRESET, user should command, AT+XRESET inorder to initialize all memory and configuration inside WizFi220.

				LOW : Data mode HIGH : Command mode
47	GPIO28 (S_ASSOCIATE)	O	Pull-down	AP Association status LOW : associated HIGH : disassociated
48	GND	P	NA	Ground
49	EXT-ANT	IO	NA	External Antenna pad

Table 2 WizFi210 Pin Description

4.3. Factory Reset Timing Diagram

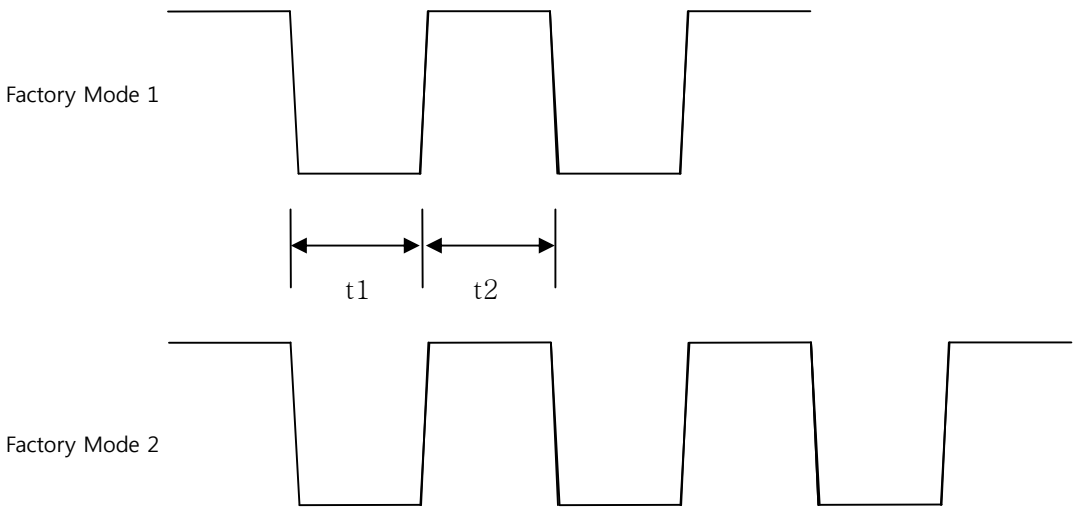

Figure 4 Factory Reset Timing Diagram

Variable	Min	Typ	Max
t1	200ms	300ms	500ms
t2	200ms	300ms	500ms

Table 3 Factory Reset Timing Value

5. EXT_nRESET guide

EXT_nRESET pin is bidirectional.

EXT_nRESET pin is an output right at power-on, and kept it asserted while the 32KHz crystal is stabilizing. Once crystal is stabilized, RESET is de-assert and it becomes an input.

MCU does need to assert the signal if there is not any problem such as hang-up.

Note: Minimum pulse width for reset is two 32KHz clock.

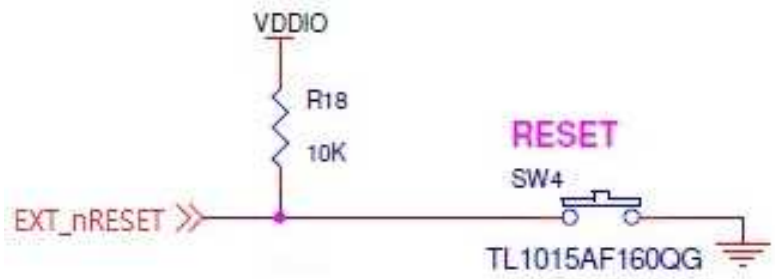

Figure 5 Reference Schematic for EXT_nRESET

EXT_nRESET signal is active low signal .

It's an output during power up, and it notifies to host processor that WizFi210 device is out of power-on-reset. After power-on-reset, this pin becomes an input. To assert EXT_nRESET is required to initialize WizFi210 without Power-on-reset.

But there are some difference between Power-on-reset and asserting EXT_nRESET.

Power-on-reset clear and initialize all configuration information which is set in WizFi210, but asserting EXT-nRESET doesn't clear and initialize some configuration information. So, if user assert EXT_nRESET for initialization of WizFi210, user should place a command, "AT+XRESET" to WizFi210 for initialization of all configuration information successfully.

6. RF Specification

Specification	Description
Modulation Technique	DSSS for 1, 2Mbps CCK for 5.5, 11Mbps
Data Rate	IEEE 802.11b: 1, 2, 5.5 and 11Mbps
Receive Sensitivity **(U.FL Connector version)**	-84dBm ± 1dB @ 11Mbps -88dBm ± 1dB @ 5.5Mbps -90dBm ± 1dB @ 2Mbps -94dBm ± 1dB @ 1Mbps
Transmit power **(U.FL Connector version)**	WizFi 210 : 8dBm ± 1dB @ 11Mbps WizFi 220 : 17dBm ± 1.5dB @ 11Mbps
Frequency Range	USA: 2.400 ~ 2.483GHz Europe: 2.400 ~ 2.483GHz Japan: 2.400 ~ 2.497GHz China: 2.400 ~ 2.483GHz
Operating Channels	USA/Canada: 11 (1~11) Major Europe Countries: 13 (1~13) France: 4 (10~13) Japan: 14 for IEEE 802.11b (1~13 or 14th), 13 for IEEE 802.11g (1~13) Korea/China: 13 (1~13)
Antenna	U.FL External Antenna Support(CON) External Antenna Pad Support(EX) Chip Antenna (Optional) (CA)

Table 4 RF Specification

7. Power Consumption

7.1. WizFi210 Mode 1(VDDRTC=VDD=3.3V, VDDIO=1.8V, Temp=25°C)

WizFi 210	Min	Type	Max	Unit
Standby mode **(Only V_{DDRTC} is active)**		35	50	µA
Idle mode **(CPU running, WLAN disconnected)**			10	mA
Receive **(-81dBm RX sensitivity)**		125	130	mA
Transmit **(+8dBm at antenna port)**		135	140	mA

Table 5 WizFi210 Mode 1(VDDIO = 1.8V)

7.2. WizFi210 Mode 2(VDDRTC=VDD=3.3V, VDDIO=3.3V, Temp=25°C)

WizFi 210	Min	Type	Max	Unit
Standby mode **(Only V_{DDRTC} is active)**		35	50	µA
Idle mode **(CPU running, WLAN disconnected)**			11	mA
Receive **(-81dBm RX sensitivity)**		125	130	mA
Transmit **(+8dBm at antenna port)**		135	140	mA

Table 6 WizFi210 Mode 2(VDDIO = 3.3V)

7.3. WizFi220 Mode 1(VDDRTC=VDD=3.3V, VDDIO=1.8V, Temp=25°C)

WizFi 220	Min	Type	Max	Unit
Standby mode **(Only V_{DDRTC} is active)**		35	50	μA
Idle mode **(CPU running, WLAN disconnected)**			12	mA
Receive **(-81dBm RX sensitivity)**		125	130	mA
Transmit **(+8dBm at antenna port)**		250	260	mA

Table 7 WizFi220 Mode 1(VDDIO = 1.8V)

7.4. WizFi220 Mode 2(VDDRTC=VDD=3.3V, VDDIO=3.3V, Temp=25°C)

WizFi 220	Min	Type	Max	Unit
Standby mode **(Only V_{DDRTC} is active)**		35	50	μA
Idle mode **(CPU running, WLAN disconnected)**			13	mA
Receive **(-81dBm RX sensitivity)**		125	130	mA
Transmit **(+8dBm at antenna port)**		250	260	mA

Table 8 WizFi220 Mode 2(VDDIO = 3.3V)

8. Dimension

8.1. Module Dimension

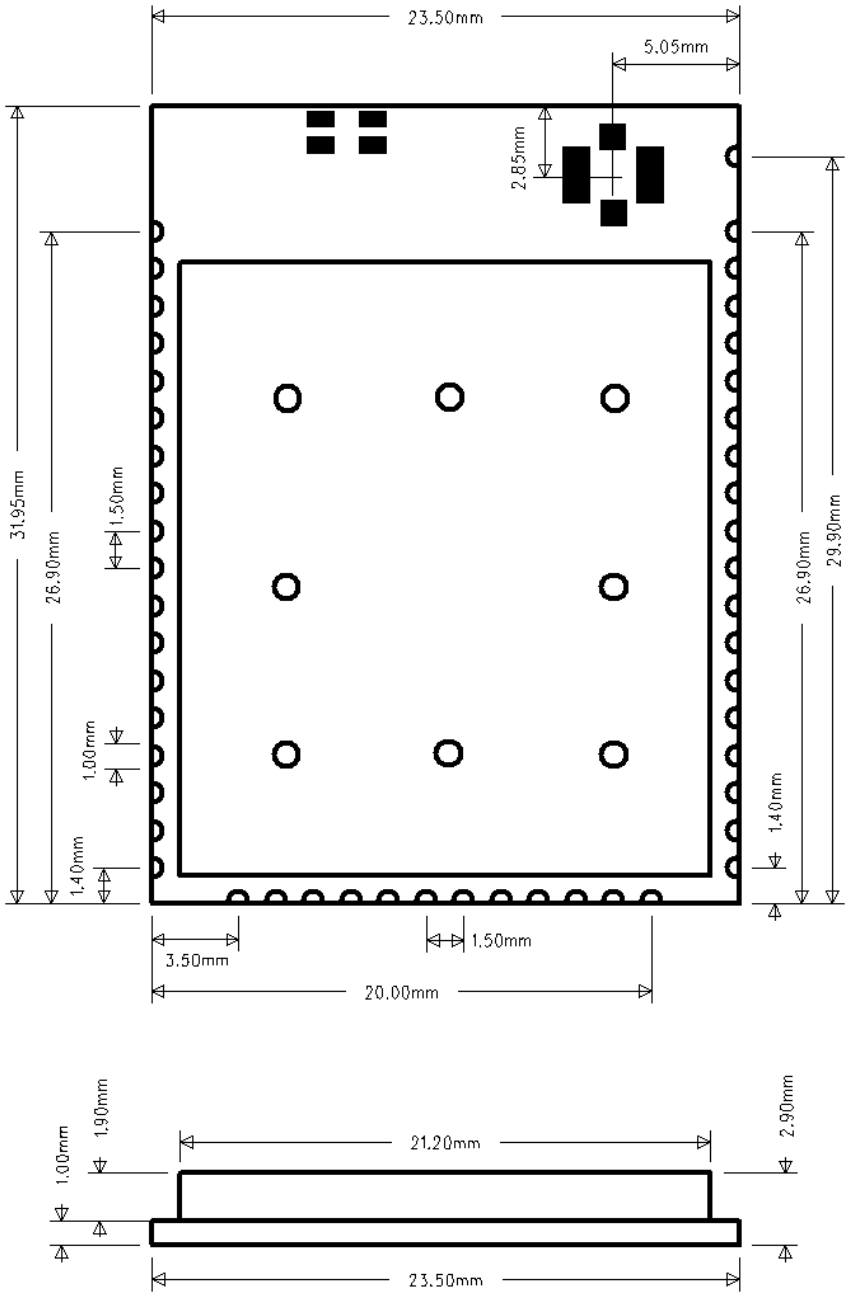

Figure 6 Module Dimension

8.2. Recommended Footprint Dimension

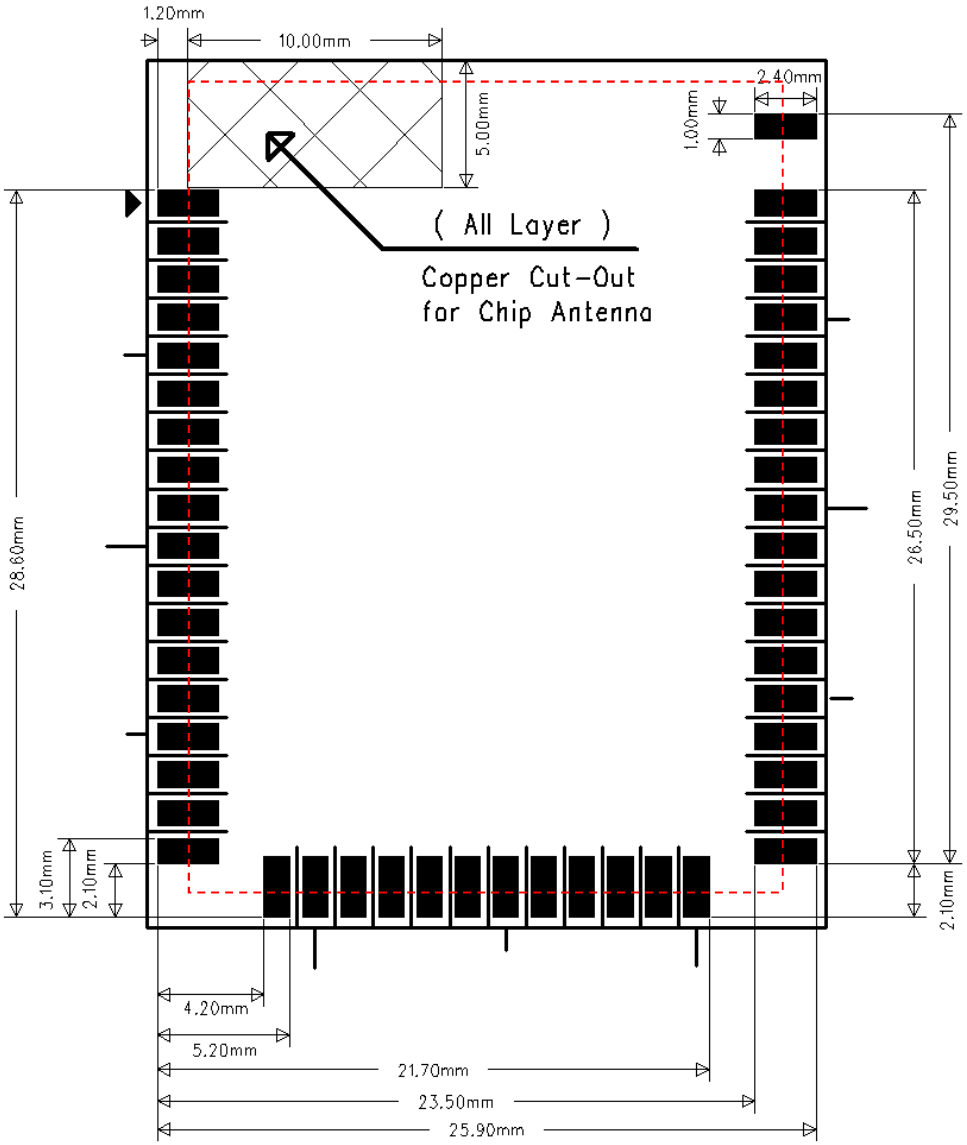

Figure 7 Recommended Footprint Dimension

9. Electrical characteristics

9.1. Operating Condition

	Min	Typ	Max	Unit
Operating Ambient Range	-40		+85	℃
RTC Supply Voltage	1.2	3.3	3.6	V
Single Supply Voltage	3.0	3.3	3.6	V

Table 9 Operating Condition

9.2. Digital Input characteristics

	Min	Typ	Max	Unit
IO Supply Voltage	1.62	1.8	1.98	V
	3	3.3	3.63	
Input Low Voltage (V_{IL})	-0.3		$0.25V_{DDIO}$	V
Input High Voltage (V_{IH})	$0.8V_{DDIO}$		V_{DDIO}	V
Schmitt trig. Low to High threshold point (V_{T+})	1.5			V
Schmitt trig. High to Low threshold point (V_{T-})			1	V

Table 10 Digital Input Characteristics

9.3. Digital Output characteristics

	Min	Typ	Max	Unit
IO Supply Voltage	1.62	1.8	1.98	V
	3	3.3	3.63	
Output Low Voltage (V_{IL})	0		0.4	V
Output High Voltage (V_{IH})	1.3		V_{DDIO}	V
Output rise time (t_{TLH})			7	ns
Output fall time (t_{THL})			7	ns

Table 11 Digital Output Characteristics

9.4. Tri-State I/O characteristics

	Min	Typ	Max	Unit
IO Supply Voltage	1.62	1.8	1.98	
	3	3.3	3.63	
Input Low Voltage (V_{IL})	-0.3		$0.25V_{DDIO}$	V
Input High Voltage (V_{IH})	$0.8V_{DDIO}$		V_{DDIO}	V
Schmitt trig. Low to High threshold point (V_{T+})	1.5			V
Schmitt trig. High to Low threshold point (V_{T-})			1	V
Pull-Up Resistor (R_u)	0.05		1	MΩ
Pull-Down Resistor (R_d)	0.05		1	V
Output Low Voltage (V_{OL})	0		0.4	V
Output High Voltage (V_{OH})	1.3		V_{DDIO}	V
Output rise time @ 3.3V (t_{ToLH})			7	ns
Output fall time @ 3.3V (t_{ToHL})			7	ns
Input rise time (t_{TiLH})			7	ns
Input fall time (t_{TiHL})			7	ns

Table 12 Tri-State I/O Characteristics

9.5. RTC Input characteristics

	Min	Typ	Max	Unit
RTC Supply Voltage (V_{DDRTC})	1.2		3.6	V
Input Low Voltage (V_{IL})	-0.3		$0.25V_{DDRTC}$	V
Input High Voltage (V_{IH})	$0.8V_{DDRTC}$		V_{DDRTC}	V
Schmitt trig. Low to High threshold point (V_{T+})	$0.57V_{DDRTC}$		$0.68V_{DDRTC}$	V
Schmitt trig. High to Low threshold point (V_{T-})	$0.27V_{DDRTC}$		$0.35V_{DDRTC}$	V

Table 13 RTC Input Characteristics

9.6. RTC Output characteristics

	Min	Typ	Max	Unit
RTC Supply Voltage (V_{DDRTC})	1.2		3.6	V
Output Low Voltage (V_{OL})	0		0.4	V
Output High Voltage (V_{OH})	$0.8V_{DDRTC}$		V_{DDRTC}	V
Output rise time (t_{TLH})	19		142	ns
Output fall time (t_{THL})	21		195	ns

Table 14 RTC Output Characteristics

9.7. Internal 1.8V regulator characteristics

	Min	Typ	Max	Unit
Output Voltage (VOUT_1V8)		1.8		V
Maximum Output Current (IVOUT_1V8)		250	300	mA
1.8V Regulator Enable "H" Voltage (EN_1V8)	1.0		VIN_3V3	V
1.8V Regulator Enable "L" Voltage (EN_1V8)	0		0.25	V

Table 15 Internal 1.8V Regulator Characteristics

9.8. Communication Interface

9.8.1. UART Interface characteristics

9.8.2. SPI Interface characteristics

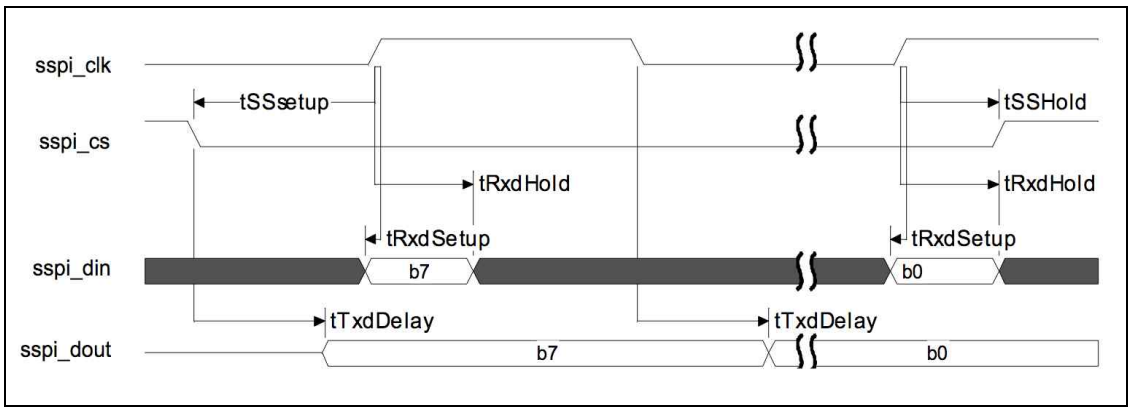

Figure 8 SPI Interface Timing Diagram

Parameter	Description	Minimum	Maximum	Unit
tSSetup	Minimum time between falling edge of Select line and first rising edge of SPI clock.	4 core SPI clock periods + 68 ns		mixed
tTxdDelay	Delay in Slave asserting TX line after falling edge of SPI clock, or the first bit after falling edge of the Select line.		4 core SPI clock periods + 68 ns	mixed
tRxdSetup	Time before rising edge of SPI clock by which received data must be ready	15		ns
tRxdHold	Time for which received data must be stable after rising edge of SPI clock	3 core SPI clock periods + 14 ns		mixed
tSSHold	Time for which the Select line will be held after the sampling edge for the final bit to be transferred	3 core SPI clock periods + 14 ns		mixed

Table 16 SPI Interface Timing value

10. Reflow Condition

	Condition	Recommend	Range	Unit
Pre-Heat	**Temperature Ramp up rate for (A)**	**3**	**2~4**	**℃/s**
	Pre-heat time (B)	**130**	**60~180**	**sec**
	Pre-heat ending temperature (C)	**200**	**150~200**	**℃**
Heating	**Peak Temperature range (D)**	**236**	**230~240**	**℃**
	Melting time that is the time over 218℃ (E)	**45**	**30~50**	**sec**

Table 17 Reflow condition

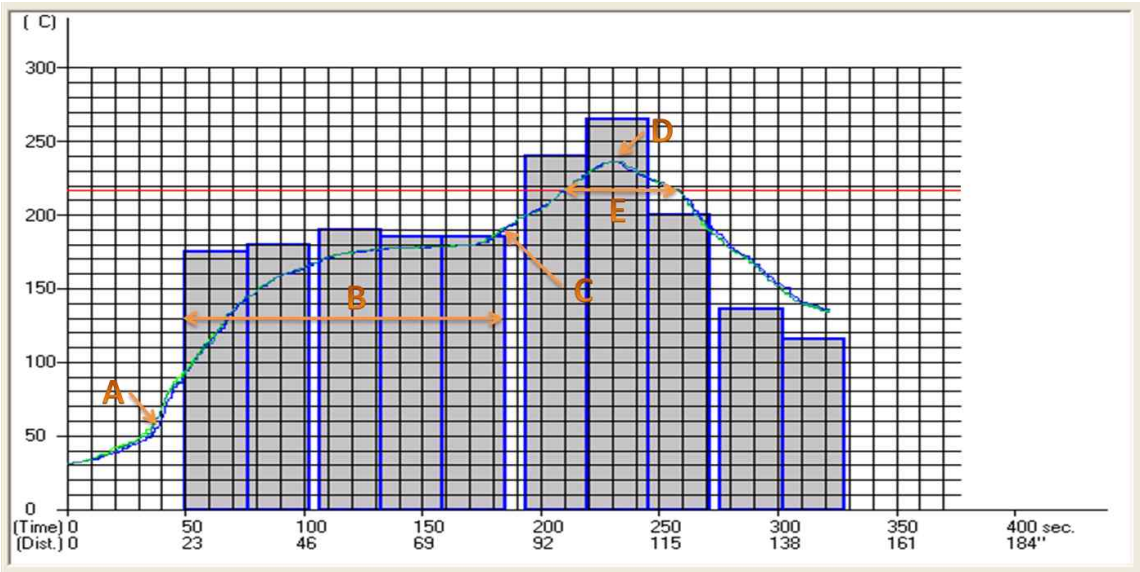

Figure 9 Reflow Chart

11. Circuit guide for On-board FW upload

WizFi210 provides some specific firmware according to its services. Until now, there are four standard firmware and some customized firmware to specific customers.

WizFi210 decides its operating mode according to the input value of GPIO27. WizFi210 operates as programming mode when GPIO27's input value is "HIGH", otherwise running mode. WizFi210 communicate with PC via UART in order to upload another firmware, so you have to connect UART0_Rx and UART0_Tx to the external interface for communicating with PC.

So, we recommend that you make your board be capable to upload another firmware as Figure 7 below.

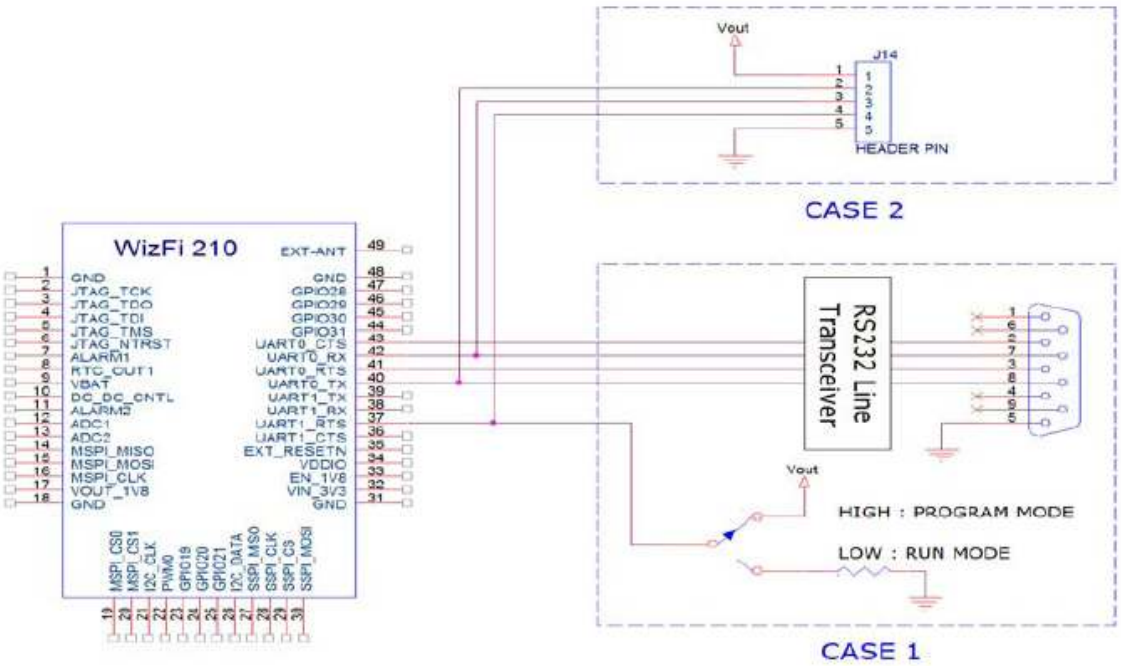

Figure 10 Reference schematic for On-Board FW Upload