Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Cortina Systems® LXT971A Single-Port 10/100 Mbps PHY Transceiver

Datasheet

The Cortina Systems® LXT971A Single-Port 10/100 Mbps PHY Transceiver (LXT971A PHY) directly supports both 100BASE-TX and 10BASE-T applications. It provides a Media Independent Interface (MII) for easy attachment to 10/100 Media Access Controllers (MACs). The LXT971A PHY is IEEE compliant, and provides a Low Voltage Positive Emitter Coupled Logic (LVPECL) interface for use with 100BASE-FX fiber networks. The LXT971A PHY supports full-duplex operation at 10 Mbps and 100 Mbps. Operating conditions for the LXT971A PHY can be set using auto-negotiation, parallel detection, or manual control. The LXT971A PHY is fabricated with an advanced CMOS process and requires only a single 2.5/3.3 V power supply. (This Datasheet also supports the LXT971 PHY.)

Applications

- Combination 10BASE-T/100BASE-TX or 100BASE-FX Network Interface Cards (NICs)
- Network printers
- 10/100 Mbps PCMCIA cards
- Cable Modems and Set-Top Boxes

Product Features

- 3.3 V Operation
- Low power consumption (300 mW typical)
- Low-power “Sleep” mode
- 10BASE-T and 100BASE-TX using a single RJ-45 connection
- IEEE 802.3-compliant 10BASE-T or 100BASE-TX ports with integrated filters
- Auto-negotiation and parallel detection
- MII interface with extended register capability
- Robust baseline wander correction
- Carrier Sense Multiple Access / Collision Detection (CSMA/CD) or full-duplex operation
- JTAG boundary scan
- MDIO serial port or hardware pin configurable
- 100BASE-FX fiber-optic capable
- Integrated, programmable LED drivers
- 64-ball Plastic Ball Grid Array (PBGA) or 64-pin Quad Flat Package (LQFP)
- LXT971ABC - Commercial (0° to 70 °C amb.)
- LXT971ABE - Extended (-40° to 85 °C amb.)
- LXT971ALC - Commercial (0° to 70 °C amb.)
- LXT971ALE - Extended (-40° to 85 °C amb.)
- LXT972ALC - Commercial (0° to 70 °C amb.)

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH CORTINA SYSTEMS® PRODUCTS.

NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

EXCEPT AS PROVIDED IN CORTINA'S TERMS AND CONDITIONS OF SALE OF SUCH PRODUCTS, CORTINA ASSUMES NO LIABILITY WHATSOEVER, AND CORTINA DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF CORTINA PRODUCTS, INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

Cortina products are not intended for use in medical, life saving, life sustaining, critical control or safety systems, or in nuclear facility applications.

Contents

Figures

Tables

Revision History

Revision 5.2 Revision Date: 13 September 2007
• Removed outdated Figure 4: *64-Pin Pb-Free LQFP Package: Pins Assignments* • Removed the ordering information. This information is now available from www.cortina-systems.com.

Revision 5.1 Revision Date: 23 July 2007
Added Section 10.0, *Package Specifications* back into Datasheet.

Revision 5.0 Revision Date: 2 July 2007
First release of this document from Cortina Systems, Inc.

Revision 004 Revision Date: 01 January 2007
Internal release. No changes.

Revision 003 Revision Date: 25 October 2005
Front page text changed.
Changed "PECL Interface" to "LVPECL Interface" in Figure 21 “Protocol Sublayers”.
Replaced text under Section 5.7.3.4, “Fiber PMD Sublayer”.
Modified first paragraph under Section 6.3, “The Fiber Interface”.
Modified text and added a new bullet in first and second set of bullets under Section 6.3, “The Fiber Interface”.
Replaced Figure 27 “Recommended LXT971A-to-3.3 V Fiber PHY Interface Circuitry”.
Replaced Figure 28 “Recommended LXT971A-to-5 V Fiber PHY Interface Circuitry”.
Added Section 10.1, *Top Label Markings*.
Modified Section 14.0, *Product Ordering Information*: added RoHS information to Table 140, *Product Ordering Information* and changed Figure 123, *Order Matrix for Cortina Systems® LXT971A Transceiver - Sample*.

Revision 002 Revision Date: 06 August 2002
Globally replaced “pseudo-PECL” with Low-Voltage PECL”, except when identified with 5 V.
Front Page: Changed “pseudo-ECL (PECL)” to “Low Voltage PECL (LVPECL). Added “JTAG Boundary Scan” to Product Features on front page.
Modified Figure 2 “LXT971A 64-Ball PBGA Assignments” (replaced TEST1 and TEST0 with GND).
Modified Figure 3 “LXT971A 64-Pin LQFP Assignments” (replaced TEST1 and TEST0 with GND).
Modified Table 1 “LQFP Numeric Pin List” (replaced TEST1 and TEST0 with GND).
Added note under Section 2.0, “Signal Descriptions”: “Intel recommends that all inputs and multi-function pins be tied to the inactive states and all outputs be left floating, if unused.”

Revision 002 **Revision Date: 06 August 2002**
Modified SD/$\overline{TP}$ description in Table 3 “LXT971A Network Interface Signal Descriptions”. Added Table note 2.
Modified Table 4 “LXT971A Miscellaneous Signal Descriptions”.
Modified Table 5 “LXT971A Power Supply Signal Descriptions”.
Added Table 8 “LXT971A Pin Types and Modes”.
Replaced second paragraph under Section 3.2.1.2, “Fiber Interface”.
Added Section 3.2.2.1, “Increased MII Drive Strength”.
Changed “Far-End Fault” title to ‘100BASE-FX Far-End Fault”. Modified first sentence under this heading.
Modified Figure 8 “Hardware Configuration Settings”.
Added paragraph after bullets under Section 3.6.7.2, “Test Loopback”.
Modified text under Section 3.7.3.4, “Fiber PMD Sublayer”.
Modified Table 13 “Supported JTAG Instructions”.
Modified Table 14 “Device ID Register”.
Added a new Section 4.3, “The Fiber Interface”.
Replaced Figure 25 “Recommended LXT971A-to-3.3 V Fiber PHY Interface Circuitry”.
Added Figure 26 “Recommended LXT971A-to-5 V Fiber PHY Interface Circuitry”.
Added Figure 27 “ON Semiconductor Triple PECL-to-LVPECL Logic Translator”.
Modified Table 17 “Absolute Maximum Ratings”.
Modified Table 18 “Operating Conditions”: Added Typ values to Vcc current.
Modified Table 20 “Digital I/O Characteristics - MII Pins”.
Modified Table 22 “I/O Characteristics - LED/CFG Pins”.
Added Table 23 “I/O Characteristics – SD/TP Pin”.
Added Table 28 “LXT971A Thermal Characteristics”.
Modified Table 33 “10BASE-T Receive Timing Parameters”
Modified Table 42 “register bit Map”. (Added Table 26 information).
Added Table 57 “Digital Configuration Register (Address 26)”.
Modified Table 58 “Transmit Control Register (Address 30)”.
Added Section 8.0, “Product Ordering Information”.

Revision 001 **Revision Date: 01 January 2001**
Clock Requirements: Modified language under Clock Requirements heading.
Table 21 I/O Characteristics REFCLK: Changed values for Input Clock Duty Cycle under Min from 40 to 35 and under Max from 60 to 65.

1.0 Introduction to This Document

This document includes information on the Cortina Systems® LXT971A Single-Port 10/100 Mbps PHY Transceiver (LXT971A PHY).

1.1 Document Overview

This document includes the following subjects:

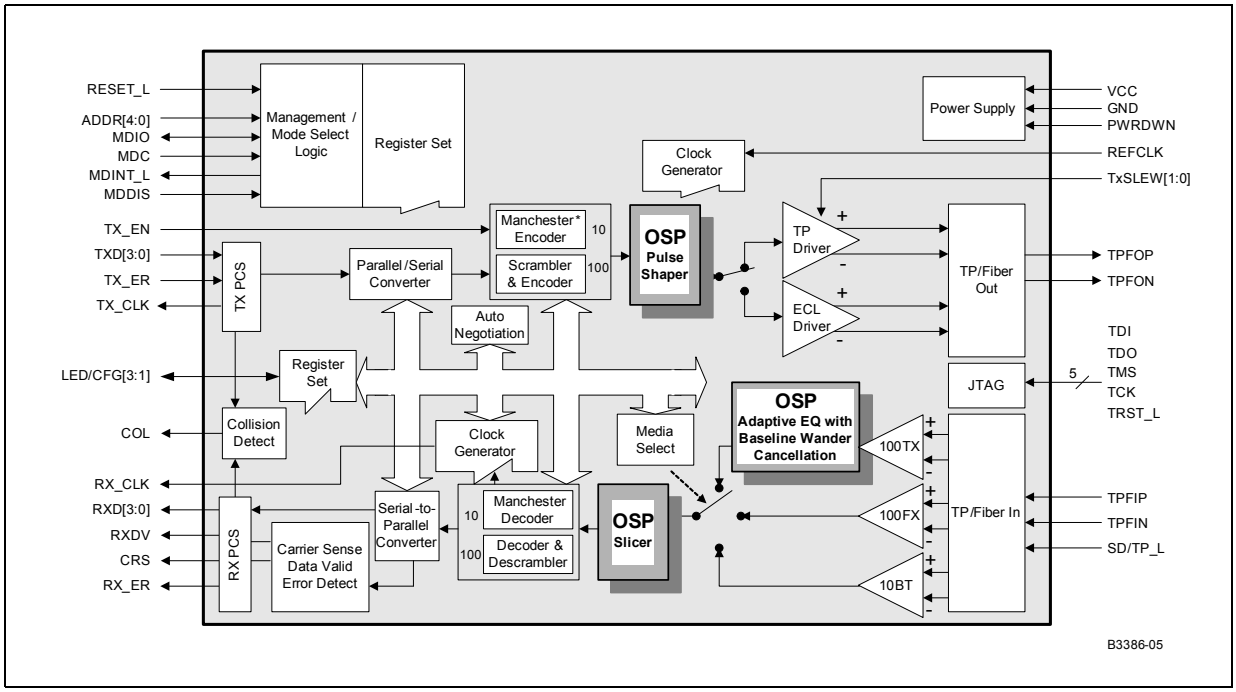
1.2 Related Documents

Table 1 Related Documents

Document Title	Document Number
Fiber Optic PHYs Connecting a PECL Interface Application Note	249015
Cortina Systems® 100BASE-FX Fiber Optic PHYs - Connecting a PECL/LVPECL Interface Application Note	250781
Cortina Systems® LXT971A, LXT972A, LXT972M Single-Port 10/100 Mbps PHY Specification Update	249354
Cortina Systems® LXT971A, LXT972A, and LXT972M 3.3 V PHY Design and Layout Guide - Application Note	249016
Magnetic Manufacturers for Networking Product Applications - Application Note	248991

2.0 Block Diagram

Figure 1 Block Diagram



3.0 Ball and Pin Assignments

See the following diagrams for signal placement:

- Figure 2, *64-Ball PBGA: Ball Assignments*, on page 13
- Figure 3, *64-Pin LQFP Package: Pins Assignments*, on page 14

See the following tables for signal lists:

- Table 3, *LQFP Numeric Pin List*, on page 14

Note: Table 2 list the signal type abbreviations used in the signal tables.

Table 2 PHY Signal Types

Abbreviation	Definition
AI	Analog Input
AO	Analog Output
I	Input
I/O	Input/Output
O	Output
OD	Open Drain

Figure 2 64-Ball PBGA: Ball Assignments

	1	2	3	4	5	6	7	8	
A	MDINT_L	CRS	TXD3	TXD0	RX_ER	VCCD	RX_DV	RXD0	A
B	REF CLK/XI	COL	TXD2	TX_EN	TX_ER	RX_ CLK	NC	RXD1	B
C	XO	RESET_L	GND	TXD1	TX_ CLK	GND	NC	RXD2	C
D	Tx SLEW0	Tx SLEW1	MDDIS	GND	VCCIO	RXD3	NC	MDIO	D
E	ADDR0	ADDR1	GND	GND	VCCIO	LED/ CFG1	MDC	PWR DWN	E
F	ADDR3	ADDR2	GND	GND	TDI	TMS	LED/ CFG2	LED/ CFG3	F
G	ADDR4	SD/ TP_L	VCCA	VCCA	TDO	TCK	GND	GND	G
H	RBIAS	TPFOP	TPFON	TPFIP	TPFIN	TRST_ L	SLEEP	PAUSE	H
	1	2	3	4	5	6	7	8	

B3477-01

Figure 3 64-Pin LQFP Package: Pins Assignments

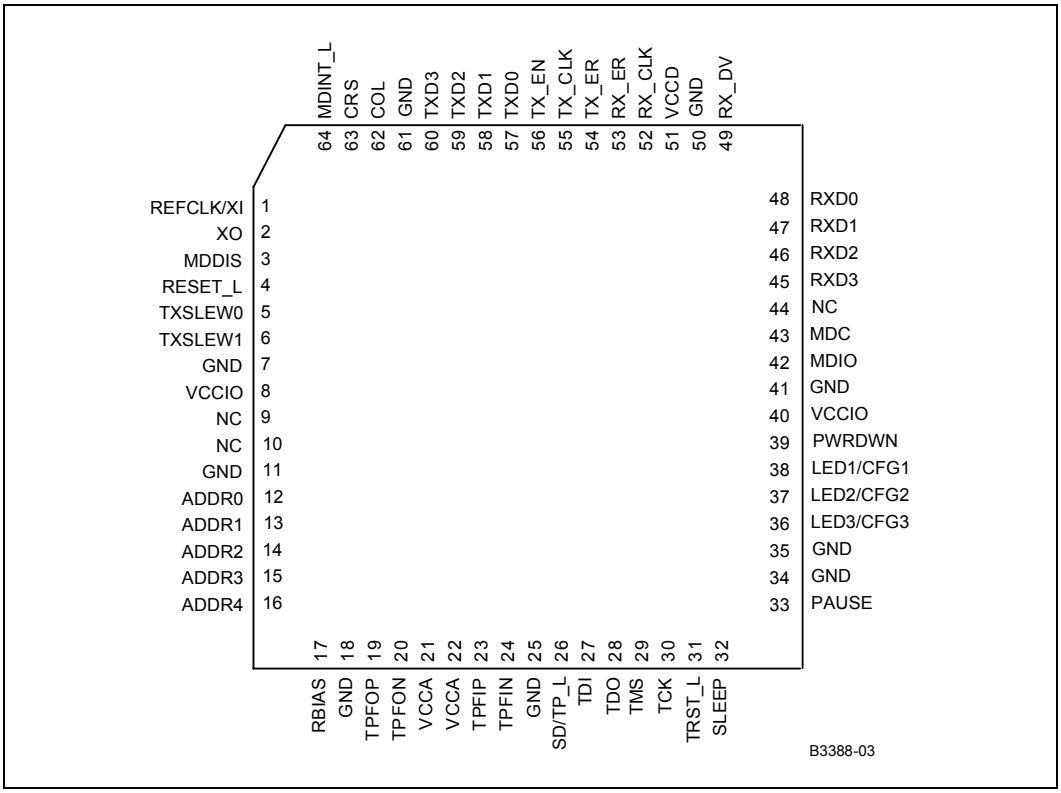


Table 3 LQFP Numeric Pin List (Sheet 1 of 3)

Pin	Symbol	Type
1	REFCLK/XI	I
2	XO	O
3	MDDIS	I
4	$\overline{\text{RESET\_L}}$	I
5	TxSLEW0	I
6	TxSLEW1	I
7	GND	–
8	VCCIO	–
9	NC	–
10	NC	–
11	GND	–
12	ADDR0	I
13	ADDR1	I
14	ADDR2	I
15	ADDR3	I

Table 3 LQFP Numeric Pin List (Sheet 2 of 3)

Pin	Symbol	Type
16	ADDR4	I
17	RBIAS	AI
18	GND	–
19	TPFOP	O
20	TPFON	O
21	VCCA	–
22	VCCA	–
23	TPFIP	I
24	TPFIN	I
25	GND	–
26	SD/TP_L	I
27	TDI	I
28	TDO	O
29	TMS	I
30	TCK	I
31	TRST_L	I
32	SLEEP	I
33	PAUSE	I
34	GND	–
35	GND	–
36	LED/CFG3	I/O
37	LED/CFG2	I/O
38	LED/CFG1	I/O
39	PWRDWN	I
40	VCCIO	–
41	GND	–
42	MDIO	I/O
43	MDC	I
44	NC	–
45	RXD3	O
46	RXD2	O
47	RXD1	O
48	RXD0	O
49	RX_DV	O
50	GND	–
51	VCCD	–
52	RX_CLK	O
53	RX_ER	O

Table 3 LQFP Numeric Pin List (Sheet 3 of 3)

Pin	Symbol	Type
54	TX_ER	I
55	TX_CLK	O
56	TX_EN	I
57	TXD0	I
58	TXD1	I
59	TXD2	I
60	TXD3	I
61	GND	–
62	COL	O
63	CRS	O
64	MDINT_L	OD

4.0 Signal Descriptions

Cortina recommends the following configurations for unused pins:

- **Unused inputs.** Configure all unused inputs and unused multi-function pins for inactive states.
- **Unused outputs.** Leave all unused outputs floating.
- **No connects.** Do not use pins designated as NC (no connect), and do not terminate them.

Note: Table 4 list the signal type abbreviations used in the signal tables.

Table 4 PHY Signal Types

Abbreviation	Definition
AI	Analog Input
AO	Analog Output
I	Input
I/O	Input/Output
O	Output
OD	Open Drain

Tables in this section include the following:

Table 5 MII Data Interface Signal Descriptions

PBGA Pin#	LQFP Pin#	Symbol	Type	Signal Description
A3 B3 C4 A4	60 59 58 57	TXD3 TXD2 TXD1 TXD0	I	**Transmit Data.** TXD is a group of parallel data signals that are driven by the MAC. TXD[3:0] transition synchronously with respect to TX_CLK. TXD[0] is the least-significant bit.
B4	56	TX_EN	I	**Transmit Enable.** The MAC asserts this signal when it drives valid data on TXD. This signal must be synchronized to TX_CLK.
C5	55	TX_CLK	O	**Transmit Clock.** TX_CLK is sourced by the PHY in both 10 and 100 Mbps operations. 2.5 MHz for 10 Mbps operation 25 MHz for 100 Mbps operation.
D6 C8 B8 A8	45 46 47 48	RXD3 RXD2 RXD1 RXD0	O	**Receive Data.** RXD is a group of parallel signals that transition synchronously with respect to RX_CLK. RXD[0] is the least-significant bit.
A7	49	RX_DV	O	**Receive Data Valid.** The PHY asserts this signal when it drives valid data on RXD. This output is synchronous to RX_CLK.
A5	53	RX_ER	O	**Receive Error.** Signals a receive error condition has occurred. This output is synchronous to RX_CLK.
B5	54	TX_ER	I	**Transmit Error.** Signals a transmit error condition. This signal must be synchronized to TX_CLK.
B6	52	RX_CLK	O	**Receive Clock.** 25 MHz for 100 Mbps operation. 2.5 MHz for 10 Mbps operation. For details, see Section 5.3.2, *Clock Requirements*, on page 30 in the Functional Description section.
B2	62	COL	O	**Collision Detected**. The PHY asserts this output when a collision is detected. This output remains High for the duration of the collision. This signal is asynchronous and is inactive during full- duplex operation.
A2	63	CRS	O	**Carrier Sense**. During half-duplex operation (register bit 0.8 = 0), the PHY asserts this output when either transmitting or receiving data packets. During full-duplex operation (register bit 0.8 = 1), CRS is asserted only during receive. CRS assertion is asynchronous with respect to RX_CLK. CRS is de-asserted on loss of carrier, synchronous to RX_CLK.

Table 6 MII Controller Interface Signal Descriptions

PBGA Pin#	LQFP Pin#	Symbol	Type	Signal Description
D3	3	MDDIS	I	**Management Data Disable**. When MDDIS is High, the MDIO is disabled from read and write operations. When MDDIS is Low at power-up or reset, the Hardware Control Interface pins control only the initial or “default” values of their respective register bits. After the power-up/reset cycle is complete, bit control reverts to the MDIO serial channel.
E7	43	MDC	I	**Management Data Clock**. Clock for the MDIO serial data channel. Maximum frequency is 8 MHz.
D8	42	MDIO	I/O	**Management Data Input/Output**. Bidirectional serial data channel for PHY/STA communication.
A1	64	MDINT_L	OD	**Management Data Interrupt**. When register bit 18.1 = 1, an active Low output on this pin indicates status change. Interrupt is cleared by reading Register 19.

Table 7 Network Interface Signal Descriptions

PBGA Pin#	LQFP Pin#	Symbol	Type	Signal Description
H2 H3	19 20	TPFOP TPFON	O	**Twisted-Pair/Fiber Outputs, Positive and Negative.** During 100BASE-TX or 10BASE-T operation, TPFOP/N pins drive IEEE 802.3 compliant pulses onto the line. During 100BASE-FX operation, TPFOP/N pins produce differential LVPECL outputs for fiber PHYs.
H4 H5	23 24	TPFIP TPFIN	I	**Twisted-Pair/Fiber Inputs, Positive and Negative.** During 100BASE-TX or 10BASE-T operation, TPFIP/N pins receive differential 100BASE-TX or 10BASE-T signals from the line. During 100BASE-FX operation, TPFIP/N pins receive differential LVPECL inputs from fiber PHYs.
G2	26	SD/TP_L	I	**Signal Detect** / Twisted Pair. SD/TP_L acts as a dual-function input, depending on theLXT971A PHY mode. **Normal, Reset, and Power-Up Operations.** “Normal” operation is operation other than reset or power-up. In either reset or power-up, SD/TP_L is used to select one of the two following media modes. • Twisted-pair mode - Connect SD/TP_L Low (register bit 16.0 = 0). • Fiber mode - Connect SD/TP_L High (register bit 16.0 = 1). **Twisted-Pair Mode.** For normal operation that uses the twisted-pair mode, connect SD/TP_L to ground. **Fiber Mode.** For normal operation that uses the fiber mode, SD/TP_L acts as the SD input from the fiber PHY.

Table 8 Standard Bus and Interface Signal Descriptions

PBGA Pin#	LQFP Pin#	Symbol	Type	Signal Description
G1 F1 F2 E2 E1	16 15 14 13 12	ADDR0	I I I I I	**Address**. Sets device address.

Table 9 Configuration and LED Driver Signal Descriptions (Sheet 1 of 2)

PBGA Pin#	LQFP Pin#	Symbol	Type	Signal Description
Note: Implement 10 kΩ pull-up/pull-down resistors if LEDs are not used in the design.				

Table 9 Configuration and LED Driver Signal Descriptions (Sheet 2 of 2)

<table>
<tr><th>PBGA Pin#</th><th>LQFP Pin#</th><th>Symbol</th><th>Type</th><th>Signal Description</th></tr>
<tr><td>D1
D2</td><td>5
6</td><td>TxSLEW0
TxSLEW1</td><td>I</td><td>Tx Output Slew Controls 0 and 1.
These pins select the TX output slew rate (rise and fall time) as follows:
<table><tr><th>TxSLEW1</th><th>TxSLEW0</th><th>Slew Rate (Rise and Fall Time)</th></tr><tr><td>0</td><td>0</td><td>3.0 ns</td></tr><tr><td>0</td><td>1</td><td>3.4 ns</td></tr><tr><td>1</td><td>0</td><td>3.9 ns</td></tr><tr><td>1</td><td>1</td><td>4.4 ns</td></tr></table></td></tr>
<tr><td>C2</td><td>4</td><td>$\overline{\text{RESET\_L}}$</td><td>I</td><td>Reset.
This active Low input is ORed with the control register Reset bit (register bit 0.15). The PHY reset cycle is extended to 258 µs (nominal) after reset is de-asserted.</td></tr>
<tr><td>H1</td><td>17</td><td>RBIAS</td><td>AI</td><td>Reference Current Bias.
This pin provides bias current for the internal circuitry. Must be tied to ground through a 22.1 kΩ, 1% resistor.</td></tr>
<tr><td>H8</td><td>33</td><td>PAUSE</td><td>I</td><td>Pause.
When set High, the PHY advertises Pause capabilities during auto-negotiation.</td></tr>
<tr><td>H7</td><td>32</td><td>SLEEP</td><td>I</td><td>Sleep.
When set High, this pin enables the PHY to go into a low-power sleep mode. The value of this pin can be overridden by register bit 16.6 when in managed mode.</td></tr>
<tr><td>E8</td><td>39</td><td>PWRDWN</td><td>I</td><td>Power Down.
When set High, this pin puts the PHY in a power-down mode.</td></tr>
<tr><td>B1
C1</td><td>1
2</td><td>REFCLK/XI
XO</td><td>I and
O</td><td>Reference Clock Input / Crystal Input and Crystal Output.
A 25 MHz crystal oscillator circuit can be connected across XI and XO. A clock can also be used at XI.
For clock requirements, see Section 5.3.2, Clock Requirements, on page 30 in the Functional Description section.</td></tr>
<tr><td>E6
F7
F8</td><td>38
37
36</td><td>LED/CFG1
LED/CFG2
LED/CFG3</td><td>I/O</td><td>LED Drivers 1-3.
These pins drive LED indicators. Each LED can display one of several available status conditions as selected by the LED Configuration Register. (For details, see Table 60, LED Configuration Register - Address 20, Hex 14, on page 91.)
Configuration Inputs 1-3.
These pins also provide initial configuration settings. (For details, see Table 13, Hardware Configuration Settings, on page 33.)</td></tr>
</table>

Table 10 Power, Ground, No-Connect Signal Descriptions

PBGA Pin#	LQFP Pin#	Symbol	Type	Signal Description
A6	51	VCCD	–	**Digital Power.** Requires a 3.3 V power supply.
D4, E3, E4, F3, F4, C6, C3, G7, G8	7, 11, 18, 25, 34, 35, 41, 50, 61	GND	–	**Ground.**
E5, D5	8, 40	VCCIO	–	**MII Power.** Requires either a 3.3 V or a 2.5 V supply. Must be supplied from the same source used to power the MAC on the other side of the MII.
G3, G4	21, 22	VCCA	–	**Analog Power.** Requires a 3.3 V power supply.
B7, C7 D7	9, 10, 44	NC	-	**No Connection**. These pins are not used and should not be terminated.

Table 11 JTAG Test Signal Descriptions

PBGA Pin#	LQFP Pin#	Symbol	Type	Signal Description
Note: These pins do not need to be terminated If a JTAG port is not used.				
F5	27	TDI	I	**Test Data Input**. Test data sampled with respect to the rising edge of TCK.
G5	28	TDO	O	**Test Data Output**. Test data driven with respect to the falling edge of TCK.
F6	29	TMS	I	**Test Mode Select**.
G6	30	TCK	I	**Test Clock**. Clock input for boundary scan.
H6	31	TRST_L	I	**Test Reset**. .

Table 12 Pin Types and Modes

Modes	RXD3:0	RX_DV	Tx/Rx CLKS Output	RX_ER Output	COL Output	CRS Output	TXD3:0 Input	TX_EN Input	TX_ER Input
HWReset	DL	DL	DH	DL	DL	DL	ID	ID	ID
SFTPWRDN	DL	DL	Active	DL	DL	DL	ID	ID	ID
HWPWRDN	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ	HZ
ISOLATE	HZ with ID	HZ with ID	HZ with ID	HZ with ID	HZ with ID	HZ with ID	ID	ID	ID
SLEEP	DL	DL	DL	DL	DL	DL	ID	ID	ID

- DH = Driven High (Logic 1)
- DL = Driven Low (Logic 0)
- HZ = High Impedance
- ID = Internal Pull-Down (Weak)

5.0 Functional Description

This chapter has the following sections:

5.1 Device Overview

The LXT971A PHY is a single-port Fast Ethernet 10/100 PHY that supports 10 Mbps and 100 Mbps networks. It complies with applicable requirements of IEEE 802.3. It directly drives either a 100BASE-TX line or a 10BASE-T line.

Note: The LXT971A PHY also supports 100BASE-FX operation through an LVPECL interface.

5.1.1 Comprehensive Functionality

The LXT971A PHY provides a standard Media Independent Interface (MII) for 10/100 MACs. The LXT971A PHY performs all functions of the Physical Coding Sublayer (PCS) and Physical Media Attachment (PMA) sublayer as defined in the IEEE 802.3 100BASE-X standard. It also performs all functions of the Physical Media Dependent (PMD) sublayer for 100BASE-TX connections.

The LXT971A PHY reads its configuration pins on power-up to check for forced operation settings.

If the LXT971A PHY is not set for forced operation, it uses auto-negotiation/parallel detection to automatically determine line operating conditions. If the PHY device on the other side of the link supports auto-negotiation, the LXT971A PHY auto-negotiates with it using Fast Link Pulse (FLP) Bursts. If the PHY partner does not support auto-negotiation, the LXT971A PHY automatically detects the presence of either link pulses (10 Mbps PHY) or Idle symbols (100 Mbps PHY) and sets its operating conditions accordingly.

The LXT971A PHY provides half-duplex and full-duplex operation at 100 Mbps and 10 Mbps.

5.1.2 Optimal Signal Processing Architecture

The LXT971A PHY incorporates high-efficiency Optimal Signal Processing (OSP) design techniques, which combine optimal properties of digital and analog signal processing.

The receiver utilizes decision feedback equalization to increase noise and cross-talk immunity by as much as 3 dB over an ideal all-analog equalizer. Using OSP mixed-signal processing techniques in the receive equalizer avoids the quantization noise and

calculation truncation errors found in traditional DSP-based receivers (typically complex DSP engines with A/D converters). This results in improved receiver noise and cross-talk performance.

The OSP signal processing scheme also requires substantially less computational logic than traditional DSP-based designs. This lowers power consumption and also reduces the logic switching noise generated by DSP engines. This logic switching noise can be a considerable source of EMI generated on the device's power supplies.

The OSP-based LXT971A PHY provides improved data recovery, EMI performance, and low power consumption.

5.2 Network Media / Protocol Support

This section includes the following:

- Section 5.2.1, *10/100 Network Interface*
- Section 5.2.2, *MII Data Interface*
- Section 5.2.3, *Configuration Management Interface*

The LXT971A PHY supports both 10BASE-T and 100BASE-TX Ethernet over twisted-pair or 100 Mbps Ethernet over fiber media (100BASE-FX).

5.2.1 10/100 Network Interface

The network interface port consists of five external pins (two differential signal pairs and a signal detect pin). The I/O pins are shared between twisted-pair (TP) and fiber. For specific pin assignments, see Section 4.0, *Signal Descriptions*, on page 17.

The LXT971A PHY output drivers can generate one of the following outputs:

- 100BASE-TX
- 10BASE-T
- 100BASE-FX

When not transmitting data, the LXT971A PHY generates IEEE 802.3-compliant link pulses or idle code. Depending on the mode selected, input signals are decoded as one of the following:

- 100BASE-TX
- 10BASE-T
- 100BASE-FX

Auto-negotiation/parallel detection or manual control is used to determine the speed of this interface.

5.2.1.1 Twisted-Pair Interface

The LXT971A PHY supports either 100BASE-TX or 10BASE-T connections over 100 Ω, Category 5, Unshielded Twisted Pair (UTP) cable. When operating at 100 Mbps, the LXT971A PHY continuously transmits and receives MLT3 symbols. When not transmitting data, the LXT971A PHY generates "IDLE" symbols.

During 10 Mbps operation, Xilink* Manchester-encoded data is exchanged. When no data is being exchanged, the line is left in an idle state. Link pulses are transmitted periodically to keep the link up.