Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Cortina Systems® LXT972M Single-Port 10/100 Mbps PHY Transceiver

Datasheet

The Cortina Systems® LXT972M Single-Port 10/100 Mbps PHY Transceiver (LXT972M PHY) directly supports both 100BASE-TX and 10BASE-T applications. The LXT972M PHY is IEEE compliant and provides a Media Independent Interface (MII) for easy attachment to 10/100 Media Access Controllers (MACs). The LXT972M PHY supports full-duplex operation at 10 Mbps and 100 Mbps. Operating conditions for the LXT972M PHY can be set using auto-negotiation, parallel detection, or manual control. The LXT972M PHY is fabricated with an advanced CMOS process and requires only a single 2.5/3.3 V power supply.

Applications

- Combination 10BASE-T/100BASE-TX Network Interface Cards (NICs)
- Wireless access points
- Network printers
- 10/100 Mbps PCMCIA cards
- Cable Modems and Set-Top Boxes

Product Features

- 3.3 V Operation
- Low power consumption (300 mW typical)
- 10BASE-T and 100BASE-TX using a single RJ-45 connection
- IEEE 802.3-compliant 10BASE-T or 100BASE-TX ports with integrated filters
- Auto-negotiation and parallel detection
- MII interface with extended register capability
- Robust baseline wander correction
- Carrier Sense Multiple Access / Collision Detection (CSMA/CD) or full-duplex operation
- JTAG boundary scan
- MDIO serial port or hardware pin configurable
- Integrated, programmable LED drivers
- 48-pin Low-profile Quad Flat Package

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH CORTINA SYSTEMS® PRODUCTS.

NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED BY THIS DOCUMENT.

EXCEPT AS PROVIDED IN CORTINA'S TERMS AND CONDITIONS OF SALE OF SUCH PRODUCTS, CORTINA ASSUMES NO LIABILITY WHATSOEVER, AND CORTINA DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO THE SALE AND/OR USE OF CORTINA PRODUCTS, INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

Cortina products are not intended for use in medical, life saving, life sustaining, critical control or safety systems, or in nuclear facility applications.

Contents

Figures

Tables

Revision History

Revision 5.2 Revision Date: 13 September 2007
• Removed outdated Figure 3: *64-Pin Pb-Free LQFP Package: Pins Assignments* • Removed the ordering information. This information is now available from www.cortina-systems.com.

Revision 5.1 Revision Date: 23 July 2007
Added Section 10.0, *Package Specifications* back into Datasheet.

Revision 5.0 Revision Date: 2 July 2007
First release of this document from Cortina Systems, Inc.

Revision 004 Revision Date: 01 January 2007
Internal release. No changes.

Revision 003 Revision Date: 14 July 2004
Figure 3, *LXT972M Transceiver Block Diagram* - Deleted ECL Driver from figure.
Section 5.1, *Device Overview* - Text changed.
Section 5.2.1.1, *Twisted-Pair Interface* - Added text on MDI crossover.
Section 5.2.1.5, *Remote Fault Detection and Reporting* - Text changed.
Section 5.3.2.1, *External Crystal/Oscillator* - Text changed.
Table 37, *Hardware Configuration Settings for Cortina Systems® LXT977 Transceiver* - Bit value for 0.8 changed.
Section 5.5.2, *Parallel Detection* - Text changed.
Section 5.6.2, *Transmit Enable* - Text changed.
Section 5.6.4, *Carrier Sense* - Text changed.
Section 5.7.3.1.1, *Preamble Handling* - Text changed.
Section 5.7.3.2.1, *Link* - Added text.
Section 5.7.3.2.2, *Link Failure Override* - Added text.
Section 5.7.3.2.4, *Receive Data Valid* - Text changed.
Section 5.7.3.3.2, *Polarity Correction* - Text changed.
Section 5.9.4, *LED Pulse Stretching* - Text changed.
Table 123, *Auto-Negotiation Next Page Transmit Register - Address 7, Hex 7* - Bits 7.10:0 and 7.13 changed.
Table 124, *Auto-Negotiation Link Partner Next Page Receive Register - Address 8, Hex 8* - Bits 8.18 and 8.10:0 changed.
Table 131, *LED Configuration Register - Address 20, Hex 14* - Bit 20.0 changed.

Revision 002 Revision Date: 14 July 2004
Text changed.
Figure 3, *LXT972M Transceiver Block Diagram* - Deleted ECL Driver from figure.
Section 5.1, *Device Overview* - Text changed.

Revision 002 **Revision Date: 14 July 2004**
Section 5.2.1.1, *Twisted-Pair Interface* - Added text on MDI crossover.
Section 5.2.1.5, *Comment: for LXT972A/972M/977-->Remote Fault Detection and Reporting* - Text changed.
Section 5.3.2.1, *External Crystal/Oscillator* - Text changed.
Table 37, *Hardware Configuration Settings for Cortina Systems® LXT977 Transceiver* - Bit value for 0.8 changed.
Section 5.5.2, *Parallel Detection* - Text changed.
Section 5.6.2, *Transmit Enable* - Text changed.
Section 5.6.4, *Carrier Sense* - Text changed.
Section 5.7.3.1.1, *Preamble Handling* - Text changed.
Section 5.7.3.2.1, *Link* - Added text.
Section 5.7.3.2.2, *Link Failure Override* - Added text.
Section 5.7.3.2.4, *Receive Data Valid* - Text changed.
Section 5.7.3.3.2, *Polarity Correction* - Text changed.
Section 5.9.4, *LED Pulse Stretching* - Text changed.
Table 123, *Auto-Negotiation Next Page Transmit Register - Address 7, Hex 7* - Bits 7.10:0 and 7.13 changed.
Table 124, *Auto-Negotiation Link Partner Next Page Receive Register - Address 8, Hex 8* - Bits 8.18 and 8.10:0 changed.
Table 131, *LED Configuration Register - Address 20, Hex 14* - Bit 20.0 changed.

Revision 001 **Revision Date: 02 July 2004**
Initial release of this document.

1.0 Introduction to This Document

This document includes information on the Cortina Systems® LXT972M Single-Port 10/100 Mbps PHY Transceiver (LXT972M PHY).

1.1 Document Overview

This document includes the following subjects:

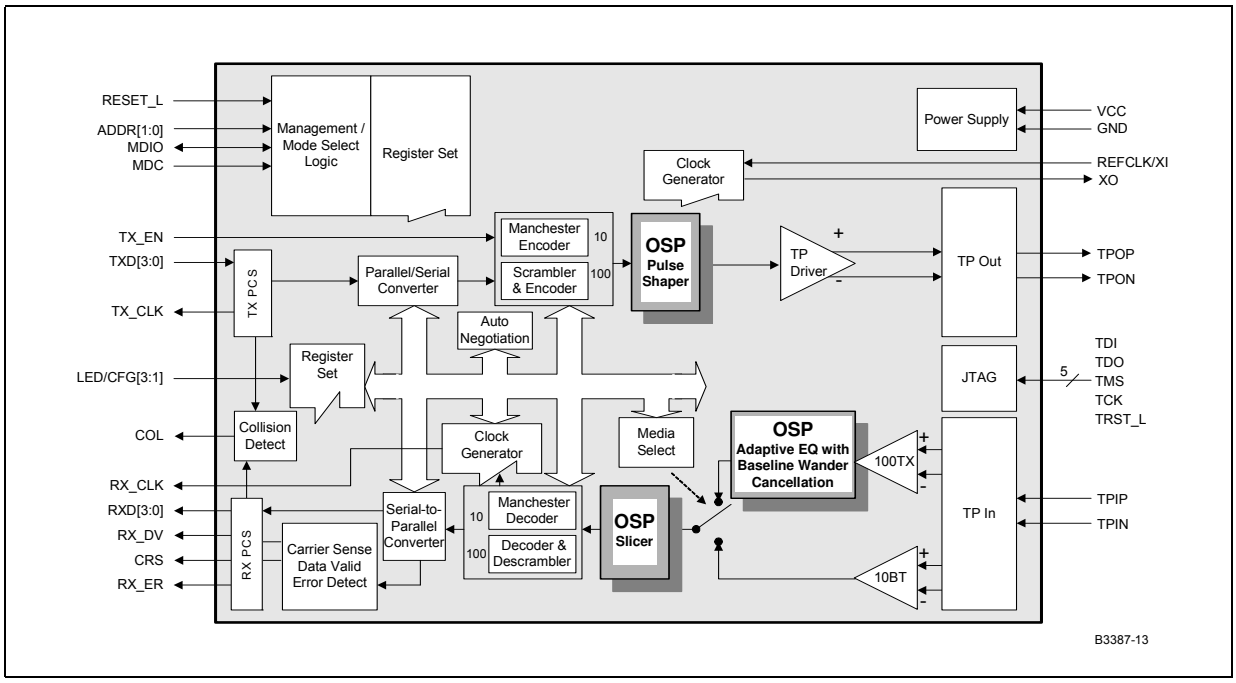
1.2 Related Documents

Table 1 Related Documents

Document Title	Document Number
Cortina Systems® LXT971A, LXT972A, LXT972M Single-Port 10/100 Mbps PHY Specification Update	249354
Cortina Systems® LXT971A, LXT972A, and LXT972M 3.3 V PHY Design and Layout Guide - Application Note	249016
Magnetic Manufacturers for Networking Product Applications - Application Note	248991

2.0 Block Diagram

Figure 1 Block Diagram



3.0 Ball and Pin Assignments

See the following diagrams for signal placement:

- Figure 2, *48-Pin LQFP Package: Pin Assignments*, on page 13

See the following tables for signal lists:

- Table 3, *LQFP Numeric Pin List*, on page 13

Note: Table 2 list the signal type abbreviations used in the signal tables.

Table 2 PHY Signal Types

Abbreviation	Definition
AI	Analog Input
AO	Analog Output
I	Input
I/O	Input/Output
O	Output
OD	Open Drain

Figure 2 48-Pin LQFP Package: Pin Assignments

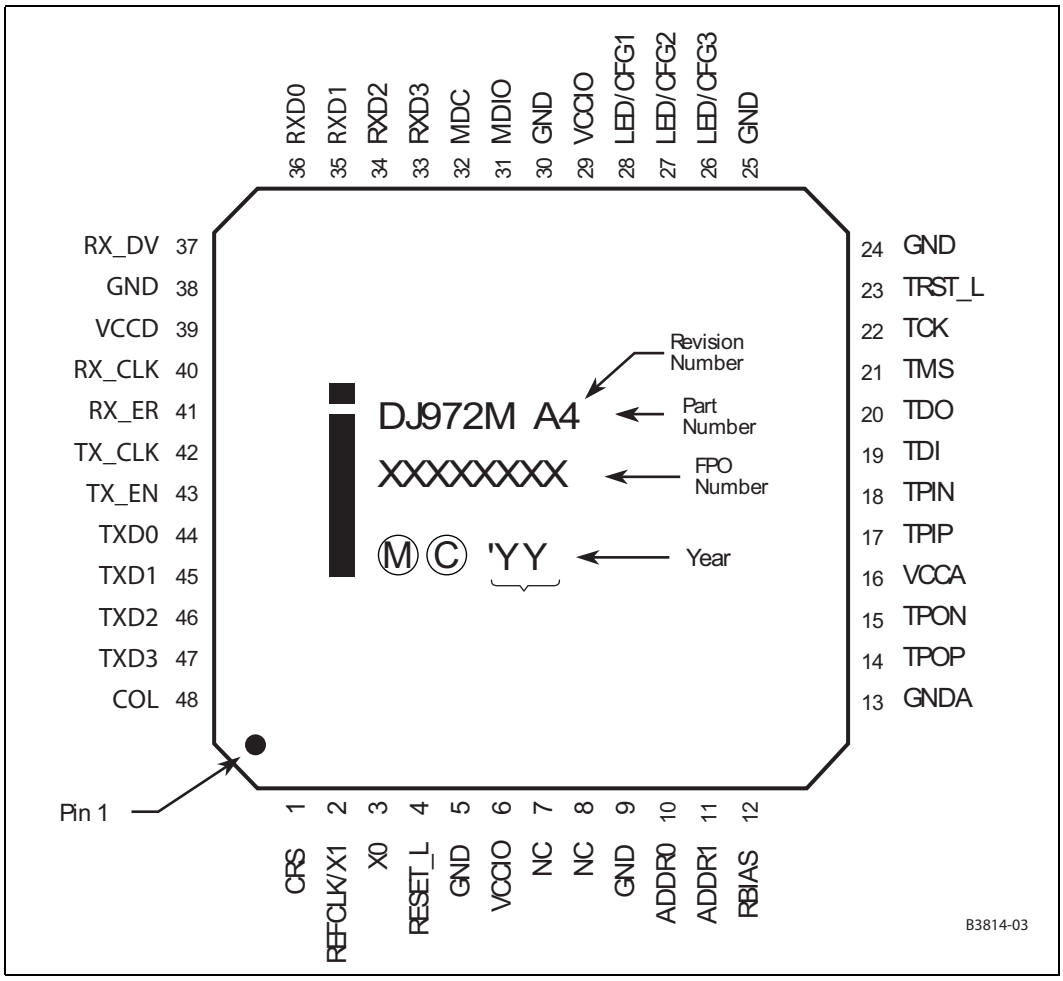


Table 3 LQFP Numeric Pin List (Sheet 1 of 2)

Pin	Symbol	Type
1	CRS	O
2	REFCLK/XI	AI
3	XO	AO
4	$\overline{\text{RESET\_L}}$	I
5	GND	–
6	VCCIO	–
7	NC	–
8	NC	–
9	GND	–
10	ADDR0	I

Table 3 LQFP Numeric Pin List (Sheet 2 of 2)

Pin	Symbol	Type
11	ADDR1	I
12	RBIAS	AI
13	GNDA	–
14	TPOP	AO
15	TPON	AO
16	VCCA	–
17	TPIP	AI
18	TPIN	AI
19	TDI	I
20	TDO	O
21	TMS	I
22	TCK	I
23	TRST_L	I
24	GND	–
25	GND	–
26	LED/CFG3	I/O
27	LED/CFG2	I/O
28	LED/CFG1	I/O
29	VCCIO	–
30	GND	–
31	MDIO	I/O
32	MDC	I
33	RXD3	O
34	RXD2	O
35	RXD1	O
36	RXD0	O
37	RX_DV	O
38	GND	–
39	VCCD	–
40	RX_CLK	O
41	RX_ER	O
42	TX_CLK	O
43	TX_EN	I
44	TXD0	I
45	TXD1	I
46	TXD2	I
47	TXD3	I
48	COL	O

4.0 Signal Descriptions

Cortina recommends the following configurations for unused pins:

- **Unused inputs.** Configure all unused inputs and unused multi-function pins for inactive states.
- **Unused outputs.** Leave all unused outputs floating.
- **No connects.** Do not use pins designated as NC (no connect), and do not terminate them.

Note: Table 4 list the signal type abbreviations used in the signal tables.

Table 4 PHY Signal Types

Abbreviation	Definition
AI	Analog Input
AO	Analog Output
I	Input
I/O	Input/Output
O	Output
OD	Open Drain

Tables in this section include the following:

Table 5 LXT972M: MII Data Interface Signal Descriptions

LQFP Pin#	Symbol	Type	Signal Description
47 46 45 44	TXD3 TXD2 TXD1 TXD0	I	**Transmit Data.** TXD is a group of parallel data signals that are driven by the MAC. TXD[3:0] transition synchronously with respect to TX_CLK. TXD[0] is the least-significant bit.
43	TX_EN	I	**Transmit Enable.** The MAC asserts this signal when it drives valid data on TXD. This signal must be synchronized to TX_CLK.
42	TX_CLK	O	**Transmit Clock.** TX_CLK is sourced by the PHY in both 10 and 100 Mbps operations. 2.5 MHz for 10 Mbps operation 25 MHz for 100 Mbps operation.
33 34 35 36	RXD3 RXD2 RXD1 RXD0	O	**Receive Data.** RXD is a group of parallel signals that transition synchronously with respect to RX_CLK. RXD[0] is the least-significant bit.
37	RX_DV	O	**Receive Data Valid.** The LXT972M PHY asserts this signal when it drives valid data on RXD. This output is synchronous to RX_CLK.
41	RX_ER	O	**Receive Error.** Signals a receive error condition has occurred. This output is synchronous to RX_CLK.
40	RX_CLK	O	**Receive Clock.** 25 MHz for 100 Mbps operation. 2.5 MHz for 10 Mbps operation. For details, see Section 5.3.2, *Clock Requirements*, on page 25 in the Functional Description section.
48	COL	O	**Collision Detected**. The LXT972M PHY asserts this output when a collision is detected. This output remains High for the duration of the collision. This signal is asynchronous and is inactive during full- duplex operation.
1	CRS	O	**Carrier Sense**. During half-duplex operation (register bit 0.8 = 0), the LXT972M PHY asserts this output when either transmitting or receiving data packets. During full-duplex operation (register bit 0.8 = 1), CRS is asserted only during receive. CRS assertion is asynchronous with respect to RX_CLK. CRS is de-asserted on loss of carrier, synchronous to RX_CLK.

Table 6 LXT972M: MII Controller Interface Signal Descriptions

LQFP Pin#	Symbol	Type	Signal Description
32	MDC	I	**Management Data Clock**. Clock for the MDIO serial data channel. Maximum frequency is 8 MHz.
31	MDIO	I/O	**Management Data Input/Output**. Bidirectional serial data channel for PHY/STA communication.

Table 7 LXT972M: Network Interface Signal Descriptions

LQFP Pin#	Symbol	Type	Signal Description
14 15	TPOP TPON	AO	**Twisted-Pair Outputs, Positive and Negative.** During 100BASE-TX or 10BASE-T operation, TPOP/N pins drive IEEE 802.3 compliant pulses onto the line.
17 18	TPIP TPIN	AI	**Twisted-Pair Inputs, Positive and Negative.** During 100BASE-TX or 10BASE-T operation, TPIP/N pins receive differential 100BASE-TX or 10BASE-T signals from the line.

Table 8 LXT972M: Standard Bus and Interface Signal Descriptions

LQFP Pin#	Symbol	Type	Signal Description
10 11	ADDR0 ADDR1	I	**Address**. Set device address.

Table 9 LXT972M: Configuration and LED Driver Signal Descriptions (Sheet 1 of 2)

LQFP Pin#	Symbol	Type	Signal Description
Note: Implement 10 kΩ pull-up/pull-down resistors if LEDs are not used in the design.			
4	$\overline{\text{RESET\_L}}$	I	**Reset**. This active Low input is Read with the control register Reset bit (register bit 0.15). The LXT972M PHY reset cycle is extended to 258 µs (nominal) after reset is de-asserted.

Table 9 LXT972M: Configuration and LED Driver Signal Descriptions (Sheet 2 of 2)

LQFP Pin#	Symbol	Type	Signal Description
12	RBIAS	AI	**Reference Current Bias**. This pin provides bias current for the internal circuitry. Must be tied to ground through a 22.1 kΩ, 1% resistor.
2 3	REFCLK/XI XO	AI and AO	**Reference Clock Input / Crystal Input and Crystal Output**. A 25 MHz crystal oscillator circuit can be connected across XI and XO. A clock can also be used at XI. Refer to Section 5.3.2, *Clock Requirements*, on page 25 in the Functional Description section.
26 27 28	LED/CFG3 LED/CFG2 LEDCFG1	I/O	**LED Drivers 1-3.** These pins drive LED indicators. Each LED can display one of several available status conditions as selected by the LED Configuration Register. (For details, see Table 54, *LED Configuration Register - Address 20, Hex 14*, on page 77.) **Configuration Inputs 1-3.** These pins also provide initial configuration settings. (For details, see Table 14, *Hardware Configuration Settings*, on page 28.)

Table 10 LXT972M: Power, Ground, No-Connect Signal Descriptions

LQFP Pin#	Symbol	Type	Signal Description
13	GNDA	–	**Analog Ground.**
5, 9, 24, 25, 30, 38	GND	–	**Ground Input/Output.** Ground return for digital I/O circuits (VCCIO).
6, 29	VCCIO	–	**MII Power.** Requires either a 3.3 V or a 2.5 V supply. Must be supplied from the same source used to power the MAC on the other side of the MII. VCCIO is 3.3 V.
16	VCCA	–	**Analog Power.** Requires a 3.3 V power supply.
39	VCCD	–	**Digital Power.** Requires a 3.3 V power supply.
7, 8	NC	–	**No Connection**. These pins are not used and must not be terminated.

Table 11 LXT972M: JTAG Test Signal Descriptions (Sheet 1 of 2)

LQFP Pin#	Symbol	Type	Signal Description
Note: These pins do not need to be terminated If a JTAG port is not used.			
19	TDI	I	**Test Data Input**. Test data sampled with respect to the rising edge of TCK.
20	TDO	O	**Test Data Output**. Test data driven with respect to the falling edge of TCK.

Table 11 LXT972M: JTAG Test Signal Descriptions (Sheet 2 of 2)

LQFP Pin#	Symbol	Type	Signal Description
21	TMS	I	**Test Mode Select**.
22	TCK	I	**Test Clock**. Clock input for boundary scan.
23	TRST_L	I	**Test Reset**. This active-low test reset input is sourced by ATE.

Table 12 LXT972M:Pin Types and Modes

Modes	RXD3:0	RX_DV	Tx/Rx CLKS Output	RX_ER Output	COL Output	CRS Output	TXD3:0 Input	TX_EN Input
HWReset	DL	DL	DH	DL	DL	DL	ID	ID
SFTPWRDN	DL	DL	Active	DL	DL	DL	ID	ID
ISOLATE	HZ with ID	HZ with ID	HZ with ID	HZ with ID	HZ with ID	HZ with ID	ID	ID

- DH = Driven High (Logic 1)
- DL = Driven Low (Logic 0)
- HZ = High Impedance
- ID = Internal Pull-Down (Weak)

5.0 Functional Description

This chapter has the following sections:

5.1 Device Overview

The LXT972M PHY is a single-port Fast Ethernet 10/100 PHY that supports 10 Mbps and 100 Mbps networks. It complies with applicable requirements of IEEE 802.3. It directly drives either a 100BASE-TX line or a 10BASE-T line.

5.1.1 Comprehensive Functionality

The LXT972M PHY provides a standard Media Independent Interface (MII) for 10/100 MACs. The LXT972M PHY performs all functions of the Physical Coding Sublayer (PCS) and Physical Media Attachment (PMA) sublayer as defined in the IEEE 802.3 100BASE-X standard. It also performs all functions of the Physical Media Dependent (PMD) sublayer for 100BASE-TX connections.

If the LXT972M PHY is not set for forced operation, it uses auto-negotiation/parallel detection to automatically determine line operating conditions. If the PHY device on the other side of the link supports auto-negotiation, the LXT972M PHY auto-negotiates with it using Fast Link Pulse (FLP) Bursts. If the PHY partner does not support auto-negotiation, the LXT972M PHY automatically detects the presence of either link pulses (10 Mbps PHY) or Idle symbols (100 Mbps PHY) and sets its operating conditions accordingly.

The LXT972M PHY provides half-duplex and full-duplex operation at 100 Mbps and 10 Mbps.

5.1.2 Optimal Signal Processing Architecture

The LXT972M PHY incorporates high-efficiency Optimal Signal Processing (OSP) design techniques, which combine optimal properties of digital and analog signal processing.

The receiver utilizes decision feedback equalization to increase noise and cross-talk immunity by as much as 3 dB over an ideal all-analog equalizer. Using OSP mixed-signal processing techniques in the receive equalizer avoids the quantization noise and calculation truncation errors found in traditional DSP-based receivers (typically complex DSP engines with A/D converters). This results in improved receiver noise and cross-talk performance.

The OSP signal processing scheme also requires substantially less computational logic than traditional DSP-based designs. This lowers power consumption and also reduces the logic switching noise generated by DSP engines. This logic switching noise can be a considerable source of EMI generated on the device's power supplies.

The OSP-based LXT972M PHY provides improved data recovery, EMI performance, and low power consumption.

5.2 Network Media / Protocol Support

This section includes the following:

- Section 5.2.1, *10/100 Network Interface*
- Section 5.2.2, *MII Data Interface*
- Section 5.2.3, *Configuration Management Interface*

The LXT972M PHY supports both 10BASE-T and 100BASE-TX Ethernet over twisted-pair

5.2.1 10/100 Network Interface

The network interface port consists of two differential signal pairs. For specific pin assignments, see Section 4.0, *Signal Descriptions*, on page 16.

The LXT972M PHY output drivers can generate one of the following outputs:

- 100BASE-TX
- 10BASE-T

When not transmitting data, the LXT972M PHY generates IEEE 802.3-compliant link pulses or idle code. Depending on the mode selected, input signals are decoded as one of the following:

- 100BASE-TX
- 10BASE-T

Auto-negotiation/parallel detection or manual control is used to determine the speed of this interface.

5.2.1.1 Twisted-Pair Interface

The LXT972M PHY supports either 100BASE-TX or 10BASE-T connections over 100 Ω, Category 5, Unshielded Twisted Pair (UTP) cable. When operating at 100 Mbps, the LXT972M PHY continuously transmits and receives MLT3 symbols. When not transmitting data, the LXT972M PHY generates "IDLE" symbols.

During 10 Mbps operation, Xilink* Manchester-encoded data is exchanged. When no data is being exchanged, the line is left in an idle state. Link pulses are transmitted periodically to keep the link up.

Only a transformer, RJ-45 connector, load resistor and bypass capacitors are required to complete this interface. On the transmit side, the LXT972M PHY has an active internal termination and does not require external termination resistors. Cortina's waveshaping technology shapes the outgoing signal to help reduce the need for external EMI filters. Four slew rate settings allow the designer to match the output waveform to the magnetic

characteristics. On the receive side, the internal impedance is high enough that it has no practical effect on the external termination circuit. (For the slew rate settings, see Table 56, *Transmit Control Register - Address 30, Hex 1E*, on page 79.)

Note: The MDIX crossover (MDIX) is supported by board design.

5.2.1.2 Remote Fault Detection and Reporting

The LXT972M PHY supports the remote fault detection and reporting mechanisms. “Remote Fault” refers to a MAC-to-MAC communication function that is transparent to PHY layer devices. It is used only during auto-negotiation, and is applicable only to twisted-pair links.

Remote Fault Detection. register bit 4.13 in the Auto-Negotiation Advertisement Register is reserved for Remote Fault indications. It is typically used when re-starting the auto-negotiation sequence to indicate to the link partner that the link is down because the advertising device detected a local fault.

When the LXT972M PHY receives a Remote Fault indication from its partner during auto-negotiation, the following occurs:

- register bit 5.13 in the Link Partner Base Page Ability Register is set.
- Remote Fault register bit 1.4 in the MII Status Register is set to pass this information to the local controller.

5.2.2 MII Data Interface

The LXT972M PHY supports a standard Media Independent Interface (MII). The MII consists of a data interface and a management interface. The MII Data Interface passes data between the LXT972M PHY and a Media Access Controller (MAC). Separate parallel buses are provided for transmit and receive. This interface operates at either 10 Mbps or 100 Mbps. The speed is set automatically, once the operating conditions of the network link have been determined. For details, see Section 5.6, *MII Operation*, on page 30.

Increased MII Drive Strength. A higher Media Independent Interface (MII) drive strength may be desired in some designs to drive signals over longer PCB trace lengths, or over high-capacitive loads, through multiple vias, or through a connector. The MII drive strength in the LXT972M PHY can be increased by setting register bit 26.11 through software control. Setting register bit 26.11 = 1 through the MDC/MDIO interface sets the MII pins (RXD[3:0], RX_DV, RX_CLK, RX_ER, COL, CRS, and TX_CLK) to a higher drive strength.

5.2.3 Configuration Management Interface

The LXT972M PHY provides both an MDIO interface and a reduced hardware control interface for device configuration and management.

5.2.3.1 MDIO Management Interface

MDIO management interface topics include the following:

- Section 5.2.3.1.1, *MDIO Addressing*
- Section 5.2.3.1.2, *MDIO Frame Structure*

The LXT972M PHY supports the IEEE 802.3 MII Management Interface also known as the Management Data Input/Output (MDIO) Interface. This interface allows upper-layer devices to monitor and control the state of the LXT972M PHY. The MDIO interface consists of a physical connection, a specific protocol that runs across the connection, and an internal set of addressable registers.

Some registers are required and their functions are defined by the IEEE 802.3 standard. The LXT972M PHY also supports additional registers for expanded functionality. The LXT972M PHY supports multiple internal registers, each of which is 16 bits wide. Specific register bits are referenced using an “X.Y” notation, where X is the register number (0-31) and Y is the bit number (0-15).

5.2.3.1.1 MDIO Addressing

The MDIO addressing protocol allows a controller to communicate with multiple PHYs. Pins ADDR[1:0] determine the PHY device address that is selected (see Table 13).

Table 13 PHY Device Address Selections

ADDR1 (Pin 11)	ADDR0 (Pin 10)	PHY Device Address Selected
0	0	0
0	1	1
1	0	28
1	1	29

5.2.3.1.2 MDIO Frame Structure

The physical interface consists of a data line (MDIO) and clock line (MDC). The frame structure is shown in Figure 3 and Figure 4 (Read and Write).

MDIO Interface timing is given in Section 7.0, *Electrical Specifications*.

Figure 3 Management Interface Read Frame Structure

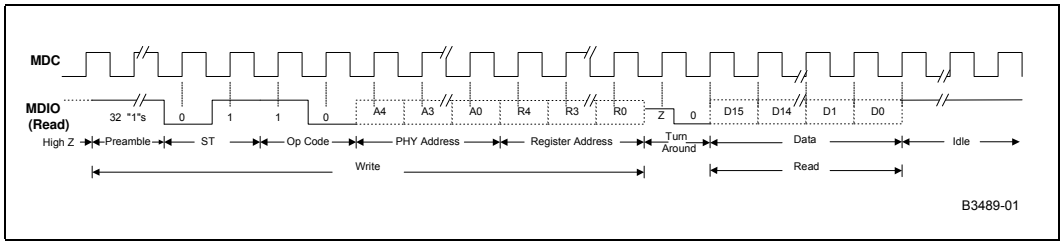
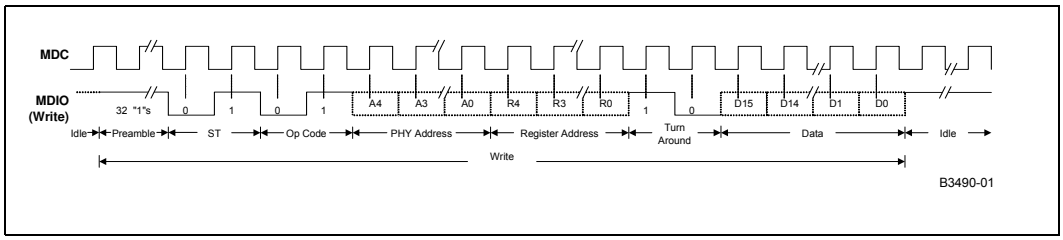


Figure 4 Management Interface Write Frame Structure



5.2.3.2 Hardware Control Interface

The LXT972M PHY provides a Hardware Control Interface for applications where the MDIO is not desired. The Hardware Control Interface uses the hardware configuration pins to set device configuration. For details, see Section 5.4.4, *Hardware Configuration Settings*, on page 28.

5.3 Operating Requirements

5.3.1 Power Requirements

The LXT972M PHY requires three power supply inputs:

- VCCA
- VCCD
- VCCIO

The digital and analog circuits require 3.3 V supplies (VCCA and VCCD). These inputs may be supplied from a single source. Each supply input must be de-coupled to ground.

An additional supply may be used for the MII (VCCIO). The supply may be either 2.5 V or 3.3 V. Also, the inputs on the MII interface are tolerant to 5 V signals from the controller on the other side of the MII interface. For MII I/O characteristics, see Table 24, *Digital I/O Characteristics*[1] *- MII Pins*, on page 52.

Notes:

1. Bring up power supplies as close to the same time as possible.
2. As a matter of good practice, keep power supplies as clean as possible.

5.3.2 Clock Requirements

5.3.2.1 External Crystal/Oscillator

The LXT972M PHY requires a reference clock input that is used to generate transmit signals and recover receive signals. It may be provided by either of two methods: by connecting a crystal across the oscillator pins (XI and XO) with load capacitors, or by connecting an external clock source to pin XI.

The connection of a clock source to the XI pin requires the XO pin to be left open. To minimize transmit jitter, Cortina recommends a crystal-based clock instead of a derived clock (that is, a PLL-based clock).

A crystal is typically used in NIC applications. An external 25 MHz clock source, rather than a crystal, is frequently used in switch applications. For clock timing requirements, see Table 25, *I/O Characteristics - REFCLK/XI and XO Pins*, on page 53.

5.3.2.2 MDIO Clock

The MII management channel (MDIO) also requires an external clock. The managed data clock (MDC) speed is a maximum of 8 MHz.

5.4 Initialization

This section includes the following topics:

- Section 5.4.1, *MDIO Control Mode and Hardware Control Mode*