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General Purpose Low-Power Audio DSP

DESCRIPTION

WM0011 Audio DSP provides Wolfson HD audio quality, with a power-budget targeted at handheld battery-powered audio devices.

WM0011 combines the advanced Tensilica HiFi EP™ audio DSP with an I/O and peripheral set optimized for flexible integration into smartphones, tablets and other portable consumer electronics devices. WM0011 is ideal for extremely power-efficient implementations of advanced voice enhancement, telephony noise reduction, voice and music CODECs and general audio enhancement.

A very wide range of audio CODECs, voice CODECs and third-party algorithms from such companies as Waves Audio, SRS Labs and Dolby are available, providing a rich portfolio of audio-processing options that can be integrated into a device with no additional software development.

WM0011 comes in a space-saving 3x3mm 49-ball W-CSP package with 0.4mm pitch.

APPLICATIONS

- Wireless audio devices – headsets, microphones, speakerphones
- Portable media devices
- Automotive
- General purpose digital signal processor for consumer audio applications
- Smartphones

FEATURES

- 260MHz Tensilica HiFi EP™ 24-bit audio digital signal processor
 - C-programmable with advanced debugging and profiling tool set
 - 256kB local RAM memory
 - 36kB Instruction / Data cache memory
 - 384kB general-purpose system RAM
 - Flexible boot options with 32kB boot ROM
 - 32 Channel DMA
 - XTAL or CMOS clock input
 - Low-power programmable PLL
- Security
 - Support for HW Authentication
 - Random Number Generator (RNG) to assist security algorithms
- Peripherals
 - SPI Master / Slave interface
 - 3 x multi-channel AIF interfaces, including I²S and TDM
 - UART
 - I²C Master
 - I²C Slave
 - 3 x 32-bit general-purpose timer modules
 - Watchdog timer
 - On-chip JTAG debug unit and trace buffer
 - GPIO
- Software-defined standby modes for extended battery life

BLOCK DIAGRAM

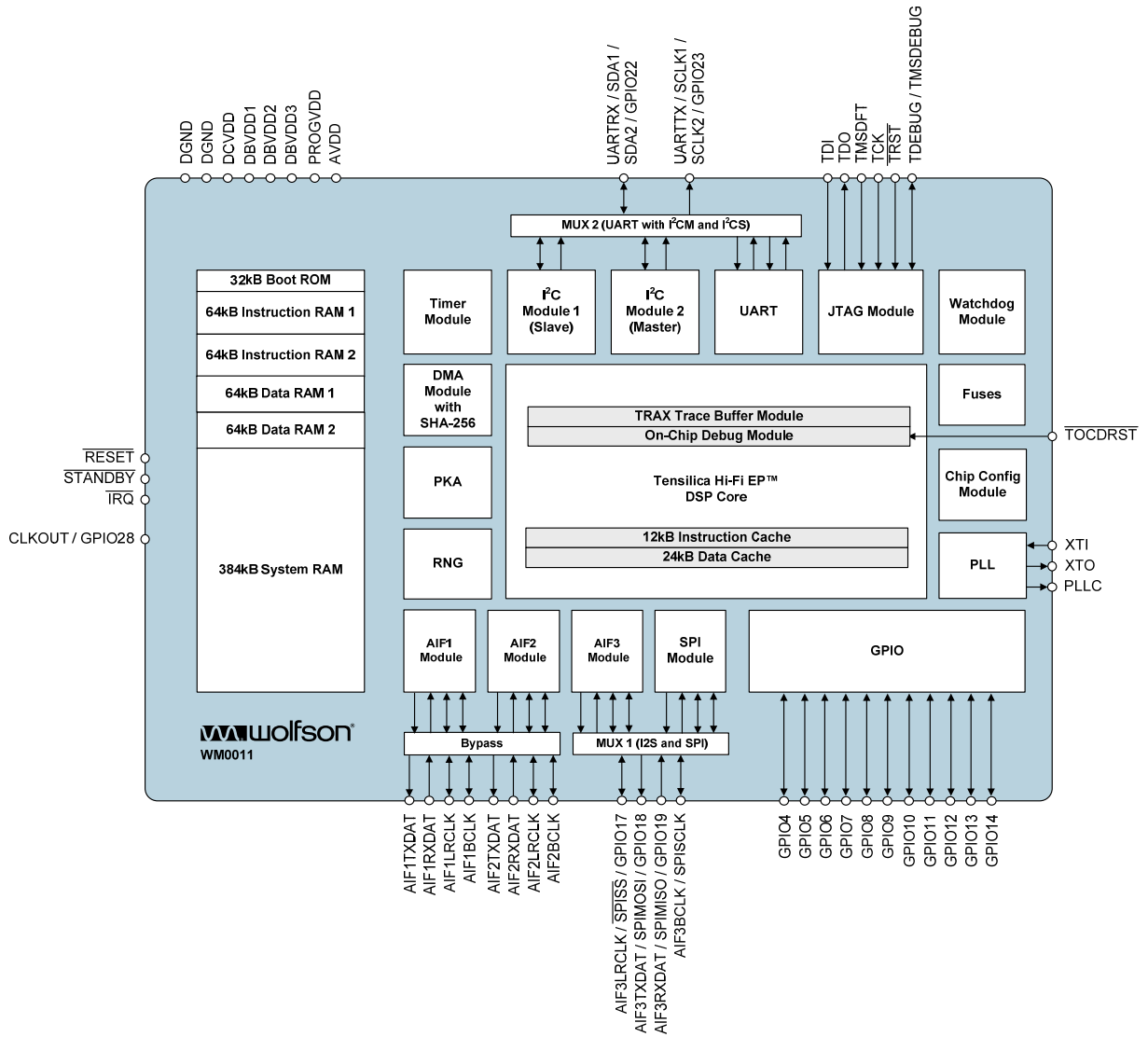


TABLE OF CONTENTS

DESCRIPTION	1
APPLICATIONS	1
FEATURES	1
BLOCK DIAGRAM	2
TABLE OF CONTENTS	3
PIN CONFIGURATION	9
ORDERING INFORMATION	10
PIN DESCRIPTION	10
ABSOLUTE MAXIMUM RATINGS	13
RECOMMENDED OPERATING CONDITIONS	13
THERMAL PERFORMANCE	14
ELECTRICAL CHARACTERISTICS	15
TYPICAL POWER CONSUMPTION	16
SIGNAL TIMING REQUIREMENTS	17
SYSTEM CLOCK & PHASE LOCKED LOOP (PLL).....	17
AUDIO INTERFACE (AIF) TIMING	18
DIGITAL AUDIO INTERFACE – MASTER MODE.....	18
DIGITAL AUDIO INTERFACE – SLAVE MODE	19
SPI INTERFACE TIMING.....	20
SPI INTERFACE – MASTER MODE	20
SPI INTERFACE – SLAVE MODE	21
CONTROL INTERFACE (I2C) TIMING.....	22
DEVICE DESCRIPTION	23
INTRODUCTION.....	23
BLOCK DIAGRAM	23
DESCRIPTION OF MODULES	24
BOOT ROM.....	24
TIGHTLY-COUPLED MEMORY (TCM) RAM.....	24
MULTI-PURPOSE RAM	24
TENSILICA HIFI EP™ DSP CORE.....	24
TIMER MODULE	25
WATCHDOG MODULE	25
GPIO MODULE	25
IRQC MODULE	25
I ² C MASTER AND SLAVE MODULE.....	26
PLL MODULE	26
AUDIO INTERFACE (AIF) MODULES.....	26
SPI MODULE.....	26
FUSE MODULE.....	27
DMA MODULE	27
TRAX TRACE BUFFER MODULE	27
JTAG MODULE	28
ON-CHIP DEBUG MODULE.....	28

POWER-ON AND RESET CONTROL	29
POWER ON RESET	29
HARDWARE RESET	30
WARM RESET	30
SOFTWARE RESET	31
JTAG RESET	31
BOOT SEQUENCE CONTROL	32
SOFTWARE / CONFIGURATION DOWNLOAD.....	32
CODE PACKET FORMAT	33
CODE HEADER DOWNLOAD	33
CODE DATA DOWNLOAD.....	34
PLL CONFIGURATION DOWNLOAD	34
BOOT STATUS AND ERROR REPORTING	35
BOOT SEQUENCE FLOW DIAGRAMS	36
INTERRUPTS	40
MEMORY MAP	42
CLOCKING	43
CRYSTAL OSCILLATOR	45
PHASE LOCKED LOOP (PLL).....	46
CORE DEVICE PERIPHERALS	48
CCM - CHIP CONFIGURATION MODULE	48
CCM FEATURES	48
CLOCKING CONTROL.....	49
RESET CONTROL	49
INTERFACE PORT SELECTION	50
GPIO / STANDBY DE-BOUNCE	50
I/O BUFFER CONTROL	50
SLEEP / WAKE-UP CONTROL	50
AIF BYPASS MODE	51
CCM REGISTER MAP.....	53
CCM_CONTROL – GENERAL CONTROL REGISTER	54
CCM_STATUS – GENERAL STATUS REGISTER	55
CCM_GPIO_SEL – PORT SELECT REGISTER.....	56
CCM_CLK_CTRL1 – CLOCK CONTROL 1 REGISTER	58
CCM_CLK_CTRL2 – CLOCK CONTROL 2 REGISTER	60
CCM_CLK_CTRL3 – CLOCK CONTROL 3 REGISTER	62
CCM_PLL_LOCK_CTRL – PLL LOCK DETECT CONTROL REGISTER	63
CCM_CLK_ENA – CLOCK ENABLE REGISTER.....	66
CCM_SOFTTRST – SOFTWARE RESET REGISTER.....	68
CCM_WKUP_CTRL – CHIP WAKEUP CONTROL REGISTER.....	69
CCM_DB_STBY – STANDBY DE-BOUNCE CONTROL REGISTER	70
CCM_DB_GINT1 – GINT1 DE-BOUNCE CONTROL REGISTER	71
CCM_DB_GINT2 – GINT2 DE-BOUNCE CONTROL REGISTER	71
CCM_SCRATCH1 – SCRATCHPAD 1 REGISTER	72
CCM_SCRATCH2 – SCRATCHPAD 2 REGISTER	72
CCM_SCRATCH3 – SCRATCHPAD 3 REGISTER	72
CCM_SCRATCH4 – SCRATCHPAD 4 REGISTER	73
CCM_IOCTRL1 – I/O CONTROL 1 REGISTER	73
CCM_IOCTRL2 – I/O CONTROL 2 REGISTER	74
CCM_IOCTRL3 – I/O CONTROL 3 REGISTER	77
CCM_IOCTRL4 – I/O CONTROL 4 REGISTER	79
CCM_IOCTRL5 – I/O CONTROL 5 REGISTER	80
CCM_IOCTRL6 – I/O CONTROL 6 REGISTER	81

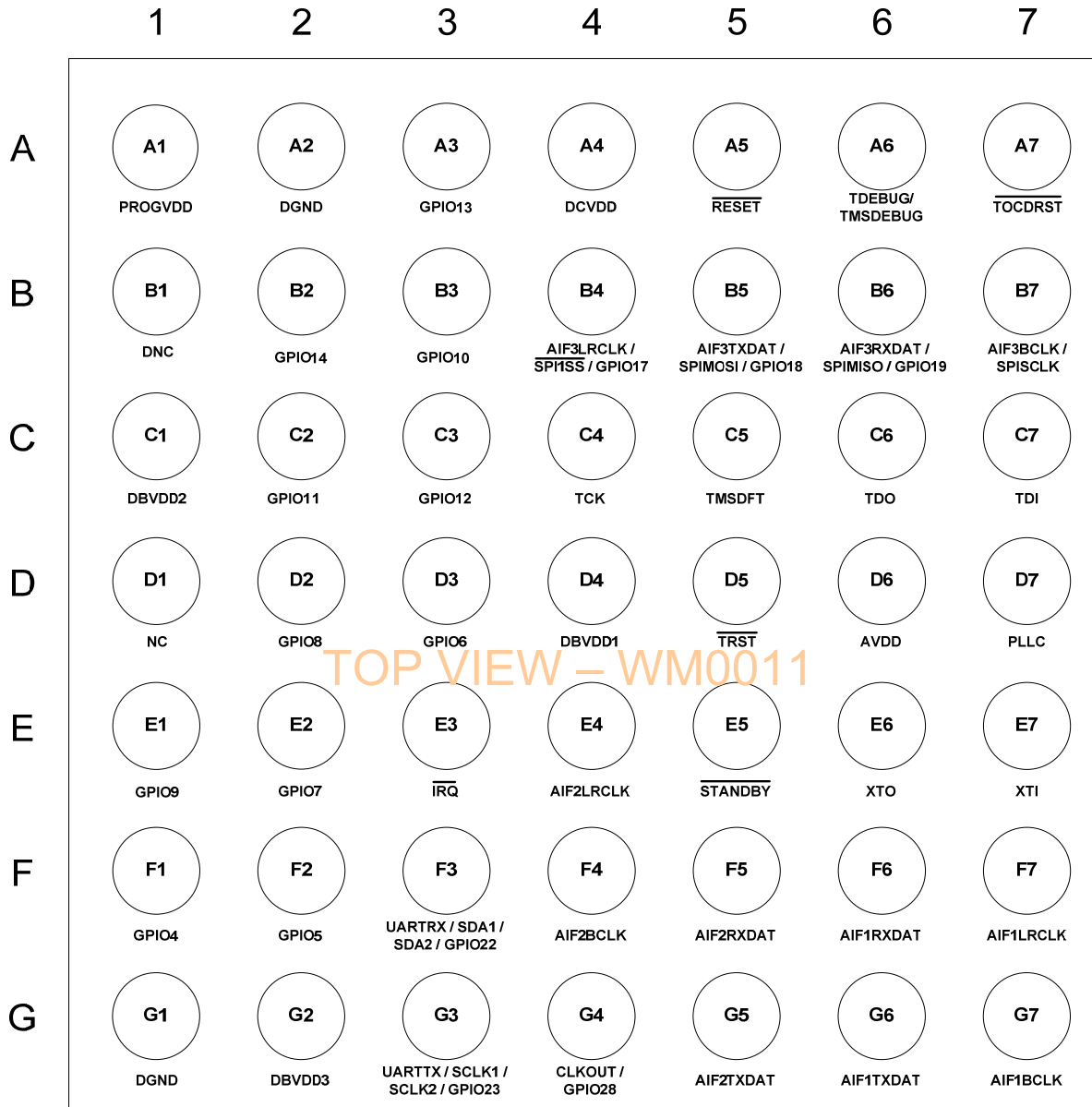
CCM_IOCTRL7 – I/O CONTROL 7 REGISTER	83
CCM_IOCTRL8 – I/O CONTROL 8 REGISTER	84
CCM_IOCTRL9 – I/O CONTROL 9 REGISTER	86
CCM_IOCTRL10 – I/O CONTROL 10 REGISTER	86
CCM_IOCTRL11 – I/O CONTROL 11 REGISTER	88
TIMER (TMR) MODULES	89
TIMER DESCRIPTION	89
TIMER INTERRUPTS	90
TIMER REGISTER MAP	90
TMR_PRESCALE – TIMER PRESCALE REGISTER	90
TMR_MAX_CNT – TIMER MAXIMUM COUNT REGISTER	91
TMR_CUR_CNT – TIMER CURRENT COUNT REGISTER	91
TMR_CTRL – TIMER CONTROL REGISTER	92
TMR_INT_STATUS – TIMER INTERRUPT STATUS REGISTER	93
I²C INTERFACE MODULE	94
I2C FEATURES	94
I2C TRANSFERS	94
I2C INTERRUPTS	97
I2C REGISTER MAP	98
I2C_CFG – I ² C CONFIGURATION REGISTER	99
I2C_STATUS – I2C STATUS REGISTER	100
I2C_INT_CTRL – I ² C INTERRUPT CONTROL REGISTER	102
I2C_MCTRL – I ² C MASTER ACCESS CONTROL REGISTER	102
I2C_MRCDATA – I ² C MASTER RECEIVE DATA REGISTER	104
I2C_MTXDATA – I ² C MASTER TRANSMIT DATA REGISTER	104
I2C_BAUD – I ² C BAUD RATE REGISTER	106
I2C_SRCDATA – I ² C SLAVE RECEIVE DATA REGISTER	107
I2C_STXDATA – I ² C SLAVE TRANSMIT DATA REGISTER	108
I2C_SLV_ADDR – I ² C SLAVE ADDRESS REGISTER	109
FUSE MEMORY	110
FUSE MEMORY DEFINITION	110
CYCLIC REDUNDANCY CHECK (CRC)	111
SOFTWARE AUTHENTICATION	112
GENERAL PURPOSE INPUT/OUTPUT (GPIO) MODULE	113
GPIO FEATURES	113
INPUT / OUTPUT CONTROL	113
LEVEL/EDGE INTERRUPT CONTROL	113
GPIO INTERRUPTS	114
GPIO REGISTER MAP	115
GPIO_OUT – GPIO OUTPUT REGISTER	115
GPIO_IN – GPIO INPUT REGISTER	116
GPIO_DIR – GPIO DIRECTION REGISTER	117
GPIO_INV – GPIO INVERSION REGISTER	117
EDGE DETECTION	118
GPIO_EDGE0 – GPIO EDGE DETECTION 0 REGISTER	119
GPIO_EDGE1 – GPIO EDGE DETECTION 1 REGISTER	119
GPIO_INT_CTRL – GPIO INTERRUPT CONTROL REGISTER	120
GPIO_INT_CLR – GPIO INTERRUPT CLEAR REGISTER	121
GPIO_INT_MSK – GPIO INTERRUPT MASK REGISTER	122
GPIO_INT_VECT – GPIO INTERRUPT VECTOR REGISTER	123
GPIO_INT_STS – GPIO INTERRUPT STATUS REGISTER	124
INTERRUPT CONTROLLER (IRQC) MODULE	125
INTERRUPT CONTROLLER (IRQC) FEATURES	125
INPUT / OUTPUT CONTROL	125

LEVEL/EDGE INTERRUPT CONTROL.....	125
IRQC MODULE INTERRUPTS.....	126
IRQC MODULE REGISTER MAP	128
IRQC_OUT – IRQ OUTPUT REGISTER.....	128
IRQC_IN – IRQ INPUT REGISTER.....	129
IRQC_DIR – IRQ DIRECTION REGISTER	129
IRQC_INV – IRQ INVERSION REGISTER.....	130
EDGE DETECTION.....	131
IRQC_EDGE0 – IRQ EDGE DETECTION 0 REGISTER	132
IRQC_EDGE1 – IRQ EDGE DETECTION 1 REGISTER	132
IRQC_INT_CTRL – IRQ INTERRUPT CONTROL REGISTER	133
IRQC_INT_CLR – IRQ INTERRUPT CLEAR REGISTER.....	134
IRQC_IRQ_MSK – IRQ INTERRUPT MASK REGISTER.....	134
IRQC_IRQ_VECT – IRQ INTERRUPT VECTOR REGISTER.....	136
IRQC_IRQ_STS – IRQ INTERRUPT STATUS REGISTER	136
IRQC_FIRQ_MSK – IRQ FAST INTERRUPT MASK REGISTER	137
IRQC_FIRQ_VECT – IRQ FAST INTERRUPT VECTOR REGISTER.....	139
IRQC_FIRQ_STS – IRQ FAST INTERRUPT STATUS REGISTER	140
TRAX TRACE BUFFER MODULE	141
TRAX REGISTER MAP	141
TRAX_CONFIG – TRAX TRACE BUFFER CONFIGURATION REGISTER	142
TRAX_CTRL – TRAX CONTROL REGISTER.....	142
TRAX_STS – TRAX STATUS REGISTER	144
TRAX_DATA – TRAX DATA REGISTER	145
TRAX_ADDR – TRAX ADDRESS REGISTER	145
TRAX_TRIG_PC – TRAX PC MATCH TRIGGER REGISTER.....	146
TRAX_PC_MATCH – TRAX PC MATCH CONTROL REGISTER.....	147
TRAX_DLY_CNT – TRAX POST-TRIGGER DELAY COUNT REGISTER.....	148
WATCHDOG TIMER (WDT) MODULE	149
WATCHDOG DESCRIPTION	149
WATCHDOG TIMER INTERRUPT	149
WATCHDOG REGISTER MAP	149
WDT_CTRL – WATCHDOG CONTROL REGISTER	150
WDT_CNT_RESTART – WATCHDOG COUNTER RESTART REGISTER.....	150
WDT_MAX_CNT – WATCHDOG MAXIMUM COUNT REGISTER	150
WDT_CUR_CNT – WATCHDOG CURRENT COUNT REGISTER.....	151
WDT_RST_LEN – WATCHDOG RESET PULSE LENGTH REGISTER.....	151
UART MODULE	152
UART FEATURES	152
UART INTERRUPTS	152
UART REGISTER MAP	153
UART_DAT - UART DATA REGISTER	153
UART_INT_CTRL - UART INTERRUPT CONTROL REGISTER.....	153
UART_FIFO_CTRL - UART FIFO CONTROL REGISTER.....	154
UART_INT_STATUS - UART INTERRUPT STATUS REGISTER	155
UART_LINE_CTRL - UART LINE CONTROL REGISTER	156
UART_LOOPBACK_CTRL - UART LOOPBACK CONTROL REGISTER.....	156
UART_LINE_STS - UART LINE STATUS REGISTER.....	157
UART_BAUD_LSW - UART BAUD LSW REGISTER.....	158
UART_BAUD_MSW - UART BAUD MSW REGISTER.....	158
SERIAL PERIPHERAL INTERFACE (SPI) MODULE	159
SPI FEATURES.....	159
SPI MASTER MODE	159
SPI SLAVE MODE.....	159

SPISCLK (CLOCK) CONFIGURATION	159
MISO/MOSI (DATA) CONFIGURATION.....	161
SPISS (SLAVE SELECT) PROTOCOL	161
SPISS (SLAVE SELECT) CONFIGURATION AND TIMING CONTROL	162
EARLY TRANSMIT DATA PHASE	163
AUTOMATED RE-TRANSMISSION OF DATA WORD	164
DOUBLE-BUFFERED TRANSMIT	164
SPI BYTE-PACKING	165
SPI DMA OPERATIONS.....	166
SPI CONTROL SEQUENCES	167
SPI INTERRUPTS	170
SPI REGISTER MAP	171
SPI_CTRL – SPI CONTROL REGISTER	171
SPI_CFG – SPI CONFIGURATION REGISTER	172
SPI_SCLKDIV – SPI CLOCK DIVISION REGISTER.....	174
SPI_STATUS – SPI STATUS REGISTER.....	174
SPI_SS_CFG– SPI SLAVE SELECT CONFIGURATION REGISTER	177
SPI_DAT– SPI DATA REGISTER	178
SPI_INT_CTRL – SPI INTERRUPT CONTROL REGISTER.....	178
SPI_DMA_CTRL– SPI DMA CONTROL REGISTER	179
SPI_BP_CNT – SPI BYTE PACK WORD COUNT REGISTER.....	179
SPI_BP_CNT_RAW – SPI BYTE PACK RAW WORD COUNT REGISTER	180
DMA CONTROLLER MODULE	181
DMA FEATURES.....	181
DMA CHANNEL CONTROL	182
DMA CHANNEL ARBITRATION.....	183
NORMAL DMA OPERATION	183
SHA MODULE DATA INPUT.....	184
DOUBLE-BUFFER DMA OPERATION.....	184
LINKED LIST DMA CHAINING	185
DMA STRIDING.....	186
BURST DATA TRANSFERS	188
DMA BYTE SWAP	188
ENDIAN BYTE SWAP	189
DMA INTERRUPTS.....	191
DMA REGISTER MAP.....	192
DMA_GLB_CTRL REGISTER.....	192
DMA_INT_STS REGISTER.....	193
DMA_TC_INT_MSK REGISTER	194
DMA_ERR_INT_MSK REGISTER	194
DMA_WMARK_INT_MSK REGISTER	194
DMA_LINKNUL_INT_MSK REGISTER.....	195
DMA_TC_STS REGISTER.....	195
DMA_ERR_STS REGISTER.....	196
DMA_WMARK_STS REGISTER.....	196
DMA_LINKNUL_STS REGISTER	197
DMA_FIFO_INT_MASK REGISTER	197
DMA_FIFO_STATUS REGISTER	197
DMA_AHB_SLAVE_ADDR REGISTER.....	198
DMA_PRI_SRC REGISTER.....	198
DMA_PRI_DST REGISTER	199
DMA_PRI_LEN REGISTER.....	199
DMA_LINK_ADDR REGISTER	200
DMA_SEC_SRC REGISTER.....	200

DMA_SEC_DST REGISTER.....	201
DMA_SEC_LEN REGISTER.....	201
DMA_COUNT REGISTER.....	202
DMA_WMARK_CNT REGISTER.....	202
DMA_CTRL1 REGISTER.....	203
DMA_CTRL2 REGISTER.....	206
DMA_SOFT_ABORT REGISTER.....	207
DMA_STRIDE REGISTER.....	207
DMA PROGRAM EXAMPLES.....	209
EXAMPLE 1: PERIPHERAL TRANSFERS USING DMA.....	209
EXAMPLE 2: MEMORY TO MEMORY TRANSFERS USING DMA.....	210
EXAMPLE 3: LINKED LIST DMA OPERATION.....	211
AIF INTERFACE MODULES.....	213
AIF FEATURES.....	213
AIF INTERFACE FORMATS.....	214
AIF INTERRUPTS.....	216
AIF REGISTER MAP.....	217
AIF_RX_DAT – AIF RECEIVE DATA REGISTER.....	217
AIF_RX_CH_ID – AIF RECEIVE CHANNEL ID REGISTER.....	218
AIF_RX_STS – AIF RECEIVE FIFO STATUS REGISTER.....	218
AIF_RX_LIMIT – AIF RECEIVE FIFO UPPER LIMIT REGISTER.....	219
AIF_TX_DAT – AIF TRANSMIT DATA REGISTER.....	219
AIF_TX_CH_ID – AIF TRANSMIT CHANNEL ID REGISTER.....	220
AIF_TX_STS – AIF TRANSMIT FIFO STATUS REGISTER.....	220
AIF_TX_LIMIT – AIF TRANSMIT FIFO LOWER LIMIT REGISTER.....	221
AIF_DATA_CFG – AIF DATA CONFIGURATION REGISTER.....	221
AIF_CLK_CFG – AIF SERIAL CLOCKING CONFIGURATION REGISTER.....	224
AIF_CTRL – AIF CONTROL REGISTER.....	225
AIF_INT_CTRL – AIF INTERRUPT CONTROL REGISTER.....	225
AIF_MCLK_DIV – AIF MCLK DIVIDER REGISTER.....	227
JTAG (JTAG) MODULE.....	228
CROSS-TRIGGER MODULE (CTM).....	228
ON-CHIP DEBUG (OCD) MODULE.....	228
APPLICATIONS INFORMATION.....	229
CONNECTIVITY DIAGRAM.....	230
PACKAGE DIMENSIONS.....	231
IMPORTANT NOTICE.....	232
ADDRESS:.....	232
REVISION HISTORY.....	233

PIN CONFIGURATION



TOP VIEW - WM0011

ORDERING INFORMATION

DEVICE	CUSTOM FUSES	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM0011ECS/R	Un-programmed	-40 to +85°C	49-ball W-CSP (Pb-free, Tape and reel)	MSL1	260°C
WM0011xxxECS/R	Custom-Programmed	-40 to +85°C	49-ball W-CSP (Pb-free, Tape and reel)	MSL1	260°C

Note:

Reel quantity = 5000

* xxx = Unique Custom Fuse part number

** Custom programmed minimum order quantity 50,000.

PIN DESCRIPTION

PIN NO	NAME	TYPE	PULL DEVICE	DESCRIPTION
Power and Ground Reference				
D4	DBVDD1	Supply	-	I/O supply (except GPIO pins 4...14)
A4	DCVDD	Supply	-	Core supply
A1	PROGVDD	Supply	-	Fuse programming supply. Connect to GND.
A2, G1	DGND	Supply	-	Ground
D6	AVDD	Supply	-	Analogue supply
D7	PLL	Reference	-	PLL capacitor connection (0.1µF recommended)
C1	DBVDD2	Supply	-	I/O supply (GPIO10, GPIO11, GPIO12, GPIO13, GPIO14 pins)
G2	DBVDD3	Supply	-	I/O supply (GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, GPIO9 pins)
Clock / Reset / Miscellaneous Interfaces				
E7	XTI	Input	-	Crystal connection or digital clock input
E6	XTO	Output	-	Crystal connection
A5	RESET	Input	Pull-Up	Device reset
E5	STANDBY	Input	Pull-Up	Standby input signal
E3	IRQ	Output	Pull-Up	Interrupt output
G4	CLKOUT/GPIO28	Input / Output	Pull-Down	Reference clock output / GPIO pin
Audio Interface 1 (AIF1)				
G6	AIF1TXDAT	Output	Pull-Down	AIF1 data output
F6	AIF1RXDAT	Input	Pull-Down	AIF1 data input
F7	AIF1LRCLK	Input / Output	Pull-Down	AIF1 frame clock
G7	AIF1BCLK	Input / Output	Pull-Down	AIF1 bit clock
Audio Interface 2 (AIF2)				
G5	AIF2TXDAT	Output	Pull-Down	AIF2 data output
F5	AIF2RXDAT	Input	Pull-Down	AIF2 data input
E4	AIF2LRCLK	Input / Output	Pull-Down	AIF2 frame clock
F4	AIF2BCLK	Input / Output	Pull-Down	AIF2 bit clock
Audio Interface 3 (AIF3) / Control Interface (SPI)				
B5	AIF3TXDAT/SPIMOSI/GPIO18	Input / Output	Pull-Down	AIF3 data output / SPI Master Out Slave In / GPIO ¹
B6	AIF3RXDAT/SPIMISO/GPIO19	Input / Output	Pull-Down	AIF3 data input / SPI Master In Slave Out / GPIO ¹
B4	AIF3LRCLK/SPISS/GPIO17	Input / Output	Pull-Up	AIF3 frame clock / SPI slave select / GPIO ¹

PIN NO	NAME	TYPE	PULL DEVICE	DESCRIPTION
B7	AIF3BCLK/SPISCLK	Input / Output	Pull-Down	AIF3 bit clock / SPI serial clock ¹
UART / I²C Master & Slave Interfaces				
F3	UARTRX/SDA1/SDA2/GPIO22	Input / Output	Pull-Down	UART RX / Serial data 1 (slave) / Serial data 2 (master) / GPIO ²
G3	UARTTX/SCLK1/SCLK2/GPIO23	Input / Output	Pull-Down	UART TX / Serial clock 1 (slave) / Serial clock 2 (master) / GPIO ²
GPIO				
F1	GPIO4	Input / Output	Pull-Up/Down	GPIO pin
F2	GPIO5	Input / Output	Pull-Up/Down	GPIO pin
D3	GPIO6	Input / Output	Pull-Up/Down	GPIO pin
E2	GPIO7	Input / Output	Pull-Up/Down	GPIO pin
D2	GPIO8	Input / Output	Pull-Up/Down	GPIO pin
E1	GPIO9	Input / Output	Pull-Up/Down	GPIO pin
B3	GPIO10	Input / Output	Pull-Up/Down	GPIO pin
C2	GPIO11	Input / Output	Pull-Up/Down	GPIO pin
C3	GPIO12	Input / Output	Pull-Up/Down	GPIO pin
A3	GPIO13	Input / Output	Pull-Up/Down	GPIO pin
B2	GPIO14	Input / Output	Pull-Up/Down	GPIO pin
Debug				
C4	TCK	Input	Pull-Up	JTAG clock
A6	TDEBUG/TMSDEBUG	Input / Output	Pull-Up	Test Mode Debug output / Test Mode Select input
C7	TDI	Input	Pull-Up	JTAG data input
C6	TDO	Output	Pull-Up	JTAG data output
C5	TMSDFT	Input	Pull-Up	JTAG mode select input
A7	$\overline{\text{TOCDRST}}$	Input	Pull-Up	Maskable chip reset from the debug tool
D5	$\overline{\text{TRST}}$	Input	Pull-Down	JTAG Test Access Port (TAP) block reset
Other				
B1	DNC			Do Not Connect
D1	NC			Not used - connect to GND.

Notes:

1. The SPI interface I/O pads are multiplexed with AIF3
2. The UART, I2C master and I2C slave signals are multiplexed into two I/O pads.
3. The I/O pad multiplexers are configured during the boot-up sequence, as determined by the Custom Fuse settings.

Table 1 identifies the default power-up condition of each of the input / output pins, assuming that the Custom Fuses are not programmed.

Application-specific parameters for configuring the input / output pins, and many other parameters, may be selected using the integrated one-time-programmable fuses. See "Boot Sequence Control" for further details.

PIN NO	NAME	DEFAULT FUNCTION / RESET CONDITION (FUSES NOT PROGRAMMED)		
E7	XTI	XTI	input	
E6	XTO	XTO	output	
A5	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	input	Pull-up enabled
E5	$\overline{\text{STANDBY}}$	$\overline{\text{STANDBY}}$	input	Pull-up enabled
E3	$\overline{\text{IRQ}}$	$\overline{\text{IRQ}}$	output	Pull-up enabled
G4	CLKOUT/GPIO28	CLKOUT	output	Pull-down enabled
G6	AIF1TXDAT	AIF1TXDAT	output	Pull-down enabled
F6	AIF1RXDAT	AIF1RXDAT	input	Pull-down enabled

PIN NO	NAME	DEFAULT FUNCTION / RESET CONDITION (FUSES NOT PROGRAMMED)		
F7	AIF1LRCLK	AIF1LRCLK	input	Pull-down enabled
G7	AIF1BCLK	AIF1BCLK	input	Pull-down enabled
G5	AIF2TXDAT	AIF2TXDAT	output	Pull-down enabled
F5	AIF2RXDAT	AIF2RXDAT	input	Pull-down enabled
E4	AIF2LRCLK	AIF2LRCLK	input	Pull-down enabled
F4	AIF2BCLK	AIF2BCLK	input	Pull-down enabled
B5	AIF3TXDAT/SPIMOSI/GPIO18	SPIMOSI	output	Pull-down enabled
B6	AIF3RXDAT/SPIMISO/GPIO19	SPIMISO	input	Pull-down enabled
B4	AIF3LRCLK/SPISS/GPIO17	SPISS	output	Pull-up enabled
B7	AIF3BCLK/SPISCLK	SPISCLK	output	Pull-down enabled
F3	UARTRX/SDA1/SDA2/GPIO22	UARTRX	input	Pull-down enabled
G3	UARTTX/SCLK1/SCLK2/GPIO23	UARTTX	output	Pull-down enabled whilst $\overline{\text{RESET}}$ is asserted. Pull-down is disabled after $\overline{\text{RESET}}$ is released. UARTTX is then actively driven.
F1	GPIO4	[Disabled]	input/output	Pull-down enabled
F2	GPIO5	[Disabled]	input/output	Pull-down enabled
D3	GPIO6	[Disabled]	input/output	Pull-down enabled
E2	GPIO7	[Disabled]	input/output	Pull-down enabled
D2	GPIO8	[Disabled]	input/output	Pull-down enabled
E1	GPIO9	[Disabled]	input/output	Pull-down enabled
B3	GPIO10	[Disabled]	input/output	Pull-down enabled whilst $\overline{\text{RESET}}$ is asserted. Pull-up is enabled after $\overline{\text{RESET}}$ is released.
C2	GPIO11	[Disabled]	input/output	Pull-down enabled
C3	GPIO12	[Disabled]	input/output	Pull-down enabled
A3	GPIO13	[Disabled]	input/output	Pull-down enabled
B2	GPIO14	[Disabled]	input/output	Pull-down enabled
C4	TCK	TCK	input	Pull-up enabled
A6	TDEBUG/TMSDEBUG	TDEBUG/TMSDEBUG		Pull-up enabled
C7	TDI	TDI	input	Pull-up enabled
C6	TDO	TDO	output	Pull-down enabled
C5	TMSDFT	TMSDFT	input	Pull-up enabled
A7	$\overline{\text{TOCDRST}}$	$\overline{\text{TOCDRST}}$	input	Pull-up enabled
D5	$\overline{\text{TRST}}$	$\overline{\text{TRST}}$	input	Pull-down enabled

Table 1 Default Pin Conditions (assuming Fuses are not programmed)

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltage (DCVDD)	DGND - 0.3V	1.6V
Supply voltage (DBVDD1, DBVDD2, DBVDD3, AVDD, PROGVD)	DGND - 0.3V	5.0V
Voltage range digital inputs (DBVDD1 domain)	DGND - 0.3V	DBVDD1 + 0.3V
Voltage range digital inputs (DBVDD2 domain)	DGND - 0.3V	DBVDD2 + 0.3V
Voltage range digital inputs (DBVDD3 domain)	DGND - 0.3V	DBVDD3 + 0.3V
Operating temperature range, T _A	-40°C	+85°C
Junction temperature, T _J	-40°C	+125°C
Storage temperature after soldering	-65°C	+150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital core supply range	DCVDD	1.14	1.2	1.32	V
Digital I/O supply range	DBVDD1	1.62	1.8	1.98	V
Digital I/O supply range (GPIO10, GPIO11, GPIO12, GPIO13, GPIO14)	DBVDD2	1.62		3.63	V
Digital I/O supply range (GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, GPIO9)	DBVDD2	1.62		3.63	V
PLL supply range	AVDD	1.14	1.2	1.32	V
Fuse programming supply	PROGVDD		0		V
Ground	DGND		0		V
Operating temperature range	T _A	-40		+85	°C

Notes:

- All supplies are independent of each other (i.e. not internally connected)
- PROGVDD must be tied to 0V during normal operation
- The WM0011 can operate with DBVDD2 tied to 0V, but GPIO10, GPIO11, GPIO12, GPIO13, GPIO14 functionality is not supported in this case
- The WM0011 can operate with DBVDD3 tied to 0V, but GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, GPIO9 functionality is not supported in this case

THERMAL PERFORMANCE

Thermal analysis should be performed in the intended application to prevent the WM0011 from exceeding maximum junction temperature. Several contributing factors affect thermal performance most notably the physical properties of the mechanical enclosure, location of the device on the PCB in relation to surrounding components and the number of PCB layers. Connecting the GND pin through thermal vias and into a large ground plane will aid heat extraction.

Three main heat transfer paths exist to surrounding air as illustrated below in:

- Package top to air (radiation)
- Package bottom to PCB (radiation)
- Package pins to PCB (conduction)

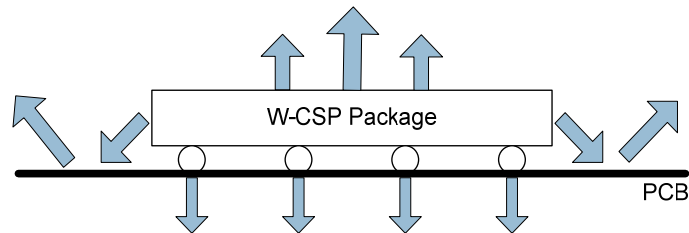


Figure 1 Heat Transfer Paths

The temperature rise T_R is given by $T_R = P_D * \Theta_{JA}$

- P_D is the power dissipated in the device.
- Θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature and is therefore a measure of heat transfer from the die to surrounding air. Θ_{JA} is determined with reference to JEDEC standard JESD51-9.

The junction temperature T_J is given by $T_J = T_A + T_R$, where T_A is the ambient temperature.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Ambient Temperature	T_A	-40		+85	°C
Junction Temperature	T_J	-40		+125	°C
Thermal Resistance	Θ_{JA}		58		°C/W

Note:

1. Junction temperature is a function of ambient temperature and of the device operating conditions. The ambient temperature limits and junction temperature limits must both be observed.
2. Thermal resistance (Θ_{JA}) is measured using JESD51-2 methodology

ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD=AVDD=1.2V, DBVDD1=DBVDD2=DBVDD3=1.8V, T_A = +25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input / Output						
Input HIGH Level, GPIO[4..9] pads	V _{IH}		0.65 x V _{DBVDD3}			V
Input LOW Level, GPIO[4..9] pads	V _{IL}				0.35 x V _{DBVDD3}	V
Input HIGH Level, GPIO[10..14] pads	V _{IH}		0.65 x V _{DBVDD2}			V
Input LOW Level, GPIO[10..14] pads	V _{IL}				0.35 x V _{DBVDD2}	V
Input HIGH Level, All other digital pads	V _{IH}		0.65 x V _{DBVDD1}			V
Input LOW Level, All other digital pads	V _{IL}				0.35 x V _{DBVDD1}	V
Output HIGH Level, GPIO[4..9] pads	V _{OH}	I _{OH} = 5mA Full strength output drive (*_DS = 1)	0.75 x V _{DBVDD3}			V
Output LOW Level, GPIO[4..9] pads	V _{OL}	I _{OL} = -5mA Full strength output drive (*_DS = 1)			0.25 x V _{DBVDD3}	V
Output HIGH Level, GPIO[10..14] pads	V _{OH}	I _{OH} = 5mA Full strength output drive (*_DS = 1)	0.75 x V _{DBVDD2}			V
Output LOW Level, GPIO[10..14] pads	V _{OL}	I _{OL} = -5mA Full strength output drive (*_DS = 1)			0.25 x V _{DBVDD2}	V
Output HIGH Level, All other digital pads	V _{OH}	I _{OH} = 1mA Full strength output drive (*_DS = 1)	0.75 x V _{DBVDD1}			V
Output LOW Level, All other digital pads	V _{OL}	I _{OL} = -1mA Full strength output drive (*_DS = 1)			0.25 x V _{DBVDD1}	V
Input Capacitance	C _{IN}				2.8	pF
Input Leakage			-10		+10	μA
Pull-up resistance, GPIO[4..14] pads		Pull-Up enabled for the respective pad (*_PU = 1)		61		kΩ
Pull-down resistance, GPIO[4..14] pads		Pull-Down enabled for the respective pad (*_PD = 1)		61		kΩ
Pull-up resistance, All other digital pads		Pull-Up enabled for the respective pad (*_PU = 1)		38		kΩ
Pull-down resistance, All other digital pads		Pull-Down enabled for the respective pad (*_PD = 1)		40		kΩ

Selectable output drive strength control is provided on the digital output pads, using the *_DS register bits. The reduced drive strength option may be used at lower clock speeds, if preferred. Specific characteristic data for reduced drive strength is not available.

TYPICAL POWER CONSUMPTION

Typical power consumption data is provided below for a number of different operating conditions.

Test Conditions:

DCVDD = AVDD = 1.2V, DBVDD1 = 1.8V, DBVDD2 = DBVDD3 = 0V, T_A = +25°C

OPERATING MODE	TEST CONDITIONS	I _{DCVDD}	I _{DBVDD1}	I _{AVDD}	TOTAL
Reset	RESE \bar{T} asserted CLKIN = 0MHz	0.2mA	0.03mA	0.05mA	0.35mW
BootROM (awaiting code download)	RESE \bar{T} de-asserted CLKIN = 24.576MHz	8.78mA	0.48mA	0.05mA	11.46mW
Sleep Mode	RESE \bar{T} de-asserted SLP_ENA=1 (CCM_WKUP_CTRL register) CLKIN = 0MHz DSPCLK disabled, AHBCLK disabled	0.25mA	0.02mA	0.05mA	0.40mW
	RESE \bar{T} de-asserted SLP_ENA=1 (CCM_WKUP_CTRL register) CLKIN = 24.576MHz DSPCLK disabled, AHBCLK disabled RAM & IRQC modules enabled	0.91mA	0.47mA	0.05mA	2.00mW
Sleep Mode AIF Bypass enabled	RESE \bar{T} de-asserted SLP_ENA=1 (CCM_WKUP_CTRL register) CLKIN = 0MHz DSPCLK disabled, AHBCLK disabled AIF Bypass Mode A enabled	0.27mA	0.16mA	0.05mA	0.67mW
	RESE \bar{T} de-asserted SLP_ENA=1 (CCM_WKUP_CTRL register) CLKIN = 24.576MHz DSPCLK disabled, AHBCLK disabled AIF Bypass Mode A enabled	0.95mA	0.60mA	0.05mA	2.28mW
Run Mode (full processor load)	RESE \bar{T} de-asserted SLP_ENA=0 (CCM_WKUP_CTRL register) CLKIN = 24.576MHz PLLOUT = 259.2MHz All peripherals enabled Processor fully loaded	90mA	0.60mA	0.10mA	109.2mW

The WM0011 supports a low-power Sleep mode, as referenced above. Note that, when the WM0011 is not in use, the Sleep mode (not the Reset mode) is recommended for typical applications. The Sleep mode allows the full processor functionality to be resumed at any time, without needing to re-load the software code. The Sleep mode also enables AIF Bypass modes to be selected.

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK & PHASE LOCKED LOOP (PLL)

Test Conditions

DCVDD=AVDD=1.2V, DBVDD1=DBVDD2=DBVDD3=1.8V, T_A = +25°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
External Clock Timing					
Chip Clock Input	CLKIN			26	MHz
Alternate Clock Input	ALTCLK			26	MHz
Timer Clock Trigger	TMRCLK			26	MHz
Input Clock duty cycle		40		60	%
Phase Locked Loop (PLL)					
PLL input frequency	CLKIN	5		26	MHz
PLL input duty cycle		40		60	%
PLL output frequency	PLLOUT	6.25		260	MHz
PLL lock time				2	ms
Internal Clock Timing					
DSP Core Clock	DSPCLK			260	MHz
AHB Bus Clock	AHBCLK			130	MHz
APB Bus Clock	APBCLK			130	MHz

Table 2 System Clock and Phase Locked Loop (PLL)

The WM0011 incorporates a 2-stage cascaded PLL circuit; the PLL timing parameters above refer to the 2-stage circuit in its entirety. Note that the specified frequency limits are not applicable to the internal reference points within the cascaded PLL circuits.

AUDIO INTERFACE (AIF) TIMING

DIGITAL AUDIO INTERFACE – MASTER MODE

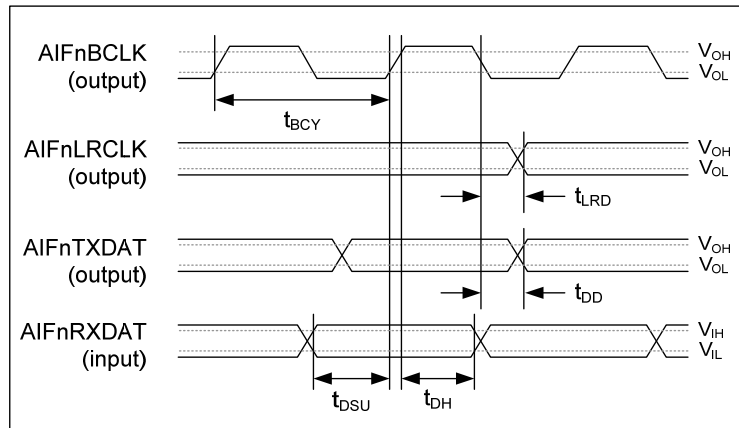


Figure 2 AIF Interface Timing – Master Mode

Test Conditions

DCVDD=AVDD=1.2V, DBVDD1=DBVDD2=DBVDD3=1.8V, $T_A = +25^\circ\text{C}$, $C_{LOAD}=5\text{pF}$ (output pins)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Master Mode					
AIFnBCLK cycle time	t_{BCY}	80			ns
AIFnBCLK duty cycle		40		60	%
AIFnLRCLK propagation delay from AIFnBCLK falling edge	t_{LRD}	0		15	ns
AIFnTXDAT propagation delay from AIFnBCLK falling edge	t_{DD}	0		15	ns
AIFnRXDAT setup time to AIFnBCLK rising edge	t_{DSU}	16.3			ns
AIFnRXDAT hold time from AIFnBCLK rising edge	t_{DH}	16.3			ns

Table 3 AIF Master Mode Timing Values

Note the timing figures quoted in the table above are for full drive strength outputs; these timings are not guaranteed for reduced drive strength.

DIGITAL AUDIO INTERFACE – SLAVE MODE

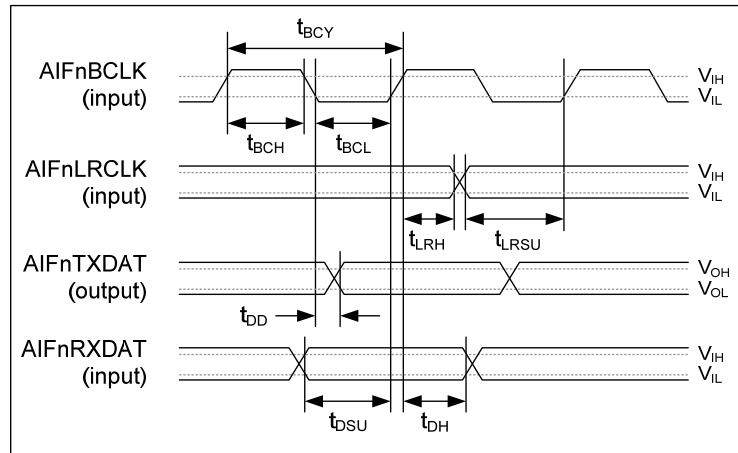


Figure 3 AIF Interface Timing – Slave Mode

Test Conditions

DCVDD=AVDD=1.2V, DBVDD1=DBVDD2=DBVDD3=1.8V, T_A = +25°C, C_{LOAD}=5pF (output pins)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Slave Mode					
AIFnBCLK cycle time	t _{BCY}	80			ns
AIFnBCLK duty cycle		35		65	%
AIFnLRCLK set-up time to AIFnBCLK rising edge	t _{LRSU}	16.3			ns
AIFnLRCLK hold time from AIFnBCLK rising edge	t _{LRH}	7.5			ns
AIFnRXDAT hold time from AIFnBCLK rising edge	t _{DH}	10			ns
AIFnTXDAT propagation delay from AIFnBCLK falling edge	t _{DD}	0		12	ns
AIFnRXDAT set-up time to AIFnBCLK rising edge	t _{DSU}	16.3			ns

Table 4 AIF Slave Mode Timing Values

Note the timing figures quoted in the table above are for full drive strength outputs; these timings are not guaranteed for reduced drive strength.

SPI INTERFACE TIMING

SPI INTERFACE – MASTER MODE

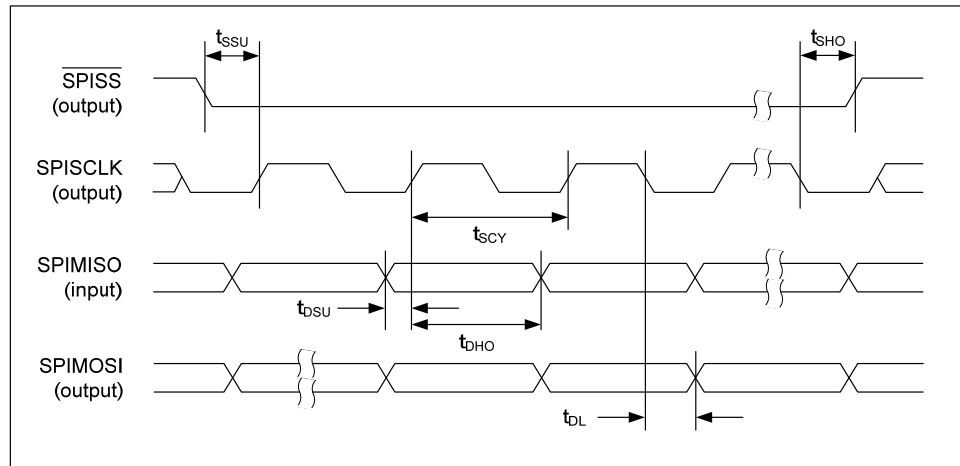


Figure 4 SPI Master Mode Timing

Note this diagram shows the mode where incoming data (SPIMISO) is sampled on the rising edge of SPISCLK, and outgoing data (SPIMOSI) transitions on the falling edge of SPISCLK.

Test Conditions

AVDD=DCVDD=1.2V, DBVDD1=DBVDD2=DBVDD3=1.8V, $T_A = +25^\circ\text{C}$, $C_{LOAD}=5\text{pF}$ (output pins), unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SPI Interface Timing - Master Mode					
SPISS set-up time to SPISCLK rising edge	t_{SSU}	25			ns
SPISS hold time from SPISCLK falling edge	t_{SHO}	25			ns
SPISCLK pulse cycle time	t_{SCY}	61.6			ns
In SPI Master mode, the maximum SPISCLK frequency is 16.25MHz. It is also required that $F_{SPISCLK} \leq F_{AHBCLK}/8$.					
SPISCLK duty cycle		40		60	%
SPIMISO set-up time to SPISCLK rising edge	t_{DSU}	10.5			ns
SPIMISO hold time from SPISCLK rising edge	t_{DHO}	2.0			ns
SPIMOSI propagation delay from SPISCLK falling edge	5pF, reduced drive strength	t_{DL}		5.1	ns
	5pF, full drive strength			4.7	
	25pF, reduced drive strength			6.3	
	25pF, full drive strength			8.7	

Table 5 SPI Master Mode Timing Values

Note the timing figures quoted in the table above are for full drive strength outputs (except where otherwise stated); these timings are not guaranteed for reduced drive strength.

SPI INTERFACE – SLAVE MODE

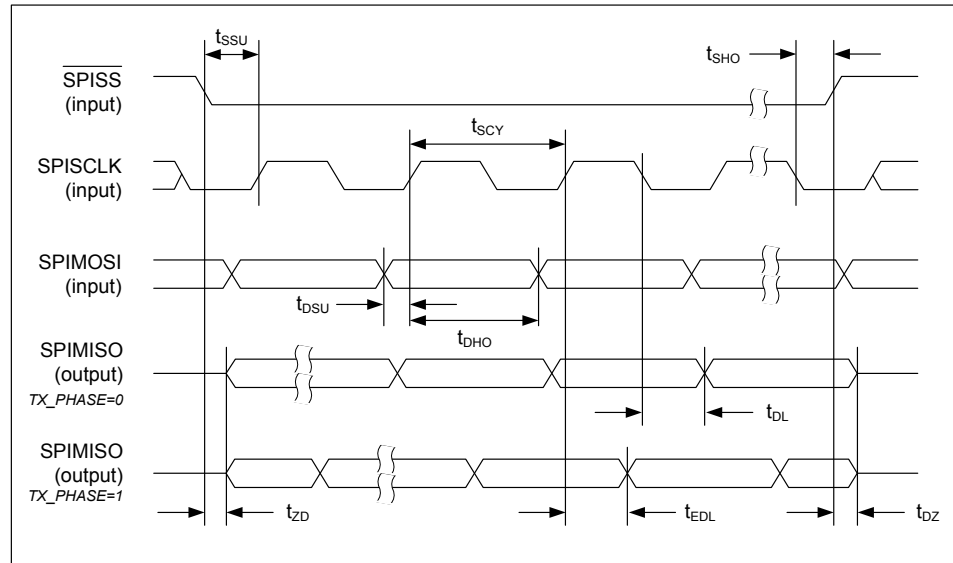


Figure 5 SPI Slave Mode Timing

Note this diagram shows the mode where incoming data (SPIMOSI) is sampled on the rising edge of SPISCLK. By default, the outgoing data (SPIMISO) transitions on the falling edge of SPISCLK. When 'Early Transmit Data Phase' mode is selected (TX_PHASE=1), the outgoing data (SPIMISO) transitions on the rising edge of SPISCLK.

Test Conditions

AVDD=DCVDD=1.2V, DBVDD1=DBVDD2=DBVDD3=1.8V, $T_A = +25^\circ\text{C}$, $C_{LOAD}=5\text{pF}$ (output pins), unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SPI Interface Timing - Slave Mode					
SPISS set-up time to SPISCLK rising edge	t_{SSU}	$t_{AHBCLK} + 1.0$			ns
SPISS hold time from SPISCLK falling edge	t_{SHO}	2.0			ns
SPISCLK pulse cycle time	t_{SCY}	38.5			ns
In SPI Slave mode, the maximum SPISCLK frequency is 26MHz. It is also required that $F_{SPISCLK} < F_{AHBCLK}$.					
SPISCLK duty cycle		40		60	%
SPIMOSI set-up time to SPISCLK rising edge	t_{DSU}	2.0			ns
SPIMOSI hold time from SPISCLK rising edge	t_{DHO}	2.0			ns
SPIMISO propagation delay from SPISCLK falling edge	$C_{LOAD}=25\text{pF}$	t_{DL}		12.1	ns
	$C_{LOAD}=5\text{pF}$			9.3	
SPIMISO propagation delay from SPISCLK rising edge (early TX data mode)	$C_{LOAD}=25\text{pF}$	t_{EDL}		14.1	ns
	$C_{LOAD}=5\text{pF}$			11.3	
SPIMISO enable from SPISS falling edge	t_{ZD}			13.6	ns
SPIMISO disable from SPISS rising edge	t_{DZ}			7.8	ns

Table 6 SPI Slave Mode Timing Values

Note the timing figures quoted in the table above are for full drive strength outputs; these timings are not guaranteed for reduced drive strength.

CONTROL INTERFACE (I2C) TIMING

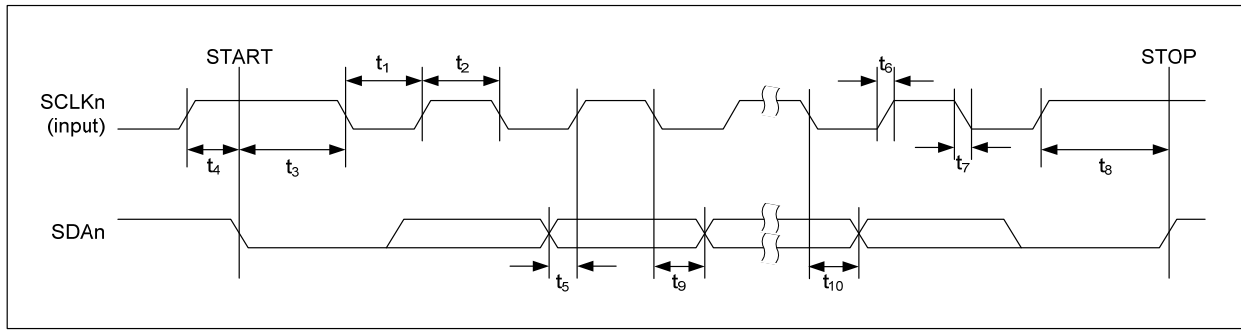


Figure 6 I²C Control Interface Timing

Test Conditions

AVDD= DCVDD=1.2V, DBVDD1=DBVDD2=DBVDD3=1.8V, T_A = +25°C, unless otherwise stated.

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
SCLKn Frequency					1000	kHz
SCLKn Low Pulse-Width		t ₁	500			ns
SCLKn High Pulse-Width		t ₂	260			ns
Hold Time (Start Condition)	Pulse filter OFF	t ₃	260			ns
	Pulse filter ON		275			
Setup Time (Start Condition)		t ₄	260			ns
SDAn, SCLKn Rise Time		t ₆			120	ns
SDAn, SCLKn Fall Time		t ₇			120	ns
Setup Time (Stop Condition)		t ₈	260			ns
SDAn Setup Time (data/ACK input)		t ₅	50			ns
SDAn Hold Time (data/ACK input)		t ₉	0			ns
SDAn Valid Time (data/ACK output)		t ₁₀			450	ns
Pulse width of spikes that will be suppressed		t _{ps}	0		50	ns

Table 7 I²C Timing Values

DEVICE DESCRIPTION

INTRODUCTION

The WM0011 is an audio DSP designed for smartphones and other high performance audio applications. The architecture is optimised for multi-channel audio processing such as software CODECs, equalisation, compression and echo cancellation.

BLOCK DIAGRAM

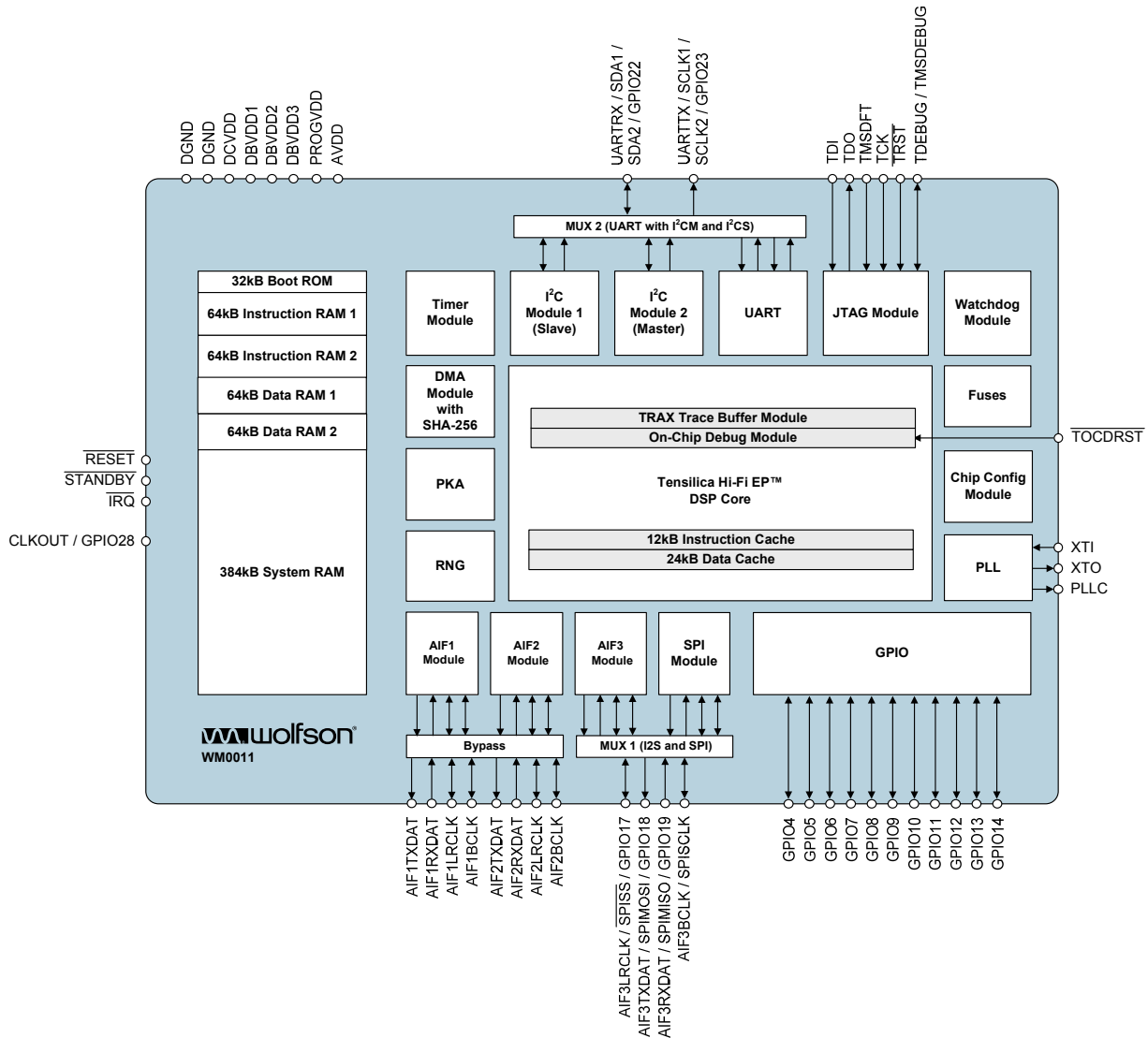


Figure 7 WM0011 Block Diagram

DESCRIPTION OF MODULES

BOOT ROM

The 32kB boot ROM allows the WM0011 to boot from a variety of sources. These are listed in the table below.

MODULE	BOOTABLE FROM
SPI Slave	External host processor
SPI Master	SST25WFxxx SPI Serial Flash

TIGHTLY-COUPLED MEMORY (TCM) RAM

The DSP's primary memory comprises 64-bit wide, zero-latency tightly coupled memory.

- 128kB of instruction RAM
- 128kB of data RAM

MULTI-PURPOSE RAM

The 384kB system RAM is connected to the DSP via the system bus. This RAM can be used for storing either instructions or data. Both data and instructions can be transferred in and out of TCM by DMA.

TENSILICA HIFI EP™ DSP CORE

The core combines a 24-bit audio DSP engine that has been optimised for highly efficient high-resolution audio processing, with a GCC-compatible (GNU Compiler Collection) general purpose RISC instruction set. It includes logic to interface with the AHB bus and the TRAX Trace Buffer, and to the JTAG TAP controller in order to provide support for On-Chip Debug (OCD). The HiFi EP™ features:

- 7-stage instruction pipeline
- One load-store unit
- 12kB 3-way Instruction Cache (64-bit width), and corresponding TAG memory
- 24kB 3-way Data Cache (64-bit width), and corresponding TAG memory
- Pre-fetch buffering for slow external RAM support
- TCM Core Instruction RAM (64-bit width)
- PIF-to-AHB-Lite Bridge, Synchronous, 64-bit width
- Three general purpose timers
- Interrupt controller, with sixteen external and five internal interrupt inputs
- On-Chip Debug (OCD) support
- Trace port and corresponding 1kB TRAX trace RAM (32-bit width)
- Floating point accelerator

For more detailed information on the Tensilica HiFi EP™ core, refer to the 'HiFi EP Audio Engine Instruction Set Architecture Reference Manual' (HIFIEP-ISA-rm.pdf), available from Tensilica.

TIMER MODULE

Three 32-bit general-purpose timers are provided. The timers can be configured as up-counters or as down-counters. The Timer block features include:

- Free-running counter operation (triggered internally or externally)
- Event counter operation (externally triggered)
- One-shot operation from either an external or an internal trigger

WATCHDOG MODULE

A watchdog timer block is provided as a means to reset the WM0011 chip in the case of a software failure. A timeout of the watchdog produces a Warm Reset (maskable) that includes a reset of most registers and state machines, and of the PLL.

GPIO MODULE

There is one GPIO controller controlling seventeen multiplexed GPIO inputs. Two of these inputs can be selected as an interrupt to HiFi EP™, or one can be selected to be used as an input to the IRQC controller.

IRQC MODULE

The IRQC controller provides fine control of interrupts (edge control, etc). It also enables wake-up, and controls the external $\overline{\text{IRQ}}$ output pin. Table 8 shows the IRQC assignments.

IRQC BIT	DIRECTION	DESCRIPTION
15	Output	Software interrupt – HiFi EP™ interrupt input
14	Output	Software interrupt – HiFi EP™ interrupt input
13	Input	Reserved
12	Input	Reserved
11	Input	Timer 2 interrupt
10	Input	Timer 1 interrupt
9	Input	DMA interrupt
8	Input	Watchdog interrupt
7	Input	$\overline{\text{STANDBY}}$ pin (Active Low) Note this input is inverted internally, and is therefore Active High at the input to the IRQC module.
6	Input	I2C interrupt
5	Input	AIF 2 interrupt
4	Input	AIF 1 interrupt
3	Input	UART interrupt
2	Input	SPI interrupt
1	Input	Cascaded interrupt input from the GPIO controller (Active Low)
0	Output	$\overline{\text{IRQ}}$ pin (Active Low)

Table 8 IRQC Interrupt assignment