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WM1811A

Multi-Channel Audio Hub CODEC for Smartphones

DESCRIPTION

The WM1811A[1] is a highly integrated ultra-low power hi-fi CODEC designed for smartphones and other portable devices rich in multimedia features.

An integrated stereo Class D speaker driver and Class W headphone driver minimize power consumption during audio playback.

The device requires only two voltage supplies, with all other internal supply rails generated from integrated LDOs.

Stereo full duplex asynchronous sample rate conversion and multi-channel digital mixing combined with powerful analogue mixing allow the device to support a huge range of different architectures and use cases.

A programmable parametric EQ provides speaker compensation in the digital playback paths. The dynamic range controller can be used in record or playback paths for maintaining a constant signal level, maximizing loudness and protecting speakers against overloading and clipping.

A smart digital microphone interface provides power regulation, a low jitter clock output and decimation filters for up to two digital microphones. Microphone activity detection with interrupt is available.Low power jack detection is supported via a dedicated input pin. Impedance sensing and measurement is provided for external accessory / push-button detection.

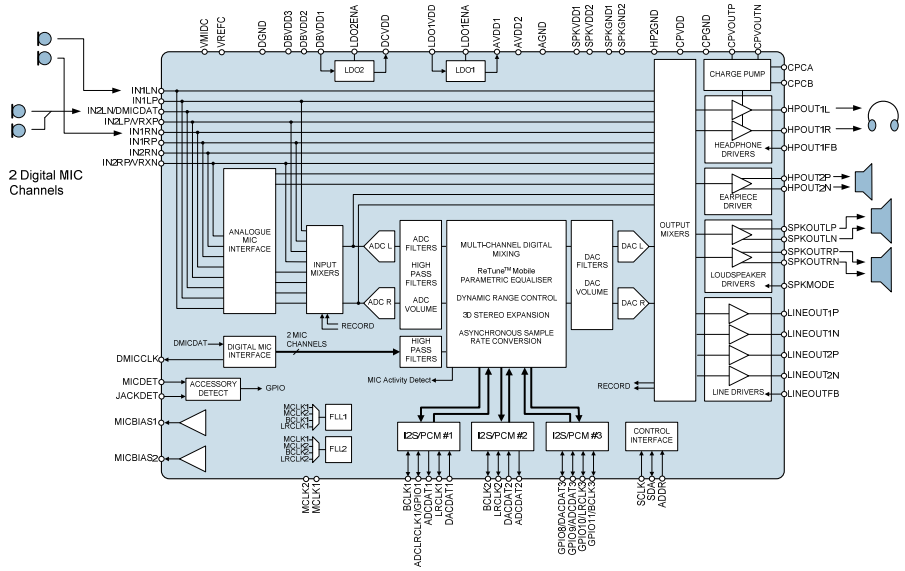
Fully differential internal architecture and on-chip RF noise filters ensure a very high degree of noise immunity. Active ground loop noise rejection and DC offset correction help prevent pop noise and suppress ground noise on the headphone outputs.

FEATURES

- 24-bit 2-channel hi-fi DAC and 2-channel hi-fi ADC
- 100dB SNR during DAC playback ('A' weighted)
- Smart MIC interface
  - Power, clocking and data input for up to two digital MICs
  - High performance analogue MIC interface
  - MIC activity detect & interrupt allows processor to sleep
  - Low power jack detection support
  - Impedance sensing for accessory / push-button detection
- 2W stereo (2 x 2W) Class D speaker driver
- Capless Class W headphone drivers
  - Integrated charge pump
  - 5.3mW total power for DAC playback to headphones
- 4 Line outputs (single-ended or differential)
- BTL Earpiece driver
- Digital audio interfaces for multi-processor architecture
  - Asynchronous stereo duplex sample rate conversion
  - Powerful mixing and digital loopback functions
- ReTune™ Mobile 5-band, 4-channel parametric EQ
- Dynamic range controller
- Dual FLL provides all necessary clocks
  - Self-clocking modes allow processor to sleep
  - All standard sample rates from 8kHz to 96kHz
- Active noise reduction circuits
  - DC offset correction removes pops and clicks
  - Ground loop noise cancellation
- Integrated LDO regulators
- 80-ball W-CSP package (4.158 x 3.876 x 0.607mm)

APPLICATIONS

- Smartphones and music phones
- Portable navigation
- Tablets, eBooks
- Portable Media Players



[1] This product is protected by Patents US 7,622,984, US 7,626,445, and GB 2,469,345

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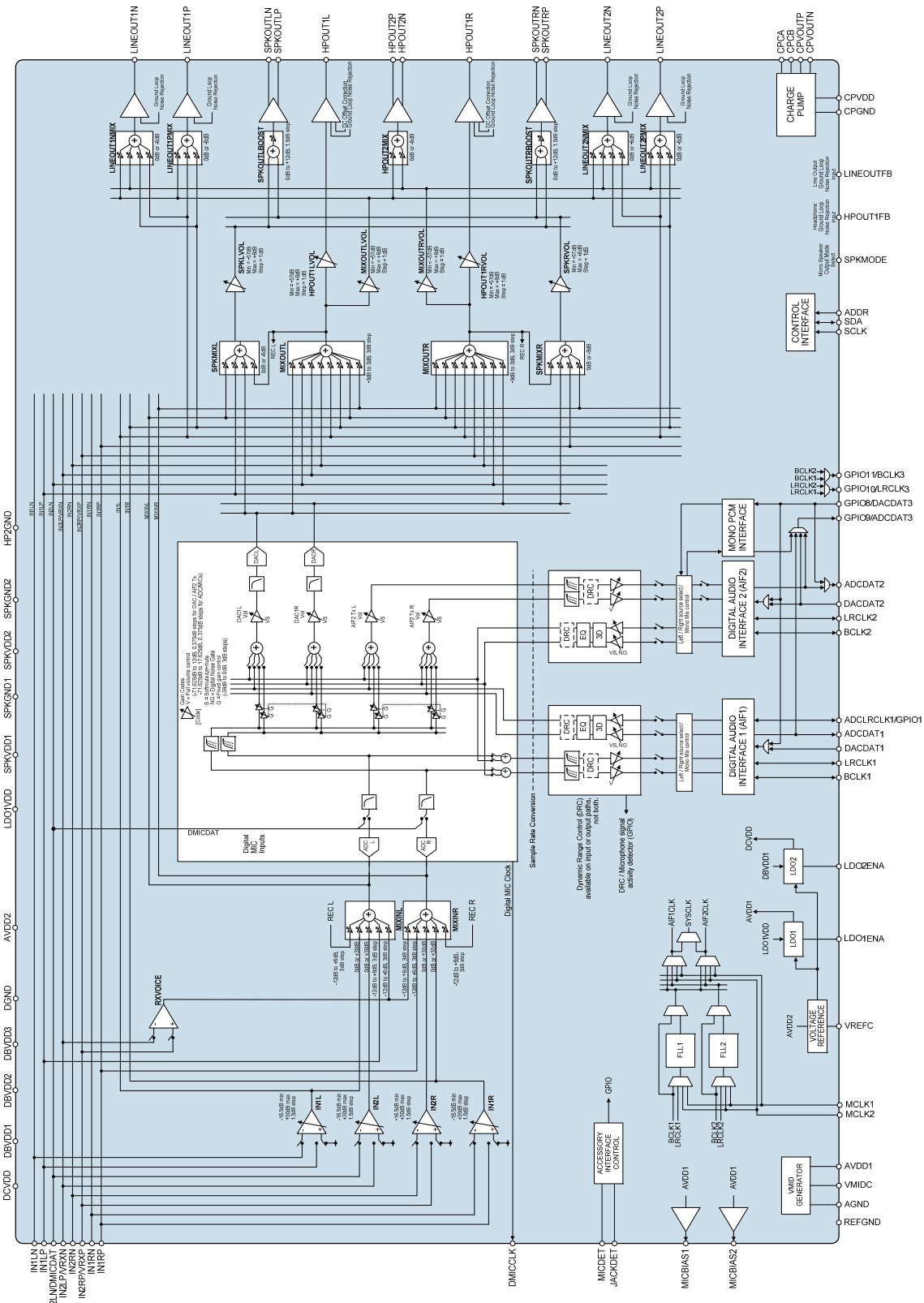
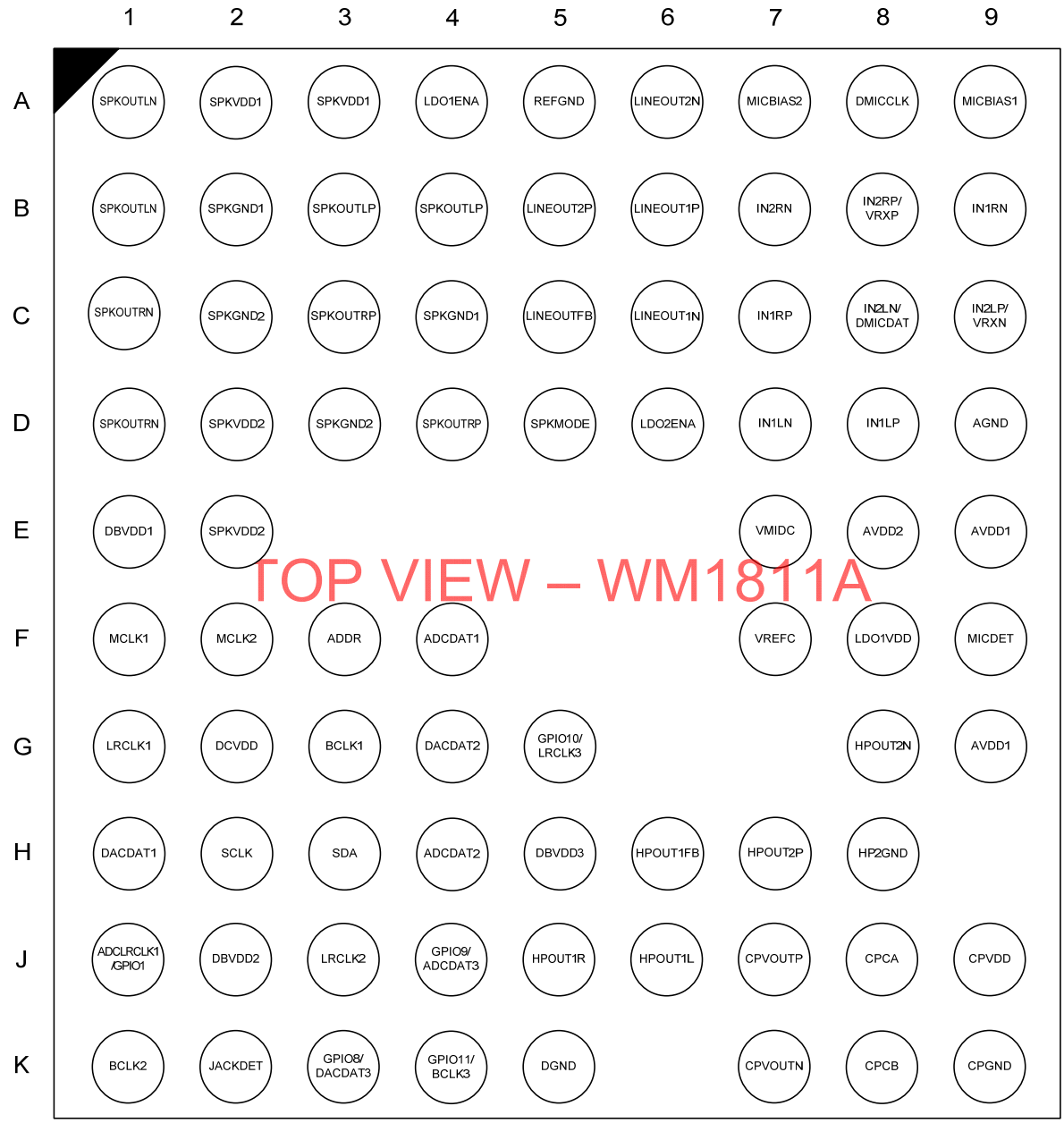
BLOCK DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURERANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM1811AECS/R	-40°C to +85°C	80-ball W-CSP (Pb-free, Tape and reel)	MSL1	260°C

Note:
Reel quantity = 5000

PIN DESCRIPTION

A description of each pin on the WM1811A is provided below.
Note that a table detailing the associated power domain for every input and output pin is provided on the following page.
Note that, where multiple pins share a common name, these pins should be tied together on the PCB.

PIN NO	NAME	TYPE	DESCRIPTION
F4	ADCDAT1	Digital Output	Audio interface 1 ADC digital audio data
H4	ADCDAT2	Digital Output	Audio interface 2 ADC digital audio data
J1	ADCLRCLK1/ GPIO1	Digital Input / Output	Audio interface 1 ADC left / right clock / General Purpose pin GPIO 1
F3	ADDR	Digital Input	2-wire (I2C) address select
D9	AGND	Supply	Analogue ground (Return path for AVDD1, AVDD2 and LDO1VDD)
E9, G9	AVDD1	Supply / Analogue Output	Analogue core supply / LDO1 Output
E8	AVDD2	Supply	Bandgap and Jack Detect reference, analogue Class D and FLL supply
G3	BCLK1	Digital Input / Output	Audio interface 1 bit clock
K1	BCLK2	Digital Input / Output	Audio interface 2 bit clock
J8	CPCA	Analogue Output	Charge pump fly-back capacitor pin
K8	CPCB	Analogue Output	Charge pump fly-back capacitor pin
K9	CPGND	Supply	Charge pump ground (Return path for CPVDD)
J9	CPVDD	Supply	Charge pump supply
K7	CPVOUTN	Analogue Output	Charge pump negative supply decoupling pin (HPOUT1L, HPOUT1R)
J7	CPVOUTP	Analogue Output	Charge pump positive supply decoupling pin (HPOUT1L, HPOUT1R)
H1	DACDAT1	Digital Input	Audio interface 1 DAC digital audio data
G4	DACDAT2	Digital Input	Audio interface 2 DAC digital audio data
E1	DBVDD1	Supply	Digital buffer (I/O) supply (core functions and Audio Interface 1)
J2	DBVDD2	Supply	Digital buffer (I/O) supply (for Audio Interface 2)
H5	DBVDD3	Supply	Digital buffer (I/O) supply (for Audio Interface 3)
G2	DCVDD	Supply / Analogue Output	Digital core supply / LDO2 output
K5	DGND	Supply	Digital ground (Return path for DCVDD, DBVDD1, DBVDD2, DBVDD3)
A8	DMICCLK	Digital Output	Digital MIC clock output
G5	GPIO10/ LRCLK3	Digital Input / Output	General Purpose pin GPIO 10 / Audio interface 3 left / right clock
K4	GPIO11/ BCLK3	Digital Input / Output	General Purpose pin GPIO 11 / Audio interface 3 bit clock
K3	GPIO8/ DACDAT3	Digital Input / Output	General Purpose pin GPIO 8 / Audio interface 3 DAC digital audio data
J4	GPIO9/ ADCDAT3	Digital Input / Output	General Purpose pin GPIO 9 / Audio interface 3 ADC digital audio data
H8	HP2GND	Supply	Analogue ground
H6	HPOUT1FB	Analogue Input	HPOUT1L and HPOUT1R ground loop noise rejection feedback
J6	HPOUT1L	Analogue Output	Left headphone output
J5	HPOUT1R	Analogue Output	Right headphone output
G8	HPOUT2N	Analogue Output	Earpiece speaker inverted output
H7	HPOUT2P	Analogue Output	Earpiece speaker non-inverted output
D7	IN1LN	Analogue Input	Left channel single-ended MIC input / Left channel negative differential MIC input
D8	IN1LP	Analogue Input	Left channel line input / Left channel positive differential MIC input
B9	IN1RN	Analogue Input	Right channel single-ended MIC input / Right channel negative differential MIC input

PIN NO	NAME	TYPE	DESCRIPTION
C7	IN1RP	Analogue Input	Right channel line input / Right channel positive differential MIC input
C8	IN2LN/ DMICDAT	Analogue Input / Digital Input	Left channel line input / Left channel negative differential MIC input / Digital MIC data input
C9	IN2LP/VRXN	Analogue Input	Left channel line input / Left channel positive differential MIC input / Mono differential negative input (RXVOICE -)
B7	IN2RN	Analogue Input	Right channel line input / Right channel negative differential MIC input
B8	IN2RP/VRXP	Analogue Input	Left channel line input / Left channel positive differential MIC input / Mono differential positive input (RXVOICE +)
K2	JACKDET	Analogue Input	Headphone jack detection input
A4	LDO1ENA	Digital Input	Enable pin for LDO1
F8	LDO1VDD	Supply	Supply for LDO1
D6	LDO2ENA	Digital Input	Enable pin for LDO2
C6	LINEOUT1N	Analogue Output	Negative mono line output / Positive left or right line output
B6	LINEOUT1P	Analogue Output	Positive mono line output / Positive left line output
A6	LINEOUT2N	Analogue Output	Negative mono line output / Positive left or right line output
B5	LINEOUT2P	Analogue Output	Positive mono line output / Positive left line output
C5	LINEOUTFB	Analogue Input	Line output ground loop noise rejection feedback
G1	LRCLK1	Digital Input / Output	Audio interface 1 left / right clock
J3	LRCLK2	Digital Input / Output	Audio interface 2 left / right clock
F1	MCLK1	Digital Input	Master clock 1
F2	MCLK2	Digital Input	Master clock 2
A9	MICBIAS1	Analogue Output	Microphone bias 1
A7	MICBIAS2	Analogue Output	Microphone bias 2
F9	MICDET	Analogue Input	Microphone & accessory sense input
A5	REFGND	Supply	Analogue ground
H2	SCLK	Digital Input	Control interface clock input
H3	SDA	Digital Input / Output	Control interface data input and output / acknowledge output
B2, C4	SPKGND1	Supply	Ground for speaker driver (Return path for SPKVDD1)
C2, D3	SPKGND2	Supply	Ground for speaker driver (Return path for SPKVDD2)
D5	SPKMODE	Digital Input	Mono / Stereo speaker mode select
A1, B1	SPKOUTLN	Analogue Output	Left speaker negative output
B3, B4	SPKOUTLP	Analogue Output	Left speaker positive output
C1, D1	SPKOUTRN	Analogue Output	Right speaker negative output
C3, D4	SPKOUTRP	Analogue Output	Right speaker positive output
A2, A3	SPKVDD1	Supply	Supply for speaker driver 1 (Left channel)
D2, E2	SPKVDD2	Supply	Supply for speaker driver 2 (Right channel)
E7	VMIDC	Analogue Output	Midrail voltage decoupling capacitor
F7	VREFC	Analogue Output	Bandgap reference decoupling capacitor

The following table identifies the power domain and ground reference associated with each of the input / output pins.

PIN NO	NAME	POWER DOMAIN	GROUND DOMAIN
F4	ADCDAT1	DBVDD1	DGND
H4	ADCDAT2	DBVDD2	DGND
J1	ADCLRCLK1/GPIO1	DBVDD1	DGND
F3	ADDR	DBVDD1	DGND
G3	BCLK1	DBVDD1	DGND
K1	BCLK2	DBVDD2	DGND
H1	DACDAT1	DBVDD1	DGND
G4	DACDAT2	DBVDD2	DGND
A8	DMICCLK	MICBIAS1	AGND
K3	GPIO8/DACDAT3	DBVDD3	DGND
J4	GPIO9/ADCDAT3	DBVDD3	DGND
G5	GPIO10/LRCLK3	DBVDD3	DGND
K4	GPIO11/BCLK3	DBVDD3	DGND
J6	HPOUT1L	CPVOUTP, CPVOUTN	CPGND
J5	HPOUT1R	CPVOUTP, CPVOUTN	CPGND
G8	HPOUT2N	AVDD1	HP2GND
H7	HPOUT2P	AVDD1	HP2GND
D7	IN1LN	AVDD1	AGND
D8	IN1LP	AVDD1	AGND
B9	IN1RN	AVDD1	AGND
C7	IN1RP	AVDD1	AGND
C8	IN2LN/DMICDAT	AVDD1 (IN2LN) or MICBIAS1 (DMICDAT)	AGND
C9	IN2LP/VRXN	AVDD1	AGND
B7	IN2RN	AVDD1	AGND
B8	IN2RP/VRXP	AVDD1	AGND
K2	JACKDET	AVDD2	AGND
A4	LDO1ENA	DBVDD1	DGND
D6	LDO2ENA	DBVDD1	DGND
C6	LINEOUT1N	AVDD1	AGND
B6	LINEOUT1P	AVDD1	AGND
A6	LINEOUT2N	AVDD1	AGND
B5	LINEOUT2P	AVDD1	AGND
G1	LRCLK1	DBVDD1	DGND
J3	LRCLK2	DBVDD2	DGND
F1	MCLK1	DBVDD1	DGND
F2	MCLK2	DBVDD1	DGND
F9	MICDET	MICBIAS2	AGND
H2	SCLK	DBVDD1	DGND
H3	SDA	DBVDD1	DGND
D5	SPKMODE	DBVDD1	DGND
A1, B1	SPKOUTLN	SPKVDD1	SPKGND1
B3, B4	SPKOUTLP	SPKVDD1	SPKGND1
C1, D1	SPKOUTRN	SPKVDD2	SPKGND2
C3, D4	SPKOUTRP	SPKVDD2	SPKGND2

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (AVDD1, DBVDD2, DBVDD3)	-0.3V	+4.5V
Supply voltages (AVDD2, DCVDD, DBVDD1)	-0.3V	+2.5V
Supply voltages (CPVDD)	-0.3V	+2.2V
Supply voltages (SPKVDD1, SPKVDD2, LDO1VDD)	-0.3V	+7.0V
Voltage range digital inputs (DBVDD1 domain)	AGND -0.3V	DBVDD1 +0.3V
Voltage range digital inputs (DBVDD2 domain)	AGND -0.3V	DBVDD2 +0.3V
Voltage range digital inputs (DBVDD3 domain)	AGND -0.3V	DBVDD3 +0.3V
Voltage range digital inputs (DMICDAT)	AGND -0.3V	AVDD1 +0.3V
Voltage range analogue inputs(AVDD1 domain)	AGND -0.3V	AVDD1 +0.3V
Voltage range analogue inputs (MICDET, LINEOUTFB)	AGND -0.3V	AVDD1 +0.3V
Voltage range analogue inputs (HPOUT1FB)	AGND -0.3V	AGND +0.3V
Voltage range analogue inputs (JACKDET) See note 1	CPVOUTN - 0.3V	AVDD2 +0.3V
Ground (DGND, CPGND, SPKGND1, SPKGND2, REFGND, HP2GND)	AGND -0.3V	AGND +0.3V
Operating temperature range, T_A	-40ºC	+85ºC
Junction temperature, T_{JMAX}	-40ºC	+150ºC
Storage temperature after soldering	-65ºC	+150ºC

Notes:

1. CPVOUTN is an internal supply rail, generated by the WM1811A Charge Pump. The CPVOUTN voltage may vary between AGND and -CPVDD.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core) See notes 7, 8	DCVDD	1.00	1.05	2.0	V
Digital supply range (I/O)	DBVDD1	1.62	1.8	2.0	V
Digital supply range (I/O)	DBVDD2, DBVDD3	1.62	1.8	3.6	V
Analogue supply 1 range See notes 3, 4, 5, 6	AVDD1	2.4	3.0	3.3	V
Analogue supply 2 range	AVDD2	1.71	1.8	2.0	V
Charge Pump supply range	CPVDD	1.71	1.8	2.0	V
Speaker supply range	SPKVDD1, SPKVDD2	2.7	5.0	5.5	V
LDO1 supply range	LDO1VDD	2.7	5.0	5.5	V
Ground	DGND, AGND, CPGND, SPKGND1, SPKGND2, REFGND, HP2GND		0		V
Power supply rise time See notes 9, 10, 11	All supplies	1			µs
Operating temperature range	T_A	-40		85	°C

Notes:

1. Analogue, digital and speaker grounds must always be within 0.3V of AGND.
2. There is no power sequencing requirement; the supplies may be enabled in any order.
3. AVDD1 must be less than or equal to SPKVDD1 and SPKVDD2.
4. An internal LDO (powered by LDO1VDD) can be used to provide the AVDD1 supply.
5. When AVDD1 is supplied externally (not from LDO1), the LDO1VDD voltage must be greater than or equal to AVDD1.
6. The WM1811A can operate with AVDD1 tied to 0V; power consumption may be reduced, but the analogue audio functions will not be supported.
7. An internal LDO (powered by DBVDD1) can be used to provide the DCVDD supply.
8. When DCVDD is supplied externally (not from LDO2), the DBVDD1voltage must be greater than or equal to DCVDD.
9. DCVDD and AVDD1 minimum rise times do not apply when these domains are powered using the internal LDOs.
10. The specified minimum power supply rise times assume a minimum decoupling capacitance of 100nF per pin. However, Wolfson strongly advises that the recommended decoupling capacitors are present on the PCB and that appropriate layout guidelines are observed (see “Applications Information” section).
11. The specified minimum power supply rise times also assume a maximum PCB inductance of 10nH between decoupling capacitor and pin.

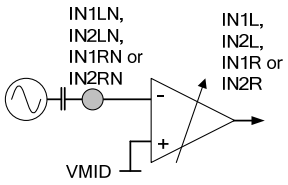
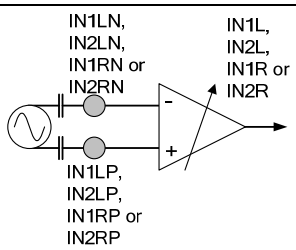
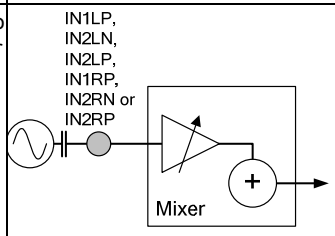
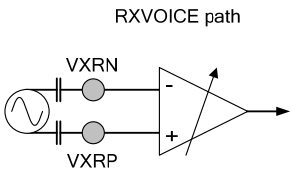
ELECTRICAL CHARACTERISTICS

INPUT SIGNAL LEVEL

Test Conditions

AVDD1 = 3.0V.

With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
A1	Full-Scale PGA Input Signal Level See notes 1, 2, 3 and 4	Single-ended PGA input			1.0 0		Vrms dBV
		Differential PGA input			1.0 0		Vrms dBV
A2	Full-Scale Line Input Signal Level See notes 1, 2, 3 and 4	Single-ended Line input to MIXINL/R, SPKMIXL/R or MIXOUTL/R mixers			1.0 0		Vrms dBV
		Differential mono line input on VRXP/VRXN to RXVOICE			1.0 0		Vrms dBV

Notes:

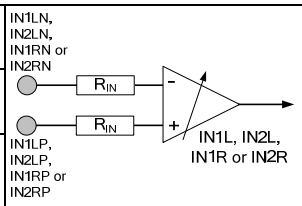
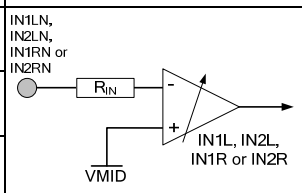
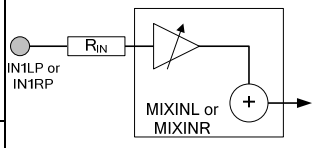
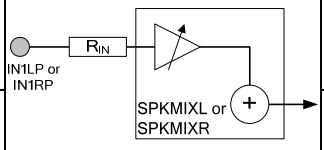
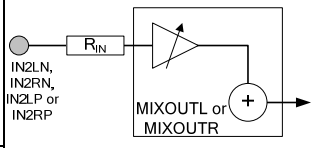
1. The full-scale input signal level changes in proportion with AVDD1. It is calculated as AVDD1/3.0.
2. When mixing line inputs, input PGA outputs and DAC outputs the total signal must not exceed 1.0Vrms (0dBV).
3. A 1.0Vrms differential signal equates to 0.5Vrms/-6dBV per input.
4. A sinusoidal input signal is assumed.

INPUT PIN RESISTANCE

Test Conditions

T_A = +25ºC.

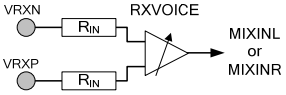
With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
B1	PGA Input Resistance Differential Mode See note 5 See "Applications Information" for details of Input resistance at all PGA Gain settings.	Gain = -16.5dB (INnx_VOL=00h)			53		kΩ
		Gain = 0dB (INnx_VOL=0Bh)			25		kΩ
		Gain = +30dB (INnx_VOL=1Fh)			1.3		kΩ
B2	PGA Input Resistance Single-Ended Mode See note 5 See "Applications Information" for details of Input resistance at all PGA Gain settings.	Gain = -16.5dB (INnx_VOL=00h)			58		kΩ
		Gain = 0dB (INnx_VOL=0Bh)			36		kΩ
		Gain = +30dB (INnx_VOL=1Fh)			2.5		kΩ
B3	Line Input Resistance See note 5	IN1LP to MIXINL, or IN1RP to MIXINR Gain = -12dB (IN1xP_MIXINx_VOL=001)			56		kΩ
		IN1LP to MIXINL, or IN1RP to MIXINR Gain = 0dB (IN1xP_MIXINx_VOL=101)			18		kΩ
		IN1LP to MIXINL, or IN1RP to MIXINR Gain = +6dB (IN1xP_MIXINx_VOL=111)			9.8		kΩ
		IN1LP to MIXINL, or IN1RP to MIXINR Gain = +15dB (IN1xP_MIXINx_VOL=111, IN1xP_MIXINx_BOOST=1)			3.7		kΩ
		IN1LPto SPKMIXL, or IN1RP to SPKMIXR (SPKATTN = -12dB)			89		kΩ
		IN1LPto SPKMIXL, or IN1RP to SPKMIXR (SPKATTN = 0dB)			27		kΩ
		IN2LN, IN2RN, IN2LP or IN2RP to MIXOUTL or MIXOUTR Gain = -9dB (*MIXOUTx_VOL=011)			43		kΩ
		IN2LN,IN2RN, IN2LP or IN2RP to MIXOUTL or MIXOUTR Gain = 0dB			18		kΩ

Test Conditions

T_A = +25ºC.

With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
		(*MIXOUTx_VOL=000)					
		RXVOICE to MIXINLorMIXINR Gain = -12dB (IN2LRP_MIXINx_VOL=001)			48		kΩ
		RXVOICE to MIXINLorMIXINR Gain = 0dB (IN2LRP_MIXINx_VOL=101)			12		kΩ
		RXVOICE to MIXINLorMIXINR Gain = +6dB (IN2LRP_MIXINx_VOL=111)			6.0		kΩ

Note 5: Input resistance will be seen in parallel with the resistance of other enabled input paths from the same pins

PROGRAMMABLE GAINS

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input PGAs (IN1L, IN2L, IN1R and IN2R)						
C1	Minimum Programmable Gain	Guaranteed monotonic		-16.5		dB
C2	Maximum Programmable Gain			+30		dB
C3	Programmable Gain Step Size			1.5		dB
Input Mixers (MIXINL and MIXINR)						
C6	Minimum Programmable Gain	Input PGA signal paths		0		dB
C7	Maximum Programmable Gain			+30		dB
C8	Programmable Gain Step Size			30		dB
C9	Minimum Programmable Gain	Direct IN1xP input signal paths (Note the available gain settings are -12, -9, -6, -3, 0, +3, +6, +15dB)		-12		dB
C10	Maximum Programmable Gain			+15		dB
C11	Programmable Gain Step Size			3		dB
	Minimum Programmable Gain	MIXOUTx Record signal paths		-12		dB
	Maximum Programmable Gain			+6		dB
	Programmable Gain Step Size			3		dB
C12	Minimum Programmable Gain	RXVOICE (VRXP-VRXN) signal paths		-12		dB
C13	Maximum Programmable Gain			+6		dB
C14	Programmable Gain Step Size			3		dB
Output Mixers (MIXOUTL and MIXOUTR)						
C17	Minimum Programmable Gain			-9		dB
C18	Maximum Programmable Gain			0		dB
C19	Programmable Gain Step Size			3		dB
Speaker Mixers (SPKMIXL and SPKMIXR)						
C21	Minimum Programmable Gain			-6		dB
C22	Maximum Programmable Gain			0		dB
C23	Programmable Gain Step Size			6		dB
Output PGAs (HPOUT1LVOL, HPOUT1RVOL, MIXOUTLVOL, MIXOUTRVOL, SPKLVOL and SPKRVOL)						
C25	Minimum Programmable Gain	Guaranteed monotonic		-57		dB
C26	Maximum Programmable Gain			+6		dB
C27	Programmable Gain Step Size			1		dB
Line Output Drivers (LINEOUT1NMIX, LINEOUT1PMIX, LINEOUT2NMIX and LINEOUT2PMIX)						
C29	Minimum Programmable Gain			-6		dB
C30	Maximum Programmable Gain			0		dB
C31	Programmable Gain Step Size			6		dB
EarpieceDriver (HPOUT2MIX)						
C33	Minimum Programmable Gain			-6		dB
C34	Maximum Programmable Gain			0		dB
C35	Programmable Gain Step Size			6		dB
Speaker Output Drivers (SPKOUTLBOOST and SPKOUTRBOOST)						
C38	Minimum Programmable Gain	(Note the available gain settings are 0, +1.5, +3, +4.5, +6, +7.5, +9, +12dB)		0		dB
C39	Maximum Programmable Gain			+12		dB
C40	Programmable Gain Step Size			1.5		dB

OUTPUT DRIVER CHARACTERISTICS

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

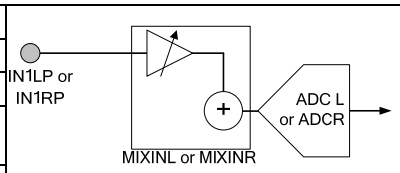
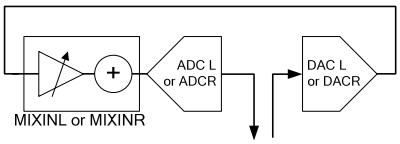
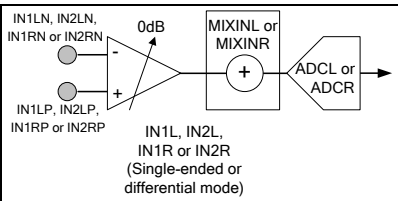
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Line Output Driver (LINEOUT1P, LINEOUT1N, LINEOUT2P, LINEOUT2N)						
	Load resistance		2			kΩ
	Load capacitance	Direct connection			100	pF
		Connection via 1kΩ series resistor			2000	
	Output discharge resistance	LINEOUTn_DISCH=1, VROI=0		8		kΩ
		LINEOUTn_DISCH=1, VROI=1, LINEOUTn_ENA=0		500		Ω
Headphone Output Driver (HPOUT1L, HPOUT1R)						
	Load resistance	Normal operation	15			Ω
		Device survival with load applied indefinitely (see note 6)	100			mΩ
	Load capacitance				500	pF
Earpiece Output Driver (HPOUT2L, HPOUT2R)						
	Load resistance		15			Ω
	Load capacitance	Direct connection			200	pF
	DC offset across load			±5		mV
Speaker Output Driver (SPKOUTLP, SPKOUTLN, SPKOUTRP, SPKOUTRN)						
	Load resistance		4			Ω
	Maximum output power (per channel)	Design rating		2		W
	DC offset across load			±5		mV
	SPKVDD leakage current	Sum of $I_{SPKVDD1}$ + $I_{SPKVDD2}$		1		µA

Note 6: In typical applications, the PCB trace resistance, jack contact resistanceand ESR of any series passive components (eg. inductor or ferrite bead) are sufficient to provide this minimum resistance; additional series components are not required.

ADC INPUT PATH PERFORMANCE

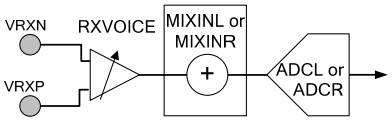
Test Conditions

AVDD1=3.0V (powered from LDO1), DCVDD=1.05V (powered from LDO2), AVDD2=DBVDD1=DBVDD2=DBVDD3=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25ºC, 1kHz sinusoidal signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
D1	**Line Inputs to ADC via MIXINL and MIXINR**						
	SNR	A-weighted			94		dB
	THD	-1dBV input			-83		dB
	THD+N	-1dBV input			-81		dB
	Channel Separation (L/R)				-100		dB
	PSRR (SPKVDDn, LDO1VDD)	100mV (pk-pk) 217Hz			92		dB
	PSRR (AVDD2, CPVDD, DBVDDn)	100mV (pk-pk) 217Hz			94		dB
D2	**Record Path (DACs to ADCs via MIXINL and MIXINR)**						
	SNR	A-weighted			92		dB
	THD	-1dBFS input			-74		dB
	THD+N	-1dBFS input			-72		dB
	Channel Separation (L/R)				-95		dB
	PSRR (SPKVDDn, LDO1VDD)	100mV (pk-pk) 217Hz			97		dB
	PSRR (AVDD2, CPVDD, DBVDDn)	100mV (pk-pk) 217Hz			94		dB
D3	**Input PGAs to ADC via MIXINL or MIXINR**						
	SNR	A-weighted		84	95		dB
	THD	-1dBV input			-82	-72	dB
	THD+N	-1dBV input			-80	-70	dB
	Channel Separation (L/R)				-100		dB
	PSRR (SPKVDDn, LDO1VDD)	100mV (pk-pk) 217Hz			100		dB
	PSRR (AVDD2, CPVDD, DBVDDn)	100mV (pk-pk) 217Hz			95		dB
	CMRR	Input PGA=-16.5dB 1V (pk-pk) 217Hz			49		dB
		Input PGA = 0dB 1V (pk-pk) 217Hz			58		
		Input PGA = +30dB 1V (pk-pk) 217Hz			73		
	Note that the Input PGA gain is controlled using the INnx_VOL registers.						

Test Conditions

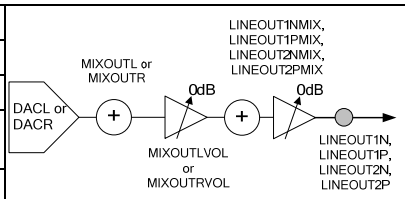
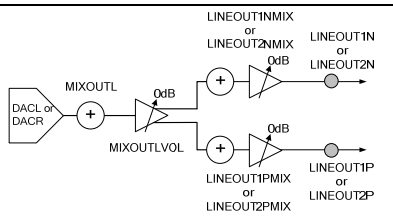
AVDD1=3.0V (powered from LDO1), DCVDD=1.05V (powered from LDO2), AVDD2=DBVDD1=DBVDD2=DBVDD3=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25ºC, 1kHz sinusoidal signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
D4	**RXVOICE to ADCL or ADCR**						
	SNR	A-weighted			94		dB
	THD	-1dBV input			-84		dB
	THD+N	-1dBV input			-82		dB
	PSRR (SPKVDDn, LDO1VDD)	100mV (pk-pk) 217Hz			102		dB
	PSRR (AVDD2, CPVDD, DBVDDn)	100mV (pk-pk) 217Hz			97		dB
	CMRR	Input PGA = -12dB 1V (pk-pk) 217Hz			56		dB
		Input PGA = 0dB 1V (pk-pk) 217Hz			63		
		Input PGA = +6dB 1V (pk-pk) 217Hz			61		
	Note that the Input PGA gain is controlled using the IN2LRP_MIXINx_VOL registers.						

DAC OUTPUT PATH PERFORMANCE

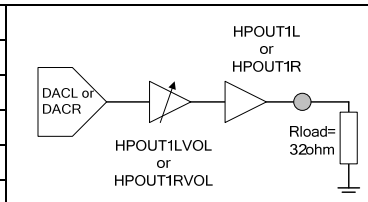
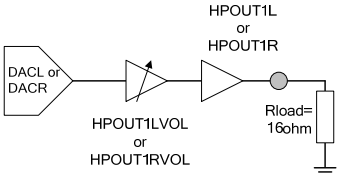
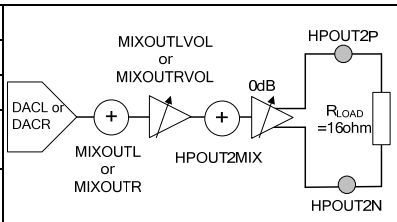
Test Conditions

AVDD1=3.0V (powered from LDO1), DCVDD=1.05V (powered from LDO2), AVDD2=DBVDD1=DBVDD2=DBVDD3=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25ºC, 1kHz sinusoidal signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
E1	**DAC to Single-Ended Line Output (Load = 10kΩ // 50pF)**						
	SNR	A-weighted			93		dB
	THD	0dBFS input			-82		dB
	THD+N	0dBFS input			-80		dB
	Channel Separation (L/R)				-90		dB
	PSRR (SPKVDDn, LDO1VDD)	100mV (pk-pk) 217Hz			85		dB
	PSRR (AVDD2, CPVDD, DBVDDn)	100mV (pk-pk) 217Hz			95		dB
	LINEOUTFB rejection	LINEOUTn_FB=1, 100mV (pk-pk) 217Hz			38		dB
E2	**DAC to Differential Line Output (Load = 10kΩ // 50pF)**						
	SNR	A-weighted			97		dB
	THD	0dBFS input			-82		dB
	THD+N	0dBFS input			-80		dB
	Channel Separation (L/R)				-90		dB
	PSRR (SPKVDDn, LDO1VDD)	100mV (pk-pk) 217Hz			87		dB
	PSRR (AVDD2, CPVDD, DBVDDn)	100mV (pk-pk) 217Hz			88		dB

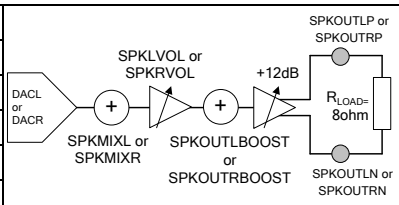
Test Conditions

AVDD1=3.0V (powered from LDO1), DCVDD=1.05V (powered from LDO2), AVDD2=DBVDD1=DBVDD2=DBVDD3=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25ºC, 1kHz sinusoidal signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
E5	**DAC to Headphone on HPOUT1L or HPOUT1R (Load = 32Ω)**						
	SNR (A-weighted)	DAC_OSR128=1			100		dB
		DAC_OSR128=0			97		dB
	THD	P_O=20mW			-74		dB
	THD+N	P_O=20mW			-72		dB
	THD	P_O=5mW			-76		dB
	THD+N	P_O=5mW			-74		dB
	Channel Separation (L/R)				-95		dB
	PSRR (SPKVDDn, LDO1VDD)	100mV (pk-pk) 217Hz			96		dB
	PSRR (AVDD2, CPVDD, DBVDDn)	100mV (pk-pk) 217Hz			89		dB
	HPOUT1FB rejection	100mV (pk-pk) 217Hz			29		dB
E6	**DAC to Headphone on HPOUT1L or HPOUT1R (Load = 16Ω)**						
	SNR (A-weighted)	DAC_OSR128=1		90	100		dB
		DAC_OSR128=0			97		dB
	THD	P_O=20mW			-82		dB
	THD+N	P_O=20mW			-80		dB
	THD	P_O=5mW			-83	-73	dB
	THD+N	P_O=5mW			-81	-71	dB
	Channel Separation (L/R)				-95		dB
	PSRR (SPKVDDn, LDO1VDD)	100mV (pk-pk) 217Hz			98		dB
	PSRR (AVDD2, CPVDD, DBVDDn)	100mV (pk-pk) 217Hz			88		dB
	HPOUT1FB rejection	100mV (pk-pk) 217Hz			29		dB
E9	**DAC to Earpiece Driver (Load = 16Ω BTL)**						
	SNR	A-weighted			97		dB
	THD	P_O=50mW			-71		dB
	THD+N	P_O=50mW			-69		dB
	PSRR (SPKVDDn, LDO1VDD)	100mV (pk-pk) 217Hz			95		dB
	PSRR (AVDD2, CPVDD, DBVDDn)	100mV (pk-pk) 217Hz			96		dB

Test Conditions

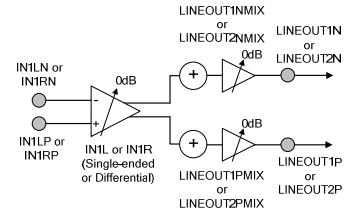
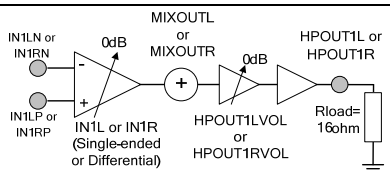
AVDD1=3.0V (powered from LDO1), DCVDD=1.05V (powered from LDO2), AVDD2=DBVDD1=DBVDD2=DBVDD3=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25ºC, 1kHz sinusoidal signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
E12	**DAC to Speaker Outputs (Load = 8Ω + 22μH BTL, Stereo Mode)** **+12dB boost (SPKOUTx_BOOST = 111)**						
	SNR	A-weighted		85	94		dB
	THD	P_O=0.5W			-65		dB
	THD+N	P_O=0.5W			-63	-53	dB
	THD	P_O=1.0W			-70		dB
	THD+N	P_O=1.0W			-68		dB
	Channel Separation (L/R)				-80		dB
	PSRR (SPKVDDn, LDO1VDD)	100mV (pk-pk) 217Hz			72		dB
	PSRR (AVDD2, CPVDD, DBVDDn)	100mV (pk-pk) 217Hz			78		dB

BYPASS PATH PERFORMANCE

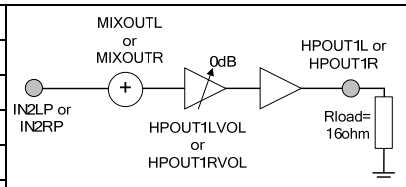
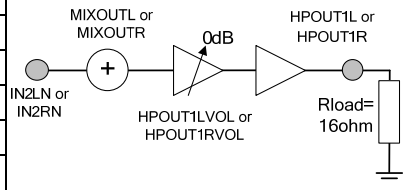
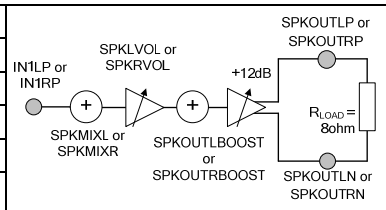
Test Conditions

AVDD1=3.0V (powered from LDO1), DCVDD=1.05V (powered from LDO2), AVDD2=DBVDD1=DBVDD2=DBVDD3=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25ºC, 1kHz sinusoidal signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
F1	**Input PGA to Differential Line Output (Load = 10kΩ // 50pF)**						
	SNR	A-weighted			100		dB
	THD	0dBV output			-90		dB
	THD+N	0dBV output			-87		dB
	PSRR (SPKVDDn, LDO1VDD)	100mV (pk-pk) 217Hz			90		dB
	PSRR (AVDD2, CPVDD, DBVDDn)	100mV (pk-pk) 217Hz			90		dB
	CMRR	Input PGA = 0dB 1V (pk-pk) 217Hz			58		dB
	Note that the Input PGA gain is controlled using the INnx_VOL registers.						
F3	**Input PGA to Headphone via MIXOUTL or MIXOUTR (Load = 16Ω)**						
	SNR	A-weighted			98		dB
	THD	P_O=20mW			-89		dB
	THD+N	P_O=20mW			-87		dB
	THD	P_O=5mW			-86		dB
	THD+N	P_O=5mW			-84		dB
	Channel Separation (L/R)				-95		dB
	PSRR (SPKVDDn, LDO1VDD)	100mV (pk-pk) 217Hz			100		dB
	PSRR (AVDD2, CPVDD, DBVDDn)	100mV (pk-pk) 217Hz			89		dB
	CMRR	Input PGA = 0dB 1V (pk-pk) 217Hz			58		dB
	Note that the Input PGA gain is controlled using the INnx_VOL registers.						

Test Conditions

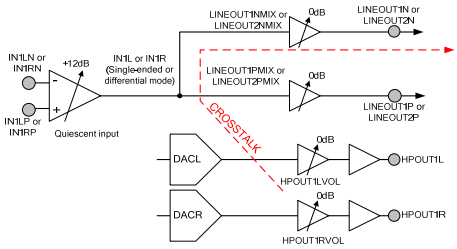
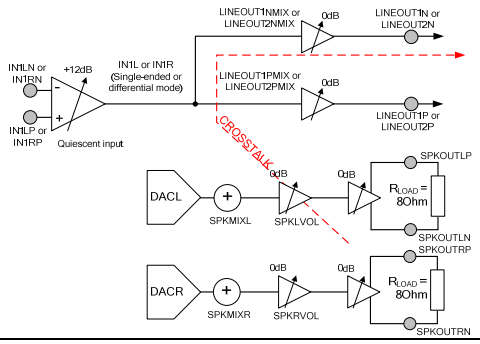
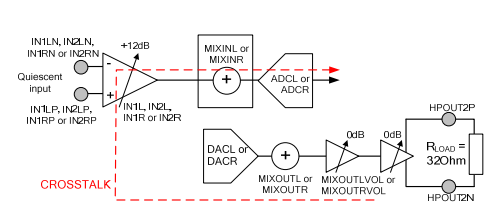
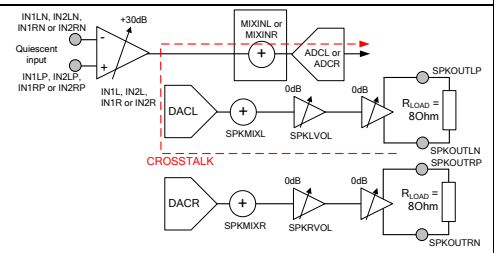
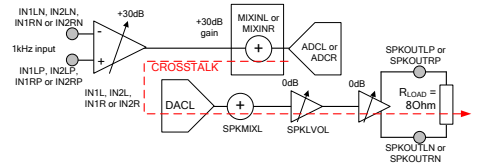
AVDD1=3.0V (powered from LDO1), DCVDD=1.05V (powered from LDO2), AVDD2=DBVDD1=DBVDD2=DBVDD3=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V, DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25ºC, 1kHz sinusoidal signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
F2	**Line Input (IN2LP or IN2RP) to Headphone via MIXOUTL or MIXOUTR (Load = 16Ω)**						
	SNR	A-weighted			100		dB
	THD	P_O=20mW			-86		dB
	THD+N	P_O=20mW			-84		dB
	THD	P_O=5mW			-84		dB
	THD+N	P_O=5mW			-82		dB
	PSRR (SPKVDDn, LDO1VDD)	100mV (pk-pk) 217Hz			93		dB
	PSRR (AVDD2, CPVDD, DBVDDn)	100mV (pk-pk) 217Hz			87		dB
F4	**Line Input (IN2LN or IN2RN) to Headphone via MIXOUTL or MIXOUTR (Load = 16Ω)**						
	SNR	A-weighted			100		dB
	THD	P_O=20mW			-84		dB
	THD+N	P_O=20mW			-82		dB
	THD	P_O=5mW			-82		dB
	THD+N	P_O=5mW			-80		dB
	Channel Separation (L/R)				-95		dB
	PSRR (SPKVDDn, LDO1VDD)	100mV (pk-pk) 217Hz			94		dB
	PSRR (AVDD2, CPVDD, DBVDDn)	100mV (pk-pk) 217Hz			87		dB
F8	**Line Input to Speaker Outputs via SPKMIXL or SPKMIXR (Load = 8Ω + 22µHBTL, Stereo Mode) +12dB boost (SPKOUTx_BOOST = 111)**						
	SNR	A-weighted			93		dB
	THD	P_O=0.5W			-62		dB
	THD+N	P_O=0.5W			-60		dB
	THD	P_O=1.0W			-67		dB
	THD+N	P_O=1.0W			-65		dB
	PSRR (SPKVDDn, LDO1VDD)	100mV (pk-pk) 217Hz			68		dB
	PSRR (AVDD2, CPVDD, DBVDDn)	100mV (pk-pk) 217Hz			76		dB

MULTI-PATH CROSSTALK

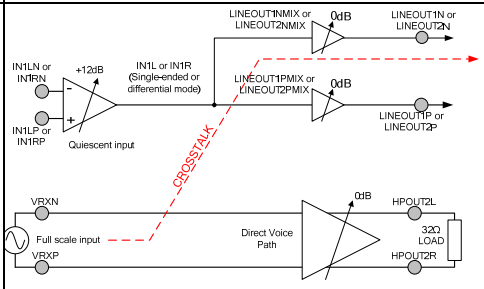
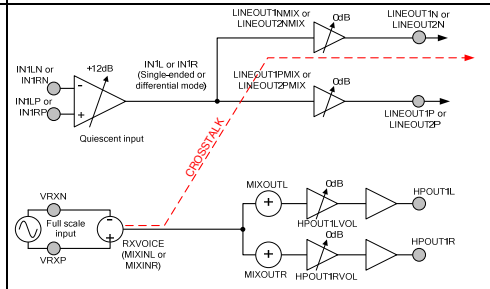
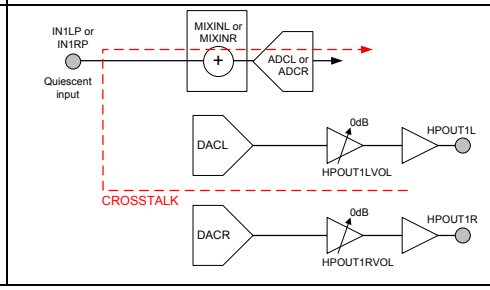
Test Conditions

AVDD1=3.0V (powered from LDO1), DCVDD=1.05V (powered from LDO2),
AVDD2=DBVDD1=DBVDD2=DBVDD3=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V,
DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25ºC, 1kHz sinusoidal signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
G1	Headset Voice Call: DAC/Headset to Tx Voice Separation 1kHz 0dBFS DAC playback direct to HPOUT1L and HPOUT1R; Quiescent input on IN1LN/P or IN1RN/P (Gain=+12dB), differential line output; Measure crosstalk at differential line output			85		dB
G2	Speakerphone Voice Call: DAC/Speaker to Tx Voice Separation 1kHz 0dBFS DAC playback to speakers, 1W/chan output; Quiescent input on IN1LN/P or IN1RN/P (Gain=+12dB), differential line output; Measure crosstalk at differential line output			100		dB
G3	Earpiece PCM Voice Call: RXVOICE to Tx Voice Separation fs=8kHz for ADC and DAC, DAC_SB_FILT=1; -5dBFS, DAC output to HPOUT2P-HPOUT2N; Quiescent input on input PGA (Gain=+12dB) to ADC via MIXINL or MIXINR; Measure crosstalk at ADC output			110		dB
G4	Speakerphone PCM Voice Call: DAC/Speaker to ADC Separation fs=8kHz for ADC and DAC, DAC_SB_FILT=1; 0dBFS DAC output to speaker (1W output); ADC record from input PGA (Gain=+30dB); Measure crosstalk on ADC output			90		dB
G5	Speakerphone PCM Voice Call: ADC to DAC/Speaker Separation fs=8kHz for ADC and DAC, DAC_SB_FILT=1; Quiescent DAC output to speaker; ADC record from input PGA (Gain=+30dB + 30dB boost); Measure crosstalk on speaker output			95		dB

Test Conditions

AVDD1=3.0V (powered from LDO1), DCVDD=1.05V (powered from LDO2),
AVDD2=DBVDD1=DBVDD2=DBVDD3=CPVDD=1.8V, LDO1VDD=SPKVDD1=SPKVDD2=5V,
DGND=AGND=CPGND=SPKGND1=SPKGND2=HP2GND=0V,
T_A = +25ºC, 1kHz sinusoidal signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
G6	Earpiece Speaker Voice Call: Tx Voice and RXVOICE Separation 1kHz Full scale differential input on VRXP-VRXN, output to HPOUT2P-HPOUT2N; Quiescent input on IN1LN/P or IN1RN/P (Gain=+12dB), differential line output; Measure crosstalk at differential line output			100		dB
G7	Headset Voice Call: Tx Voice and RXVOICE Separation 1kHz full scale differential input on VRXP-VRXN via RXVOICE to MIXOUTL and MIXOUTR, output to HPOUT1L and HPOUT1R; Quiescent input on IN1LN/P or IN1RN/P (Gain=+12dB), differential line output; Measure crosstalk at differential line output			90		dB
G8	Stereo Line Record and Playback: DAC/Headset to ADC Separation -5dBFS input to DACs, playback to HPOUT1L and HPOUT1R; ADC record from line input; Measure crosstalk on ADC output			95		dB

DIGITAL INPUT / OUTPUT

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input / Output (except DMICDAT and DMICCLK) **Digital I/O is referenced to DBVDD1, DBVDD2 or DBVDD3. See "Pin Description" for the domain applicable to each pin.**						
H16	Input HIGH Level, V_{IH}		0.8×DBVDDn			V
H17	Input LOW Level, V_{IL}				0.2×DBVDDn	V
Note that digital input pins should not be left unconnected / floating.						
H18	Output HIGH Level, V_{OH}	I_{OH}=1mA	0.8×DBVDDn			V
H19	Output LOW Level, V_{OL}	I_{OL}=-1mA			0.2×DBVDDn	V
H20	Input capacitance			10		pF
H21	Input leakage		-0.9		0.9	µA
Digital Microphone Input / Output (DMICDAT and DMICCLK)						
H22	DMICDAT input HIGH Level, V_{IH}		0.65 × MICBIAS1			V
H23	DMICDAT input LOW Level, V_{IL}				0.35 x MICBIAS1	V
H24	DMICCLK output HIGH Level, V_{OH}	I_{OH}=1mA	0.8 × MICBIAS1			V
H25	DMICCLK output LOW Level, V_{OL}	I_{OL}=-1mA			0.2 x MICBIAS1	V
H26	Input capacitance			10		pF
H27	Input leakage		-0.9		0.9	µA

DIGITAL FILTER CHARACTERISTICS

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Decimation Filter						
	Passband	+/- 0.05dB	0		0.454 fs	
		-6dB		0.5fs		
	Passband Ripple				+/- 0.05	dB
	Stopband		0.546 fs			
	Stopband Attenuation	f > 0.546 fs	85			dB
	Group Delay				2	ms
DAC Interpolation Filter						
	Passband	+/- 0.05dB	0		0.454 fs	
		-6dB		0.5 fs		
	Passband Ripple	0.454 fs			+/- 0.05	dB
	Stopband		0.546 fs			
	Stopband Attenuation	f> 0.546 fs	85			dB
	Group Delay				2	ms