WM72016

16Kbit Secure F-RAM Memory with Gen-2 RFID Access & Serial Port Direct Memory Access

RAMTRON

DESCRIPTION

The WM72016 is a RFID transponder IC with nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory, or F-RAM, is nonvolatile and performs reads and writes like a RAM. It provides reliable data retention for 20 years while eliminating the complexities, overhead, and system level reliability problems caused by EEPROM and other nonvolatile memories.

Unlike EEPROM's, the WM72016 write operations are zero power – there is no power or speed premium paid for executing writes into the WM72016 as compared to read power and speed. Operation of the memory is fully symmetric: it has an equivalent read and write range.

The WM72016's RFID interface is compatible with the EPC Class-1 Generation-2 UHF RFID Protocol for Communications at 860 MHz – 960 MHz, Version 1.2.0 Specification for RFID Air Interface.

The WM72016 is a two chip configuration offered in various forms: standard IC package or wafers. All specifications discussed herein are applicable to the combined chipset operation.

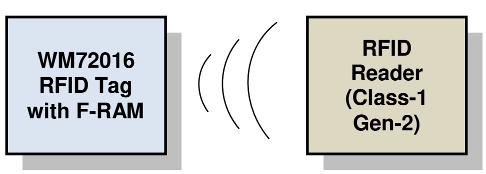

Figure 1. System Block Diagram

FEATURES

16 Kbit Ferroelectric Nonvolatile RAM

- Organized as 1024 x 16 bits
- Very High Read/Write Endurance (> 10^{14})
- 20-Year Data Retention
- Gamma Stability Demonstrated to > 30 kGy
- Symmetric Read/Write Operation
- Advanced High-Reliability Ferroelectric Process

Interface and Security Features

- EPC Class 1 Gen2 (ISO18000-6C) RFID Compatible Interface (revision 1.2.0)
- 192-Bit Memory: 96-Bit Electronic Product Code™ (EPC), 32-Bit Access Password, 32-Bit KILL Password, 64-Bit TID Memory (Factory Programmed and Locked)
- Inventory, Read, Write and Erase features
- Kill Command
- Block Permalock Command
- Access Command
- UHF carrier frequencies from 860 MHz to 960 MHz ISM band, ASK demodulation
- Tag-to-reader link frequencies up to 640Kbps
- Reader-to-tag asymptotical transmission rates up to 128Kbps
- Supports FM0 and MMS data encoding formats
- Serial Port Interface

Custom Features

- Stored Address Pointer to Improve Data Write Speed
- Stored Address Pointer Lock
- Block Write Command
- Variable USER memory block size support
- Interrupt Generation

Ultra Low Power Operation

- Memory Read/Write Sensitivity: < -6 dBm (typ.)

Industry Standard Configurations

- Industrial Temperature -40° C to +85° C
- Bumped Wafers
- 8-pin UDFN

This is a product that has fixed target specifications but are subject to change pending characterization results.

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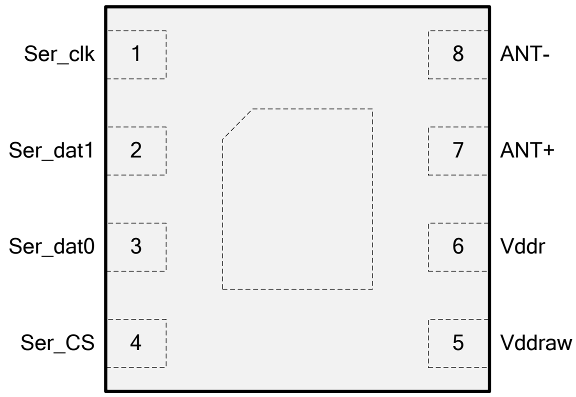
PIN CONFIGURATION (UDFN PACKAGE)

Top View
(PCB Layout)



3.0 mm × 3.0 mm body, 0.65 mm pad pitch

PIN DESCRIPTION

Pin Name	Pin Number	Type	Description
ANT+, ANT-	7, 8	Input	RFID Antenna. Connect to external RFID antenna terminals. Connect ANT- to external RFID antenna terminal, also acts as ground.
Ser_clk	1	Input	Serial interface clock
Ser_dat1, Ser_dat0	2, 3	I/O	Serial interface bi-directional data
Ser_CS	4	I/O	Serial interface bi-directional chip select/interrupt
Vddraw	5	PWR	Power supply input pin. DC supply (2.1V to 3.0V)
Vddr	6	PWR	Power supply output pin. This supply is internally generated via the RF field. The Vddr and Vddraw pins are tied together for most applications. Contact the factory for other applications such as battery assisted systems.

FUNCTIONAL DESCRIPTION

The WM72016 is a non-volatile memory device with an industry standard UHF RFID interface that enables processing data in and out of memory as a generic passive RFID transponder. Unlike other transponder ICs, the WM72016 transponder IC contains high density symmetric read/write F-RAM memory that enables unique applications of an RFID solution.

When combined with an appropriate antenna design, WM72016 will power up with energy harvested directly from the RF field. Following an internally generated reset state, the IC configures itself according to pre-programmed configuration settings that were stored in F-RAM non-volatile memory at wafer probe, packaged parts test, or end unit transponder personalization at end-user depot. Configuration settings are read out of memory and applied prior to enabling data transmission in or out of memory.

As specified in the Gen2 standard, the chip receives and processes commands transmitted by the RFID interrogator (reader). All required and most optional commands are supported. In addition to these, WM72016 supports a number of custom commands that take advantage of F-RAM's unique ultra low power and symmetrical characteristics.

Referring to Figure 2, the transponder IC's consist of an RFID interface, control and authentication logic, F-RAM memory, and power management unit. The external antenna is connected directly to the RFID interface where the RF signal is rectified with high efficiency Schottky diode based rectifier. The rectified voltage is multiplied up within the Schottky array and then regulated to supply power to on-chip resources.

Also included in the RFID Interface is a modulator/demodulator that detects incoming signals and modulates the input impedance to enable backscattering of returned signals. The control and authentication logic processes commands to enable access in and out of F-RAM memory.

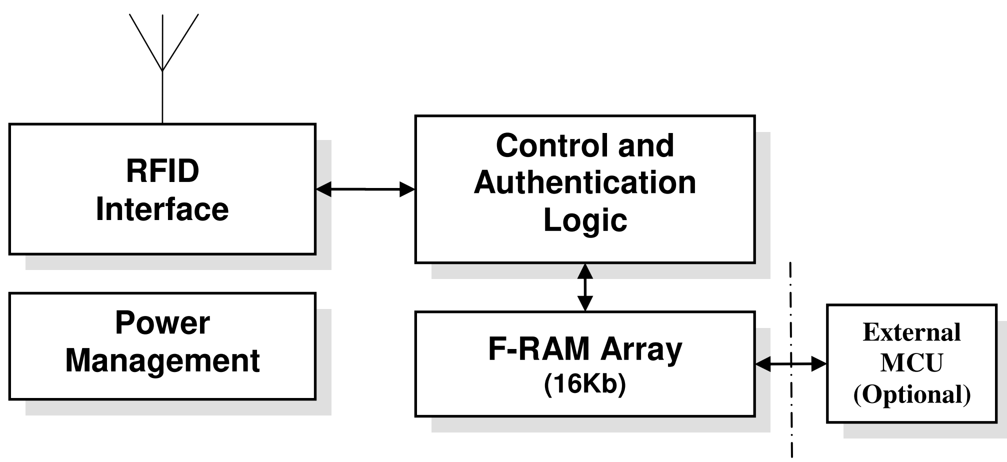


Figure 2. Block Diagram

MEMORY MAP

WM72016's memory is partitioned according to the logical and physical mapping shown in the table below.

Table 1: Memory Map

DSPI Address	Gen-2 Memory Bank	Gen-2 Address	Word Pointer (EBV8)	Description
0x000	RESERVED	0x000	0x00	Kill Password[31:16]
0x001	RESERVED	0x001	0x01	Kill Password[15:0]
0x002	RESERVED	0x002	0x02	Access Password[31:16]
0x003	RESERVED	0x003	0x03	Access Password[15:0]
0x004	EPC	0x000	0x00	CRC
0x005	EPC	0x001	0x01	PC
0x006	EPC	0x002	0x02	EPC - Word 0 (MSW)
0x007	EPC	0x003	0x03	EPC - Word 1
0x008	EPC	0x004	0x04	EPC - Word 2
0x009	EPC	0x005	0x05	EPC - Word 3
0x00A	EPC	0x006	0x06	EPC - Word 4
0x00B	EPC	0x007	0x07	EPC - Word 5 (LSW)
0x00C	EPC	0x008	0x08	EPC - read memory
0x00D	EPC	0x009	0x09	EPC - read memory
0x00E	SERVICE	0x00A	0x0A	RESERVED
0x00F	SERVICE	0x00B	0x0B	RESERVED
0x010	TID	0x000	0x00	TID - Word 0: x**E201**
0x011	TID	0x001	0x01	TID - Word 1: x**6216**
0x012	TID	0x002	0x02	TID - Word 2: Serial #1
0x013	TID	0x003	0x03	TID - Word 3: Serial #2
0x014	USER	0x000	0x00	RESERVED
0x015	USER	0x001	0x01	RFU
0x016	USER	0x002	0x02	Control/Status Register
0x017	USER	0x003	0x03	Working Stored Address Register
0x018	USER	0x004	0x04	
0x019	USER	0x005	0x05	
0x01A	USER	0x006	0x06	USER Memory - Start
0x01B	USER	0x007	0x07	
0x0FE	USER	0x0EA	0x816A	
0x0FF	USER	0x0EB	0x816B	
0x100	USER	0x0EC	0x816C	
0x101	USER	0x0ED	0x816D	
…	…	…	…	
0x1FE	USER	0x1EA	0x836A	
0x1FF	USER	0x1EB	0x836B	
0x200	USER	0x1EC	0x836C	
0x201	USER	0x1ED	0x836D	
…	…	…	…	
0x3BA	USER	0x3A6	0x8726	
0x3BB	USER	0x3A7	0x8727	**16k Memory: END**
0x3BC	USER	0x3A8	0x8728	**(BLK_SIZE = 1 word/block)**
0x3BD	USER	0x3A9	0x8729	
0x3BE	USER	0x3AA	0x872A	

DSPI Address	Gen-2 Memory Bank	Gen-2 Address	Word Pointer (EBV8)	Description
…	…	…	…	
0x3DA	USER	0x3C6	0x8746	
0x3DB	USER	0x3C7	0x8747	
0x3DC	USER	0x3C8	0x8748	**16k Memory: END (BLK_SIZE = 2 words/block)**
0x3DD	USER	0x3C9	0x8749	
0x3DE	USER	0x3CA	0x874A	
…	…	…	…	
0x3EA	USER	0x3D6	0x8756	
0x3EB	USER	0x3D7	0x8757	
0x3EC	USER	0x3D8	0x8758	**16k Memory: END (BLK_SIZE = 4 words/block)**
0x3ED	USER	0x3D9	0x8759	
0x3EE	USER	0x3DA	0x875A	
…	…	…	…	
0x3F3	USER	0x3DF	0x875F	
0x3F4	USER	0x3E0	0x8760	**16k Memory: END (BLK_SIZE = 8 words/block)**
0x3F5	USER	0x3E1	0x8761	
0x3F6	USER	0x3E2	0x8762	
0x3F7	USER	0x3E3	0x8763	
0x3F8	USER	0x3E4	0x8764	**16k Memory: END (BLK_SIZE = 16 words/block)**
0x3F9	USER	0x3E5	0x8765	
0x3FA	USER	0x3E6	0x8766	**16k Memory: END (BLK_SIZE = 32 words/block)**
0x3FB	USER	0x3E7	0x8767	**(BLK_SIZE > 32 words/block)**
0x3FC	USER	0x3E8	0x8768	RESERVED
0x3FD	USER	0x3E9	0x8769	RESERVED
0x3FE	USER	0x3EA	0x876A	RESERVED
0x3FF	USER	0x3EB	0x876B	RESERVED

NOTE: When accessing the memory through the DSPI serial port, care must be taken to ensure that reserved memory required to store critical parameters for the operation of the device is not altered.

GEN2 WM72016 MEMORY BANKS

The RFID memory banks reside in Ramtron's non-volatile F-RAM memory. F-RAM brings many benefits to the WM72016. The first benefit is the size of the memory itself – 16k-bit, most of which is available in the USER memory bank. F-RAM's impact on the Gen2 protocol is most dramatically seen when writing to WM72016 memory. Unlike EEPROM memory, no charge pump or memory soak time is required to write to WM72016 memory resulting in zero time and zero power penalties. The write cycle is completed immediately, allowing an interrogator to continue writing additional data to memory with no time penalty incurred due to the memory itself. A comparison between F-RAM and EEPROM memories is shown in Figure 3. The figure shows the minimum number of Gen2 instructions required to perform a SELECT, INVENTORY, and ACCESS sequence of commands to write a data word to memory. The same interrogator command sequence is transmitted to the WM72016 and an EEPROM-based RFID. The effect of the EEPROM time penalty is shown within the context of the protocol.

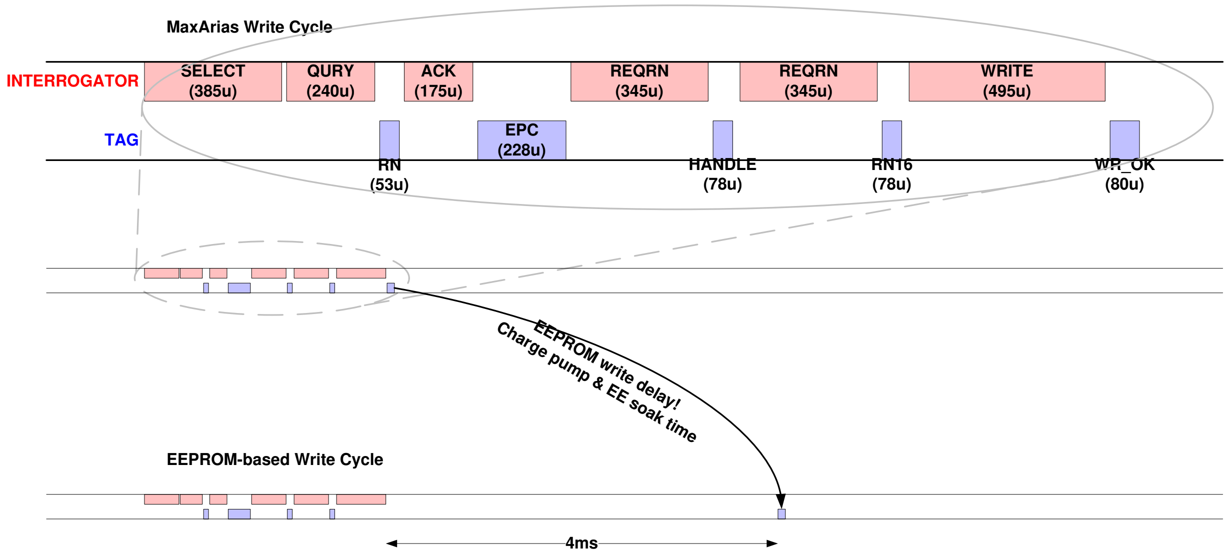


Figure 3. Gen2 Memory Write Cycle Comparison: F-RAM vs. EEPROM Memories

RESERVED: KILL Password:
The kill password provides a mechanism to permanently disable the WM72016 RFID from responding to any and all Gen2 interrogator commands. The mandatory KILL command can be issued by a RFID interrogator in either the OPEN or SECURED states. The WM72016 is permanently killed through a four-instruction sequence of REQRN and KILL commands as detailed in the Gen2 standard. The KILL password is a 32-bit value stored as 2 16-bit data words in reserved memory. The most significant KILL password is stored in reserved memory bank address 0x00 with the least significant word stored in reserved memory bank address 0x01. The kill function can be permanently disabled by setting both KILL password words to 0x0000, and permanently locking the KILL password in the reserved memory bank. Once the kill password has been set, it should be permanently locked using the LOCK command. The WM72016 is shipped from the factory with the kill password memory unlocked. The kill state of the device only affects the Gen2 RFID processor – the DSPI serial port will continue to function normally.

RESERVED: ACCESS Password:
The access password provides a security mechanism to prevent unauthorized RFID interrogators from writing to WM72016 memory. Non-zero access passwords require the WM72016 be placed in the SECURED state prior to writing to it. This is accomplished through a four-instruction sequence of REQRN and ACCESS commands as described in the Gen2 standard. An access password with a value of zero requires no authentication prior to writing to WM72016 memory. The ACCESS password is a 32-bit value stored as two 16-bit data words in reserved memory. The most significant ACCESS password is stored in reserved memory bank address 0x02 with the least significant word stored in reserved memory bank address 0x03. Once the access password has been set, it should be permanently locked using the LOCK command. The WM72016 is shipped from the factory with the access password memory unlocked. The value of the access password has no effect on the functionality of the DSPI serial port.

EPC Memory Bank:
The EPC memory bank accommodates 8 words: 1 protocol control (PC) word, a 6-word (96-bit) memory space for an EPC identifier, and a 1-word CRC. The CRC word is calculated as part of the WM72016 power-on initialization routine and written into the EPC memory bank address 0x00. The PC and 6-word EPC identifier are completely programmable. The Protocol Control field is shown in Figure 4.

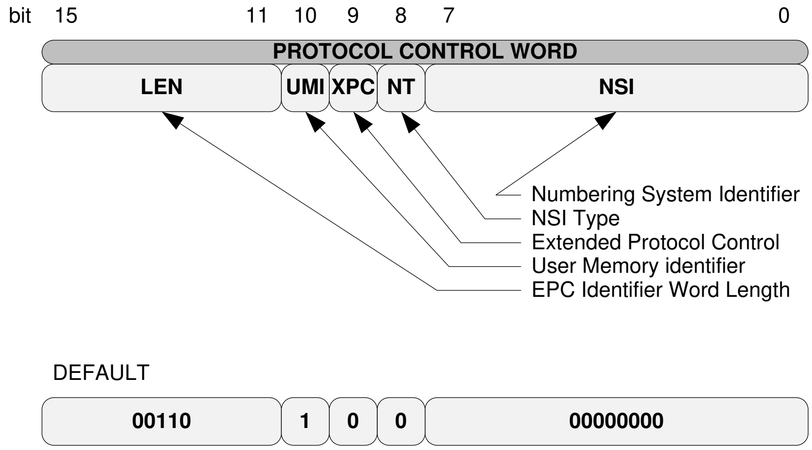


Figure 4. EPC Protocol Control Word

The five most significant bits of the PC indicates the size of the EPC identifier in words – for a 96-bit (6-word) EPC identifier, the PC should be programmed to 0b0011_0xxx_xxxx_xxxx. The LEN parameter of the PC word may not be greater than 0b00110 – a LEN parameter of 0b00000 has an EPC identifier length of zero words resulting in only the PC and CRC words when WM72016 is acknowledged. The UMI bit (User Memory Identifier) is asserted to a logic one by WM72016 and mapped to bit 10 of the PC word. In the event the host writes a logic zero to the UMI bit, the memory location will be written with a logic zero, however the backscattered EPC identifier will assert the UMI bit to a logic one which is also used in the calculation of the CRC. WM72016 does not support extended protocol control and should be written with a logic zero. PC word bits 8 down to 0 of the PC word are factory-initialized to zero. The WM72016 is shipped from the factory with the EPC memory bank unlocked.

TID Memory Bank:

The TID memory bank consists of 4 words (64 bits), and is defined as shown in Table 2. The TID memory bank is permanently locked at the factory and obeys the ISO/IEC 15963 numbering convention.

Table 2: TID memory Bank Fields

Bit Field	Value (hex)	Description
00_h – 07_h	E2	ISO/IEC 15963 class-identifier
08_h – 13_h	016	Mask-Designer Identifier (MDID) – Ramtron International
14_h – $1F_h$	216	Tag model number
20_h – $3F_h$		32-bit unique identifier

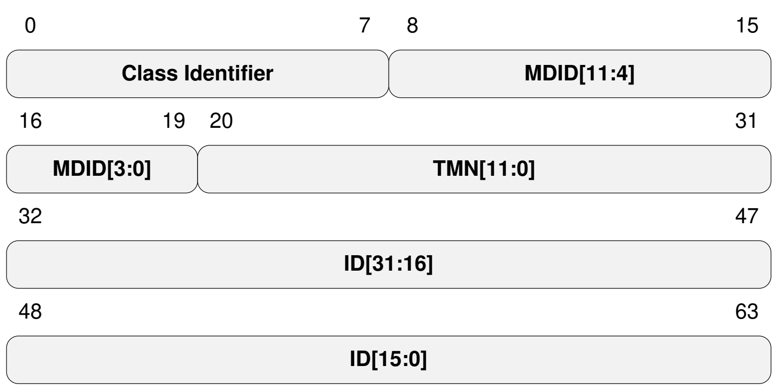


Figure 5. TID Memory Bank Fields

USER Memory Bank:
The USER memory bank comprises two special-function control words, factory-reserved words, and up to 993 available memory locations. Refer to Table 1 for detail on the WM72016 memory structure. The USER memory bank may be completely locked through the LOCK command. WM72016 also supports the BLOCKPERMALOCK command providing the ability to lock contiguous words of USER memory, with word block sizes as small as a single word up to a maximum block size of 128 words. The USER memory bank ships from the factory completely unlocked.

TAG-TO-READER DATA ENCODING

The WM72016 supports both encoding formats defined in the Gen2 standard:

- FM0 baseband (FM0)
- Miller modulation of a subcarrier (MMS)

Data encoding is performed in the WM72016 as described in the Gen2 standard. A FM0 data symbol is transmitted with period *T* which is defined by the tag-to-reader link frequency. The difference between a logic 0 and a logic 1 is defined by an additional mid-bit transition for a logic 0 as shown below in Figure 6. Data encoding using Miller modulation of a subcarrier (MMS) is further defined by a rate parameter *M* that defines the number of link frequency cycles per data bit: 2, 4, or 8, resulting in data encoding defined as MMS2, MMS4, or MMS8 respectively. MMS data encoding results in a phase inversion of the sub-carrier frequency when one of the following conditions occurs:

- At the mid-bit of a logic 1 data bit, or
- At the bit-boundary of two consecutive logic 0s.

The following set of four figures depicts the data bit values “00”, “01”, “10” and “11” for FM0 and MMS data encoding formats. The same link frequency is shown for all cases, however the MMS parameter *M* lengthens the baseband bit period by 2, 4, or 8 as shown in Figure 7, Figure 8, and Figure 9.

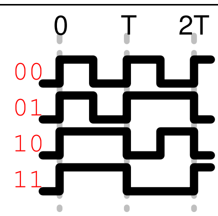


Figure 6. FM0 Data Encoding

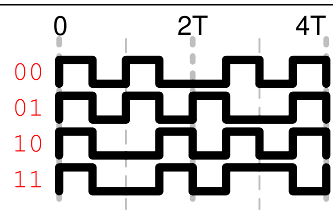


Figure 7. MMS2 Data Encoding

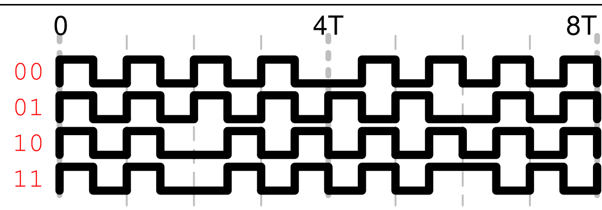


Figure 8. MMS4 Data Encoding

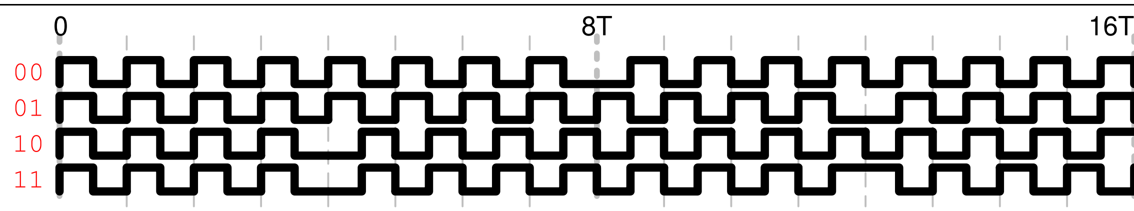


Figure 9. MMS8 Data Encoding

CONTROL/STATUS REGISTER

Accessing the unique features of WM72016 is accomplished through the Control/Status register in F-RAM non-volatile memory. The register is located at physical address 0x016 or USER memory address 0x002. The Control/Status word register is organized as shown in Table 3 below. Care should be exercised when writing the Control/Status register word if it is to remain unlocked.

LCK	PLCK	RFU	BW EN	BLKSIZ	WRP	WRP EN	ALCK	AINC

Figure 10. Control/Status Register

Table 3: Control/Status Word Register

<table>
<tr><th>Bit</th><th>Mnemonic</th><th>Function</th><th>Initial Value</th></tr>
<tr><td>15</td><td>LOCK</td><td rowspan="2">Memory locking of this register.
<table>
<tr><th>LOCK</th><th>PERMALOCK</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>0</td><td>Register unlocked</td></tr>
<tr><td>0</td><td>1</td><td>Register permanently unlocked</td></tr>
<tr><td>1</td><td>0</td><td>Register writeable only from the SECURED state</td></tr>
<tr><td>1</td><td>1</td><td>Register permanently locked</td></tr>
</table></td><td>0</td></tr>
<tr><td>14</td><td>PERMALOCK</td><td>0</td></tr>
<tr><td>13</td><td>RFU</td><td>Reserved for future use</td><td>0</td></tr>
<tr><td>12</td><td>RFU</td><td>Reserved for future use</td><td>0</td></tr>
<tr><td>11</td><td>RFU</td><td>Reserved for future use</td><td>0</td></tr>
<tr><td>10</td><td>RFU</td><td>Reserved for future use</td><td>0</td></tr>
<tr><td>9</td><td>RFU</td><td>Reserved for future use</td><td>0</td></tr>
<tr><td>8</td><td>RFU</td><td>Reserved for future use</td><td>0</td></tr>
<tr><td>7</td><td>BLKWREN</td><td>Enables use of the custom command BLOCKWRITE.</td><td>1</td></tr>
<tr><td>6</td><td>BLKSIZ[2]</td><td rowspan="3">USER memory block size.
<table>
<tr><th>BLKSIZ[2:0]</th><th># words</th><th>BLKSIZ[2:0]</th><th># words</th></tr>
<tr><td>000</td><td>1</td><td>100</td><td>16</td></tr>
<tr><td>001</td><td>2</td><td>101</td><td>32</td></tr>
<tr><td>010</td><td>4</td><td>110</td><td>64</td></tr>
<tr><td>011</td><td>8</td><td>111</td><td>128</td></tr>
</table></td><td>1</td></tr>
<tr><td>5</td><td>BLKSIZ[1]</td><td>1</td></tr>
<tr><td>4</td><td>BLKSIZ[0]</td><td>0</td></tr>
<tr><td>3</td><td>WRPSTAT</td><td>Indicates if the Working Stored Address has wrapped.
<table>
<tr><th>Logic State</th><th>Description</th></tr>
<tr><td>0</td><td>Wrapping has not occurred</td></tr>
<tr><td>1</td><td>Wrapping has occurred at least once</td></tr>
</table></td><td>0</td></tr>
<tr><td>2</td><td>WRPEN</td><td>Enables wrapping of the Working Stored Address when it reaches the top of logical memory.
<table>
<tr><th>Logic State</th><th>Description</th></tr>
<tr><td>0</td><td>DISABLE memory wrapping</td></tr>
<tr><td>1</td><td>ENABLE memory wrapping.</td></tr>
</table></td><td>0</td></tr>
<tr><td>1</td><td>AUTOLOCK</td><td>Enable Automatic Locking of all user memory between the start of USER memory and the Working Stored Address register.
<table>
<tr><th>Logic State</th><th>Description</th></tr>
<tr><td>0</td><td>Auto-lock DISABLED</td></tr>
<tr><td>1</td><td>Auto-lock ENABLED</td></tr>
</table></td><td>0</td></tr>
<tr><td>0</td><td>AUTOINCR</td><td>Enable the Working Stored Address word to Auto-Increment when performing an unaddressed write cycle.
<table>
<tr><th>Logic State</th><th>Description</th></tr>
<tr><td>0</td><td>DISABLE auto-increment of stored address register</td></tr>
<tr><td>1</td><td>ENABLE auto-increment of stored address register</td></tr>
</table></td><td>0</td></tr>
</table>

Upon power up, WM72016's control logic reads the control word out of memory and configures itself accordingly. User applications may change the control word as needed providing the register has not been permanently locked. The Control/Status word may be read by the application at any time.

Register Locking: The LOCK and PERMALOCK control bits are implemented in a similar manner as locking bits used for Gen2 memory bank locking with the exception that the lock control bits are incorporated into the register they are locking. As such, attention needs to be placed on how the contents of the *Control/Status* word are written when the register is not completely unlocked.

Table 4: Control/Status Word Locking

LOCK	PERMA-LOCK	Description
0	0	Register unlocked. All control bits, including the LOCK and PERMALOCK bits can be written to from the OPEN or SECURED states.
0	1	Register permanently unlocked. All control bits can be written from the OPEN or SECURED states. The LOCK and PERMALOCK bits must be set to logic values 0 and 1 respectively when writing the *Control/Status* word.
1	0	Register locked. All control bits can be written to only from the SECURED state. The register cannot be written to in the OPEN state. The LOCK and PERMALOCK bits must be set to logic values 1 and 0 respectively when writing the *Control/Status* word.
1	1	Register permanently locked. The register cannot be written in any circumstance.

Block Write Enable: The BLKWREN control bit enables usage of the WM72016 custom command BLOCKWRITE. The BLKWREN parameter is internally updated during power-on WM72016 initialization. In the event the host application toggles the state of BLKWREN either through the Gen2 or serial interfaces, a WM72016 power cycle is required to reflect the change.

Block Size: The 3 BLKSIZ[2:0] control bits adjust the USER memory block sizes as shown in Table 5. This provides a host application the ultimate flexibility in determining a balance between the USER memory requirements and the granularity of the number of USER memory words per block. The larger the granularity of the block size, the greater amount of available USER memory. The effect of the block size on available USER memory is shown in Table 1. The total number of USER memory words available as a function of the block size is shown in Table 5 below. It is of utmost importance that the 3-bit block size is not modified once set, which would otherwise result in corruption of block permalock status bits.

Table 5: Available USER Memory

Memory	BLKSIZ	Words/Block	Free USER Memory (words)
16k	000	1	931
16k	001	2	963
16k	010	4	979
16k	011	8	987
16k	100	16	991
16k	101	32	993
16k	110	64	993
16k	111	128	993

Wrap Status: The WRPSTAT status bit is asserted to a logic one when the following conditions are true:

(a) WRPEN=1, AUTOINCR=1 and AUTOLOCK=0,
(b) The contents of the *Working Stored Address* register address the last USER memory location, and
(c) An unaddressed WRITE command is received.

The WRPSTAT can be cleared by the RFID interrogator by writing a logic zero to the WRPSTAT bit.

Wrap Enable: Asserting the WRPEN control bit to a logic one enables the USER memory wrapping feature. The wrap enable feature allows the stored address pointer to wrap back to the factory-set initial stored address value of 0x006. In this manner, the WM72016 memory acts as a circular buffer. Clearing the WRPEN control bit disables wrapping resulting in a write-once memory. In this case, when the *Working Stored Address* reaches the end of user memory, no additional unaddressed write cycles will be possible. The WRPEN and AUTOLOCK control bits are mutually exclusive – only one of the two control bits may be asserted at any given time.

Auto Lock Enable: Asserting the AUTOLOCK control bit to a logic one enables memory locking of the USER memory span between the start of USER memory and the *Working Stored Address*. The AUTOLOCK and WRPEN control bits are mutually exclusive – only one of the two control bits may be asserted at any given time. The automatic locking feature can only be used when AUTOINCR is asserted to a logic one.

Auto Increment: Asserting AUTOINCR control bit to a logic one enables the Working Stored Address increment function. Upon receiving an unaddressed write cycle, the WM72016 increments the pointer stored in the *Working Stored Address* register to point to the next free memory location then writes the cover-coded data word to the respective memory location. This functionality removes any requirement for a RFID interrogator to determine where free USER memory is located and manipulating the memory pointer itself.

WORKING STORED ADDRESS

To better utilize the F-RAM's fast write capability, memory has been architected using an optional *Working Stored Address* register. The stored address function enables automation of the storage of large blocks of user data, such as pedigree or tracking information. This feature enables a RFID interrogator the ability to use a standard Gen2 WRITE command using a designated address of 0x3FFF (0xFF7F EBV-formatted) as a redirect pointer to use the contents of the *Working Stored Address* register – this is referred to as an ***unaddressed write (UNADDR_WRITE)***. The *Working Stored Address* is a USER memory address pointer used to address the first available USER memory data word as shown in Figure 12. The *Working Stored Address* is a read/write register located at address 0x003 in USER memory. It may be used to address USER memory only – it is an address pointer to a memory location within the USER memory bank and cannot be used to address other memory banks or memory regions in the WM72016. It may be manually updated by simply writing to USER memory address 0x003 or will automatically increment when the AUTOINCR control bit in the *Control/Status* register is asserted to a logic one and an unaddressed write command is received.

LCK	PLCK	RFU	INIT EN	ADDR[9:0]

Figure 11. Working Stored Address Register

Table 6: Working Stored Address – Bit Definitions

<table>
<tr><th>Bit</th><th>Mnemonic</th><th>Function</th><th>Initial Value</th></tr>
<tr><td>15</td><td>LOCK</td><td rowspan="2">Memory locking of this register.
<table>
<tr><th>LOCK</th><th>PERMALOCK</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>0</td><td>Register unlocked</td></tr>
<tr><td>0</td><td>1</td><td>Register permanently unlocked</td></tr>
<tr><td>1</td><td>0</td><td>Register writeable only from the SECURED state</td></tr>
<tr><td>1</td><td>1</td><td>Register permanently locked</td></tr>
</table></td><td>0</td></tr>
<tr><td>14</td><td>PERMALOCK</td><td>0</td></tr>
<tr><td>13:11</td><td>RFU</td><td>Reserved for future use</td><td>0</td></tr>
<tr><td>10</td><td>INITEN</td><td>When asserted to a logic '1', sets the contents of the Initial Stored Address register with the value defined in the 10-bit address field in bits 9 through 0 written to this register using a Gen2 write instruction.</td><td>0</td></tr>
<tr><td>9:0</td><td>ADDR</td><td>Working stored address pointer</td><td>006</td></tr>
</table>

Working Stored Address Pointer	Gen-2 Memory Bank	Gen-2 Address	Description	
	RESERVED	0x000 - 0X003	RESERVED - passwords	MEMORY UNAVAILABLE
	EPC	0x000 - 0x009	EPC	
	SERVICE	0x00A	RESERVED	
	SERVICE	0x00B	RESERVED	
	TID	0x000 - 0x003	TID	
	USER	0x000	RESERVED	
	USER	0x001	RFU	
	USER	0x002	Control/Status Register	
	USER	0x003	Working Stored Address Register: 0x0006	
	USER	0x004		
	USER	0x005		
⇨	USER	0x006	**USER Memory - START**	AVAILABLE MEMORY
	USER	0x007		
	USER	0x008		
	USER	…	…	
	USER		**USER Memory - END**	

Figure 12. USER Memory Bank: Working Stored Address Register

The syntax for an unaddressed write command is shown in Figure 13 below. All protocol requirements governing implementation of a WRITE command also apply to the UNADDR_WRITE command.

WRITE (0xC3)	Membank (0b11)	WordPtr (0xF7FF)	16-bit Data (cover-coded) (0x*NNNN*)	Handle (0x*HHHH*)	CRC-16 (0x*CCCC*)

Figure 13. Unaddressed Write Syntax

Upon reception of a valid UNADDR_WRITE command, the WM72016 examines the state of the AUTOINCR control bit:

AUTOINCR=0: The 16-bit data word cover-coded in the unaddressed write instruction is written to the memory address stored in the *Working Stored Address* register. The contents of the *Working Stored Address* register remain unaltered. To avoid the memory being over-written, the *Working Stored Address* register must be manually updated.

AUTOINCR=1: The *Working Stored Address* register is incremented by one, followed by the 16-bit data word being written to memory. The contents of the *Working Stored Address* register will reflect the memory address just written to. A single unaddressed write cycle is shown in Figure 14 with the AUTOINCR control bit set to a logic one. The *Working Stored Address* has an initial value of 0x0006 as shown in Figure 12. An unaddressed write cycle (with AUTOINCR=1) increments the address pointer to 0x0007 followed by a write cycle to the WM72016 memory resulting in data word $DATA_0$ being written to USER memory address 0x007. Figure 15 depicts an additional seven discrete unaddressed write cycles (REQRN command for cover-coding not shown). Prior to unaddressed write commands, the *Working Stored Address* has a memory address of $addr_n$. An unaddressed write command with data payload $DATA_n$ is written to $addr_{n+1}$; the following unaddressed write command with data payload $DATA_{n+1}$ is written to $addr_{n+2}$, and so on. Upon completion of the final unaddressed write command, the memory pointer contents of the *Working Stored Address* will be $addr_{n+8}$, reflecting the memory address of the last unaddressed write cycle. In this manner, the RFID interrogator does not have to read the memory contents to discern the next available memory location. **This substantially reduces the time required in the RF field yielding greater throughput of a population of tags**.

The *Working Stored Address* pointer will be factory-initialized to the start of USER memory then managed by the memory controller or the host application as required.

Working Stored Address Pointer	Gen-2 Memory Bank	Gen-2 Address	Description	
	RESERVED	0x000 - 0X003	RESERVED - passwords	MEMORY UNAVAILABLE
	EPC	0x000 - 0x009	EPC	
	SERVICE	0x00A	RESERVED	
	SERVICE	0x00B	RESERVED	
	TID	0x000 - 0x003	TID	
	USER	0x000	RESERVED	
	USER	0x001	RFU	
	USER	0x002	Control/Status Register	
	USER	0x003	Working Stored Address Register: 0x0007	
	USER	0x004		
	USER	0x005		
	USER	0x006	USER Memory - START	AVAILABLE MEMORY
⇨	USER	0x007	**UNADDR_WRITE: DATA0**	
	USER	0x008		
	USER	…	…	
	USER		**USER Memory - END**	

Figure 14. Single Unaddressed Write Cycle, AUTOINCR=1

Working Stored Address Pointer	Gen-2 Memory Bank	Gen-2 Address	Description	
	RESERVED	0x000 - 0X003	RESERVED - passwords	MEMORY UNAVAILABLE
	EPC	0x000 - 0x009	EPC	
	SERVICE	0x00A	RESERVED	
	SERVICE	0x00B	RESERVED	
	TID	0x000 - 0x003	TID	
	USER	0x000	RESERVED	
	USER	0x001	RFU	
	USER	0x002	Control/Status Register	
	USER	0x003	Working Stored Address Register: 0x000E	
	USER	0x004		
	USER	0x005		
	USER	0x006	USER Memory - START	AVAILABLE MEMORY
	USER	0x007	UNADDR_WRITE: DATA0	
	USER	0x008	UNADDR_WRITE: DATA1	
	USER	0x009	UNADDR_WRITE: DATA2	
	USER	0x00A	UNADDR_WRITE: DATA3	
	USER	0x00B	UNADDR_WRITE: DATA4	
	USER	0x00C	UNADDR_WRITE: DATA5	
	USER	0x00D	UNADDR_WRITE: DATA6	
⇨	USER	0x00E	**UNADDR_WRITE: DATA7**	
	USER	0x00F		
	USER	0x010		
	USER	0x011		
	…	…	…	
	…	…	…	
			USER Memory - END	

Figure 15. Multiple Unaddressed Write Cycles, AUTOINCR=1

INITIAL STORED ADDRESS

The *Initial Stored Address* is a preset address pointer that is loaded into the *Working Stored Address* when a memory wrap occurs after an unaddressed write command is executed. A memory wrap only occurs if the WRPEN control bit is asserted to a logic one and the AUTOLOCK control bit is cleared to a logic zero in the *Control/Status* register and the *Working Stored Address* points to the last free memory location in the USER memory bank (last memory location depends on the set block size).

The contents of the *Initial Stored Address* may be altered by setting the INITEN bit to a logic one through a Gen2 write cycle to the *Working Stored Address* register – refer to Table 6 above. When the INITEN control bit is set during a write cycle, the contents of the *Working Stored Address* register in USER memory 0x003 are not affected.

Use of an *Initial Stored Address* register provides flexibility when using the wrap enable feature of WM72016. It may be set to the start of USER memory, allowing the entire USER memory bank to be utilized. Alternatively, it may be set to a higher memory address within the USER memory bank. This mechanism would provide for a *static* USER memory bank and a *dynamic* USER memory bank as shown in Figure 16 below. In the example shown in Figure 16, the *Working Stored Address* points to address 0x3F8 after having written user_log_data[*n*] with an unaddressed write command. The subsequent unaddressed write cycle will increment (wrap) the *Working Stored Address* to the value defined by the *Initial Stored Address*, defined in this example as 0x000A, and write the value user_log_data[*n*+1] to USER memory bank 0x00A, over-writing the previous data contents user_log_data[0]. In the example shown, four memory locations are used for *static* memory, or memory that will not be over-written when a wrap condition has occurred.

Working Stored Address Pointer	Gen-2 Memory Bank	Gen-2 Address	Description	
	RESERVED	0x000 - 0X003	RESERVED - passwords	MEMORY UNAVAILABLE
	EPC	0x000 - 0x009	EPC	
	SERVICE	0x00A	RESERVED	
	SERVICE	0x00B	RESERVED	
	TID	0x000 - 0x003	TID	
	USER	0x000	RESERVED	
	USER	0x001	RFU	
	USER	0x002	Control/Status Register	
	USER	0x003	Working Stored Address Register: 0x03F8	
	USER	0x004		
	USER	0x005		
Initial Stored Address	USER	0x006	user_static_data0	**STATIC**
	USER	0x007	user_static_data1	
	USER	0x008	user_static_data2	
	USER	0x009	user_static_data3	
	USER	0x00A	user_log_data[0], user_log_data[*n*+1]	**DYNAMIC**
	USER	0x00B	user_log_data[1]	
	USER	0x00C	…	
	USER	0x00D	…	
	USER	0x00E	…	
	USER	0x00F	…	
	USER	0x010	…	
	USER	0x011	…	
	…	…	…	
	USER	0x3F7	user_log_data[*n*-1]	
⇨	USER	0x3F8	user_log_data[*n*]	

Figure 16. Initial Stored Address Example – Block Size = 128 words/block

The Initial Stored Address is factory-initialized with a value of 0x0006 (USER memory bank address 0x006).

SUPPORTED COMMANDS

The WM72016 supports the following Select, Inventory, and Access commands as described in the EPCglobal class 1 generation 2 UHF RFID Specification. Please refer to the referenced document for detailed descriptions of these commands.

- Select
- Query
- QueryAdjust
- QueryRep
- ACK
- NAK
- Req_RN
- Read
- Write
- Kill
- Lock
- Access
- BlockWrite *
- BlockPermalock

MAXARIAS GEN2 CUSTOM COMMAND: BLOCKWRITE

The WM72016 supports a customized version of the BLOCKWRITE command to support unique features within the device. The BLOCKWRITE command optional feature is enabled by asserting the BLKWREN control bit in the *Control/Status* register to a logic one, after which the WM72016 will require a power cycle to initialize itself. To support other features within the WM72016, the BLOCKWRITE command uses the address stored in the *Working Stored Address* register. The address pointer passed in the BLOCKWRITE command is the physical address 0x3FFF (EBV formatted address = 0xF7FF), representing the same address used for unaddressed write cycles. A single BLOCKWRITE command carries a maximum data payload of 127 words. BLOCKWRITE commands with data payloads greater than 127 words may optionally be written to unlocked memory, however WM72016 will not acknowledge the BLOCKWRITE command with a success message. In this event, the host interrogator may perform one or more READ cycles to verify USER memory data contents.

Prior to transmitting a BLOCKWRITE command, the interrogator must set the *Working Stored Address* register through a standard Gen2 WRITE command. The BLOCKWRITE command is shown in Figure 17 below.

BLKWRITE (0xC7)	Membank (0b11)	WordPtr (0xF7FF)	WordCnt (0x*NN*)	Data (x*NN* × 16-bit data)	Handle (0x*HHHH*)	CRC-16 (0x*CCCC*)

Figure 17. Block Write Syntax

BLOCKWRITE commands do not support the auto-increment feature used for UNADDR_WRITE commands. As such, the *Working Stored Address* must be manually updated by the host interrogator and will not be altered by a BLOCKWRITE command. When using the streaming capabilities of the BLOCKWRITE command, care should be taken to consider the logic state of the AUTOINCR control bit. As with UNADDR_WRITE commands, the *Working Stored Address* register is incremented prior to writing data to memory when AUTOINCR=1 affecting the first USER memory address written to. Figure 18 shows an 8-word BLOCKWRITE command with AUTOINCR=0; Figure 19 shows a BLOCKWRITE command with AUTOINCR=1. In the respective figures, when AUTOINCR=0, data is written starting at the address defined by the *Working Stored Address* register – 0x006; when AUTOINCR=1, data is written starting at the next *free* address defined by the contents of the *Working Stored Address* incremented by one, or 0x007. It is important to note that in both cases, the value stored in the *Working Stored Address* register does not change for a BLOCKWRITE command – in the example shown, it remains at a value of 0x006.

Working Stored Address Pointer	Gen-2 Memory Bank	Gen-2 Address	Description	
	RESERVED	0x000 - 0X003	RESERVED - passwords	MEMORY UNAVAILABLE
	EPC	0x000 - 0x009	EPC	
	SERVICE	0x00A	RESERVED	
	SERVICE	0x00B	RESERVED	
	TID	0x000 - 0x003	TID	
	USER	0x000	RESERVED	
	USER	0x001	RFU	
	USER	0x002	Control/Status Register	
	USER	0x003	Working Stored Address Register: 0x0006	
	USER	0x004		
	USER	0x005		
⇨	USER	0x006	BLKWRITE: DATA0	AVAILABLE MEMORY
	USER	0x007	BLKWRITE: DATA1	
	USER	0x008	BLKWRITE: DATA2	
	USER	0x009	BLKWRITE: DATA3	
	USER	0x00A	BLKWRITE: DATA4	
	USER	0x00B	BLKWRITE: DATA5	
	USER	0x00C	BLKWRITE: DATA6	
	USER	0x00D	BLKWRITE: DATA7	
	USER	0x00E		
	USER	0x00F		
	…	…	…	
			USER Memory - END	

Figure 18. BLOCKWRITE Command: AUTOINCR=0

Working Stored Address Pointer	Gen-2 Memory Bank	Gen-2 Address	Description	
	RESERVED	0x000 - 0X003	RESERVED - passwords	MEMORY UNAVAILABLE
	EPC	0x000 - 0x009	EPC	
	SERVICE	0x00A	RESERVED	
	SERVICE	0x00B	RESERVED	
	TID	0x000 - 0x003	TID	
	USER	0x000	RESERVED	
	USER	0x001	RFU	
	USER	0x002	Control/Status Register	
	USER	0x003	Working Stored Address Register: 0x0006	
	USER	0x004		
	USER	0x005		
⇨	USER	0x006	USER Memory - START	AVAILABLE MEMORY
	USER	0x007	BLKWRITE: DATA0	
	USER	0x008	BLKWRITE: DATA1	
	USER	0x009	BLKWRITE: DATA2	
	USER	0x00A	BLKWRITE: DATA3	
	USER	0x00B	BLKWRITE: DATA4	
	USER	0x00C	BLKWRITE: DATA5	
	USER	0x00D	BLKWRITE: DATA6	
	USER	0x00E	BLKWRITE: DATA7	
	USER	0x00F		
	…	…	…	
			USER Memory - END	

Figure 19. BLOCKWRITE Command: AUTOINCR=1

DUAL SERIAL PERIPHERAL INTERFACE (DSPI)

The WM72016 employs a dual serial peripheral interface (DSPI) bus providing a serial communication port to a host microcontroller for the purpose of directly reading and writing memory. The interface uses four pins as shown in Table 7.

Table 7: DSPI Interface

Signal Name	Direction	Description
CS	INPUT/OUTPUT	Chip Select
D1	INPUT/OUTPUT	Data bit 1
D0	INPUT/OUTPUT	Data bit 0
CLK	INPUT	Clock

A single DSPI access cycle is composed of a 16-bit instruction word and a 16-bit data word as shown in Figure 20. A DSPI read/write cycle is initiated by asserting CS high followed by 16 clock cycles. The host drives the first set of 8 clock cycles to write 2 data bytes comprising an instruction word – the second set of 8 clock cycles are required for the 16-bit data word. Command and data bits are interleaved across two DSPI data signals in such a manner that odd numbered bits are driven on one data signal while even numbered bits are driven on the other data signal as shown in section *DSPI Serial Port Timing*. This results in a 16-bit word transfer on the D0 and D1 signals every 8 clock cycles.

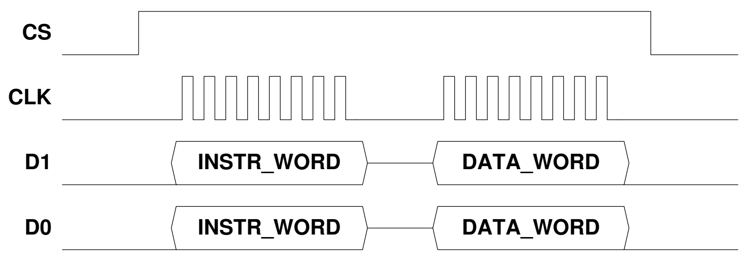


Figure 20. DSPI Cycle

WRITE CYCLES

DSPI write cycles are detailed in the *DSPI Serial Port Timing* section. The host microcontroller drives all four DSPI signals for the duration of the cycle. The WM72016 uses the rising edge of CLK to shift in the 2 data bits presented on the D1 and D0 signals. The host microcontroller shall obey the timing constraints detailed in Table 10. The host microcontroller asserts the 2 data bits prior to the rising edge of CLK. The host microcontroller shifts the instruction word with the first set of 8 CLK cycles and shifts the data word on the second set of 8 CLK cycles. The write cycle is terminated by clearing the CS signal.

READ CYCLES

SPI read cycles are detailed in the *DSPI Serial Port Timing* section. The host microcontroller shall transmit the instruction word in the same manner as done for DSPI write cycles. The WM72016 uses the rising edge of CLK to shift in the 2 data bits presented on the D1 and D0 signals. Once the instruction word has been completely transmitted and the CLK signal has been cleared to a logic zero, the host shall tri-state the D1 and D0 signals allowing the WM72016 to drive the data bits for the remainder of the read cycle. The WM72016 shall shift a pair of data bits on D1 and D0 on the rising edge of CLK – the host shall use the falling edge of CLK to capture the data pair into its shift register. The host shall transmit a total of 8 CLK cycles to receive the entire data word, after which it clears the CS to a logic zero to terminate the read cycle.

The syntax of the instruction word is detailed in Table 8.

Table 8: DSPI Instruction Word

Signal	Mnemonic	Bit	Description
Read/Write	RW	15	Read/Write Control. RW is asserted to logic '1' for a read cycle. RW is cleared to logic '0' for write cycle.
Opcode	OP	14..10	Instruction opcode.
Address	A	9..0	MaxArias physical memory address.

The read/write bit (RW) sets the data direction of the subsequent data word(s). On write cycles, the host continues to drives the DSPI bus with data words. The MaxArias WM72016 uses the rising edge of CLK to register data presented on D0 and D1. On read cycles, the host drives the DSPI bus with the instruction word, then tri-states the D0 and D1 signals while receiving data from MaxArias memory.

The opcode (OP) parameter is a 5-bit value that can take on the following values shown in Table 9.

Table 9: DSPI Opcode Values

Mnemonic	OPCODE[4:0]	Description
NORM	11001	Normal read/write instruction.
INTEND	11101	Interrupt end instruction.
-	*Others*	RESERVED

Two instruction opcodes available in the WM72016 are:
1. NORM – normal opcode for all read/write instructions, and
2. INTEND – DSPI serial port control register opcode.

The address parameter of the DSPI instruction word is a 10-bit value capable of addressing the entire WM72016 1024-word physical memory. Physical memory addressing is shown in the left-most column in Table 1. In the event that memory arbitration is required between the RFID and serial interfaces, the RFID interface will always have priority. The only exception to this rule is WM72016 interrupt generation, during which time the serial port has full control over the memory. **Care needs to be taken to ensure that reserved memory required to store critical parameters for the operation of the device are not altered**.

DSPI Data Streaming
Data may be streamed into the WM72016 (write cycles) or out of WM72016 (read cycles) using a single instruction word and 2 or more consecutive data words as shown in Figure 21. The example shown in the figure depicts n+1 data words. The host microcontroller initiates the read or write instruction in the same manner as detailed earlier: the CS signal is asserted, followed by 8 CLK cycles to shift the instruction word and 8 CLK cycles to shift the data word. From this point forward, each set of 8 CLK cycles is used to read or write the next WM72016 memory location. While the CS signal remains at a logic one, the WM72016 automatically increments an internal address pointer after every data word cycle has completed. The state of the AUTOINCR bit in the *Control/Status* register and the contents of the *Working Stored Address* have no impact on DSPI data streaming. Likewise, AUTOINCR and the *Working Stored Address* register are not affected by DSPI serial port data streaming. The data streaming cycle is terminated once CS has been cleared to a logic zero. The DSPI streaming capability removes the requirement for multiple instruction words, greatly improving bandwidth requirements.

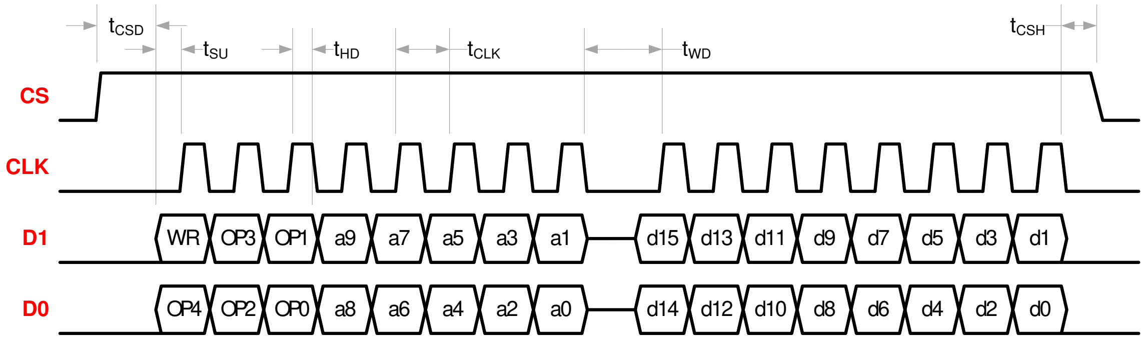


Figure 21. DSPI Write Cycle Detail

Note: In the event of a simultaneous memory access, the RFID request will take priority over the secondary DSPI serial interface.

MICROCONTROLLER INTERRUPTS

The WM72016 is capable of generating interrupts initiated by a RFID interrogator to a microcontroller on the serial port. Interrupt generation provides a mechanism to alert a host microcontroller that a RFID interrogator is present and to take control of the memory with no possibility of interruption from the RFID interface. During an interrupt, all RFID commands are disregarded until an INTEND DSPI command is received to terminate the interrupt and return control back to the RFID interface.

An interrupt is generated from the WM72016 to the host by writing two standard Gen2 write cycles to USER memory addresses 0x004 and 0x005. The XOR operation of the two data words written to the two respective addresses must equal 0x1234. As with all Gen2 write commands, the WM72016 must be in the OPEN or SECURED state prior to executing the write command sequence. Should the WM72016 RFID have a non-zero ACCESS password, the device must be transitioned to the SECURED state by correctly accessing the tag with the device's ACCESS password. The RFID interrogator then transmits two cover-coded WRITE commands to USER memory addresses 0x004 and 0x005 whose two data words when XORed together result in a value of 0x1234. A correct sequence of the WRITE commands will result in the WM72016 asserting an interrupt by driving the DSPI CS high. Upon detection of a high state on the CS signal, the host microcontroller drives two clock cycles on the DSPI CLK to acknowledge and clear the WM72016 interrupt. The host microcontroller now has full and uninhibited access to the WM72016 memory. Any attempted access by a RFID interrogator during this period will be disregarded until one of two conditions has occurred:

- The host microcontroller has released control of the WM72016 memory by writing an instruction with the INTEND opcode, or
- The WM72016 has been power-cycled.

The entire interrupt generation sequence is shown in Figure 22. Note that the values x1200 and x0034 shown in Figure 22 are shown for illustration purposes only – *any* two values whose XOR operation results in a value of x1234 will generate a DSPI interrupt. The host microcontroller releases its control of the WM72016 memory by writing an instruction with an INTEND opcode refer to Table 9. The contents of the DSPI write data word payload that follows the instruction word are ignored but must be present to constitute a valid DSPI command.

NOTE: Should the outcome of two write cycles to USER memory locations 0x004 and 0x005 result in a XOR value that is not 0x1234, the interrupt mechanism will be disabled until the WM72016 has been power-cycled. In this case, the two memory locations may be used as standard USER memory, however any future use of these memory locations may potentially generate an unintended interrupt – as such, it is not recommended to use these memory locations as part of the standard USER memory bank.

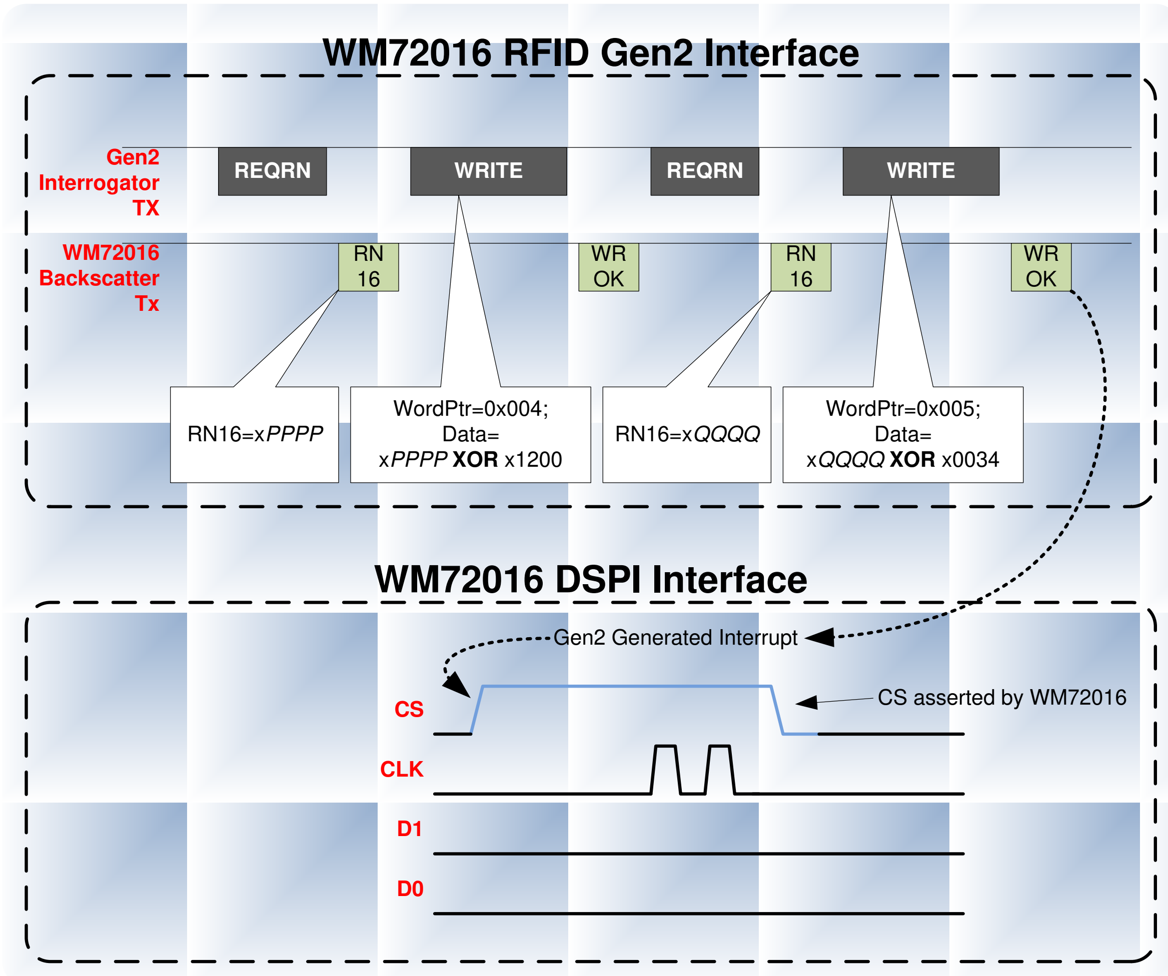


Figure 22. Gen2 Interrupt Generation

SPECIFICATIONS

WM72016's RFID Interface conforms to the *Specification for RFID Air Interface EPC Class-1 Generation-2 UHF RFID Protocol for Communications at 860 MHz – 960 MHz, Version 1.2.0*.

Options and Exceptions are noted here:

State Persistence Requirements

WM72016 features infinite state retention for S1, S2, S3, and SL State flags. State flag S0 has no persistence and will always return to state 'A' upon a power cycle.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Ratings	Notes
V_{DDR}, V_{DDRAW}	Power Supply Voltage with respect to ANT-	-1.0V to +4.5V	
V_{IN}	Voltage on any serial port pin with respect to ANT-	-1.0V to +4.5V and $V_{IN} < V_{DD}$+1.0V	
T_{STG}	Storage Temperature	-55°C to + 125°C	
T_{OP}	Operating Temperature	-40°C to +85°C	
T_{LEAD}	Lead Temperature (Soldering, 10 seconds)	260° C	
V_{ESD} (ANT+, ANT-)	Electrostatic Discharge Voltage - Human Body Model (JEDEC Std JESD22-A114-B) - Charged Device Model (JEDEC Std JESD22-C101-A) - Machine Model (JEDEC Std JESD22-A115-A)	 500V 1kV 50V	
V_{ESD} (All other pins)	Electrostatic Discharge Voltage - Human Body Model (JEDEC Std JESD22-A114-B) - Charged Device Model (JEDEC Std JESD22-C101-A) - Machine Model (JEDEC Std JESD22-A115-A)	 1.5kV 1.5kV 200V	
ME	Memory Endurance: Read or Write or Erase	$1x10^{14}$	1
RF_{exp}	RF Exposure	+10dBm (800 ~ 1000 MHz)	
	Package Moisture Sensitivity Level	MSL-2	

1. A degradation in memory endurance may occur for VDDR_EXT levels beyond the maximum specification.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

RF Operating Characteristics (T_A = -40° C to + 85° C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
S_R	Read Sensitivity		-6		dBm	
S_W	Write Sensitivity		-6		dBm	
Fr	Max Sustainable Read Rate @ S_R		640		Kbits/s	1
Fw	Max Sustainable Write Rate @ S_w		160		Kbits/s	1
t_{ST}	Power-on time		1.0	1.5	ms	
$\Delta\ \Gamma$	Change in Modulator Reflection Coefficient		TBD	TBD		
Z_{IN}	Input Impedance @ f_{IN}=915MHz		63 – j199		Ohms	2

Note:
1. Actual read & write speeds are constrained by the EPC Class 1 Gen2 data communication standard.
2. Z_{IN} is measured at S_R/S_W.

DSPI SERIAL PORT TIMING

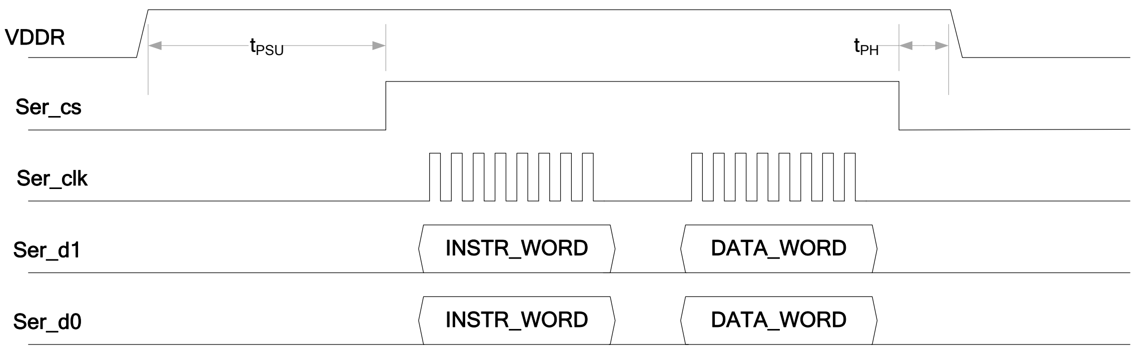


Figure 23. DSPI Power Supply Timing

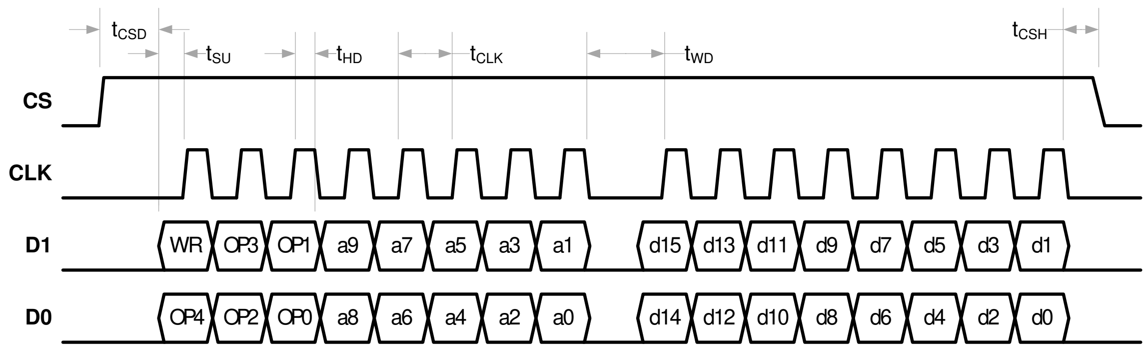


Figure 24. DSPI Write Cycle Detail

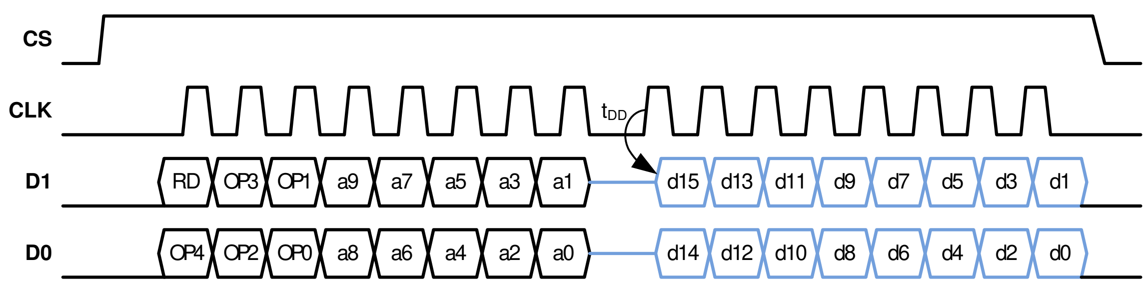


Figure 25. DSPI Read Cycle Detail