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WM8196

(8 + 8) Bit Output 16-bit CIS/CCD AFE/Digitiser

DESCRIPTION

The WM8196 is a 16-bit analogue front end/digitiser IC which processes and digitises the analogue output signals from CCD sensors or Contact Image Sensors (CIS) at pixel sample rates of up to 12MSPS.

The device includes three analogue signal processing channels each of which contains Reset Level Clamping, Correlated Double Sampling and Programmable Gain and Offset adjust functions. Three multiplexers allow single channel processing. The output from each of these channels is time multiplexed into a single high-speed 16-bit Analogue to Digital Converter. The digital output data is available in 8 or 4-bit wide multiplexed format.

An internal 4-bit DAC is supplied for internal reference level generation. This may be used during CDS to reference CIS signals or during Reset Level Clamping to clamp CCD signals. An external reference level may also be supplied. ADC references are generated internally, ensuring optimum performance from the device.

Using an analogue supply voltage of 5V and a digital interface supply of either 5V or 3.3V, the WM8196 typically only consumes 300mW when operating from a single 5V supply.

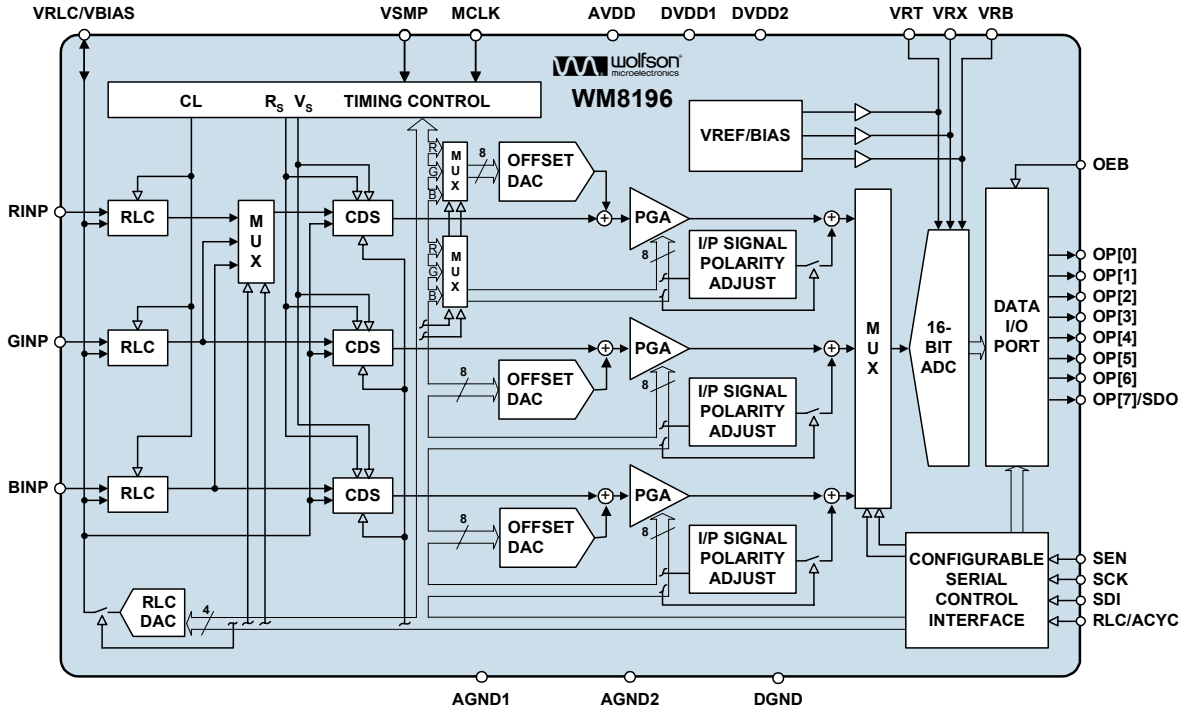
FEATURES

- 16-bit ADC
- 12MSPS conversion rate
- Low power – 320mW typical
- 5V single supply or 5V/3.3V dual supply operation
- Single or 3 channel operation
- Correlated double sampling
- Programmable gain (8-bit resolution)
- Programmable offset adjust (8-bit resolution)
- Programmable clamp voltage
- 8 or 4-bit wide multiplexed data output formats
- Internally generated voltage references
- 28-lead SSOP package
- Serial control interface

APPLICATIONS

- Flatbed and sheetfeed scanners
- USB compatible scanners
- Multi-function peripherals
- High-performance CCD sensor interface

BLOCK DIAGRAM



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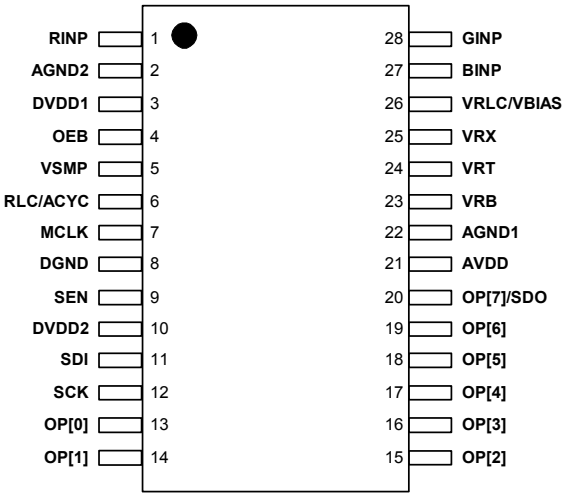
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVELS	PEAK SOLDERING TEMPERATURE
WM8196SCDS/V	0 to 70°C	28-lead SSOP (Pb free)	MSL3	260°C
WM8196SCDS/RV	0 to 70°C	28-lead SSOP (Pb free, tape and reel)	MSL3	260°C

Note:

Reel quantity = 2,000

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION					
1	RINP	Analogue input	Red channel input video.					
2	AGND2	Supply	Analogue ground (0V).					
3	DVDD1	Supply	Digital supply (5V) for logic and clock generator. This must be operated at the same potential as AVDD.					
4	OEB	Digital input	Output Hi-Z control, all digital outputs disabled when OEB = 1.					
5	VSMP	Digital input	Video sample synchronisation pulse.					
6	RLC/ACYC	Digital input	RLC (active high) selects reset level clamp on a pixel-by-pixel basis – tie high if used on every pixel. ACYC autocycles between R, G, B inputs.					
7	MCLK	Digital input	Master clock. This clock is applied at N times the input pixel rate (N = 2, 3, 6, 8 or any multiple of 2 thereafter depending on input sample mode).					
8	DGND	Supply	Digital ground (0V).					
9	SEN	Digital input	Enables the serial interface when high.					
10	DVDD2	Supply	Digital supply (5V/3.3V), all digital I/O pins.					
11	SDI	Digital input	Serial data input.					
12	SCK	Digital input	Serial clock.					
			Digital multiplexed output data bus. ADC output data (d15:d0) is available in two multiplexed formats as shown, under the control of register MUXOP [1:0] See 'Output Formats' description in Device Description section for further details.					
			8+8-bit		**4+4+4+4-bit**			
			A	**B**	**A**	**B**	**C**	**D**
13	OP[0]	Digital output	d8	d0				
14	OP[1]	Digital output	d9	d1				
15	OP[2]	Digital output	d10	d2				
16	OP[3]	Digital output	d11	d3				
17	OP[4]	Digital output	d12	d4	d12	d8	d4	d0
18	OP[5]	Digital output	d13	d5	d13	d9	d5	d1
19	OP[6]	Digital output	d14	d6	d14	d10	d6	d2
20	OP[7]/SDO	Digital output	d15	d7	d15	d11	d7	d3
			Alternatively, pin OP[7]/SDO may be used to output register read-back data when OEB = 0 and SEN has been pulsed high. See Serial Interface description in Device Description section for further details.					
21	AVDD	Supply	Analogue supply (5V). This must be operated at the same potential as DVDD1.					
22	AGND1	Supply	Analogue ground (0V).					
23	VRB	Analogue output	Lower reference voltage. This pin must be connected to AGND via a decoupling capacitor.					
24	VRT	Analogue output	Upper reference voltage. This pin must be connected to AGND via a decoupling capacitor.					
25	VRX	Analogue output	Input return bias voltage. This pin must be connected to AGND via a decoupling capacitor.					
26	VRLC/VBIAS	Analogue I/O	Selectable analogue output voltage for RLC or single-ended bias reference. This pin would typically be connected to AGND via a decoupling capacitor. VRLC can be externally driven if programmed Hi-Z.					
27	BINP	Analogue input	Blue channel input video.					
28	GINP	Analogue input	Green channel input video.					

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Analogue supply voltage: AVDD	GND - 0.3V	GND + 7V
Digital supply voltages: DVDD1 – 2	GND - 0.3V	GND + 7V
Digital ground: DGND	GND - 0.3V	GND + 0.3V
Analogue grounds: AGND1 – 2	GND - 0.3V	GND + 0.3V
Digital inputs, digital outputs and digital I/O pins	GND - 0.3V	DVDD2 + 0.3V
Analogue inputs (RINP, GINP, BINP)	GND - 0.3V	AVDD + 0.3V
Other pins	GND - 0.3V	AVDD + 0.3V
Operating temperature range: T_A	0°C	+70°C
Storage temperature prior to soldering	30°C max / 85% RH max	
Storage temperature after soldering	-65°C	+150°C

Notes:

1. GND denotes the voltage of any ground pin.
2. AGND1, AGND2 and DGND pins are intended to be operated at the same potential. Differential voltages between these pins will degrade performance.

RECOMMENDED OPERATING CONDITIONS

CONDITION		SYMBOL	MIN	TYP	MAX	UNITS
Operating temperature range		T_A	0		70	°C
Analogue supply voltage		AVDD	4.75	5.0	5.25	V
Digital core supply voltage		DVDD1	4.75	5.0	5.25	V
Digital I/O supply voltage	5V I/O	DVDD2	4.75	5.0	5.25	V
	3.3V I/O	DVDD2	2.97	3.3	3.63	V

THERMAL PERFORMANCE

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Performance						
Thermal resistance – junction to case	$R_{\theta JC}$	$T_{ambient}$ = 25°C		23.9		°C/W
Thermal resistance – junction to ambient	$R_{\theta JA}$			67.1		°C/W

Notes:

1. Figures given are for package mounted on 4-layer FR4 according to JESD51-5 and JESD51-7.

ELECTRICAL CHARACTERISTICS

Test Conditions
AVDD = DVDD1 = 5.0V, DVDD2 = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 24MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overall System Specification (including 16-bit ADC, PGA, Offset and CDS functions)						
Conversion Rate				12		MSPS
Full-scale input voltage range (see Note 1)				0.4 4.08		Vp-p Vp-p
Input signal limits (see Note 2)	V_{IN}		0		AVDD	V
Full-scale transition error		Gain = 0dB; PGA[7:0] = 4B(hex)		20		mV
Zero-scale transition error		Gain = 0dB; PGA[7:0] = 4B(hex)		20		mV
Differential non-linearity	DNL			1.25		LSB
Integral non-linearity	INL			25		LSB
Channel to channel gain matching				1		%
Total output noise		Min Gain Max Gain		4.5 14		LSB rms LSB rms
References						
Upper reference voltage	VRT			2.85		V
Lower reference voltage	VRB			1.35		V
Input return bias voltage	VRX		1.4	1.65	1.6	V
Diff. reference voltage (VRT-VRB)	V_{RTB}			1.5		V
Output resistance VRT, VRB, VRX				1		Ω
VRLC/Reset-Level Clamp (RLC)						
RLC switching impedance				50		Ω
VRLC short-circuit current				2		mA
VRLC output resistance				2		Ω
VRLC Hi-Z leakage current		VRLC = 0 to AVDD			1	µA
RLCDAC resolution				4		bits
RLCDAC step size, RLCDACRNG = 0	$V_{RLCSTEP}$	AVDD=5V		0.25		V/step
RLCDAC step size, RLCDACRNG = 1	$V_{RLCSTEP}$			0.17		V/step
RLCDAC output voltage at code 0(hex), RLCDACRNG = 0	V_{RLCBOT}	AVDD=5V		0.39		V
RLCDAC output voltage at code 0(hex), RLCDACRNG = 1	V_{RLCBOT}			0.26		V
RLCDAC output voltage at code F(hex) RLCDACRNG, = 0	V_{RLCTOP}	AVDD=5V		4.16		V
RLCDAC output voltage at code F(hex), RLCDACRNG = 1	V_{RLCTOP}			2.81		V
VRLC deviation			-50		+50	mV
Offset DAC, Monotonicity Guaranteed						
Resolution				8		bits
Differential non-linearity	DNL			0.1	0.5	LSB
Integral non-linearity	INL			0.25	1	LSB
Step size				2.04		mV/step
Output voltage		Code 00(hex) Code FF(hex)		-260 +260		mV mV

Notes:

1. **Full-scale input voltage** denotes the maximum amplitude of the input signal at the specified gain.
2. **Input signal limits** are the limits within which the full-scale input voltage signal must lie.

Test Conditions
AVDD = DVDD1 = 5.0V, DVDD2 = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 24MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Programmable Gain Amplifier						
Resolution				8		bits
Gain				$\frac{208}{283 - PGA[7:0]}$		V/V
Max gain, each channel	G_{MAX}			7.4		V/V
Min gain, each channel	G_{MIN}			0.74		V/V
Gain error, each channel				1		%
Analogue to Digital Converter						
Resolution				16		Bits
Speed				12		MSPS
Full-scale input range (2*(VRT-VRB))				3		V
DIGITAL SPECIFICATIONS						
Digital Inputs						
High level input voltage	V_{IH}		0.8 ∗ DVDD2			V
Low level input voltage	V_{IL}				0.2 ∗ DVDD2	V
High level input current	I_{IH}				1	µA
Low level input current	I_{IL}				1	µA
Input capacitance	C_I			5		pF
Digital Outputs						
High level output voltage	V_{OH}	I_{OH} = 1mA	DVDD2 - 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 1mA			0.5	V
High impedance output current	I_{OZ}				1	µA
Digital IO Pins						
Applied high level input voltage	V_{IH}		0.8 ∗ DVDD2			V
Applied low level input voltage	V_{IL}				0.2 ∗ DVDD2	V
High level output voltage	V_{OH}	I_{OH} = 1mA	DVDD2 - 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 1mA			0.5	V
Low level input current	I_{IL}				1	µA
High level input current	I_{IH}				1	µA
Input capacitance	C_I			5		pF
High impedance output current	I_{OZ}				1	µA
Supply Currents						
Total supply current – active (Three channel mode)		MCLK = 24MHz		60		mA
Total supply current – active (Single channel mode)		LINEBYLINE = 1 MCLK = 24MHz		45		mA
Total analogue supply current – active (Three channel mode)	I_{AVDD}	MCLK = 24MHz		56		mA
Total analogue supply current – active (One channel mode)	I_{AVDD}	LINEBYLINE = 1 MCLK = 24MHz		41		mA
Digital core supply current, DVDD1 – active (Note1)		MCLK = 24MHz		3		mA
Digital I/O supply current, DVDD2 – active (Note1)		MCLK = 24MHz		1		mA
Supply current – full power down mode				300		µA

INPUT VIDEO SAMPLING

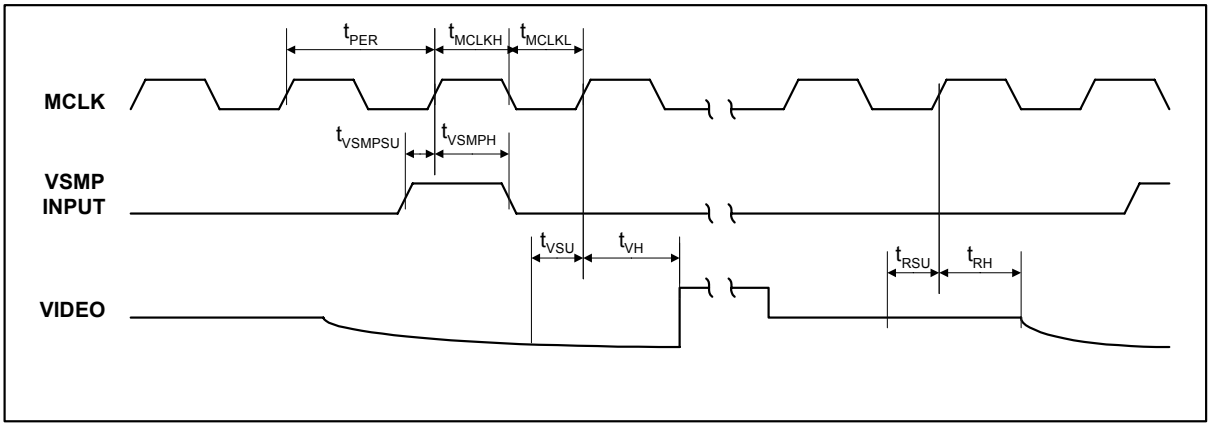


Figure 1 Input Video Timing

Note:

1. See Page 14 (Programmable VSMP Detect Circuit) for video sampling description.

Test Conditions

AVDD = DVDD1 = 5.0V, DVDD2 = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 24MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MCLK period	t_{PER}		41.6			ns
MCLK high period	t_{MCLKH}		18.8			ns
MCLK low period	t_{MCLKL}		18.8			ns
VSMP set-up time	t_{VSMPSU}		6			ns
VSMP hold time	t_{VSMPH}		3			ns
Video level set-up time	t_{VSU}		10			ns
Video level hold time	t_{VH}		3			ns
Reset level set-up time	t_{RSU}		10			ns
Reset level hold time	t_{RH}		3			ns

Notes:

1. t_{VSU} and t_{RSU} denote the set-up time required after the input video signal has settled.
2. Parameters are measured at 50% of the rising/falling edge.

OUTPUT DATA TIMING

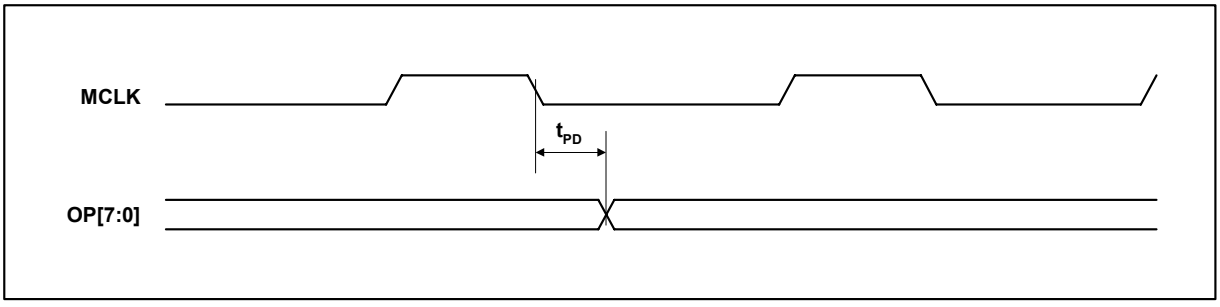


Figure 2 Output Data Timing

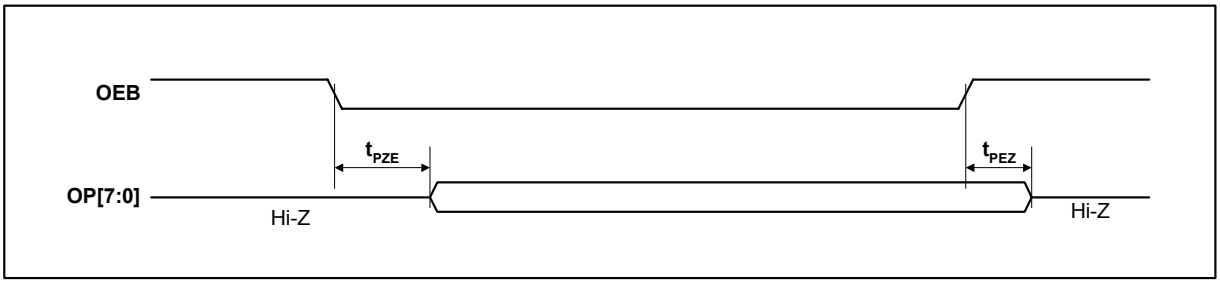


Figure 3 Output Data Enable Timing

Test Conditions
AVDD = DVDD1 = 5.0V, DVDD2 = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 24MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output propagation delay	t_{PD}	I_{OH} = 1mA, I_{OL} = 1mA	10	18	30	ns
Output enable time	t_{PZE}				20	ns
Output disable time	t_{PEZ}				15	ns

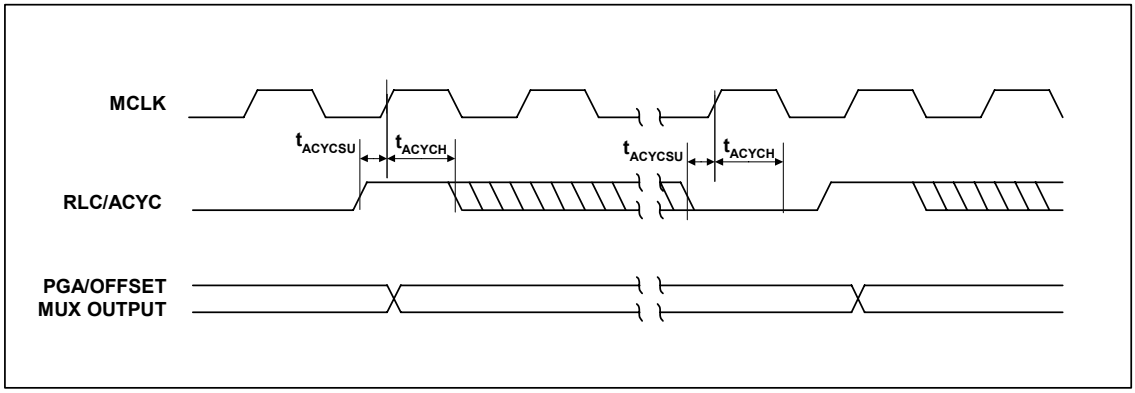


Figure 4 Auto Cycle Timing

Test Conditions
AVDD = DVDD1 = 5.0V, DVDD2 = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 24MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Auto Cycle set-up time	t_{ACYCSU}		6			ns
Auto Cycle hold time	t_{ACYCH}		3			ns

SERIAL INTERFACE

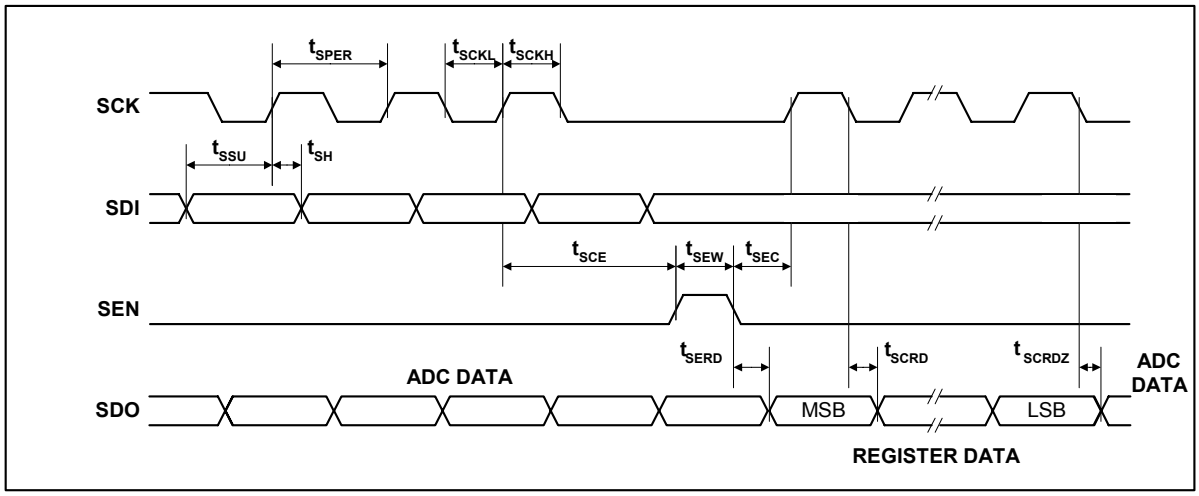


Figure 5 Serial Interface Timing

Test Conditions
AVDD = DVDD1 = 5.0V, DVDD2 = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 24MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SCK period	t_{SPER}		41.6			ns
SCK high	t_{SCKH}		18.8			ns
SCK low	t_{SCKL}		18.8			ns
SDI set-up time	t_{SSU}		6			ns
SDI hold time	t_{SH}		6			ns
SCK to SEN set-up time	t_{SCE}		12			ns
SEN to SCK set-up time	t_{SEC}		12			ns
SEN pulse width	t_{SEW}		25			ns
SEN low to SDO = Register data	t_{SERD}				30	ns
SCK low to SDO = Register data	t_{SCRD}				30	ns
SCK low to SDO = ADC data	t_{SCRDZ}				30	ns

Note:

1. Parameters are measured at 50% of the rising/falling edge

INTERNAL POWER ON RESET CIRCUIT

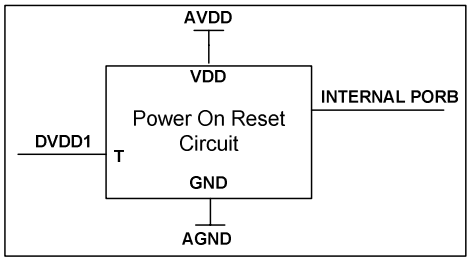


Figure 6 Internal Power On Reset Circuit Schematic

The WM8196 includes an internal Power-On-Reset Circuit, as shown in Figure 6, which is used to reset the digital logic into a default state after power up. The POR circuit is powered from AVDD and monitors DVDD1. It asserts PORB low if AVDD or DVDD1 is below a minimum threshold.

The power supplies can be brought up in any order but is important that either AVDD is brought up and is stable before DVDD comes up or vice versa as shown in Figure 7 and Figure 8.

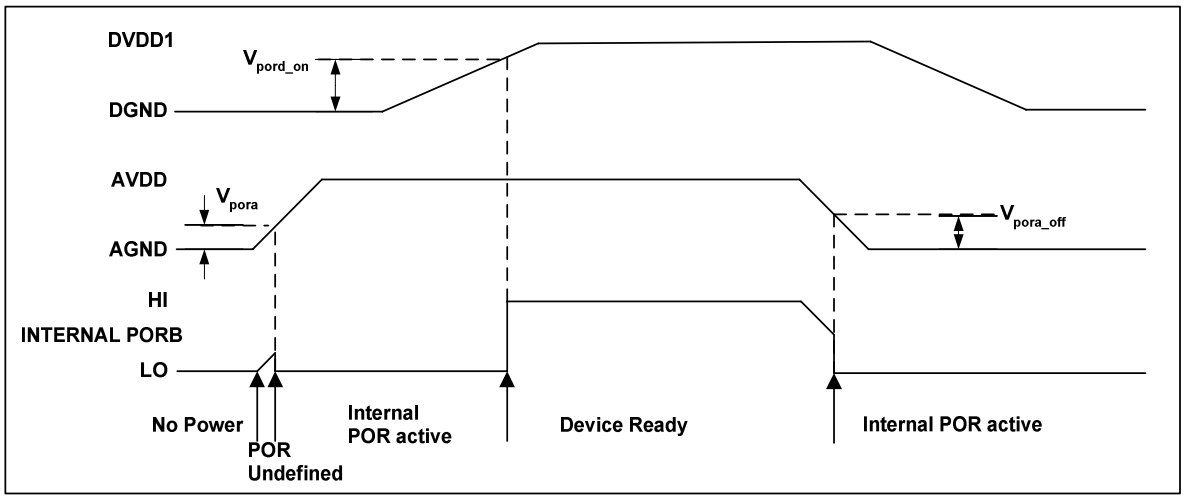


Figure 7 Typical Power up Sequence where AVDD is Powered before DVDD1

Figure 7 shows a typical power-up sequence where AVDD is powered up first. When AVDD rises above the minimum threshold, Vpora, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. Now AVDD is at full supply level. Next DVDD1 rises to Vpord_on and PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where AVDD falls first, PORB is asserted low whenever AVDD drops below the minimum threshold Vpora_off.

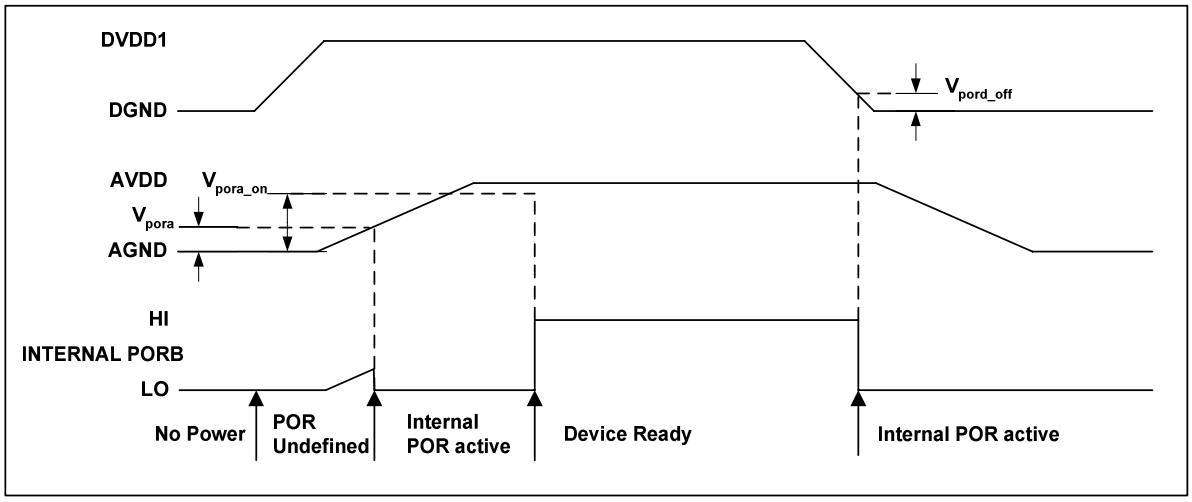


Figure 8 Typical Power up Sequence where DVDD1 is Powered before AVDD

Figure 8 shows a typical power-up sequence where DVDD1 is powered up first. It is assumed that DVDD1 is already up to specified operating voltage. When AVDD goes above the minimum threshold, Vpora, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When AVDD rises to Vpora_on, PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where DVDD1 falls first, PORB is asserted low whenever DVDD1 drops below the minimum threshold Vpord_off.

SYMBOL	TYP	UNIT
V_{pora}	0.6	V
V_{pora_on}	1.2	V
V_{pora_off}	0.6	V
V_{pord_on}	0.7	V
V_{pord_off}	0.6	V

Table 1 Typical POR Operation (typical values, not tested)

Note: It is recommended that every time power is cycled to the WM8196 a software reset is written to the software register to ensure that the contents of the control registers are at their default values before carrying out any other register writes.

DEVICE DESCRIPTION

INTRODUCTION

A block diagram of the device showing the signal path is presented on Page 1.

The WM8196 samples up to three inputs (RINP, GINP and BINP) simultaneously. The device then processes the sampled video signal with respect to the video reset level or an internally/externally generated reference level using either one or three processing channels.

Each processing channel consists of an Input Sampling block with optional Reset Level Clamping (RLC) and Correlated Double Sampling (CDS), an 8-bit programmable offset DAC and an 8-bit Programmable Gain Amplifier (PGA).

The ADC then converts each resulting analogue signal to a 16-bit digital word. The digital output from the ADC is presented on an 8-bit wide bi-directional bus, with optional 8 or 4-bit multiplexed formats.

On-chip control registers determine the configuration of the device, including the offsets and gains applied to each channel. These registers are programmable via a serial interface.

INPUT SAMPLING

The WM8196 can sample and process one to three inputs through one or three processing channels as follows:

Colour Pixel-by-Pixel: The three inputs (RINP, GINP and BINP) are simultaneously sampled for each pixel and a separate channel processes each input. The signals are then multiplexed into the ADC, which converts all three inputs within the pixel period.

Monochrome: A single chosen input (RINP, GINP, or BINP) is sampled, processed by the corresponding channel, and converted by the ADC. The choice of input and channel can be changed via the control interface, e.g. on a line-by-line basis if required.

Colour Line-by-Line: A single chosen input (RINP, GINP, or BINP) is sampled and multiplexed into the red channel for processing before being converted by the ADC. The input selected can be switched in turn (RINP → GINP → BINP → RINP…) together with the PGA and Offset DAC control registers by pulsing the RLC/ACYC pin. This is known as auto-cycling. Alternatively, other sampling sequences can be generated via the control registers. This mode causes the blue and green channels to be powered down. Refer to the Line-by-Line Operation section for more details.

RESET LEVEL CLAMPING (RLC)

To ensure that the signal applied to the WM8196 lies within its input range (0V to AVDD) the CCD output signal is usually level shifted by coupling through a capacitor, $C_{IN.}$ The RLC circuit clamps the WM8196 side of this capacitor to a suitable voltage during the CCD reset period.

A typical input configuration is shown in Figure 9. An internal clamp pulse, CL, is generated from MCLK and VSMP by the Timing Control Block. When CL is active the voltage on the WM8196 side of C_{IN}, at RINP, is forced to the VRLC/VBIAS voltage (V_{VRLC}) by closing of switch 1. When the CL pulse turns off switch 1 opens, the voltage at RINP initially remains at V_{VRLC} but any subsequent variation in sensor voltage (from reset to video level) will couple through C_{IN} to RINP.

RLC is compatible with both CDS and non-CDS operating modes, as selected by switch 2. Refer to the CDS/non-CDS Processing section.

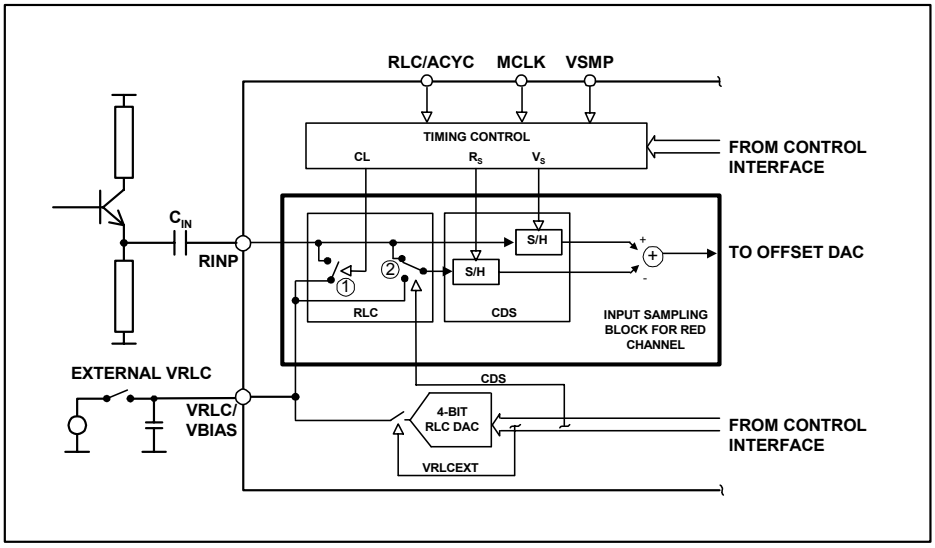


Figure 9 Reset Level Clamping and CDS Circuitry

If auto-cycling is not required, RLC can be selected by pin RLC/ACYC. Figure 10 illustrates control of RLC for a typical CCD waveform, with CL applied during the reset period.

The input signal applied to the RLC/ACYC pin is sampled on the positive edge of MCLK that occurs during each VSMP pulse. The sampled level, high (or low) controls the presence (or absence) of the internal CL pulse on the next reset level. The position of CL can be adjusted by using control bits CDSREF[1:0] (Figure 11).

If auto-cycling is required, pin RLC/ACYC is no longer available for this function and control bit RLCINT determines whether clamping is applied.

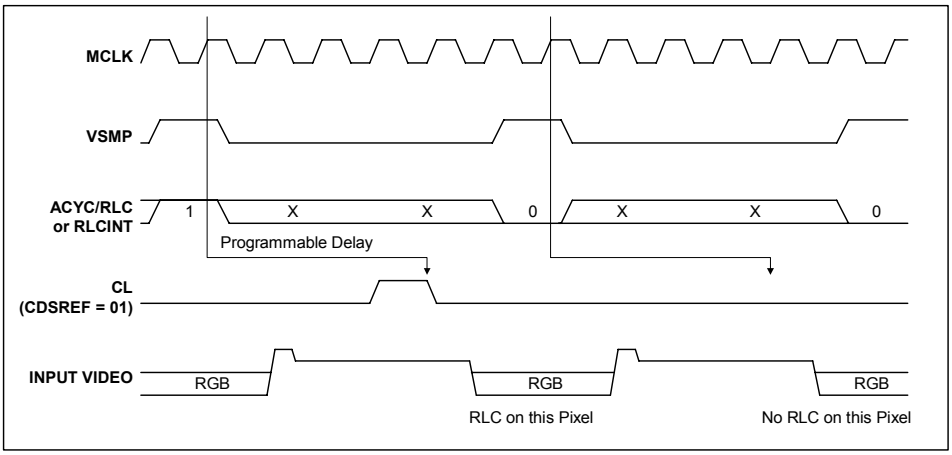


Figure 10 Relationship of RLC Pin, MCLK and VSMP to Internal Clamp Pulse, CL

The VRLC/VBIAS pin can be driven internally by a 4-bit DAC (RLCDAC) by writing to control bits RLCV[3:0]. The RLCDAC range and step size may be increased by writing to control bit RLCDACRNG. Alternatively, the VRLC/VBIAS pin can be driven externally by writing to control bit VRLCEXT to disable the RLCDAC and then applying a d.c. voltage to the pin.

CDS/NON-CDS PROCESSING

For CCD type input signals, the signal may be processed using CDS, which will remove pixel-by-pixel common mode noise. For CDS operation, the video level is processed with respect to the video reset level, regardless of whether RLC has been performed. To sample using CDS, control bit CDS must be set to 1 (default), this sets switch 2 into the position shown in Figure 9 and causes the signal reference to come from the video reset level. The time at which the reset level is sampled, by clock R_S/CL, is adjustable by programming control bits CDSREF[1:0], as shown in Figure 11.

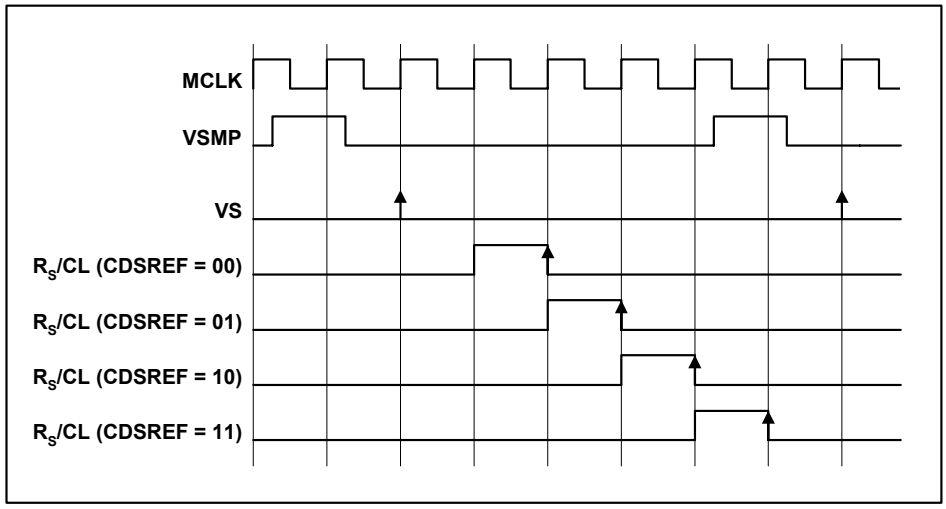


Figure 11 Reset Sample and Clamp Timing

For CIS type sensor signals, non-CDS processing is used. In this case, the video level is processed with respect to the voltage on pin VRLC/VBIAS, generated internally or externally as described above. The VRLC/VBIAS pin is sampled by R_s at the same time as V_s samples the video level in this mode; non-CDS processing is achieved by setting switch 2 in the lower position, CDS = 0.

OFFSET ADJUST AND PROGRAMMABLE GAIN

The output from the CDS block is a differential signal, which is added to the output of an 8-bit Offset DAC to compensate for offsets and then amplified by an 8-bit PGA. The gain and offset for each channel are independently programmable by writing to control bits DAC[7:0] and PGA[7:0].

The gain characteristic of the WM8196 PGA is shown in Figure 12. Figure 13 shows the maximum device input voltage that can be gained up to match the ADC full-scale input range (3V).

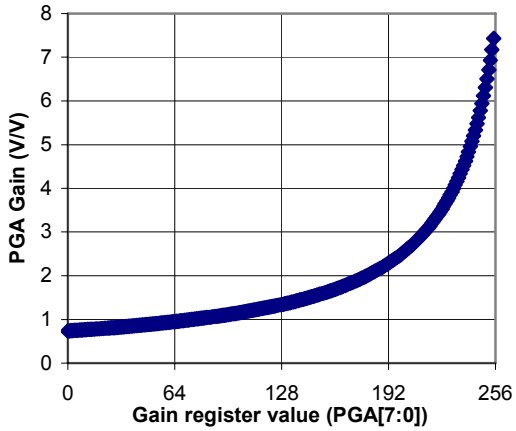


Figure 12 PGA Gain Characteristic

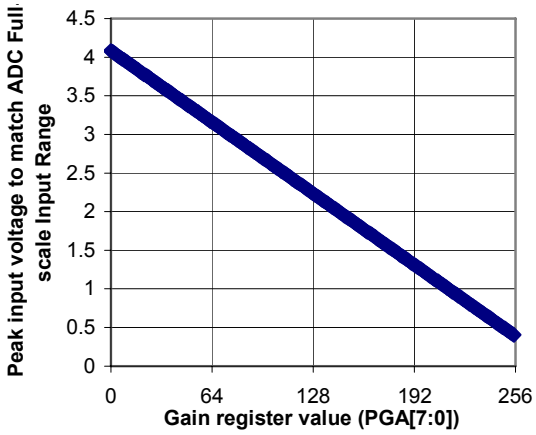


Figure 13 Peak Input Voltage to Match ADC Full-scale Range

In colour line-by-line mode the gain and offset coefficients for each colour can be multiplexed in order (Red → Green → Blue → Red…) by pulsing the ACYC/RLC pin, or controlled via the FME, ACYCNRLC and INTM[1:0] bits. Refer to the Line-by-Line Operation section for more details.

ADC INPUT BLACK LEVEL ADJUST

The output from the PGA should be offset to match the full-scale range of the ADC (3V). For negative-going input video signals, a black level (zero differential) output from the PGA should be offset to the top of the ADC range by setting register bits PGAFS[1:0]=10. For positive going input signal the black level should be offset to the bottom of the ADC range by setting PGAFS[1:0]=11. Bipolar input video is accommodated by setting PGAFS[1:0]=00 or PGAFS[1:0]=01 (zero differential input voltage gives mid-range ADC output).

OVERALL SIGNAL FLOW SUMMARY

Figure 14 represents the processing of the video signal through the WM8196.

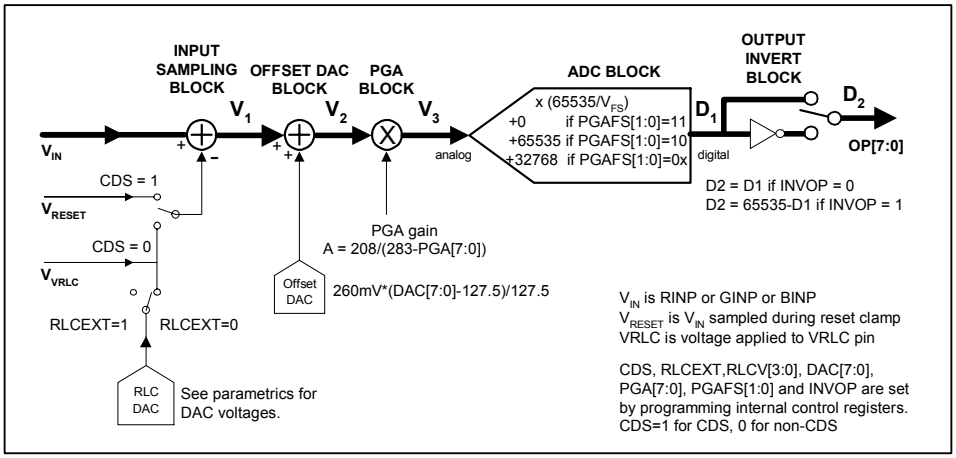


Figure 14 Overall Signal Flow

The **INPUT SAMPLING BLOCK** produces an effective input voltage $\mathbf{V_1}$. For CDS, this is the difference between the input video level V_{IN} and the input reset level V_{RESET}. For non-CDS this is the difference between the input video level V_{IN} and the voltage on the VRLC/VBIAS pin, V_{VRLC}, optionally set via the RLC DAC.

The **OFFSET DAC BLOCK** then adds the amount of fine offset adjustment required to move the black level of the input signal towards 0V, producing $\mathbf{V_2}$.

The **PGA BLOCK** then amplifies the white level of the input signal to maximise the ADC range, outputting voltage $\mathbf{V_3}$.

The **ADC BLOCK** then converts the analogue signal, $\mathbf{V_3}$, to a 16-bit unsigned digital output, $\mathbf{D_1}$.

The digital output is then inverted, if required, through the **OUTPUT INVERT BLOCK** to produce $\mathbf{D_2}$.

CALCULATING OUTPUT FOR ANY GIVEN INPUT

The following equations describe the processing of the video and reset level signals through the WM8196. The values if V_1 V_2 and V_3 are often calculated in reverse order during device setup. The PGA value is written first to set the input Voltage range, the Offset DAC is then adjusted to compensate for any Black/Reset level offsets and finally the RLC DAC value is set to position the reset level correctly during operation.

Note: Refer to WAN0123 for detailed information on device calibration procedures.

INPUT SAMPLING BLOCK: INPUT SAMPLING AND REFERENCING

If CDS = 1, (i.e. CDS operation) the previously sampled reset level, V_{RESET}, is subtracted from the input video.

$$\mathbf{V_1} = V_{IN} - V_{RESET} \quad \text{..... Eqn. 1}$$

If CDS = 0, (non-CDS operation) the simultaneously sampled voltage on pin VRLC is subtracted instead.

$$\mathbf{V_1} = V_{IN} - V_{VRLC} \quad \text{..... Eqn. 2}$$

If RLCEXT = 1, V_{VRLC} is an externally applied voltage on pin VRLC/VBIAS.

If RLCEXT = 0, V_{VRLC} is the output from the internal RLC DAC.

$$V_{VRLC} = (V_{RLCSTEP} * RLCV[3:0]) + V_{RLCBOT} \quad \text{Eqn. 3}$$

$V_{RLCSTEP}$ is the step size of the RLC DAC and V_{RLCBOT} is the minimum output of the RLC DAC.

OFFSET DAC BLOCK: OFFSET (BLACK-LEVEL) ADJUST

The resultant signal $\mathbf{V_1}$ is added to the Offset DAC output.

$$\mathbf{V_2} = \mathbf{V_1} + \{260mV * (DAC[7:0]-127.5)\} / 127.5 \quad \text{Eqn. 4}$$

PGA NODE: GAIN ADJUST

The signal is then multiplied by the PGA gain,

$$\mathbf{V_3} = \mathbf{V_2} * 208/(283- PGA[7:0]) \quad \text{Eqn. 5}$$

ADC BLOCK: ANALOGUE-DIGITAL CONVERSION

The analogue signal is then converted to a 16-bit unsigned number, with input range configured by PGAFS[1:0].

$$\mathbf{D_1}[15:0] = INT\{ (\mathbf{V_3}/V_{FS}) * 65535\} + 32767 \quad PGAFS[1:0] = 00 \text{ or } 01 \quad \text{Eqn. 6}$$

$$\mathbf{D_1}[15:0] = INT\{ (\mathbf{V_3}/V_{FS}) * 65535\} \quad PGAFS[1:0] = 11 \quad \text{Eqn. 7}$$

$$\mathbf{D_1}[15:0] = INT\{ (\mathbf{V_3}/V_{FS}) * 65535\} + 65535 \quad PGAFS[1:0] = 10 \quad \text{Eqn. 8}$$

where the ADC full-scale range, V_{FS} = 3V

OUTPUT INVERT BLOCK: POLARITY ADJUST

The polarity of the digital output may be inverted by control bit INVOP.

$$\mathbf{D_2}[15:0] = \mathbf{D_1}[15:0] \quad (INVOP = 0) \quad \text{Eqn. 9}$$

$$\mathbf{D_2}[15:0] = 65535 - \mathbf{D_1}[15:0] \quad (INVOP = 1) \quad \text{Eqn. 10}$$

OUTPUT FORMATS

The digital data output from the ADC is available to the user in 8 or 4-bit wide multiplexed formats by setting control bit MUXOP[1:0]. Latency of valid output data with respect to VSMP is programmable by writing to control bits DEL[1:0]. The latency for each mode is shown in the Operating Mode Timing Diagrams section.

Figure 15 shows the output data formats for Modes 1 – 2 and 4 – 6. Figure 16 shows the output data formats for Mode 3. Table 2 summarises the output data obtained for each format.

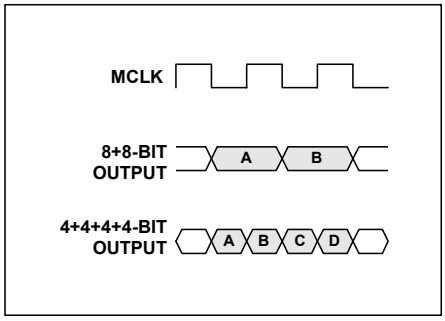


Figure 15 Output Data Formats (Modes 1 – 2, 4 – 6)

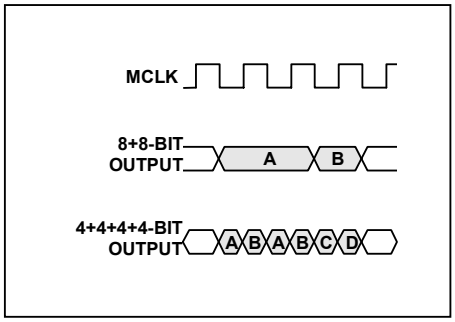


Figure 16 Output Data Formats (Mode 3)

OUTPUT FORMAT	MUXOP[1:0]	OUTPUT PINS	OUTPUT
8+8-bit multiplexed	00, 01, 10	OP[7:0]	A = d15, d14, d13, d12, d11, d10, d9, d8 B = d7, d6, d5, d4, d3, d2, d1,d0
4+4+4+4-bit (nibble)	11	OP[7:4]	A = d15, d14, d13, d12 B = d11, d10, d9, d8 C = d7, d6, d5, d4 D = d3, d2, d1, d0

Table 2 Details of Output Data Shown in Figure 15 and Figure 16.

CONTROL INTERFACE

The internal control registers are programmable via the serial digital control interface. The register contents can be read back via the serial interface on pin OP[7]/SDO.

Note: It is recommended that a software reset is carried out after the power-up sequence, before writing to any other register. This ensures that all registers are set to their default values (as shown in Table 6).

SERIAL INTERFACE: REGISTER WRITE

Figure 17 shows register writing in serial mode. Three pins, SCK, SDI and SEN are used. A six-bit address (a5, 0, a3, a2, a1, a0) is clocked in through SDI, MSB first, followed by an eight-bit data word (b7, b6, b5, b4, b3, b2, b1, b0), also MSB first. Each bit is latched on the rising edge of SCK. When the data has been shifted into the device, a pulse is applied to SEN to transfer the data to the appropriate internal register. Note all valid registers have address bit a4 equal to 0 in write mode.

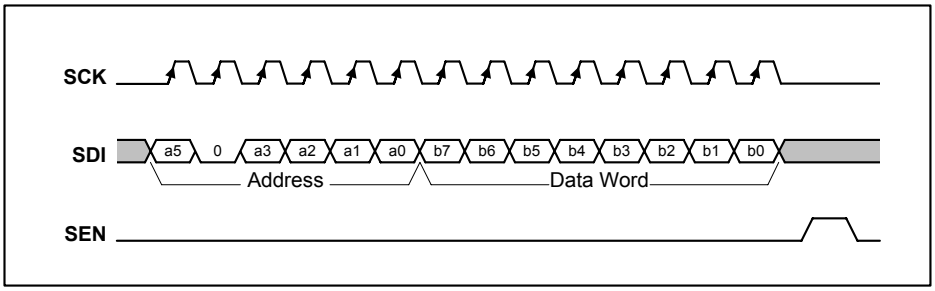


Figure 17 Serial Interface Register Write

A software reset is carried out by writing to Address “000100” with any value of data, i.e. Data Word = XXXXXXXX.

SERIAL INTERFACE: REGISTER READ-BACK

Figure 18 shows register read-back in serial mode. Read-back is initiated by writing to the serial bus as described above but with address bit a4 set to 1, followed by an 8-bit dummy data word. Writing address (a5, 1, a3, a2, a1, a0) will cause the contents (d7, d6, d5, d4, d3, d2, d1, d0) of corresponding register (a5, 0, a3, a2, a1, a0) to be output MSB first on pin SDO (on the falling edge of SCK). Note that pin SDO is shared with an output pin, OP[7], therefore OEB should always be held low when register read-back data is expected on this pin. The next word may be read in to SDI while the previous word is still being output on SDO.

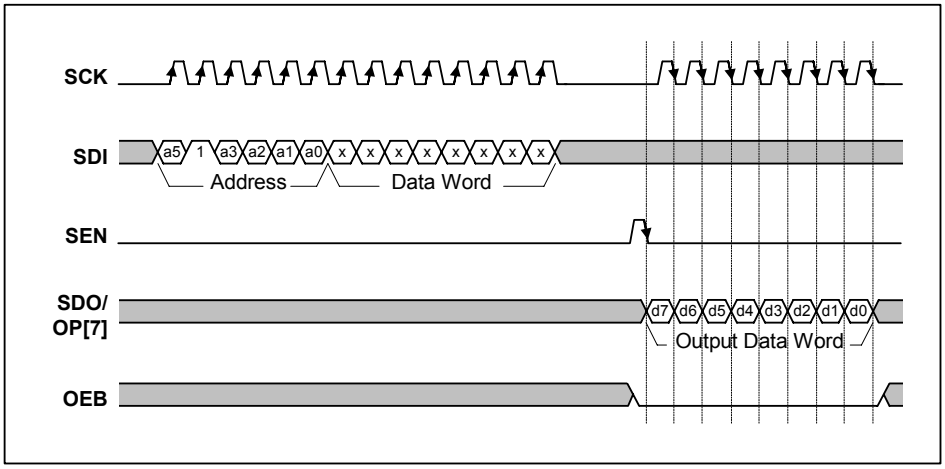


Figure 18 Serial Interface Register Read-back

TIMING REQUIREMENTS

To use this device a master clock (MCLK) of up to 24MHz and a per-pixel synchronisation clock (VSMP) of up to 12MHz are required. These clocks drive a timing control block, which produces internal signals to control the sampling of the video signal. MCLK to VSMP ratios and maximum sample rates for the various modes are shown in Table 5.

PROGRAMMABLE VSMP DETECT CIRCUIT

The VSMP input is used to determine the sampling point and frequency of the WM8196. Under normal operation a pulse of 1 MCLK period should be applied to VSMP at the desired sampling frequency (as shown in the Operating Mode Timing Diagrams) and the input sample will be taken on the first rising MCLK edge after VSMP has gone low. However, in certain applications such a signal may not be readily available. The programmable VSMP detect circuit in the WM8196 allows the sampling point to be derived from any signal of the correct frequency, such as a CCD shift register clock, when applied to the VSMP pin.

When enabled, by setting the VSMPDET control bit, the circuit detects either a rising or falling edge (determined by POSNNEG control bit) on the VSMP input pin and generates an internal VSMP pulse. This pulse can optionally be delayed by a number of MCLK periods, specified by the VDEL[2:0] bits. Figure 19 shows the internal VSMP pulses that can be generated by this circuit for a typical clock input signal. The internal VSMP pulse is then applied to the timing control block in place of the normal VSMP pulse provided from the input pin. The sampling point then occurs on the first rising MCLK edge after this internal VSMP pulse, as shown in the Operating Mode Timing Diagrams.

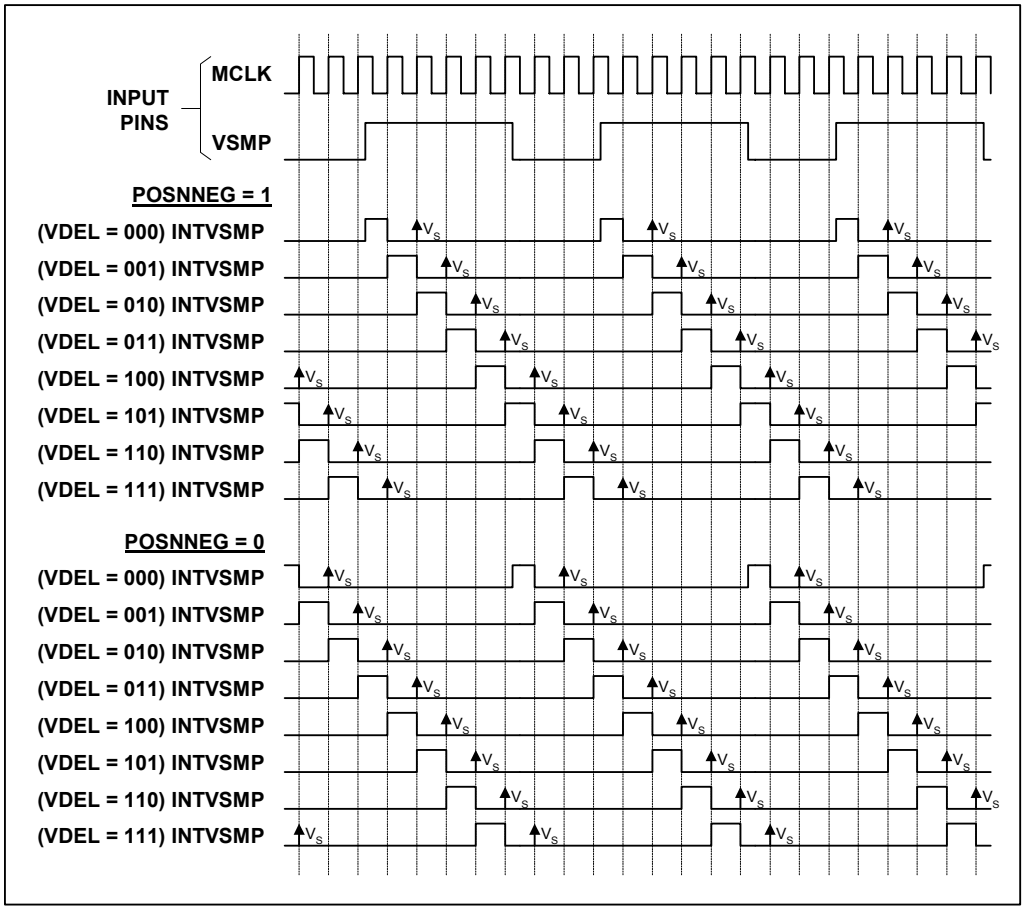


Figure 19 Internal VSMP Pulses Generated by Programmable VSMP Detect Circuit

REFERENCES

The ADC reference voltages are derived from an internal bandgap reference, and buffered to pins VRT and VRB, where they must be decoupled to ground. Pin VRX is driven by a similar buffer, and also requires decoupling. The output buffer from the RLCDAC also requires decoupling at pin VRLC/VBIAS

POWER SUPPLY

The WM8196 can run from a 5V single supply or from split 5V (core) and 3.3V (digital interface) supplies.

POWER MANAGEMENT

Power management for the device is performed via the Control Interface. The device can be powered on or off completely setting by the EN bit and SELPD bit low. Alternatively, when control bit SELPD is high, only blocks selected by further control bits (SELDIS[3:0]) are powered down. This allows the user to optimise power dissipation in certain modes, or to define an intermediate standby mode to allow a quicker recovery into a fully active state. In Line-by-line operation, the green and blue channel PGAs are automatically powered down.

All the internal registers maintain their previously programmed value in power down modes and the Control Interface inputs remain active. Table 3 summarises the power down control bit functions.

EN	SELDPD	
0	0	Device completely powers down.
1	0	Device completely powers up.
X	1	Blocks with respective SELDIS[3:0] bit high are disabled.

Table 3 Power Down Control

LINE-BY-LINE OPERATION

Certain linear sensors (e.g. Contact Image Sensors) give colour output on a line-by-line basis. i.e. a full line of red pixels followed by a line of green pixels followed by a line of blue pixels. In order to accommodate this type of signal the WM8196 can be set into Monochrome mode, with the input channel switched by writing to control bits CHAN[1:0] between every line. Alternatively, the WM8196 can be placed into colour line-by-line mode by setting the LINEBYLINE control bit. When this bit is set the green and blue processing channels are powered down and the device is forced internally to only operate in MONO mode (because only one colour is sampled at a time) through the red channel. Figure 20 shows the signal path when operating in colour line-by-line mode.

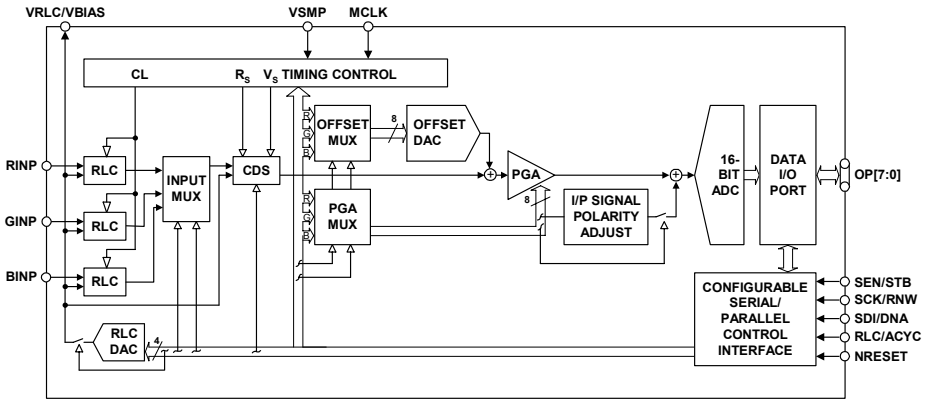


Figure 20 Signal Path When in Line-by-Line Mode

In this mode the input multiplexer and (optionally) the PGA/Offset register multiplexers can be auto-cycled by the application of pulses to the RLC/ACYC input pin by setting the ACYCNRLC register bit. See Figure 4 for detailed timing information. The multiplexers change on the first MCLK rising edge after RLC/ACYC is taken high. A write to the auto-cycle reset register causes these multiplexers to be reset; selecting the RINP pin and the RED offset/gain registers. Alternatively, all three multiplexers can be controlled via the serial interface by writing to register bits INTM[1:0] to select the desired colour. It is also possible for the input multiplexer to be controlled separately from the PGA and Offset multiplexers. Table 4 describes all the multiplexer selection modes that are possible.

FME	ACYCNRLC	NAME	DESCRIPTION
0	0	Internal, no force mux	Input mux, offset and gain registers determined by internal register bits INTM1, INTM0.
0	1	Auto-cycling, no force mux	Input mux, offset and gain registers auto-cycled, RINP → GINP → BINP → RINP… on RLC/ACYC pulse.
1	0	Internal, force mux	Input mux selected from internal register bits FM1, FM0; Offset and gain registers selected from internal register bits INTM1, INTM0.
1	1	Auto-cycling, force mux	Input mux selected from internal register bits FM1, FM0; Offset and gain registers auto-cycled, RED → GREEN → BLUE → RED… on RLC/ACYC pulse.

Table 4 Colour Selection Description in Line-by-Line Mode

OPERATING MODES

Table 5 summarises the most commonly used modes, the clock waveforms required and the register contents required for CDS and non-CDS operation.

MODE	DESCRIPTION	CDS AVAILABLE	MAX SAMPLE RATE	SENSOR INTERFACE DESCRIPTION	TIMING REQUIRE-MENTS	REGISTER CONTENTS WITH CDS	REGISTER CONTENTS WITHOUT CDS
1	Colour Pixel-by-Pixel	Yes	4MSPS	The 3 input channels are sampled in parallel. The signal is then gain and offset adjusted before being multiplexed into a single data stream and converted by the ADC, giving an output data rate of 12MSPS max.	MCLK max = 24MHz MCLK: VSMP ratio is 6:1	SetReg1: 03(hex)	SetReg1: 01(hex)
2	Monochrome/ Colour Line-by-Line	Yes	4MSPS	As mode 1 except: Only one input channel at a time is continuously sampled.	MCLK max = 24MHz MCLK: VSMP ratio is 6:1	SetReg1: 07(hex)	SetReg1: 05(hex)
3	Fast Monochrome/ Colour Line-by-Line	Yes	8MSPS	Identical to mode 2	MCLK max = 24MHz MCLK: VSMP ratio is 3:1	Identical to mode 2 plus SetReg3: bits 5:4 must be set to 0(hex)	Identical to mode 2
4	Maximum speed Monochrome/ Colour Line-by-Line	No	12MSPS	Identical to mode 2	MCLK max = 24MHz MCLK: VSMP ratio is 2:1	CDS not possible	SetReg1: 45(hex)
5	Slow Colour Pixel-by-Pixel	Yes	3MSPS	Identical to mode 1	MCLK max = 24MHz MCLK: VSMP ratio is 2n:1, $n \geq 4$	Identical to mode 1	Identical to mode 1
6	Slow Monochrome/ Colour Line-by-Line	Yes	3MPS	Identical to mode 2	MCLK max = 24MHz MCLK: VSMP ratio is 2n:1, $n \geq 4$	Identical to mode 2	Identical to mode 2

Table 5 WM8196 Operating Modes

Notes:

1. In Monochrome mode, SetReg3 bits 7:6 determine which input is to be sampled.
2. For Colour Line-by-Line, set control bit LINEBYLINE. For input selection, refer to Table 4, Colour Selection Description in Line-by-Line Mode.

OPERATING MODE TIMING DIAGRAMS

The following diagrams show 8-bit multiplexed output data and MCLK, VSMP and input video requirements for operation of the most commonly used modes as shown in Table 5. The diagrams are identical for both CDS and non-CDS operation. Outputs from RINP, GINP and BINP are shown as R, G and B respectively. X denotes invalid data.

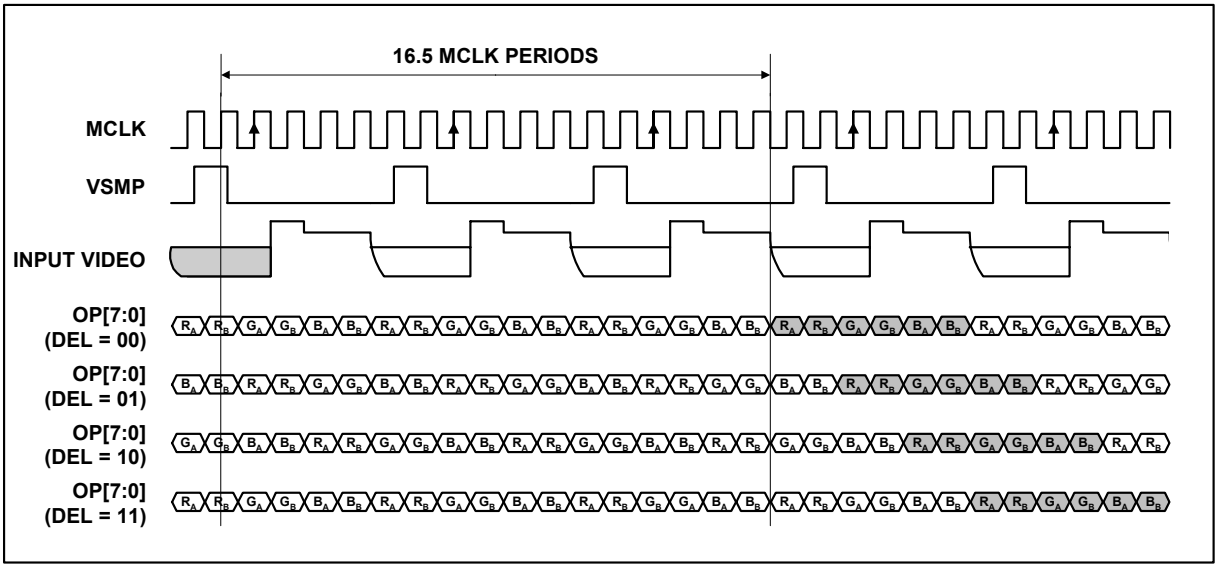


Figure 21 Mode 1 Operation

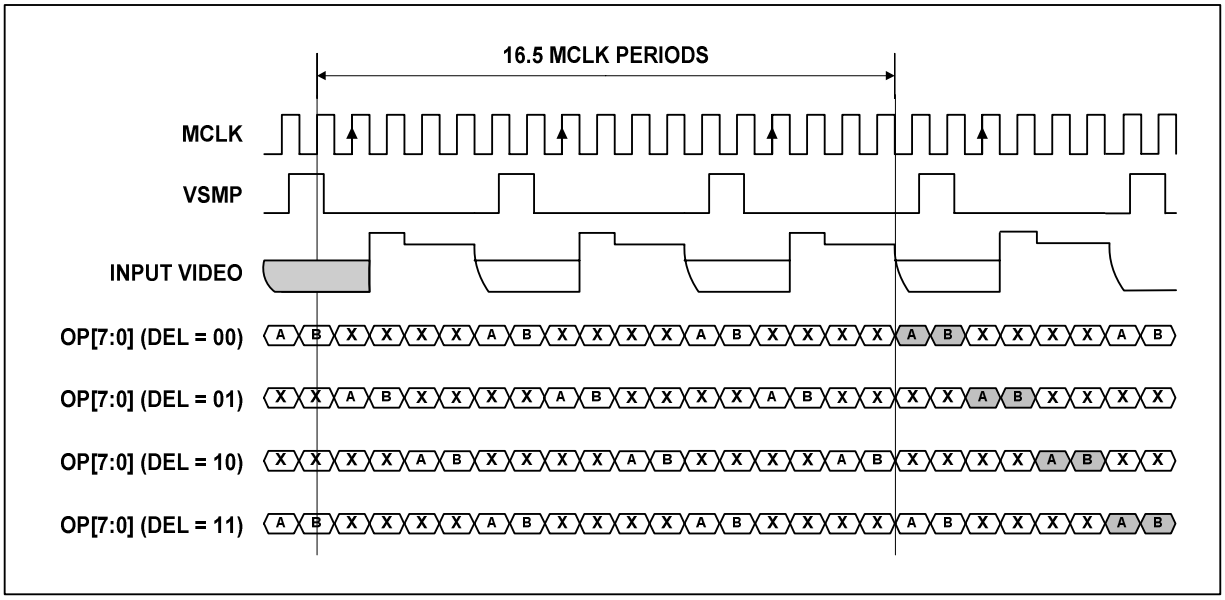


Figure 22 Mode 2 Operation

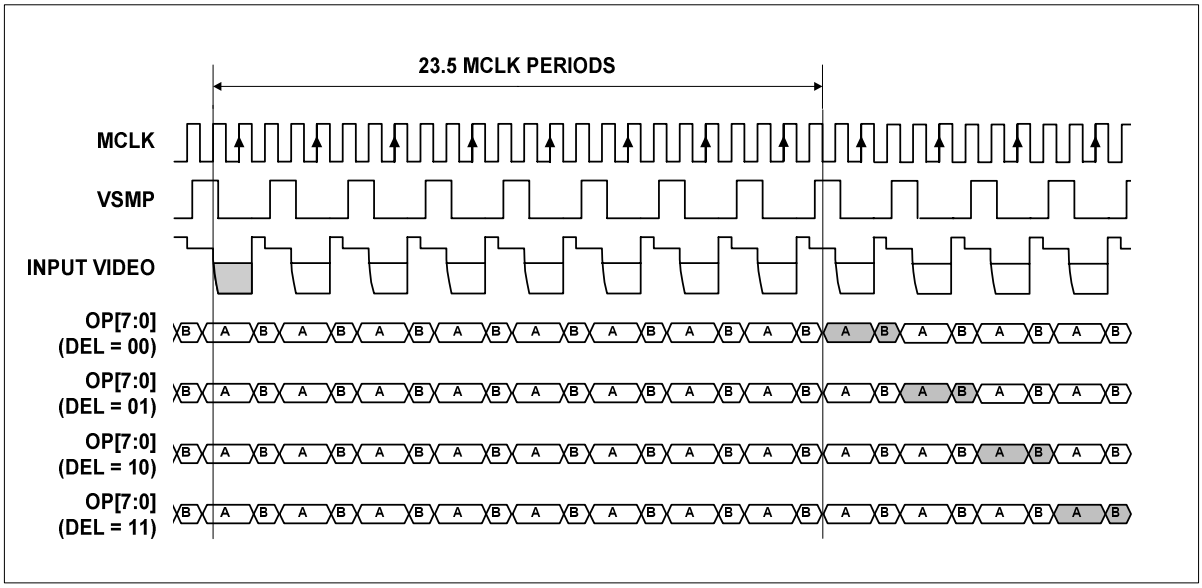


Figure 23 Mode 3 Operation

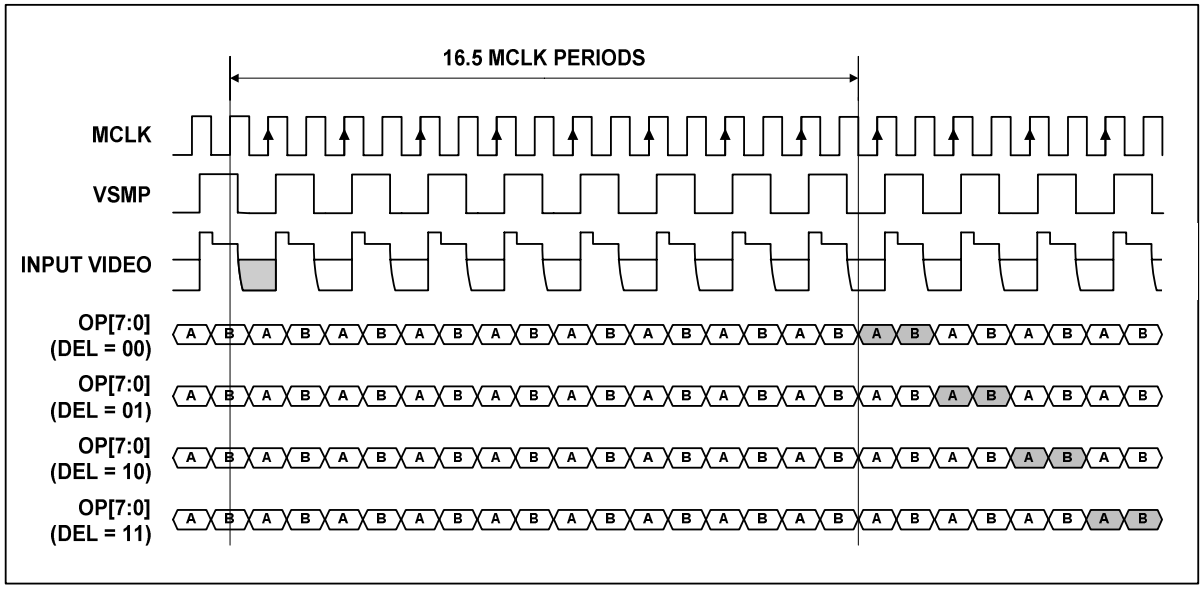


Figure 24 Mode 4 Operation

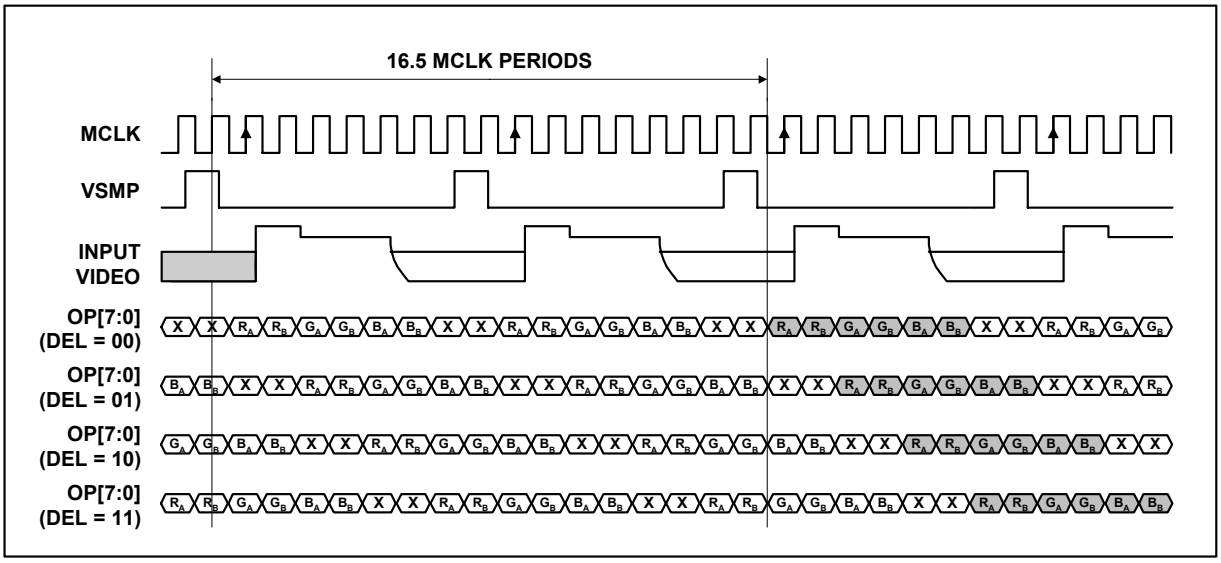


Figure 25 Mode 5 Operation (MCLK:VSMP Ratio = 8:1)

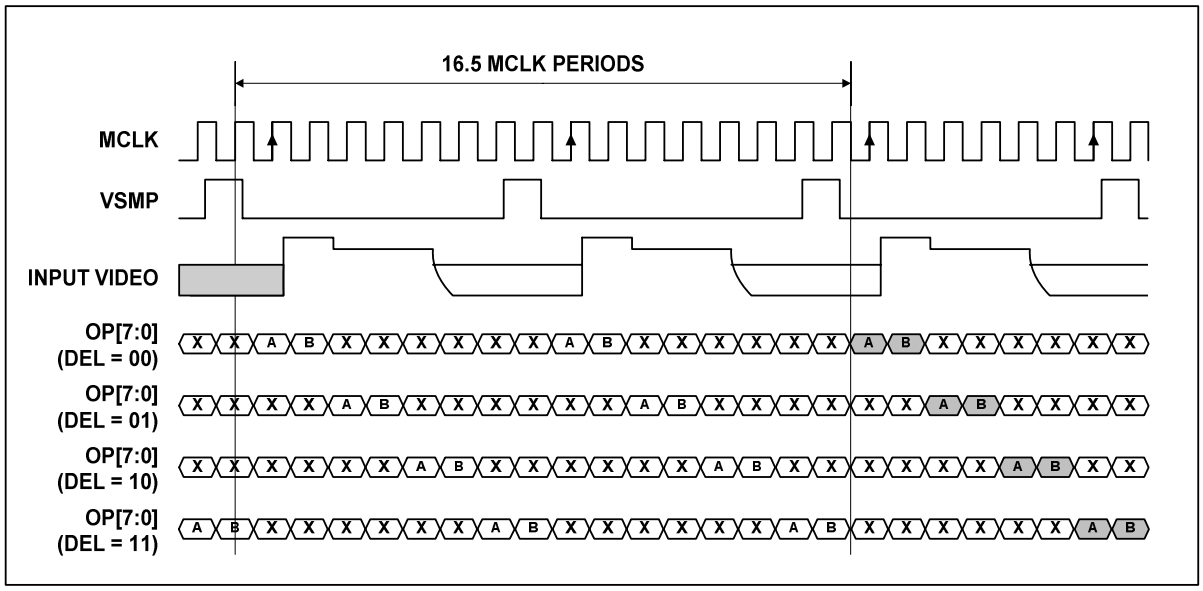


Figure 26 Mode 6 Operation (MCLK:VSMP Ratio = 8:1)