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WM8224

60MSPS 3-Channel AFE with Multiple Device Operation and Programmable Automatic Black Level Calibration

DESCRIPTION

The WM8224 is an analogue front end/digitiser IC which processes and digitises the analogue output signals from CCD sensors or Contact Image Sensors (CIS) at pixel sample rates of up to 60MSPS.

The device includes three analogue signal processing channels each of which contains Reset Level Clamping, Correlated Double Sampling and Programmable Gain and Offset adjust functions. The output from each of these channels is time multiplexed into a single high-speed 16-bit Analogue to Digital Converter. The digital data is available in a variety of output formats via the flexible data port.

An internal 4-bit DAC is supplied for internal reference level generation. This may be used during CDS to reference CIS signals or during Clamping to clamp CCD signals. An external reference level may also be supplied. ADC references are generated internally, ensuring optimum performance from the device.

A programmable automatic Black-Level Calibration function is available to adjust the DC offset of the output data. A daisy chain feature allows multiple devices to operate together using the same control interface and output data bus.

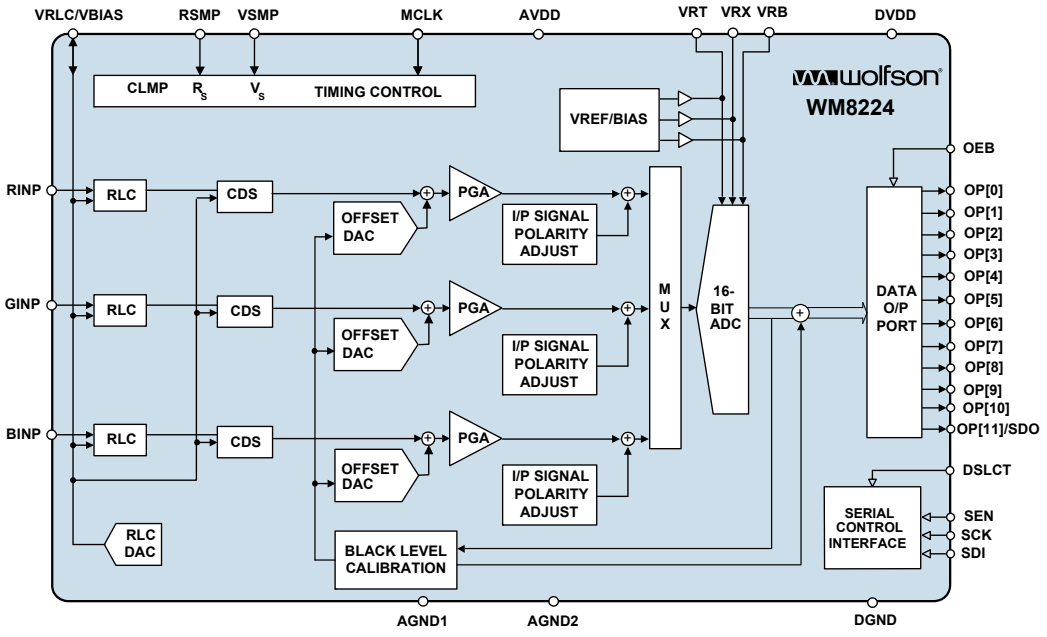
FEATURES

- 12 or 16-bit ADC, 40MSPS conversion rate
- 8 or 10-bit ADC, 60MSPS conversion rate
- Low power – 360 mW typical
- 3.3V single supply operation
- 3 channel operation
- Daisy Chain feature for multiple device use
- Correlated double sampling
- Programmable gain (9-bit resolution)
- Programmable offset adjust (8-bit resolution)
- Flexible clamp timing
- Programmable clamp voltage
- Internally generated voltage references
- Automatic Black Level Calibration
- 32-lead QFN package
- Serial control interface

APPLICATIONS

- Digital Copiers
- USB2.0 compatible scanners
- Multi-function peripherals
- High-speed CCD/CIS sensor interface

BLOCK DIAGRAM



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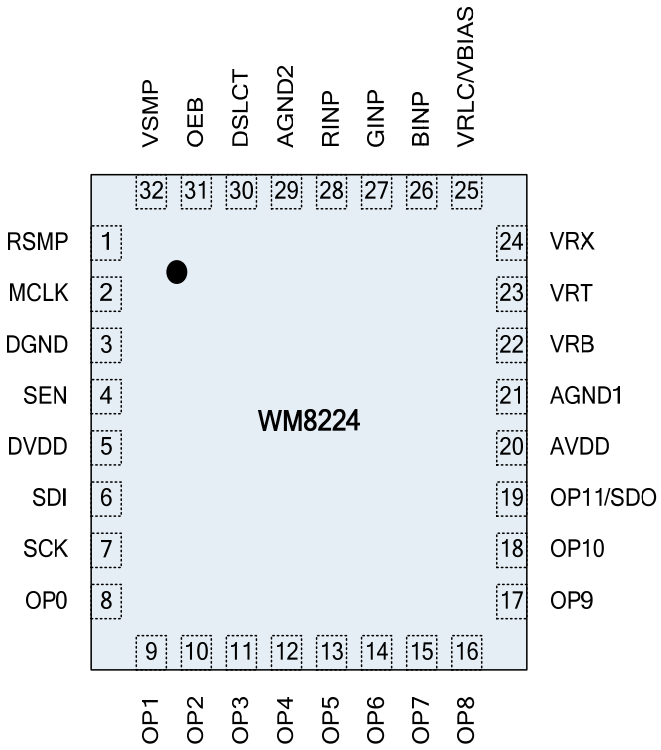
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8224CSEFL	0 to 70°C	32-lead QFN (5x5x0.9mm) (Pb-free)	MSL1	260°C
WM8224CSEFL/R	0 to 70°C	32-lead QFN (5x5x0.9mm) (Pb-free, tape and reel)	MSL1	260°C

Note:

Reel quantity = 3,500

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	RSMP	Digital input	Reset sample pulse (when CDS=1) or clamp control.
2	MCLK	Digital input	Master (ADC) clock. This clock determines the ADC conversion rate.
3	DGND	Supply	Digital ground.
4	SEN	Digital input	Enables the serial interface when high.
5	DVDD	Supply	Digital supply for logic, clock generator and digital input/output pads.
6	SDI	Digital input	Serial interface data input.
7	SCK	Digital input	Serial interface clock.
			Digital output data bus. ADC output data (d15:d0) is available in a variety of output formats.
8	OP[0]	Digital output	d0 (LSB)
9	OP[1]	Digital output	d1
10	OP[2]	Digital output	d2
11	OP[3]	Digital output	d3
12	OP[4]	Digital output	d4
13	OP[5]	Digital output	d5
14	OP[6]	Digital output	d6
15	OP[7]	Digital output	d7
16	OP[8]	Digital output	d8
17	OP[9]	Digital output	d9
18	OP[10]	Digital output	d10
19	OP[11]/SDO	Digital output	d11 (MSB)
			Alternatively, pin OP[11]/SDO may be used to output register read-back data. See Serial Interface description in Device Description section for further details.
20	AVDD	Supply	Analogue supply. This must be operated at the same potential as DVDD.
21	AGND1	Supply	Analogue ground.
22	VRB	Analogue output	Lower reference voltage. This pin must be connected to AGND via a decoupling capacitor.
23	VRT	Analogue output	Upper reference voltage. This pin must be connected to AGND via a decoupling capacitor.
24	VRX	Analogue output	Input return bias voltage. This pin must be connected to AGND via a decoupling capacitor.
25	VRLC/VBIAS	Analogue I/O	Selectable analogue output voltage for RLC or single-ended bias reference. This pin would typically be connected to AGND via a decoupling capacitor. VRLC can be externally driven if programmed Hi-Z.
26	BINP	Analogue input	Blue channel input video.
27	GINP	Analogue input	Green channel input video.
28	RINP	Analogue input	Red channel input video.
29	AGND2	Supply	Analogue ground.
30	DSLCT	Digital Tristate Input	Sets 2-bit device ID for daisy chain operation: 0 = Device ID is 00 1 = Device ID is 01 Z = Device ID is 10
31	OEB	Digital input	Output Hi-Z control. All digital outputs set to high-impedance state when input pin OEB=1, if AUTOZ=0. Note that readback function will override high-impedance on OP11 **This pin has an internal 100kΩ pull-down resistor to AGND.**
32	VSMP	Digital input	Video sample pulse.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Analogue supply voltage: AVDD	GND - 0.3V	GND + 5V
Digital supply voltage: DVDD	GND - 0.3V	GND + 5V
Digital ground: DGND	GND - 0.3V	GND + 0.3V
Analogue grounds: AGND1 – 2	GND - 0.3V	GND + 0.3V
Analogue inputs (RINP, GINP, BINP)	GND - 0.3V	AVDD + 0.3V
Other Analogue pins	GND - 0.3V	AVDD + 0.3V
Digital I/O pins	GND – 0.3V	DVDD + 0.3V
Operating temperature range: T_A	0°C	+70°C
Storage temperature prior to soldering	30°C max / 85% RH max	
Storage temperature after soldering	-65°C	+150°C

Notes:

1. GND denotes the voltage of any ground pin.
2. AGND1, AGND2 and DGND pins are intended to be operated at the same potential. Differential voltages between these pins will degrade performance.

RECOMMENDED OPERATING CONDITIONS

CONDITION	SYMBOL	MIN	TYP	MAX	UNITS
Operating temperature range	T_A	0		70	°C
Analogue supply voltage	AVDD	2.97	3.3	3.63	V
Digital core and I/O supply voltage	DVDD	2.97	3.3	3.63	V

THERMAL PERFORMANCE

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Performance						
Thermal resistance – junction to case	$R_{\theta JC}$	$T_{ambient}$ = 25°C		10.27		°C/W
Thermal resistance – junction to ambient	$R_{\theta JA}$			29.45		°C/W

Notes:

Figure 3 Figures given are for package mounted on 4-layer FR4 according to JESD51-5 and JESD51-7.

ELECTRICAL CHARACTERISTICS

40MHZ OPERATION

Test Conditions
AVDD = DVDD = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 40MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overall System Specification (including 16-bit ADC, PGA, Offset and CDS functions)						
Max Conversion rate				40		MSPS
Full-scale input voltage range (see Note 1)		LOWREFS=0, Max Gain		0.25		Vp-p
		LOWREFS=0, Min Gain		3.03		Vp-p
		LOWREFS=1, Max Gain		0.15		Vp-p
		LOWREFS=1, Min Gain		1.82		Vp-p
Input signal limits (see Note 2)	V_{IN}	FOL_EN=0	AGND-0.3		AVDD+0.3	V
		FOL_EN=1, minimum		AGND		V
		FOL_EN=1, maximum		AGND+1.2		V
Input capacitance	C_{IN}	RINP, GINP, BINP to AGND		10		pF
Full-scale transition error		Gain = 0dB; PGA[8:0] = 18(hex)		20		mV
Zero-scale transition error		Gain = 0dB; PGA[8:0] = 18(hex)		20		mV
Differential non-linearity	DNL	16-bit		1.2		LSB
Integral non-linearity (pk-pk/2)	INL	16-bit		56		LSB
Channel to channel gain matching				1.3		%
Output noise		Unity Gain (Unused channels grounded)		10.2		LSB rms
Programmable Gain Amplifier						
Resolution				9		bits
Gain			$0.66 + \frac{7.34}{511} * PGA[8:0]$			V/V
Max gain, each channel	G_{MAX}			8		V/V
Min gain, each channel	G_{MIN}			0.66		V/V
Analogue to Digital Converter						
Resolution				16		bits
Speed				40		MSPS
Full-scale input range (2*(VRT-VRB))		LOWREFS=0		2		V
		LOWREFS=1		1.2		V

60MHZ OPERATION

Test Conditions
AVDD = DVDD = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 60MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overall System Specification (including 10-bit ADC, PGA, Offset and CDS functions)						
Max Conversion rate				60		MSPS
Full-scale input voltage range (see Note 1)		LOWREFS=0, Max Gain		0.26		Vp-p
		LOWREFS=0, Min Gain		3.03		Vp-p
		LOWREFS=1, Max Gain		0.16		Vp-p
		LOWREFS=1, Min Gain		1.82		Vp-p
Input signal limits (see Note 2)	V_{IN}	FOL_EN=0	AGND-0.3		AVDD+0.3	V
		FOL_EN=1, minimum		AGND		V
		FOL_EN=1, maximum		AGND+1.2		V
Input capacitance	C_{IN}	RINP, GINP, BINP to AGND		10		pF
Full-scale transition error		Gain = 0dB; PGA[8:0] = 18(hex)		20		mV

Test Conditions
AVDD = DVDD = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 60MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Zero-scale transition error		Gain = 0dB; PGA[8:0] = 18(hex)		20		mV
Differential non-linearity	DNL	10-bit		0.5		LSB
Integral non-linearity (pk-pk/2)	INL	10-bit		7		LSB
Channel to channel gain matching				2.5		%
Output noise		Unity Gain 10-bit (Unused channels grounded)		0.5		LSB rms
Programmable Gain Amplifier						
Resolution				9		bits
Gain			$0.66 + \frac{7.34}{511} * PGA[8:0]$			V/V
Max gain, each channel	G_{MAX}			7.7		V/V
Min gain, each channel	G_{MIN}			0.65		V/V
Analogue to Digital Converter						
Resolution				10		bits
Speed				60		MSPS
Full-scale input range (2*(VRT-VRB))		LOWREFS=0		2		V
		LOWREFS=1		1.2		V

Notes:

1. **Full-scale input voltage** denotes the differential input signal amplitude (V_{IN}-VRLC in non-CDS mode, V_{IN}-RESET level in CDS mode) that can be gained to match the ADC full-scale input range.
2. **Input signal limits** are the limits within which each input voltage and VRLC reference must lie.

GENERAL CHARACTERISTICS

Test Conditions
AVDD = DVDD = 3.3V, AGND = DGND = 0V, T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
References						
Upper reference voltage	VRT	LOWREFS=0 LOWREFS=1		2.05 1.85		V V
Lower reference voltage	VRB	LOWREFS=0 LOWREFS=1		1.05 1.25		V V
Input return bias voltage	VRX			1.25		V
Diff. Reference voltage (VRT-VRB)	V_{RTB}	LOWREFS=0 LOWREFS=1		1.0 0.6		V V
Output resistance VRT, VRB, VRX				1		Ω
VRLC/Reset-Level Clamp (RLC)						
RLC switching impedance				50		Ω
VRLC short-circuit current				2		mA
VRLC output resistance				2		Ω
VRLC Hi-Z leakage current		VRLC = 0 to AVDD			1	µA
RLCDAC resolution				4		bits
RLCDAC step size	$V_{RLCSTEP}$	RLCDACRNG=0,		0.173		V/step
	$V_{RLCSTEP}$	RLCDACRNG=1, LOWREFS=0		0.11		V/step
	$V_{RLCSTEP}$	RLCDACRNG=1, LOWREFS=1		0.097		V/step
RLCDAC output voltage at code 0(hex)	V_{RLCBOT}	RLCDACRNG=0, RLCDAC[3:0]=0000,		0.4		V
	V_{RLCBOT}	RLCDACRNG=1, RLCDAC[3:0]=0000,		0.4		V
RLCDAC output voltage at code F(hex)	V_{RLCTOP}	RLCDACRNG=0, RLCDAC[3:0]=1111,		3.0		V
	V_{RLCTOP}	RLCDACRNG=1, RLCDAC[3:0]=1111, LOWREFS = 0		2.05		V
	V_{RLCTOP}	RLCDACRNG=1, RLCDAC[3:0]=1111, LOWREFS = 1		1.85		V
VRLC DNL			-0.5		+0.5	LSB
VRLC INL			-0.5		+0.5	LSB
Offset DAC, Monotonicity Guaranteed						
Resolution				8		bits
Differential non-linearity	DNL			0.1	0.5	LSB
Integral non-linearity	INL			0.75	1	LSB
Step size				2.04		mV/step
Output voltage		Code 00(hex) Code FF(hex)		-250 +250		mV mV
DIGITAL SPECIFICATIONS						
Digital Inputs						
High level input voltage	V_{IH}		0.7 * DVDD			V
Low level input voltage	V_{IL}				0.2 * DVDD	V
High level input current	I_{IH}				1	µA
Low level input current	I_{IL}				1	µA
Input capacitance	C_I			5		pF

Test Conditions
AVDD = DVDD = 3.3V, AGND = DGND = 0V, T_A = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Outputs						
High level output voltage	V_{OH}	I_{OH} = 1mA	DVDD – 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 1mA			0.5	V
High impedance output current	I_{OZ}				1	µA
Digital IO Pins						
Applied high level input voltage	V_{IH}		0.7 * DVDD			V
Applied low level input voltage	V_{IL}				0.2 * DVDD	V
High level output voltage	V_{OH}	I_{OH} = 1mA	DVDD – 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 1mA			0.5	V
Low level input current	I_{IL}				1	µA
High level input current	I_{IH}				1	µA
Input capacitance	C_I			5		pF
Output Impedance	Ro	Io = 1mA		38		Ω
High impedance output current	I_{OZ}				1	µA
Supply Currents						
Analogue supply current – active		FOL_EN=0		93		mA
		FOL_EN=1		141		mA
Digital supply current – active		FOL_EN=0		7.3		mA
		FOL_EN=1		8		mA
Total supply current – active		FOL_EN=0		100.3		mA
		FOL_EN=1		149		mA
Total supply current – full power down mode				150	200	µA

INPUT VIDEO SAMPLING

CDS MODE (CDS=1)

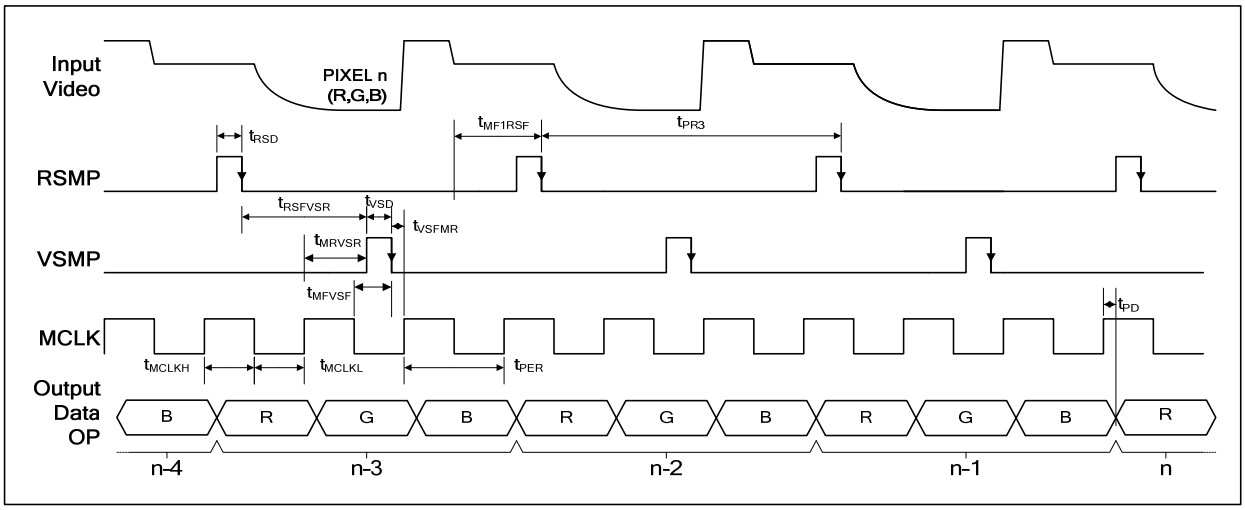


Figure 1 Three-channel CDS Operation (CDS=1)

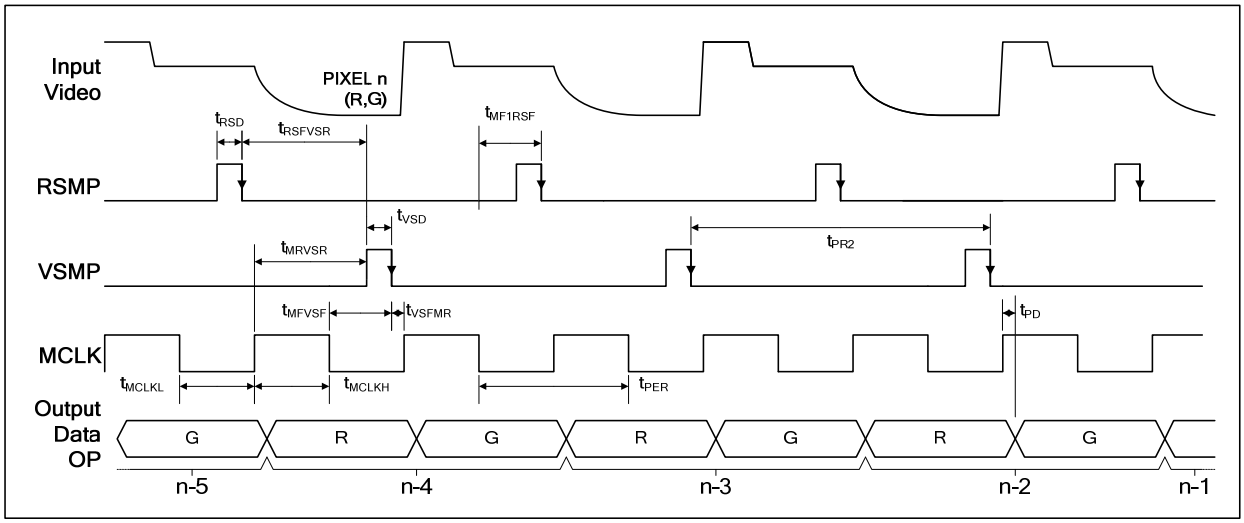


Figure 2 Two-channel CDS Operation (CDS=1)

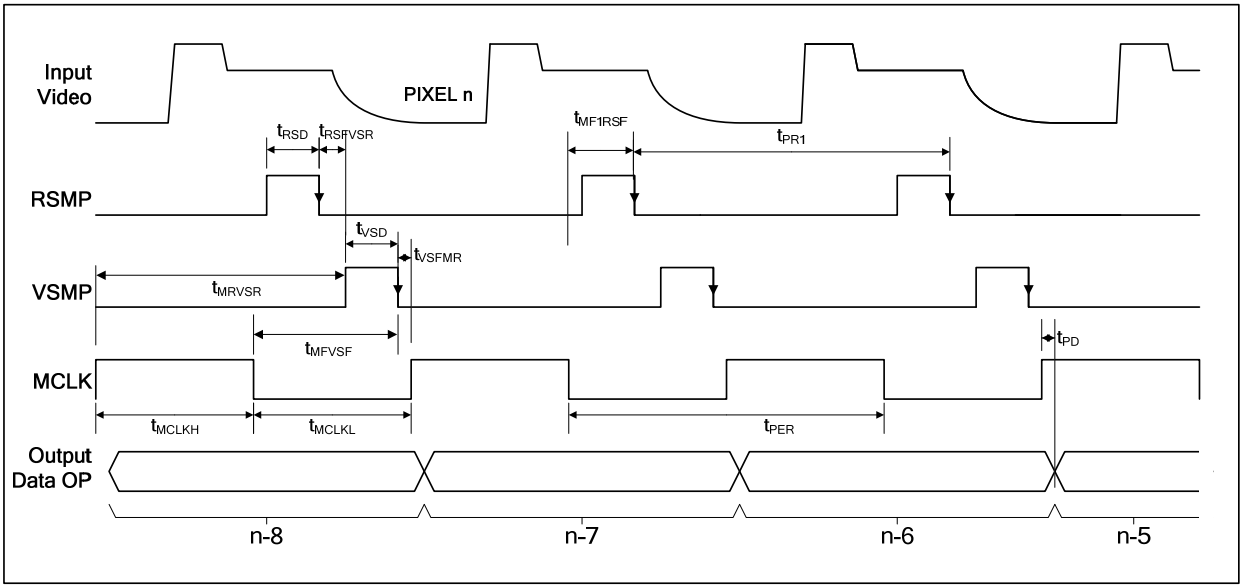


Figure 3 One-channel CDS Operation (CDS=1)

Notes:

1. The relationship between input video signal and sample points is controlled by VSMP and RSMP.
2. When VSMP is high the input video signal is connected to the Video sampling capacitors.
3. When RSMP is high the input video signal is connected to the Reset sampling capacitors.
4. Non-CDS operation is also possible; VSMP, MCLK timing is unchanged, RSMP is not required in this mode but can be used to control input clamping.

NON-CDS MODE (CDS=0)

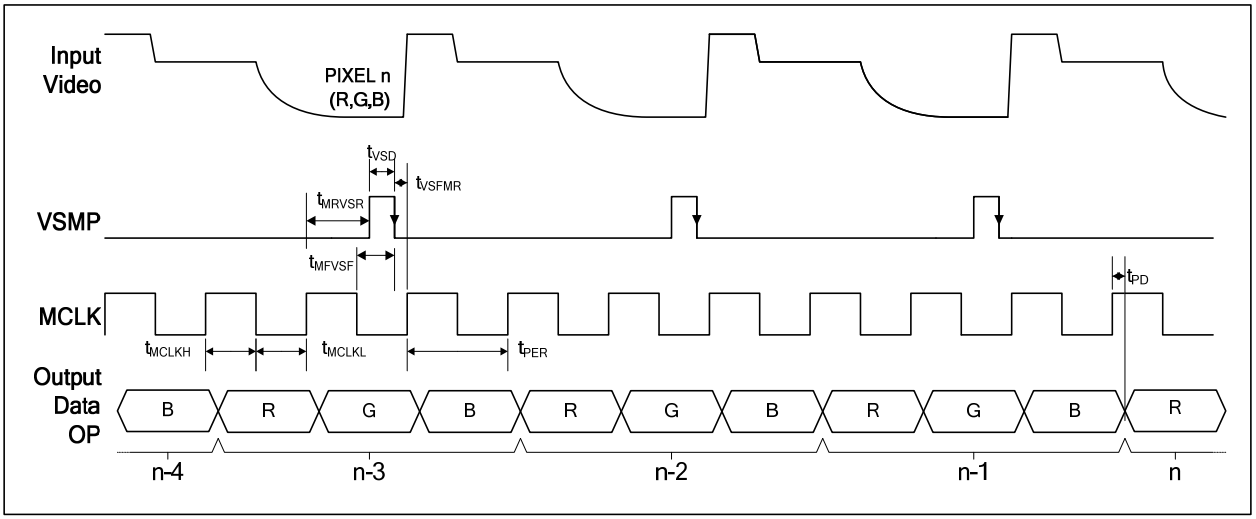


Figure 4 Three-channel non-CDS Operation (CDS=0)

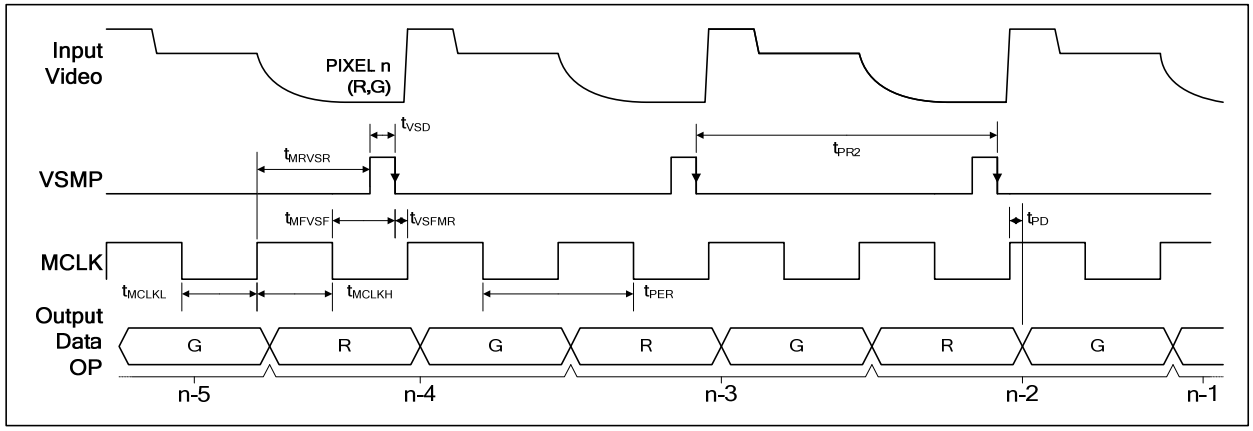


Figure 5 Two-channel non-CDS Operation (CDS=0)

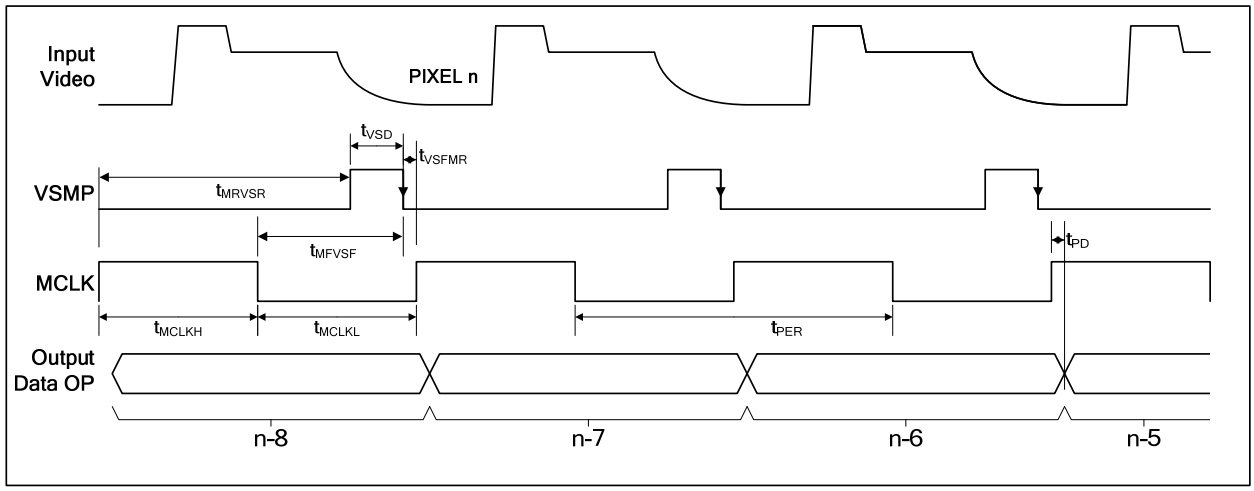


Figure 6 One-channel non-CDS Operation (CDS=0)

Notes:

1. The relationship between input video signal and sample points is controlled by VSMP and RSMP.
2. When VSMP is high the input video signal is connected to the Video sampling capacitors and VRLC is connected to the Reset sampling capacitors.
3. RSMP is not required in this mode but can be used to control input clamping.

Test Conditions
AVDD = DVDD = 3.3V, AGND = DGND = 0V, T_A = 25°C.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MCLK period, ACLKDIV=00 (default)	t_{PER}	12 or 16 bit	25			ns
	t_{PER}	8 or 10 bit	16.67			ns
MCLK high period	t_{MCLKH}			0.5		MCLK periods
MCLK low period	t_{MCLKL}			0.5		MCLK periods
MCLK Duty Cycle			45:55		55:45	%
RSMP pulse high time	t_{RSD}		3			ns
VSMP pulse high time	t_{VSD}		2			ns
RSMP falling to VSMP rising time	t_{RSFVSR}		0			ns
MCLK rising to VSMP rising time	t_{MRVSR}		3			ns
MCLK falling to VSMP falling time	t_{MFVSF}		7			ns
VSMP falling to MCLK rising time	t_{VSFMR}		0			ns
1st MCLK falling edge after VSMP falling to RSMP falling time	t_{MF1RSF}		7			ns
3-channel mode pixel period	t_{PR3}		3			MCLK periods
2-channel mode pixel period	t_{PR2}		2			MCLK periods
1-channel mode pixel period	t_{PR1}		1			MCLK periods
Output latency. From 1st rising edge of MCLK after VSMP falling to data output	LAT	OPDEL[3:0]=0000, ACLKDIV=00		7		MCLK periods

Notes:

1. Parameters are measured at 50% of the rising/falling edge.

OUTPUT DATA TIMING

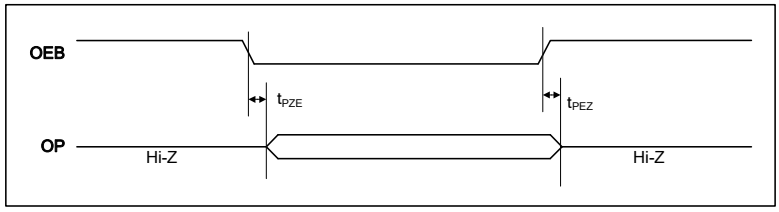


Figure 7 Output Enable/Disable Timing from OEB Pin

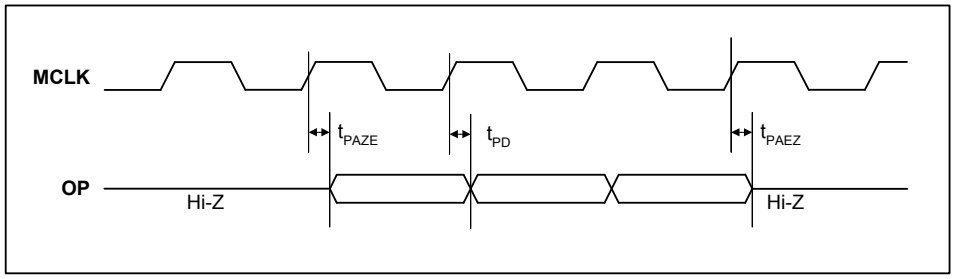


Figure 8 Output Enable/Disable Timing with AUTOZ=1

Test Conditions
AVDD = DVDD = 3.3V, AGND = DGND = 0V, T_A = 25°C, MCLK = 40MHz unless otherwise stated..

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output propagation delay	t_{PD}	I_{OH} & I_{OL} = 1mA AUTOZ=0	3	4.5	7	ns
Output enable time, from OEB falling edge	t_{PZE}			5		ns
Output disable time, from OEB rising edge.	t_{PEZ}			3		ns
Automatic output enable time from MCLK rising edge.	t_{PAZE}	AUTOZ=1, OEDEL=01		5.5		ns
Automatic output disable time from MCLK rising edge.	t_{PAEZ}	AUTOZ=1, all OEDEL settings		3		ns

SERIAL INTERFACE

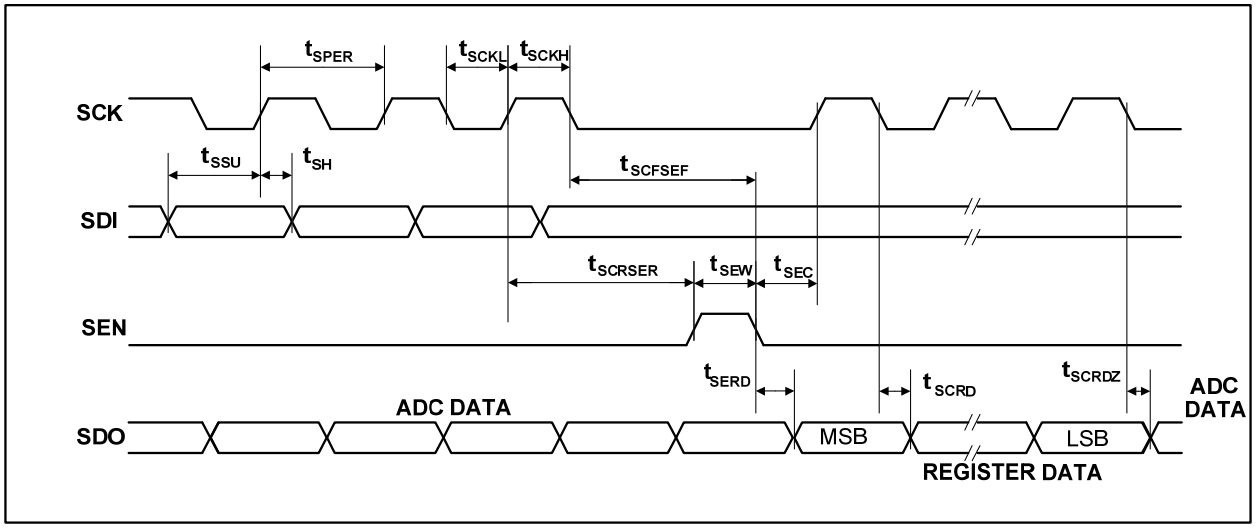


Figure 9 Serial Interface Timing

Test Conditions
AVDD = DVDD = 3.3V, AGND = DGND = 0V, T_A = 25°C, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SCK period	t_{SPER}		83.3			ns
SCK high	t_{SCKH}		37.5			ns
SCK low	t_{SCKL}		37.5			ns
SDI set-up time	t_{SSU}		6			ns
SDI hold time	t_{SH}		6			ns
SCK Rising to SEN Rising	t_{SCRSER}		37.5			ns
SCK Falling to SEN Falling	t_{SCFSEF}		12			ns
SEN to SCK set-up time	t_{SEC}		12			ns
SEN pulse width	t_{SEW}		60			ns
SEN low to SDO = Register data	t_{SERD}				30	ns
SCK low to SDO = Register data	t_{SCRD}				30	ns
SCK low to SDO = ADC data	t_{SCRDZ}				30	ns

Note:

Figure 3 Parameters are measured at 50% of the rising/falling edge

INTERNAL POWER ON RESET CIRCUIT

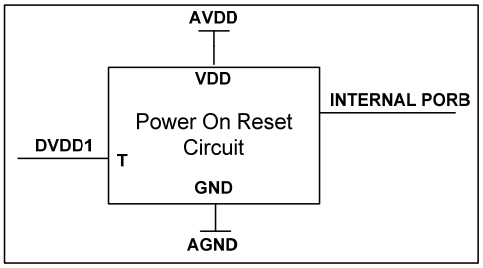


Figure 10 Internal Power On Reset Circuit Schematic

The WM8224 includes an internal Power-On-Reset Circuit, as shown in Figure 10, which is used to reset the digital logic into a default state after power up. The POR circuit is powered from AVDD and monitors DVDD. It asserts PORB low if AVDD or DVDD is below a minimum threshold.

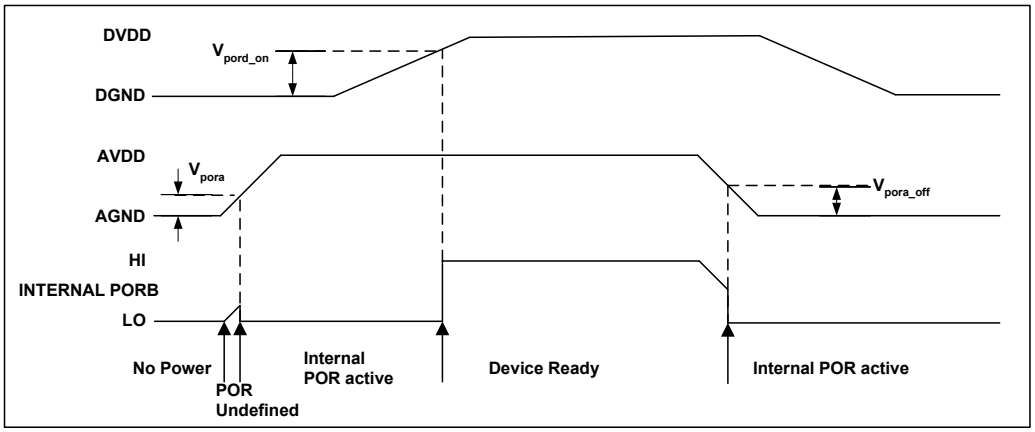


Figure 11 Typical Power up Sequence where AVDD is Powered before DVDD

Figure 11 shows a typical power-up sequence where AVDD is powered up first. When AVDD rises above the minimum threshold, Vpora, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. Now AVDD is at full supply level. Next DVDD rises to Vpord_on and PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where AVDD falls first, PORB is asserted low whenever AVDD drops below the minimum threshold Vpora_off.

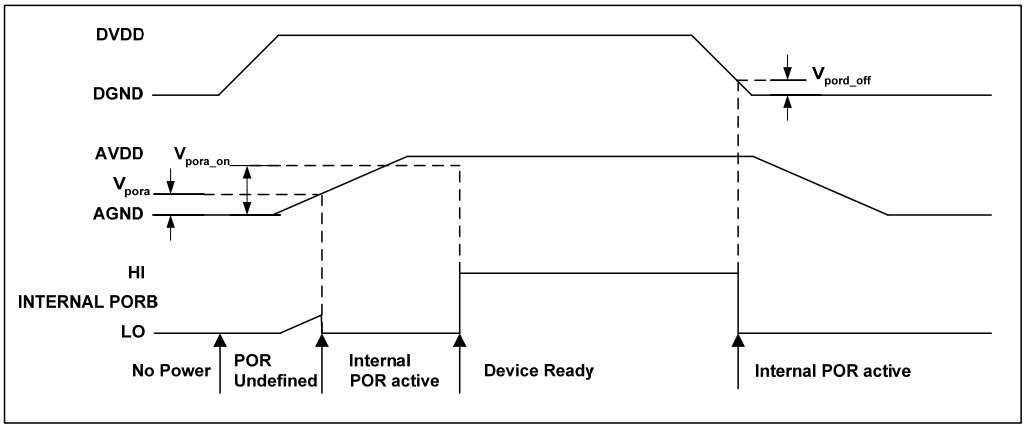


Figure 12 Typical Power up Sequence where DVDD is Powered before AVDD

Figure 12 shows a typical power-up sequence where DVDD is powered up first. First it is assumed that DVDD is already up to specified operating voltage. When AVDD goes above the minimum threshold, Vpora, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When AVDD rises to Vpora_on, PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where DVDD falls first, PORB is asserted low whenever DVDD drops below the minimum threshold Vpord_off.

SYMBOL	MIN	TYP	MAX	UNIT
V_{pora}	0.4	0.6	0.8	V
V_{pora_on}	0.9	1.2	1.6	V
V_{pora_off}	0.4	0.6	0.8	V
V_{pord_on}	0.5	0.7	0.9	V
V_{pord_off}	0.4	0.6	0.8	V

Table 1 Typical POR Operation (typical values, not tested)

Note: It is recommended that every time power is cycled to the WM8224 a software reset is written to the software register to ensure that the contents of the control registers are at their default values before carrying out any other register writes.

DEVICE DESCRIPTION

INTRODUCTION

A block diagram of the device showing the signal path is presented on the front page of this datasheet.

The WM8224 samples up to three inputs (RINP, GINP and BINP) simultaneously. The device then processes the sampled video signal with respect to the video reset level or an internally/externally generated reference level using between one and three processing channels.

Each processing channel consists of an Input Sampling block with optional Reset Level Clamping (RLC) and Correlated Double Sampling (CDS), an 8-bit programmable offset DAC and a 9-bit Programmable Gain Amplifier (PGA).

The processing channel outputs are switched alternately by a 3:1 multiplexer to the ADC input.

The ADC then converts each resulting analogue signal to a digital word. The digital output from the ADC is presented in a variety of possible output formats onto the output bus, OP[11:0]. The twelve output pins can be set to a high impedance state using either the OEB control pin or the OPD register bit.

On-chip control registers determine the configuration of the device, including the offsets and gains applied to each channel. These registers are programmable via a serial interface.

The device has a Black-Level Calibration function which allows the D.C. offset determined during the optically-black pixels at the beginning of the linear sensor to be removed during the image-pixels.

CONFIGURABLE RESOLUTION OF ADC

The WM8224 has a configurable ADC resolution. The default setting is 16 bits resolution. This can be changed by the user by changing a register setting.

The register RES[1:0] can be changed to alter the resolution from 16 bits to either 12, 10 or 8 bits resolution.

INPUT SAMPLING

The WM8224 can sample and process up to three inputs through one to three processing channels as follows:

Colour Pixel-by-Pixel: The three inputs (RINP, GINP and BINP) are simultaneously sampled for each pixel and a separate channel processes each input. The signals are then multiplexed into the ADC, which converts all three inputs within the pixel period.

Two Channel Pixel-by-pixel: Two input channels (RINP and GINP, RINP and BINP, or GINP and BINP) are simultaneously sampled for each pixel and a separate channel processes each input. The signals are then multiplexed into the ADC, which converts both inputs within the pixel period. The unused channel can be changed via the control interface. The unused channel is powered down when this mode is selected.

Monochrome: A single chosen input (RINP, GINP, or BINP) is sampled, processed by the corresponding channel, and converted by the ADC. The choice of input channel can be changed via the control interface. The unused channels are powered down when this mode is selected.

RESET LEVEL CLAMPING (RLC)

To ensure that the signal applied to the WM8224 lies within the supply voltage range (0V to AVDD) the output signal from a CCD is usually level shifted by coupling through a capacitor, $C_{IN.}$ The RLC circuit clamps the WM8224 side of this capacitor to a suitable voltage through a CMOS switch during the CCD reset period (pixel clamping) or during the black pixels (line clamping). In order for clamping to produce correct results the input voltage during the clamping must be a constant value.

Note that if the ac coupling capacitor (C_{IN}) is used in non-CDS mode (CDS=0), then to minimise code drift, line clamping should be used and internal input voltage buffers enabled using the FOL_EN register bit. Alternatively, if the input signal contains a stable reference/reset level then pixel clamping should be used, and the voltage buffers need not be enabled.

The WM8224 allows the user to control the RLC switch in a variety of ways as illustrated in Figure 13. This figure shows a single channel, however all 3 channels are identical, each with its own clamp switch controlled by the common CLMP signal.

The method of control chosen depends upon the characteristics of the input video. The RLCEN register bit must be set to 1 to enable clamping, otherwise the RLC switch cannot be closed (by default RLCEN=1).

Note that unused inputs should be left floating, or grounded through a decoupling capacitor, if reset level clamping is used.

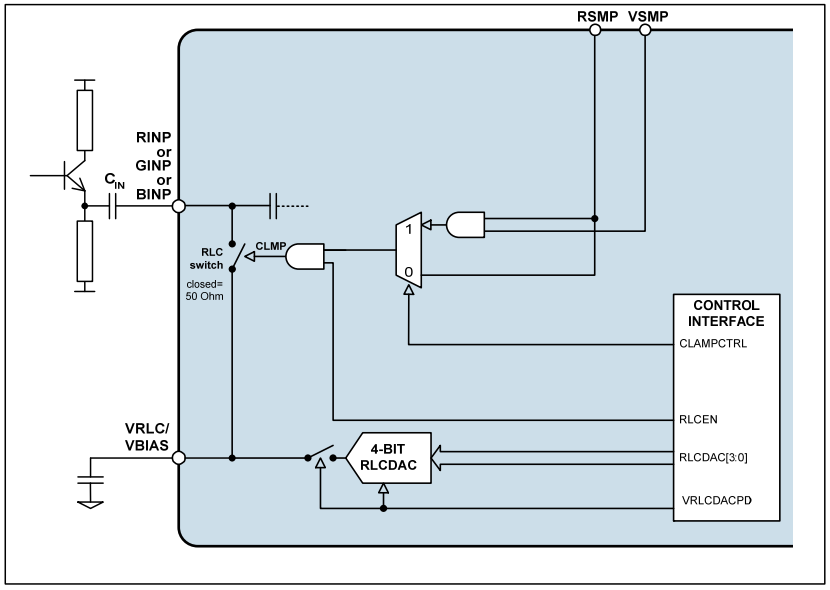


Figure 13 RLC Clamp Control Options

When an input waveform has a stable reference level on every pixel it may be desirable to clamp every pixel during this period. Setting CLMPCTRL=0 means that the RLC switch is closed whenever the RSMP input pin is high, as shown in Figure 14.

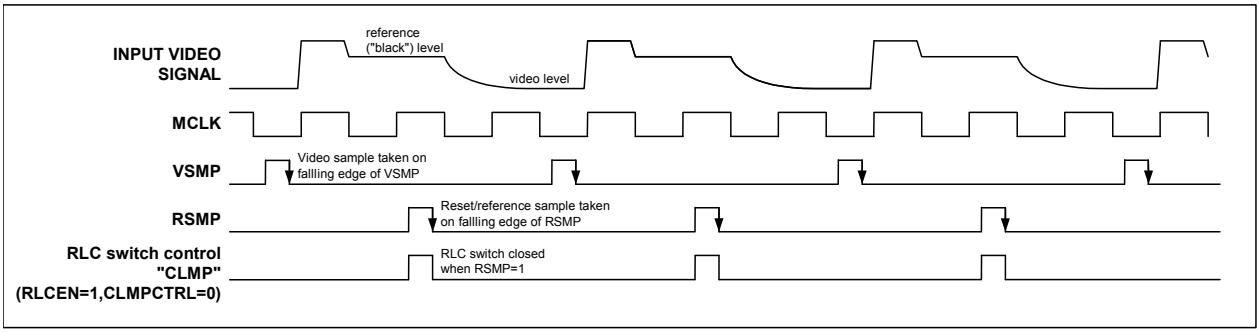


Figure 14 Reset Level Clamp Operation (CLMPCTRL=0), CDS operation shown, non-CDS also possible

In situations where the input video signal does not have a stable reference level it may be necessary to clamp only during those pixels which have a known state (e.g. the dummy, or “black” pixels at the start or end of a line on most image sensors). This is known as line-clamping and relies on the input capacitor to hold the DC level between clamp intervals. In non-CDS mode (CDS=0) this can be done directly by controlling the RSMP input pin to go high during the black pixels only. Note that internal input voltage buffers should be enabled using the FOL_EN register bit when using this mode of operation.

Alternatively it is possible to use RSMP to identify the black pixels and enable the clamp at the same time as the input is being sampled (i.e. when VSMP is high and RSMP is high). This mode is enabled by setting CLMPCTRL=1 and the operation is shown in Figure 15.

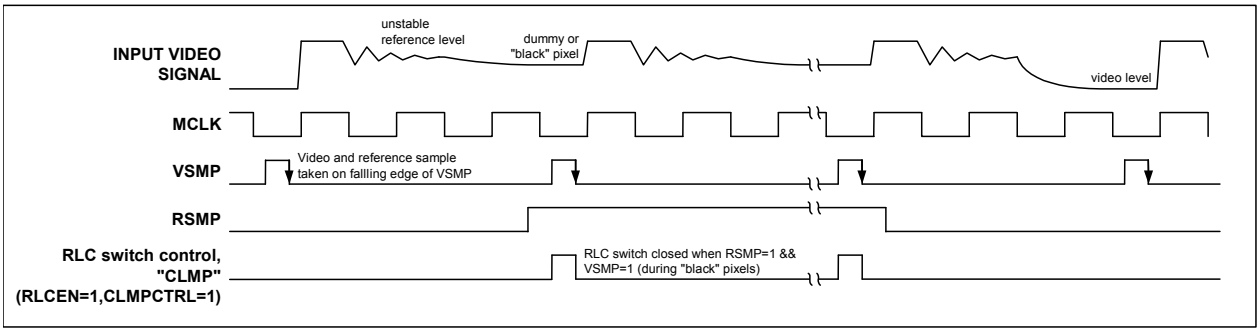


Figure 15 Reset Level Clamp Operation (CLMPCTRL=1), non-CDS mode only

RLCEN	CLAMPCTRL	OUTCOME	USE
0	X	RLC is not enabled. RLC switch is always open.	When input is DC coupled and within supply rails.
1	0	RLC switch is controlled directly from RSMP input pin: RSMP=0: switch is open RMSP=1: switch is closed	When ASIC explicitly provides a reset sample signal and the input video waveform has a suitable reset level.
1	1	VSMP applied as normal, RSMP is used to indicate the location of black pixels RLC switch is controlled by logical combination of RSMP and VSMP: RSMP && VSMP = 1: switch is closed Switch is re-opened when: VSMP=0 (non-CDS mode) VSMP=0 and RSMP=0 (CDS mode)	When clamping during the video period of black pixels or there is no stable per-pixel reference level. This method of operation is generally only sensible in non-CDS mode.

Table 2 Reset Level Clamp Control Summary

CDS/NON-CDS PROCESSING

For CCD type input signals, containing a fixed reference/reset level, the signal may be processed using Correlated Double Sampling (CDS), which will remove pixel-by-pixel common mode noise. With CDS processing the input waveform is sampled at two different points in time for each pixel, once during the reference/reset level and once during the video level. To sample using CDS, register bit CDS must be set to 1 (default). This causes the signal reference to come from the video reference level as shown in Figure 16.

The video sample is always taken on the falling edge of the input VSMP signal (VS). In CDS-mode the reset level is sampled on the falling edge of the RSMP input signal (RS).

For input signals that do not contain a reference/reset level (e.g. CIS sensor signals), non-CDS processing is used (CDS=0). In this case, the video level is processed with respect to the voltage on pin VRLC/VBIAS. The VRLC/VBIAS voltage is sampled at the same time as VSMP samples the video level in this mode. Note that if the ac coupling capacitor (C_{IN}) is used in non-CDS mode (CDS=0), then to minimise code drift, line clamping should be used and internal input voltage buffers enabled using the FOL_EN register bit. Alternatively, if the input signal contains a stable reference/reset level then pixel clamping should be used, and the voltage buffers need not be enabled.

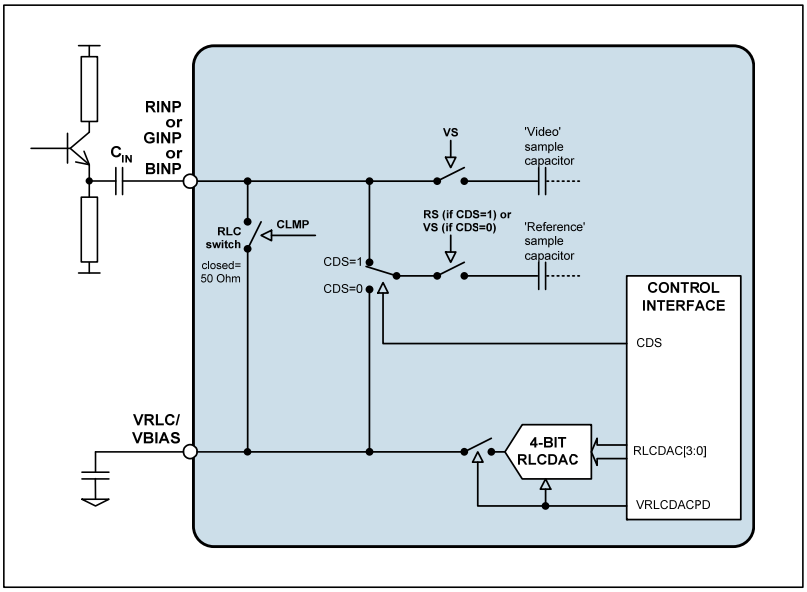


Figure 16 CDS/non-CDS Input Configuration

OFFSET ADJUST AND PROGRAMMABLE GAIN

The output from the CDS block is a differential signal, which is added to the output of an 8-bit Offset DAC to compensate for offsets and then amplified by a 9-bit PGA. The gain and offset for each channel are independently programmable by writing to control bits DAC[7:0] and PGA[8:0].

The gain characteristic of the WM8224 PGA is shown in Figure 17. Figure 18 shows the maximum device input voltage that can be gained up to match the ADC full-scale input range (default=2V).

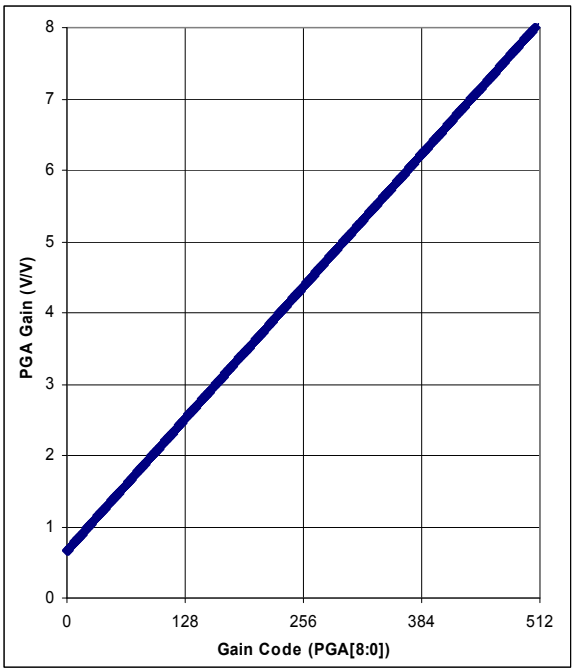


Figure 17 PGA Gain Characteristic

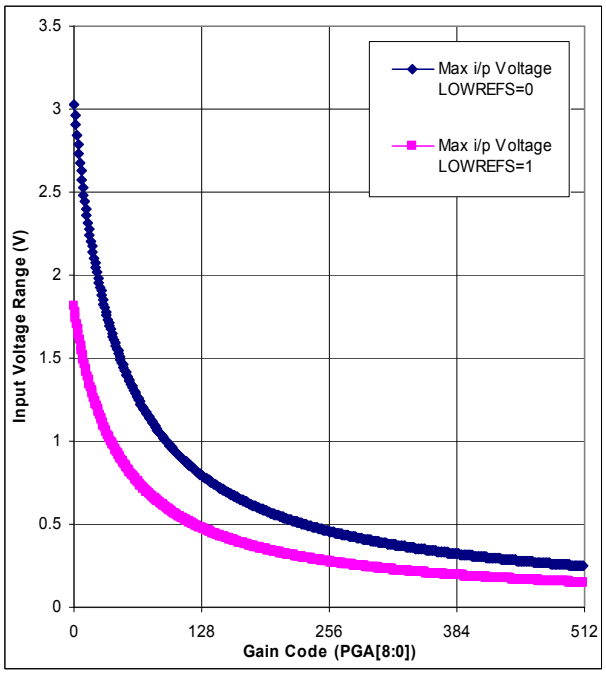


Figure 18 Peak Input Voltage to Match ADC Full-scale Range

ADC INPUT BLACK LEVEL ADJUST

The output from the PGA can be offset to match the full-scale range of the differential ADC (2*[VRT-VRB]).

For negative-going input video signals, a black level (zero differential) output from the PGA should be offset to the top of the ADC range by setting register bits PGAFS[1:0]=10. This will give an output code of FFFF (hex) from the WM8224 for zero input. If code zero is required for zero differential input then the INVOP bit should be set.

For positive going input signals the black level should be offset to the bottom of the ADC range by setting PGAFS[1:0]=11. This will give an output code of 0000 (hex) from the WM8224 for zero input.

Bipolar input video is accommodated by setting PGAFS[1:0]=00 or PGAFS[1:0]=01. Zero differential input voltage gives mid-range ADC output, 7FFF (hex).

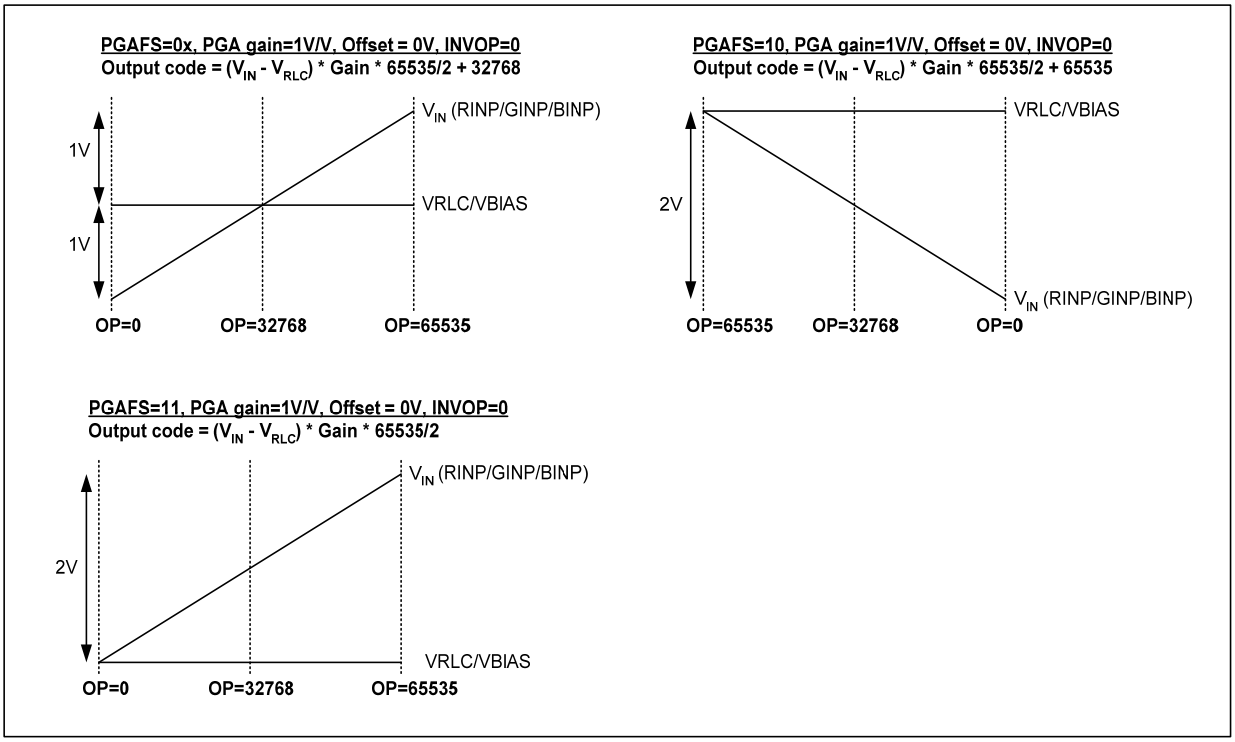


Figure 19 ADC Input Black Level Adjust Settings

OVERALL SIGNAL FLOW SUMMARY

Figure 20 represents the processing of the video signal through the WM8224.

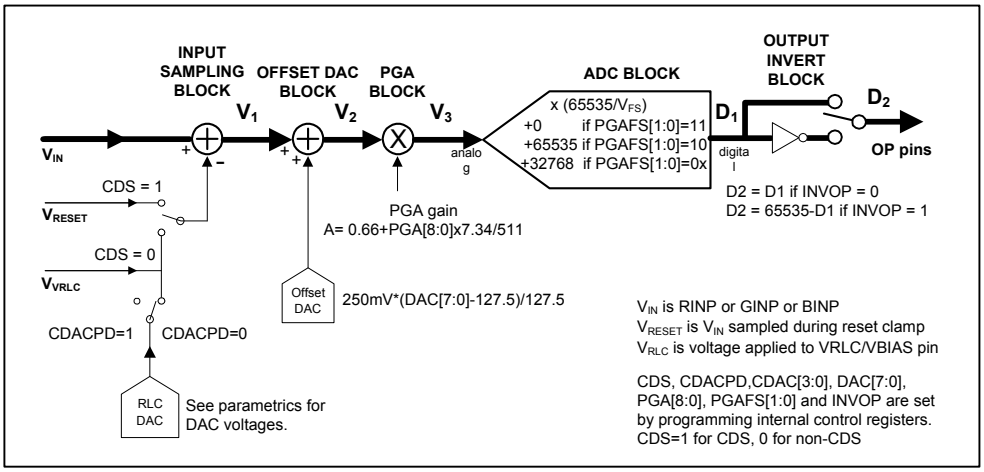


Figure 20 Overall Signal Flow

The **INPUT SAMPLING BLOCK** produces an effective input voltage $\mathbf{V_1}$. For CDS, this is the difference between the input video level V_{IN} and the input reset level V_{RESET}. For non-CDS this is the difference between the input video level V_{IN} and the voltage on the VRLC/VBIAS pin, V_{VRLC}, optionally set via the RLC DAC.

The **OFFSET DAC BLOCK** then adds the amount of fine offset adjustment required to move the black level of the input signal towards 0V, producing $\mathbf{V_2}$.

The **PGA BLOCK** then amplifies the white level of the input signal to maximise the ADC range, outputting voltage $\mathbf{V_3}$.

The **ADC BLOCK** then converts the analogue signal, $\mathbf{V_3}$, to a 16-bit unsigned digital output, $\mathbf{D_1}$.

The digital output is then inverted, if required, through the **OUTPUT INVERT BLOCK** to produce $\mathbf{D_2}$.

CALCULATING THE OUTPUT CODE FOR A GIVEN INPUT

The following equations describe the processing of the video and reset level signals through the WM8224.

INPUT SAMPLING BLOCK: INPUT SAMPLING AND REFERENCING

If CDS = 1, (i.e. CDS operation) the previously sampled reset level, V_{RESET}, is subtracted from the input video, V_{IN} (= RINP, GINP or BINP).

$$\mathbf{V_1} = V_{IN} - V_{RESET} \quad \text{Eqn. 1}$$

If CDS = 0, (non-CDS operation) the simultaneously sampled voltage on pin VRLC is subtracted instead.

$$\mathbf{V_1} = V_{IN} - V_{VRLC} \quad \text{Eqn. 2}$$

If VRLCDACPD = 1, V_{VRLC} is an externally applied voltage on pin VRLC/VBIAS.

If VRLCDACPD = 0, V_{VRLC} is the output from the internal RLC DAC.

$$V_{VRLC} = (V_{RLCSTEP} * \text{RLC DAC[3:0]}) + V_{RLCBOT} \quad \text{Eqn. 3}$$

$V_{RLCSTEP}$ is the step size of the RLC DAC and V_{RLCBOT} is the minimum output of the RLC DAC.

OFFSET DAC BLOCK: OFFSET (BLACK-LEVEL) ADJUST

The resultant signal $\mathbf{V_1}$ is added to the Offset DAC output.

$$\mathbf{V_2} = \mathbf{V_1} + \{250mV * (\text{DAC[7:0]}-127.5)\} / 127.5 \quad \text{Eqn. 4}$$

PGA NODE: GAIN ADJUST

The signal is then multiplied by the PGA gain.

$$\mathbf{V_3} = \mathbf{V_2} * (0.66 + \text{PGA[8 :0]}x7.34/511) \quad \text{Eqn. 5}$$

ADC BLOCK : ANALOGUE-DIGITAL CONVERSION

The analogue signal is then converted to a 16-bit unsigned number, with input range configured by PGAFS[1:0].

$$\mathbf{D_1}[15:0] = \text{INT}\{(\mathbf{V_3}/V_{FS}) * 65535\} + 32767 \quad \text{PGAFS[1:0] = 00 or 01} \quad \text{Eqn. 6}$$

$$\mathbf{D_1}[15:0] = \text{INT}\{(\mathbf{V_3}/V_{FS}) * 65535\} \quad \text{PGAFS[1:0] = 11} \quad \text{Eqn. 7}$$

$$\mathbf{D_1}[15:0] = \text{INT}\{(\mathbf{V_3}/V_{FS}) * 65535\} + 65535 \quad \text{PGAFS[1:0] = 10} \quad \text{Eqn. 8}$$

where the ADC full-scale range, V_{FS} = 2V when LOWREFS=0 and V_{FS} = 1.2V when LOWREFS=1.

OUTPUT INVERT BLOCK: POLARITY ADJUST

The polarity of the digital output may be inverted by control bit INVOP.

$$\mathbf{D_2}[15:0] = \mathbf{D_1}[15:0] \quad (\text{INVOP} = 0) \quad \text{Eqn. 9}$$

$$\mathbf{D_2}[15:0] = 65535 - \mathbf{D_1}[15:0] \quad (\text{INVOP} = 1) \quad \text{Eqn. 10}$$

OUTPUT FORMATS

The output from the WM8224 can be presented in several different formats under control of the OPFORM register bit as shown in Figure 21. In addition the data can be presented at different resolutions.

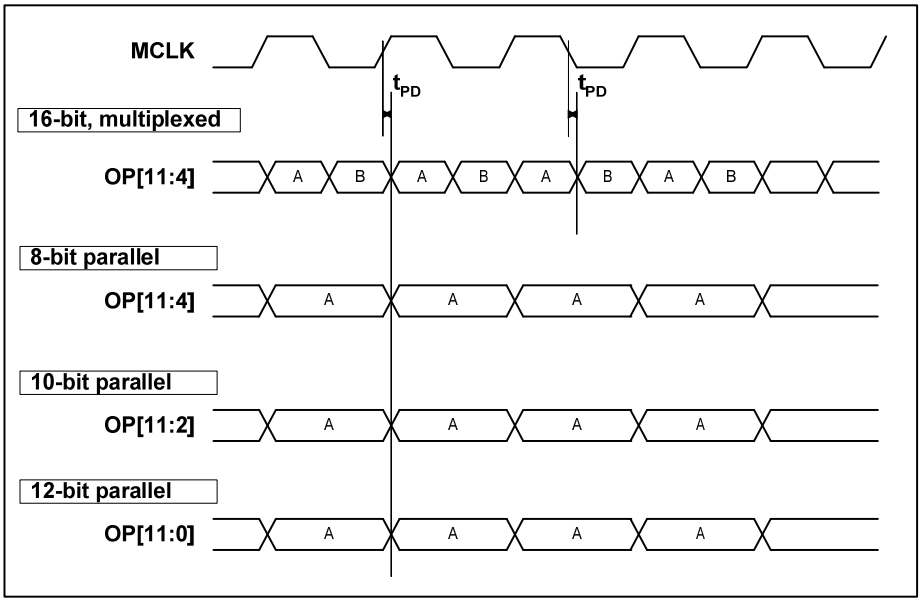


Figure 21 Output Data Formats

OPFORM	OUTPUT FORMAT	OUTPUT PINS	RES[1:0]	RESOLUTION	OUTPUT
0	Multiplexed	OP[11:4]	11	16-bit	A[7:0] = {d15, d14, d13, d12, d11, d10, d9, d8} B[7:0] = {d7, d6, d5, d4, d3, d2, d1,d0}
			10	12-bit	A[7:0] = {d15, d14, d13, d12, d11, d10, d9, d8} B[7:0] = {d7, d6, d5, d4, 0, 0, 0, 0}
			01	10-bit	A[7:0] = {d15, d14, d13, d12, d11, d10, d9, d8} B[7:0] = {d7, d6, 0, 0, 0, 0, 0, 0}
			00	8-bit	Not valid
1	Parallel	OP[11:0]	11	16-bit	Not valid
		OP[11:0]	10	12-bit	A[11:0] ={ d15, d14, d13, d12, d11, d10, d9, d8,d7,d6,d5,d4}
		OP[11:2]	01	10-bit	A[9:0] = {d15, d14, d13, d12, d11, d10, d9, d8,d7,d6}
		OP[11:4]	00	8-bit	A[7:0] = {d15, d14, d13, d12, d11, d10, d9, d8}

Table 3 Details of Output Data Formats (as shown in Figure 21)