Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

WM8233

210MSPS 6-Channel AFE with Sensor Timing Generation and LVDS/CMOS Data Output

DESCRIPTION

The WM8233 is a 16-bit analogue front end/digitiser IC which processes and digitises the analogue output signals from CCD sensors or Contact Image Sensors (CIS) at pixel sample rates of up to 35MSPS per channel.

The device has six analogue signal processing channels each of which contains Reset Level Clamping, Correlated Double Sampling (also Sample and Hold), Programmable Gain, Automatic Gain Control (AGC) and Offset adjust functions.

The output from each of these channels is time multiplexed, in pairs, into three high-speed 16-bit Analogue to Digital Converters. The digital data is available in a variety of output formats via the flexible data port.

The WM8233 has a user selectable LVDS or CMOS output architecture.

An internal 5-bit DAC is supplied for internal reference level generation. This may be used during CDS to reference CIS signals or during clamping to clamp CCD signals. An external reference level may also be supplied. ADC references are generated internally, ensuring optimum performance from the device.

A programmable automatic Black-Level Calibration function is available to adjust the DC offset of the output data.

The WM8233 features a sensor timing clock generator for both CCD and CIS sensors. The clock generator can accept a slow or fast reference clock input and also has a flexible timing adjustment function for output timing clocks to allow use of many different sensors.

FEATURES

- 210MSPS conversion rate
- 16-bit ADC resolution
- Current consumption – 350mA
- 3.3V single supply operation
- Sample and hold /correlated double sampling
- Programmable offset adjust (8-bit resolution)
- Flexible clamp timing
- Pixel clamp / line clamp mode
- Programmable clamp voltage
- Programmable CIS/CCD timing generator
- Internally generated voltage references
- Compliant for Spread Spectrum Clock
- LVDS/CMOS output options
  - LVDS 5pair 490MHz 35-bit data
  - CMOS 90MHz output maximum
- Complete on chip clock generator. MCLK 5MHz to 35MHz
- Internal timing adjustment
- Automatic Gain Control
- Automatic Black Level Calibration
- 56-lead QFN package 8mm x 8mm
- Serial control interface

APPLICATIONS

- Digital copiers
- USB2.0 compatible scanners
- Multi-function peripherals
- High-speed CCD/CIS sensor interface

Copyright © Cirrus Logic, Inc., 2010–2016
(All Rights Reserved)

BLOCK DIAGRAM

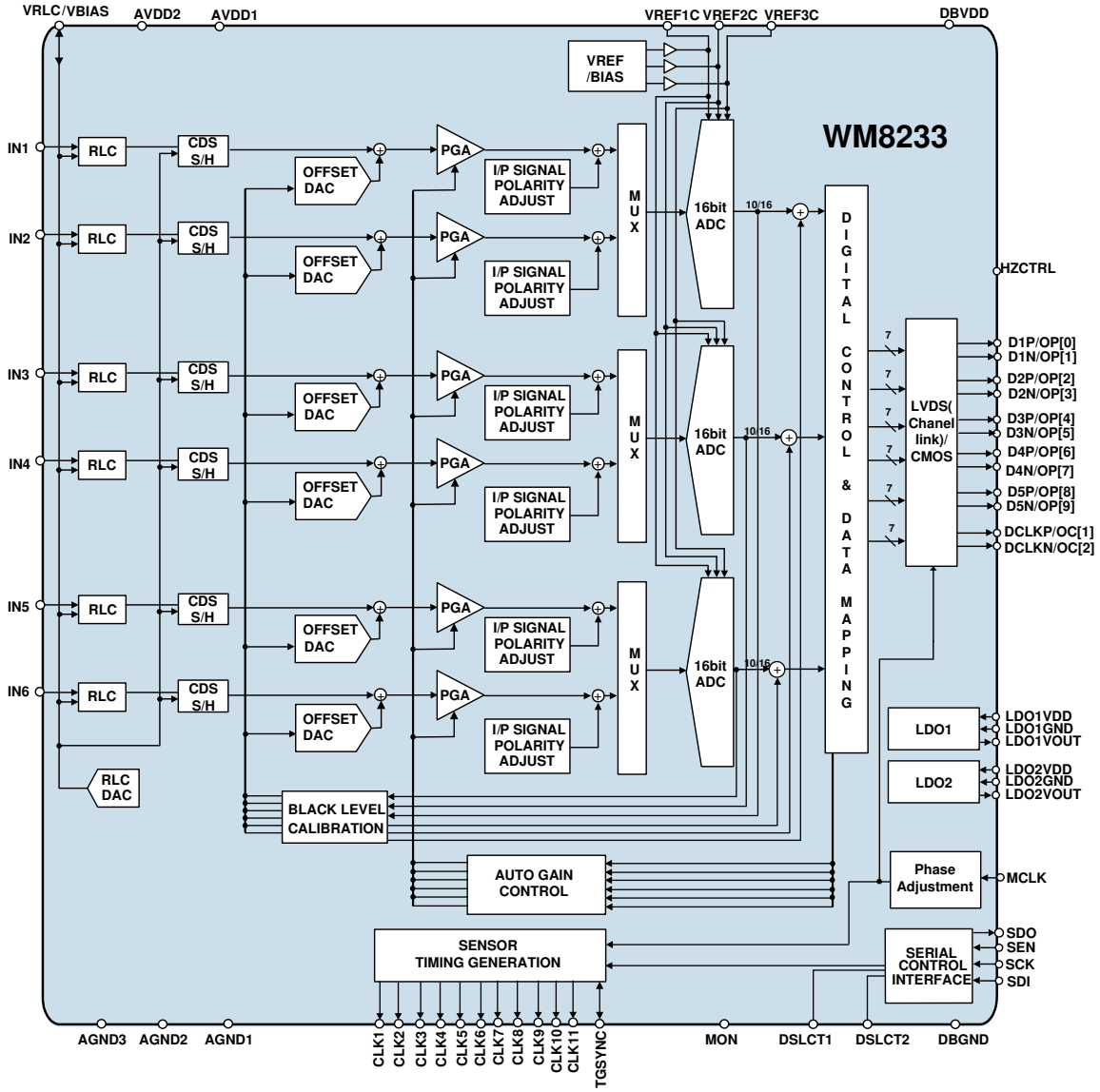
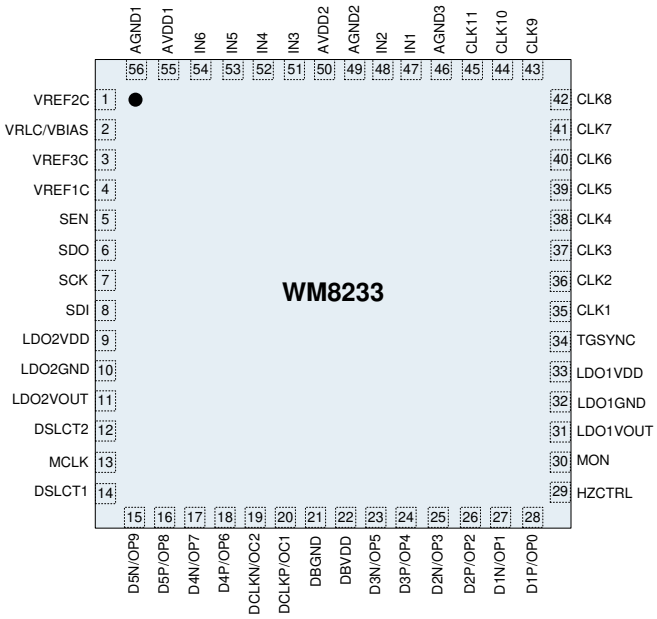


TABLE OF CONTENTS

PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8233GEFL/V	-40 to 85°C	56-lead QFN (8 x 8 x 0.85 mm) (Pb-free)	MSL3	260°C
WM8233GEFL/RV	-40 to 85°C	56-lead QFN (8 x 8 x 0.85 mm) (Pb-free, tape and reel)	MSL3	260°C

Reel quantity = 2,200

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	VREF2C	Analogue output	Mid reference voltage. This pin must be connected to AGND via a decoupling capacitor.
2	VRLC/VBIAS	Analogue I/O	Reference voltage input/output
3	VREF3C	Analogue output	Lower reference voltage. This pin must be connected to AGND via a decoupling capacitor.
4	VREF1C	Analogue output	Upper reference voltage. This pin must be connected to AGND via a decoupling capacitor.
5	SEN	Digital input	Enables the serial interface when high.
6	SDO	Digital output	Serial interface data output
7	SCK	Digital input	Serial interface clock.
8	SDI	Digital input	Serial interface data input
9	LDO2VDD	Supply	Analogue supply
10	LDO2GND	Supply	Analogue ground
11	LDO2VOUT	Supply	LDO output This pin must be connected to AGND via a decoupling capacitor.
12	DSLCT2	Analogue input	Device select 2
13	MCLK	Analogue input	Master clock
14	DSLCT1	Analogue input	Device select 1
15	D5N/OP[9]	LVDS output	LVDS Data output 5 – Negative / CMOS output 9.
16	D5P/OP[8]	LVDS output	LVDS Data output 5 – Positive / CMOS output 8.
17	D4N/OP[7]	LVDS output	LVDS Data output 4 – Negative / CMOS output 7.
18	D4P/OP[6]	LVDS output	LVDS Data output 4 – Positive / CMOS output 6.
19	DCLKN/OC[2]	LVDS output	LVDS Clock Output – Negative/ CMOS flag output.
20	DCLKP/OC[1]	LVDS output	LVDS Clock Output – Positive/ CMOS clock output.
21	DBGND	Supply	Analogue ground
22	DBVDD	Supply	Analogue supply
23	D3N/OP[5]	LVDS output	LVDS Data output 3 – Negative / CMOS output 5.
24	D3P/OP[4]	LVDS output	LVDS Data output 3 – Positive / CMOS output 4.
25	D2N/OP[3]	LVDS output	LVDS Data output 2 – Negative / CMOS output 3.
26	D2P/OP[2]	LVDS output	LVDS Data output 2 – Positive / CMOS output 2.
27	D1N/OP[1]	LVDS output	LVDS Data output 1 – Negative / CMOS output 1.
28	D1P/OP[0]	LVDS output	LVDS Data output 1 – Positive / CMOS output 0.
29	HZCTRL	Digital input	Internal use only. Must be connected to AGND.
30	MON	Analogue output	Clock monitor
31	LDO1VOUT	Supply	LDO output. This pin must be connected to AGND via a decoupling capacitor.
32	LDO1GND	Supply	Analogue ground
33	LDO1VDD	Supply	Analogue supply
34	TGSYNC	Digital I/O	Sensor Timing Sync pulse
35	CLK1	Digital output	Sensor Timing Output 1
36	CLK2	Digital output	Sensor Timing Output 2
37	CLK3	Digital output	Sensor Timing Output 3
38	CLK4	Digital output	Sensor Timing Output 4
39	CLK5	Digital output	Sensor Timing Output 5
40	CLK6	Digital output	Sensor Timing Output 6
41	CLK7	Digital output	Sensor Timing Output 7
42	CLK8	Digital output	Sensor Timing Output 8
43	CLK9	Digital output	Sensor Timing Output 9
44	CLK10	Digital output	Sensor Timing Output 10
45	CLK11	Digital output	Sensor Timing Output 11
46	AGND3	Supply	Analogue ground

PIN	NAME	TYPE	DESCRIPTION
47	IN1	Analogue input	Analogue input 1
48	IN2	Analogue input	Analogue input 2
49	AGND2	Supply	Analogue ground
50	AVDD2	Supply	Analogue supply
51	IN3	Analogue input	Analogue input 3
52	IN4	Analogue input	Analogue input 4
53	IN5	Analogue input	Analogue input 5
54	IN6	Analogue input	Analogue input 6
55	AVDD1	Supply	Analogue supply
56	AGND1	Supply	Analogue ground

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus Logic tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Analogue supply voltage: AVDD1-2, LDO1VDD-2, DBVDD	GND - 0.3V	GND + 5V
Analogue grounds: AGND1-3, LDO1GND-LDO2GND, DBGND	GND - 0.3V	GND + 0.3V
Analogue inputs (IN1-6)	GND - 0.3V	AVDD + 0.3V
Other Analogue pins	GND - 0.3V	AVDD + 0.3V
Digital I/O pins	GND - 0.3V	AVDD + 0.3V
Operating temperature range: T_A	-40°C	+85°C
Storage temperature prior to soldering	30°C max / 85% RH max	
Storage temperature after soldering	-65°C	+150°C

Notes:

1. GND denotes the voltage of any ground pin.
2. AGND, LDOGND and DBGND pins are intended to be operated at the same potential. Differential voltages between these pins will degrade performance.

RECOMMENDED OPERATING CONDITIONS

CONDITION	SYMBOL	MIN	TYP	MAX	UNITS
Operating temperature range	T_A	-40		85	°C
Analogue Supply voltage	AVDD1-2 LDO1VDD-LDO2VDD DBVDD	2.97	3.3	3.63	V

ELECTRICAL CHARACTERISTICS

Test Conditions
AVDD = LDOVDD = DBVDD = 3.3V, AGND = LDOGND = DBGND= 0V, T_A = 25°C, MCLK= 35MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overall System Specification (including 10-bit ADC, PGA, Offset and CDS functions)						
Conversion rate per channel			5		35	MSPS
Full-scale input voltage (see Note 1)		ADCFS=0, Max Gain		0.12		Vp-p
		ADCFS=0, Min Gain		2.0		Vp-p
		ADCFS=1, Max Gain		0.18		Vp-p
		ADCFS=1, Min Gain		3.0		Vp-p
Input signal voltage range	V_{IN}	SF_INP=0	AGND		AVDD	V
		SF_INP=1	AGND		1.2	V
Input capacitance	C_{IN}	Inputs to AGND		10	12	pF
Full-scale transition error		Gain = 0dB; AGAIN[4:0] = 02(hex) DGAIN[11:0] = 6AB(hex)		20		mV
Zero-scale transition error		Gain = 0dB; AGAIN[4:0] = 02(hex) DGAIN[11:0] = 6AB(hex)		20		mV
Differential non-linearity	DNL	10-bit		+/-0.5	+/-1.5	LSB
Integral non-linearity (pk-pk/2)	INL	10-bit		+/-1	+/-4	LSB
Channel to channel gain matching	Min Gain			5		%
	Max Gain			15		%
Output noise		10-bit, Unity Gain (Unused channels grounded)		0.5	2.5	LSB rms
Channel to channel crosstalk		10-bit		+/-0.5		LSB
Channel to channel offset matching		BLC disabled		70	210	mV
Programmable Gain Amplifier						
Total Resolution (Ga + Gd)	G_T			12		bits
Analogue Gain	Ga		0.6 + 0.3 * AGAIN[4:0]			V/V
Max gain, each channel (Ga)	Ga_{MAX}	AGAIN[4:0] = 1F(hex)	8.00	9.9	11.43	V/V
Min gain, each channel (Ga)	Ga_{MIN}	AGAIN[4:0] = 0(hex)	0.44	0.6	0.77	V/V
Digital Gain	Gd		DGAIN[11:0] / 2^{11}			V/V
Max gain, each channel (Gd)	Gd_{MAX}	DGAIN[11:0] = FFF(hex)		2		V/V
Min gain, each channel (Gd)	Gd_{MIN}	DGAIN[11:0] = 400 (hex)		0.5		V/V
Max gain, each channel (Ga + Gd)	G_{TMAX}	AGAIN[4:0] = 1F(hex) DGAIN[11:0] = FFF(hex)		19.8		V/V
Min gain, each channel (Ga + Gd)	G_{TMIN}	AGAIN[4:0] = 0(hex) DGAIN[11:0] = 400 (hex)		0.3		V/V
Analogue to Digital Converter						
Resolution				16		bits
Speed					70	MSPS

Test Conditions

AVDD = LDOVDD = DBVDD = 3.3V, AGND = LDOGND = DBGND= 0V, T_A = 25°C, MCLK= 35MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
References						
Upper reference voltage	V_{REF1C}	ADCFS=0		2.05		V
		ADCFS=1		2.25		V
Lower reference voltage	V_{REF3C}	ADCFS=0		1.25		V
		ADCFS=1		1.05		V
Input return bias voltage	V_{REF2C}		1.14	1.2	1.26	V
Diff. Reference voltage (VREF1C-VREF3C)	$V_{REF1C3C}$	ADCFS=0	0.72	0.8	0.88	V
		ADCFS=1	1.00	1.2	1.35	V
Output resistance VREF1C, VREF3C, VREF2C				1		Ω
VRLC/Reset-Level Clamp (RLC)						
VRLC input voltage range (see Note 2)	VRLC	SF_INP=0	0.11		3.0	V
		SF_INP=1	0.11		1.2	
RLC switching impedance				50		Ω
RLC short-circuit current				2		mA
RLC output resistance				2		Ω
RLC Hi-Z leakage current		VRLC = 0 to AVDD			1	µA
RLCDAC resolution				5		bits
RLCDAC step size	$V_{RLCSTEP}$	VRLC_TOP_SEL=0		0.09		V/step
		VRLC_TOP_SEL=1		0.048		
RLCDAC output voltage at code 0(hex)	V_{RLCBOT}	VRLC_TOP_SEL=0, VRLC_VSEL[4:0]=00000		0.2		V
		VRLC_TOP_SEL=1, VRLC_VSEL[4:0]=00000		0.11		V
RLCDAC output voltage at code 1F(hex)	V_{RLCTOP}	VRLC_TOP_SEL=0, VRLC_VSEL[4:0]=11111		3.0		V
		VRLC_TOP_SEL=1, VRLC_VSEL[4:0]=11111		1.6		V
VRLC DNL				0.5		LSB
VRLC INL				0.5		LSB
Offset DAC, Monotonicity Guaranteed						
Resolution				8		bits
Differential non-linearity	DNL			0.5	1	LSB
Integral non-linearity	INL			0.5	1	LSB
Step size				2.04		mV/step
Output voltage		Code 00(hex)	-400	-250	-100	mV
		Code FF(hex)	+100	+250	+400	mV
DIGITAL SPECIFICATIONS						
Digital Inputs						
High level input voltage	V_{IH}		0.7 * AVDD			V
Low level input voltage	V_{IL}				0.2 * AVDD	V
High level input current	I_{IH}				1	µA
Low level input current	I_{IL}				1	µA
Input capacitance	C_I			5		pF

Test Conditions

AVDD = LDOVDD = DBVDD = 3.3V, AGND = LDOGND = DBGND= 0V, T_A = 25°C, MCLK= 35MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
CMOS Outputs						
High level output voltage	V_{OH}	I_{OH} = 6mA	AVDD – 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 1mA			0.5	V
High impedance output current	I_{OZ}				1	µA
TG Outputs						
High level output voltage	V_{OHTG}	I_{OH} = 1mA	AVDD – 0.5			V
Low level output voltage	V_{OLTG}	I_{OL} = 1mA			0.5	V
High impedance output current	I_{OZTG}	Grounded			1	µA
Digital IO Pins						
Applied high level input voltage	V_{IH}		0.7 * AVDD			V
Applied low level input voltage	V_{IL}				0.2 * AVDD	V
High level output voltage	V_{OH}	I_{OH} = 1mA	AVDD – 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 1mA			0.5	V
Low level input current	I_{IL}				1	µA
High level input current	I_{IH}				1	µA
Input capacitance	C_I			5		pF
Output Impedance	R_O	I_O = 1mA		22		Ω
High impedance output current	I_{OZ}				1	µA
LVDS Outputs						
Differential load impedance	R_L		90	100	110	Ω
Differential steady-state output voltage magnitude	$\|V_{OD}\|$	LVDS_AMP=011, R_L=100Ω		200		mV
Change in the steady-state differential output voltage magnitude between opposite binary states	$\Delta\|V_{OD}\|$	R_L=100Ω			15	mV
Steady-state common-mode output voltage	V_{OC}(SS)	R_L=100Ω		1.25		V
Peak-to-peak common-mode output	V_{OC}(PP)			20	50	mV
Short-circuit output current	I_{OS}		–6		6	mA
High-impedance state output current	I_{OZ}		–10		10	uA
Supply Currents						
Total supply current – active		SF_INP=0, SF_VRLC=0		350		mA
		SF_INP=1, SF_VRLC=1		390		mA
Total supply current – full power down mode				1.2		mA

Notes:

1. **Full-scale input voltage** denotes the differential input signal amplitude (V_{IN}-VRLC in non-CDS mode, V_{IN}-RESET level in CDS mode) that corresponds to the ADC full-scale input level.
2. **If AVDD < 3.0V, the VRLC input voltage must not exceed AVDD.**

INTERNAL POWER ON RESET CIRCUIT

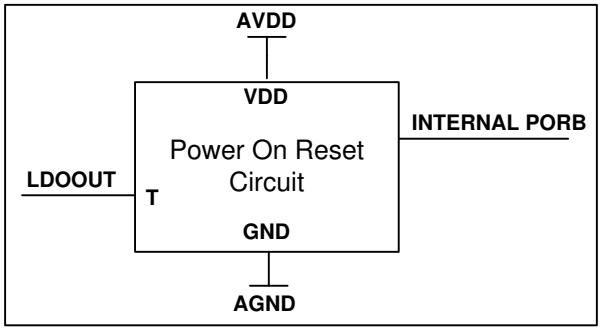


Figure 1 Internal Power On Reset Circuit Schematic

The WM8233 includes an internal Power-On-Reset Circuit, as shown in Figure 1, which is used reset the digital logic into a default state after power up. The POR circuit is powered from AVDD and monitors LDOOUT. It asserts PORB low if AVDD or LDOOUT is below a minimum threshold.

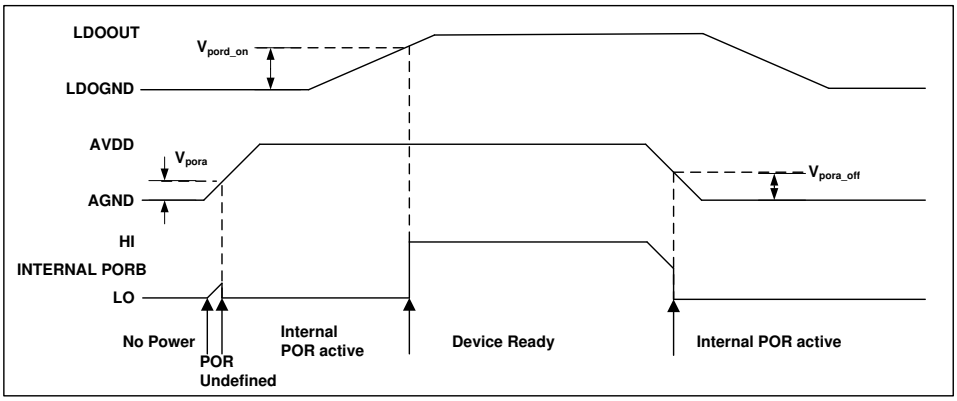


Figure 2 Typical Power up Sequence where AVDD is Powered before LDOOUT

Figure 2 shows a typical power-up sequence where AVDD is powered up first. When AVDD rises above the minimum threshold, Vpora, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When LDOOUT rises to Vpord_on, PORB is released high and all registers are in their default state and writes to the control interface may take place. On power down, where AVDD falls first, PORB is asserted low whenever AVDD drops below the minimum threshold Vpora_off.

SYMBOL	MIN	TYP	MAX	UNIT
Vpora	0.4	0.6	0.8	V
Vpora_off	0.4	0.6	0.8	V
Vpord_on	0.5	0.7	0.9	V

Table 1 Typical POR Operation (typical values, not tested)

SIGNAL TIMING REQUIREMENTS

SERIAL CONTROL INTERFACE

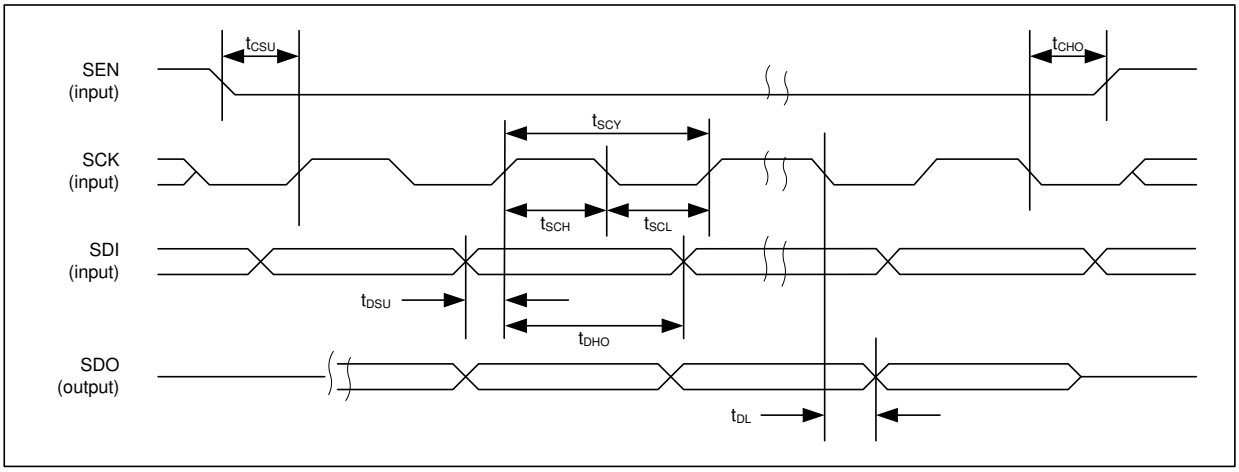


Figure 3 Serial Interface Timing

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SEN falling edge to SCK rising edge	t_{CSU}		20			ns
SCK falling edge to SEN rising edge	t_{CHO}		20			ns
SCK pulse cycle time	t_{SCY}		83.3			ns
SCK pulse width low	t_{SCL}		33			ns
SCK pulse width high	t_{SCH}		33			ns
SDI to SCK set-up time	t_{DSU}		20			ns
SDI to SCK hold time	t_{DHO}		20			ns
SCK falling edge to SDO transition	t_{DL}				33	ns

The internal control registers are programmable via the serial digital control interface. The register contents can be read back via the serial interface on pin SDO.

It is recommended that a software reset is carried out after the power-up sequence, before writing to any other register. This ensures that all registers are set to their default values.

DEVICE IDENTIFICATION

Up to 4 WM8233 devices can share a common set of serial interface pins. Each device on the common interface bus must be given a different device ID. The device ID is set by the input pin DSLCT2 and DSLCT1 as shown in Table 2.

DSLCT2	DSLCT1	DEVICE ID (ID[1:0])
L	L	00
L	H	01
H	L	10
H	H	11

Table 2 Device Identification

REGISTER WRITE

Figure 4 shows the sequence of operations for performing a register write. Three pins, SCK, SDI and SEN are used for the control interface. A 16-bit address (R/W, CS0, CS1, CS2, A11 to A0) is clocked in through SDI, MSB first, followed by an 8-bit data word (b7 to b0), also MSB first. Setting address bit R/W to 0 indicates that the operation is a register write. The device ID bits (CS0 and CS1) indicate which device is being written to on a shared control bus. A register write with CS2 set to 1 writes data to all devices on the common bus. Each bit is latched on the rising edge of SCK. When the data has been shifted into the device, a rising edge on the SEN pin transfers the data to the appropriate internal register.

CS2	CS1 (DSLCT2)	CS0 (DSLCT1)	DESCRIPTION
0	ID[1:0]		Indicated a device to write data
1	X	X	Writes data to all devices

Table 3 Device Identification

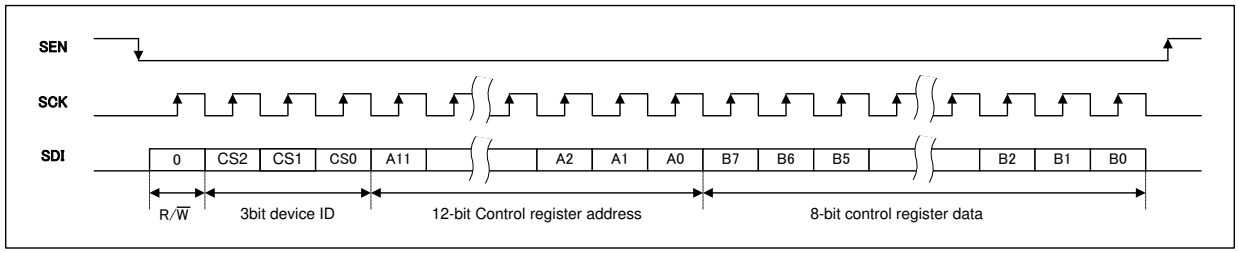


Figure 4 Serial Interface Register Write

REGISTER READ-BACK

Figure 5 shows register read-back in serial mode. Read-back is initiated by writing to the serial bus as described above but with address bit R/W set to 1, followed by an 8-bit dummy data word. Writing address (A11 to A0) will cause the contents (B7 to B0) of corresponding register in the addressed device to be output MSB first on pin SDO (on the following edge of SCK). In this mode, the CS2 register should be set to 0.

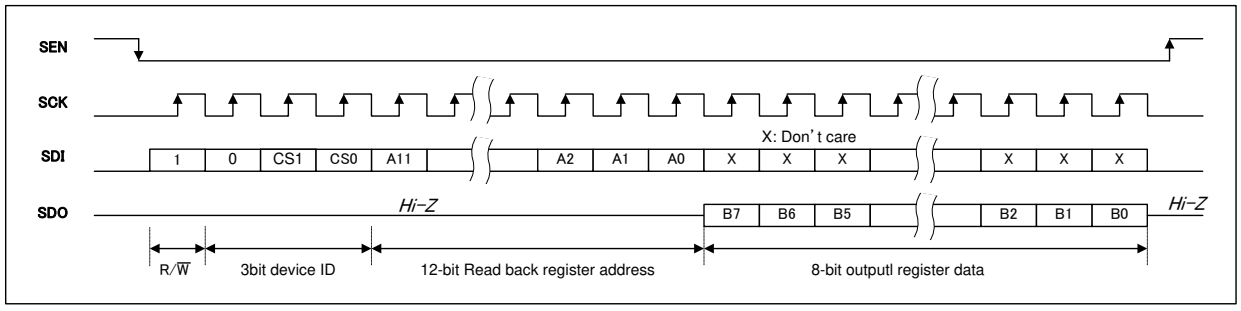


Figure 5 Serial Interface Register Read-back

INPUT VIDEO SAMPLING

NON-CDS (S/H) MODE

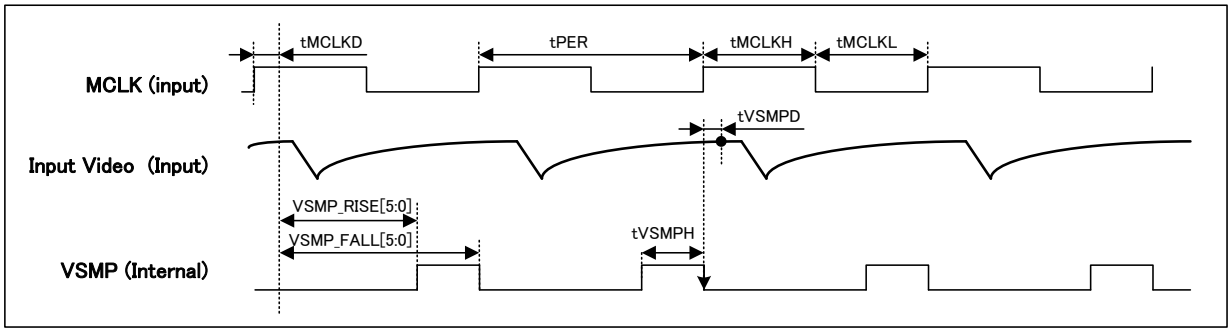


Figure 6 Input Video Timing (Non-CDS (S/H) mode)

CDS MODE

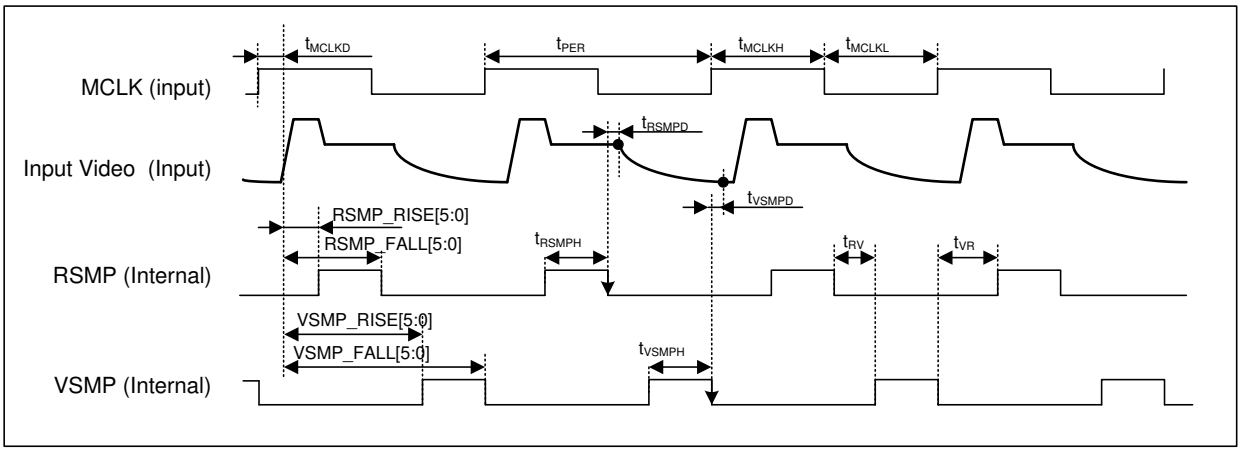


Figure 7 Input Video Timing (CDS mode)

Test Conditions

AVDD = LDOVDD = DBVDD = 3.3V, AGND = LDOGND = DBGND= 0V, T_A = 25°C, MCLK= 35MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MCLK cycle period (see note 2)	t_{PER}		28.6		200	ns
MCLK high period (see note 2)	t_{MCLKH}		0.4 * t_{PER}	0.5 * t_{PER}	0.6 * t_{PER}	ns
MCLK low period (see note 2)	t_{MCLKL}		0.4 * t_{PER}	0.5 * t_{PER}	0.6 * t_{PER}	ns
MCLK rising edge to DLL tap 0	t_{MCLKD}			18		ns
Aperture delay (from RSMP falling edge)	t_{RSMPD}			5		ns
Aperture delay (from VSMP falling edge)	t_{VSMPD}			5		ns
RSMP high period	t_{RSMPH}		5			ns
VSMP high period	t_{VSMPH}		5		13 * t_{PER}/60	ns
RSMP falling edge to VSMP rising edge	t_{RV}		0.5			ns
VSMP falling edge to RSMP rising edge	t_{VR}		0.5			ns
Output data latency (from 1st falling edge of VSMP)	LAT	LVDS 10-bit 5pair mode		10		clock
		Other output modes		9		clock

Notes:

1. 1clock = t_{PER} (MCLK cycle period)
2. MCLK cycle period and MCLK high/low period are measured at 50% of the respective rising/falling edges

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R130 (82h) RSMP rise	5:0	RSMP_RISE[5:0]	01_1100	RSMP rise edge (0 to 59)
R131 (83h) RSMP fall	5:0	RSMP_FALL[5:0]	10_0110	RSMP fall edge (0 to 59)
R132 (84h) VSMP rise	5:0	VSMP_RISE[5:0]	00_1000	VSMP rise edge (0 to 59)
R133 (85h) VSMP fall	5:0	VSMP_FALL[5:0]	10_1000	VSMP fall edge (0 to 59)

OUTPUT DATA TIMING (CMOS OUTPUT)

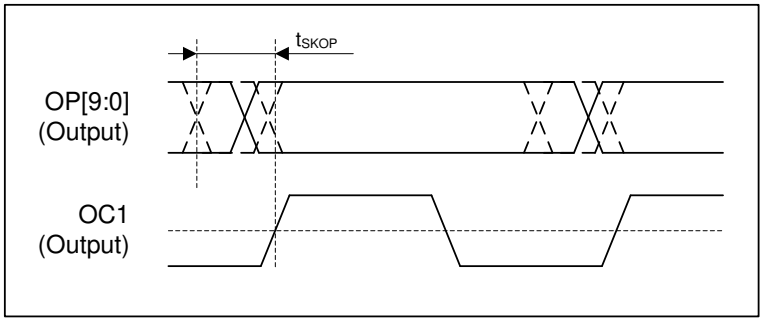


Figure 8 CMOS Output Data Timing

Test Conditions
AVDD = LDOVDD = DBVDD = 3.3V, AGND = LDOGND = DBGND= 0V, T_A = 25°C, MCLK= 35MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Data output skew	t_{SKOP}			+/-500		ps

OUTPUT DATA TIMING (LVDS OUTPUT)

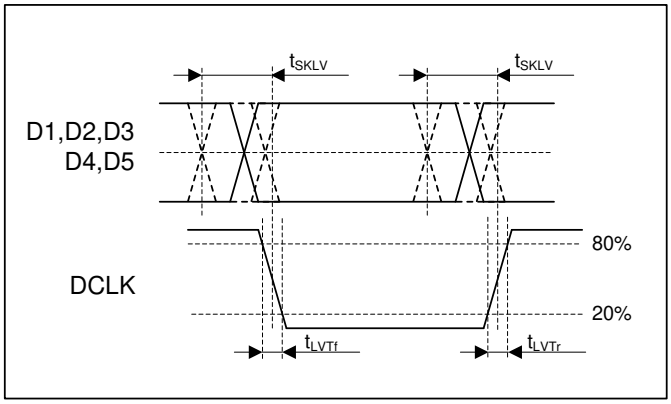


Figure 9 LVDS Output Data Timing

Test Conditions
AVDD = LDOVDD = DBVDD = 3.3V, AGND = LDOGND = DBGND= 0V, T_A = 25°C, MCLK= 15MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
LVDS output skew	t_{SKLV}			+/-250		ps
LVDS output signal rise time	t_{LVTr}				1	ns
LVDS output signal fall time	t_{LVTf}				1	ns

DEVICE DESCRIPTION

INTRODUCTION

A block diagram of the device showing the signal path is presented on the front page of this datasheet.

The WM8233 samples up to six inputs (IN1, IN2IN2, IN3, IN4, IN5 and IN6) simultaneously. The device then processes the sampled video signal with respect to the video reset level or an internally/externally generated reference level using between one and six processing channels.

Each processing channel consists of an Input Sampling block with optional Reset Level Clamping (RLC) and Correlated Double Sampling (CDS), an 8-bit programmable offset DAC and a 12-bit Programmable Gain Amplifier (PGA).

The processing channel outputs are switched, in pairs, alternately by a 2:1 multiplexer to the three ADC inputs.

The ADC then converts each resulting analogue signal to a digital word. The digital output from the ADC is presented in a variety of possible output formats in LVDS and CMOS format.

On-chip control registers determine the configuration of the device, including the offsets and gains applied to each channel. These registers are programmable via a serial interface.

The device has an automatic Black-Level Calibration function which allows the D.C. offset determined during the optically-black pixels at the beginning of the linear sensor to be removed during the image-pixels.

The WM8233 also has an Automatic Gain Control function which automatically adjusts the gain to an appropriate level for a detected input level.

The device incorporates a sensor timing generation function which allows CCD and CMOS sensor timing to be controlled directly from the device using internal clock generation and register settings.

RESET LEVEL CLAMPING (RLC)

To ensure that the signal applied to the WM8233 lies within the supply voltage range (0V to AVDD), the output signal from a CCD is usually level shifted by coupling through a capacitor, $C_{IN.}$ The RLC circuit clamps the WM8233 side of this capacitor to a suitable voltage through a CMOS switch during the CCD reset period (pixel clamping) or during the black pixels (line clamping). In order for clamping to produce correct results the input voltage during the clamping must be a constant value.

Note that if the A.C. coupling capacitor (C_{IN}) is used in non-CDS mode (CDS=0), then to minimise code drift, line clamping should be used and internal input voltage buffers enabled using the SF_INP and SF_VRLC register bit. Alternatively, if the input signal contains a stable reference/reset level, then pixel clamping should be used, and the voltage buffers need not be enabled.

The WM8233 allows the user to control the RLC switch in a variety of ways as illustrated in Figure 10. This figure shows a single channel; however, all 6 channels are identical, each with its own clamp switch controlled by the common CLMP signal.

The method of control chosen depends upon the characteristics of the input video. The VRLCEN register bit must be set to 1 to enable clamping; otherwise, the RLC switch cannot be closed (by default VRLCEN=1).

Note that unused inputs should be left floating, or grounded through a decoupling capacitor, if reset level clamping is used.

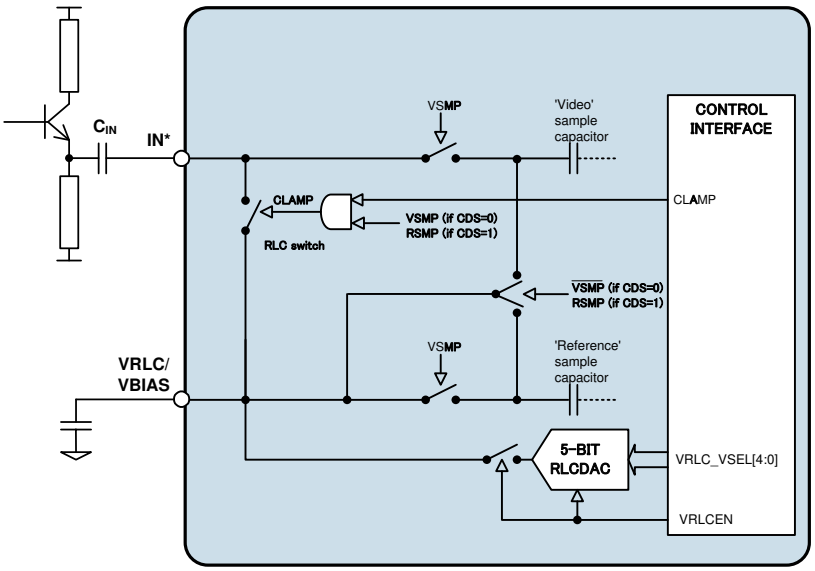


Figure 10 RLC Clamp Control Options

In CDS operation, when an input waveform has a stable reference level on every pixel, it may be desirable to clamp every pixel during this period. Setting CLAMP=high means that the RLC switch is closed whenever the RSMP is high, as shown in Figure 11.

In non-CDS operation, setting CLAMP=high means that the RLC switch is closed whenever the VSMP is high, as shown in Figure 12.

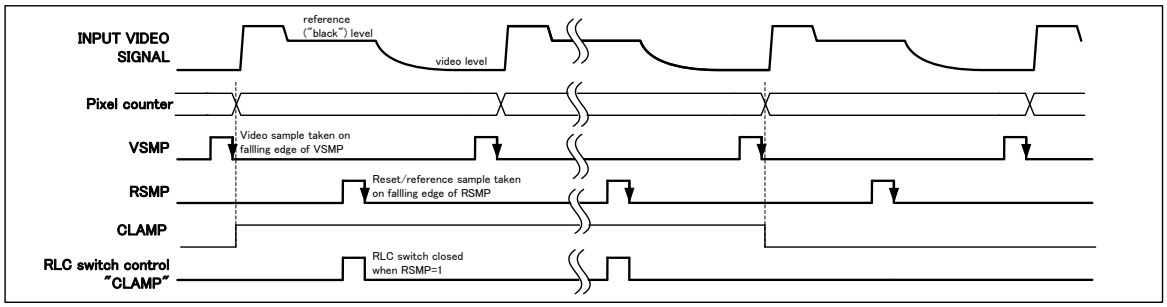


Figure 11 Reset Level Clamp Operation, CDS operation shown

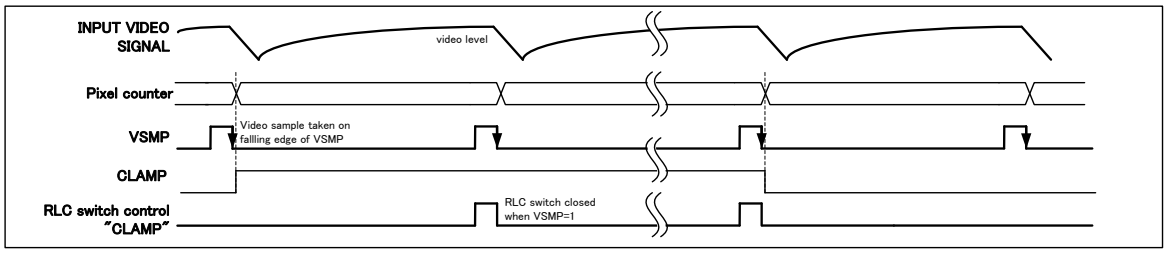


Figure 12 Line Clamp Operation, non-CDS operation shown

CDS/NON-CDS PROCESSING

For CCD type input signals, containing a fixed reference/reset level, the signal may be processed using Correlated Double Sampling (CDS), which will remove pixel-by-pixel common mode noise. With CDS processing, the input waveform is sampled at two different points in time for each pixel, once during the reference/reset level and once during the video level. To sample using CDS, register bit CDS must be set to 1 (default = 0). This causes the signal reference to come from the video reference level as shown in Figure 13.

For input signals that do not contain a reference/reset level (e.g. CIS sensor signals), non-CDS processing is used (CDS=0). In this case, the video level is processed with respect to the voltage on pin VRLC/VBIAS. The VRLC/VBIAS voltage is sampled at the same time as input samples the video level in this mode. Note that if the A.C. coupling capacitor (C_{IN}) is used in non-CDS mode (CDS=0), then to minimise code drift, line clamping should be used and internal input voltage buffers enabled using the CLPMD register bit. Alternatively, if the input signal contains a stable reference/reset level, then pixel clamping should be used, and the voltage buffers need not be enabled.

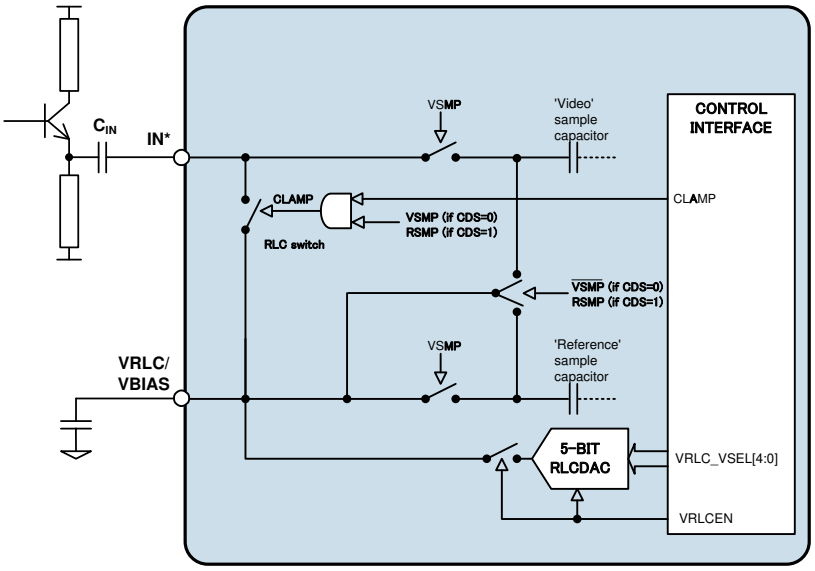


Figure 13 CDS/non-CDS Input Configuration

OFFSET ADJUST AND PROGRAMMABLE GAIN

The output from the CDS block is a differential signal, which is added to the output of an 8-bit Offset DAC to compensate for offsets and then amplified by a 12-bit PGA. The gain and offset for each channel are independently programmable by writing to control bits DACINP[7:0] for the Offset DAC, and AGAIN[4:0] and DGAIN[11:0] for the PGA.

The gain characteristic of the WM8233 PGA is shown in Figure 14.

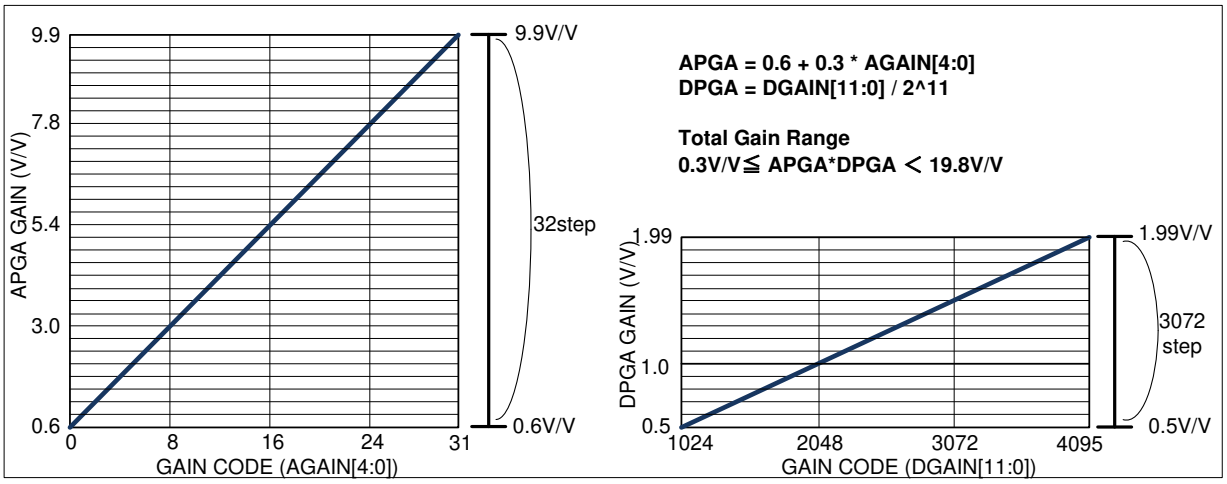


Figure 14 PGA Gain Characteristic

ADC INPUT BLACK LEVEL ADJUST

The output from the PGA can be offset to match the full-scale range of the differential ADC (1.5*[VREF1C-VREF3C]).

For negative-going input video signals, a black level (zero differential) output from the PGA should be offset to the top of the ADC range by setting register bits PGAFS=0. For positive going input signals the black level should be offset to the bottom of the ADC range by setting PGAFS=1.

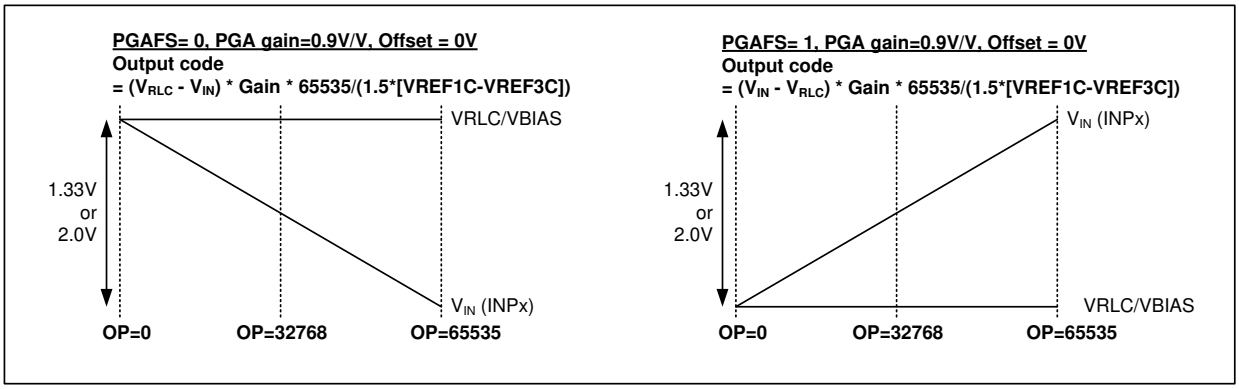


Figure 15 ADC Input Black Level Adjust Settings

OVERALL SIGNAL FLOW SUMMARY

Figure 16 represents the processing of the video signal through the WM8233.

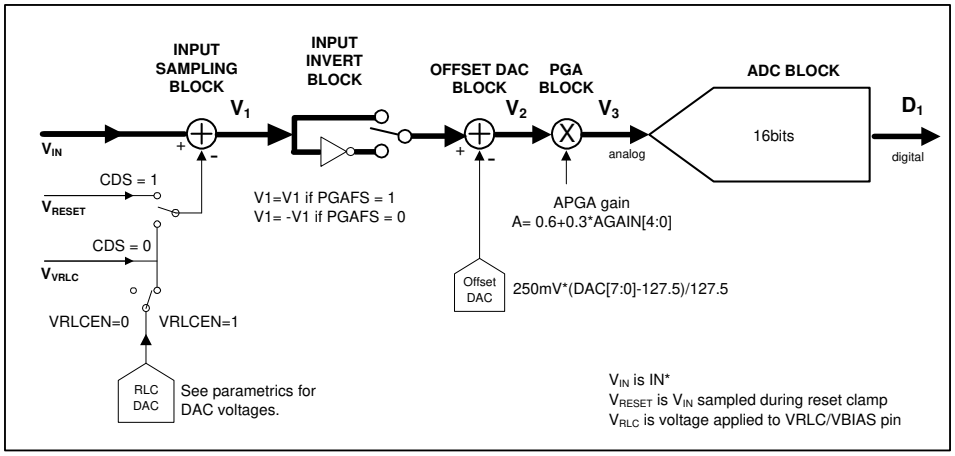


Figure 16 Overall Signal Flow

The **INPUT SAMPLING BLOCK** produces an effective input voltage $\mathbf{V_1}$. For CDS, this is the difference between the input video level V_{IN} and the input reset level V_{RESET}. For non-CDS this is the difference between the input video level V_{IN} and the voltage on the VRLC/VBIAS pin, V_{VRLC}, optionally set via the RLC DAC.

The **OFFSET DAC BLOCK** then adds the amount of fine offset adjustment required to move the black level of the input signal towards 0V, producing $\mathbf{V_2}$.

The **PGA BLOCK** then amplifies the white level of the input signal to maximise the ADC range, outputting voltage $\mathbf{V_3}$.

The **ADC BLOCK** then converts the analogue signal, $\mathbf{V_3}$, to a 16-bit unsigned digital output, $\mathbf{D_1}$.

ADC PGA BIAS CURRENT CONTROL

The WM8233 can be changed the bias current for PGA and ADC comparator as the following step. It would be effective for high frequency operation.

1. R1C0h=1
2. R1CBh=11h

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R448 (1C0h) User access control2	0	User_KEY2	0	0 = User access2 disabled 1 = User access2 enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R459 (1CBh) Comp control	1:0	PT_COMP	01	01 = Standard operation 11 = High performance operation Other = Inhibit.

Notes:

1. To change the Comp control, the USER_KEY2 bit must be set to '1'.
2. If it's not required to change this register, must be set as default.

PLL DLL SETUP

WM8233 is supporting wide range of input frequency. PLL_EXDIV_SEL[2:0], LVDLGAIN[1:0] and DLGAIN[1:0] must be configured by MCLK clock rate and data output format.

Note that after PLL and DLL configuration, the device must be reset as the following step.

- R03[1:0]=11 (PDMD=1, PD=1)
- Delay 1ms
- R03[1:0]=00 (Normal operation)

Also, several LVDS operation mode is required to change internal LDO configuration to perform LVDS clocking properly. The following register need to set to change the LDO configuration.

- R1B0h=1
- R1B4h=12h

	Max sample rate	MCLK Clock rate [MHz]	23.4 ~ 35.0	21.1 ~ 23.3	20.0 ~ 21.0	17.5 ~ 19.99	15.0 ~ 17.49	12.5 ~ 14.99	12.0 ~ 12.49	8.33 ~ 11.99	7.5 ~ 8.32	6.0 ~ 7.49	5.0 ~ 5.99
CMOS 10 bit	15MHz	PLL_EXDIV_SEL[2:0]					000	000	000	001	001	001	001
		LVDLGAIN[1:0]											
		DLGAIN[1:0]					01	10	10	10	10	10	10
		LDO setting											
LVDS 5pair 10bit	35MHz	PLL_EXDIV_SEL[2:0]	001	001	001	001	001	001	010	010	010	011	011
		LVDLGAIN[1:0]	00	00	00	01	01	01	01	01	01	10	10
		DLGAIN[1:0]	01	01	01	01	01	10	10	10	10	10	10
		LDO setting	12h	12h	12h								
LVDS 5pair 16bit	23.3MHz	PLL_EXDIV_SEL[2:0]		001	001	001	001	001	001	001	010	010	010
		LVDLGAIN[1:0]		00	00	00	00	01	01	01	01	01	01
		DLGAIN[1:0]		01	01	01	01	10	10	10	10	10	10
		LDO setting		12h	12h	12h	12h						
LVDS 3pair 10bit LVDS 4pair 12bit	21.0MHz	PLL_EXDIV_SEL[2:0]			001	001	001	001	001	001	010	010	010
		LVDLGAIN[1:0]			00	00	00	01	01	01	01	01	01
		DLGAIN[1:0]			01	01	01	10	10	10	10	10	10
		LDO setting			12h	12h	12h						
LVDS 3pair 16bit	10.5MHz	PLL_EXDIV_SEL[2:0]								001	001	001	001
		LVDLGAIN[1:0]								00	00	01	01
		DLGAIN[1:0]								10	10	10	10
		LDO setting								12h	12h		

Table 4 PLL and DLL Setting

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R28 (1Ch) PLL divider control 1	6:4	PLL_EXDIV_ SEL[2:0]	001	Select EX DIV ratio. Need to set according to input frequency. See Table 4. 000 = 1 001 = 2 010 = 4 011 = 8 100 = 16 101 to 111 = reserved.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R128 (80h) DLL config 1	5:4	DLGAIN[1:0]	01	gain control of DLL delay line Need to set according to input frequency. See Table 4.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R129 (81h) DLL config 2	5:4	LVDLGAIN[1:0]	00	gain control of LVDS DLL delay line Need to set according to input frequency. See Table 4.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R432 (1B0h) User access control	0	USER_KEY	0	0 = User access disabled 1 = User access enabled

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R436 (1B4h) LDO2 control	4:0	LDO2 VSEL	1_0000	1_0000 = 1.8V 1_0010 = 2.0V

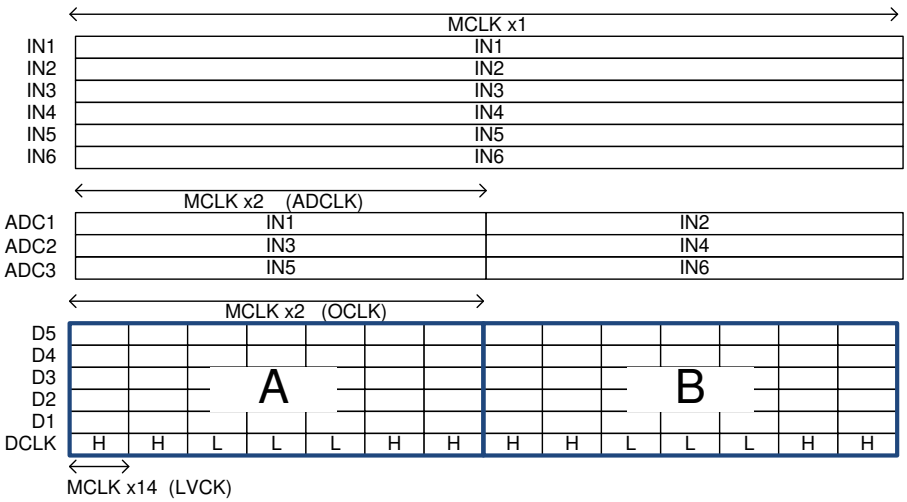
OUTPUT DATA FORMAT

The output from the WM8233 can be presented in several different formats under control of the CMOSMODE and the LVDSMODE register. Depending on the output modes, the maximum MCLK rate is different as shown in Table 5.

MODES	DESCRIPTION	OUTPUT DATA RATE	MAXIMUM MCLK RATE
1	LVDS 10-bit 5pair	MCLK x14	35MSPS
2	LVDS 16-bit 5pair	MCLK x21	23.3MSPS
3	LVDS 10-bit 3pair	MCLK 21	21.0MSPS
4	LVDS 16-bit 3pair	MCLK x42	10.5MSPS
5	LVDS 12-bit 4pair	MCLK 21	21.0MSPS
6	CMOS 10-bit	MCLK x6	15MSPS

Table 5 Output Format and Data Rate

LVDS 10-BIT 5PAIR MODE



A							
D5	S0	S1	S2	IN1[0]	IN1[1]	IN1[2]	IN1[3]
D4	IN1[4]	IN1[5]	IN1[6]	IN1[7]	IN1[8]	IN1[9]	S3
D3	S4	IN2[0]	IN2[1]	IN2[2]	IN2[3]	IN2[4]	IN2[5]
D2	IN2[6]	IN2[7]	IN2[8]	IN2[9]	IN3[0]	IN3[1]	IN3[2]
D1	IN3[3]	IN3[4]	IN3[5]	IN3[6]	IN3[7]	IN3[8]	IN3[9]
DCLK	H	H	L	L	L	H	H

B							
D5	S0	S1	S2	IN4[0]	IN4[1]	IN4[2]	IN4[3]
D4	IN4[4]	IN4[5]	IN4[6]	IN4[7]	IN4[8]	IN4[9]	S3
D3	S4	IN5[0]	IN5[1]	IN5[2]	IN5[3]	IN5[4]	IN5[5]
D2	IN5[6]	IN5[7]	IN5[8]	IN5[9]	IN6[0]	IN6[1]	IN6[2]
D1	IN6[3]	IN6[4]	IN6[5]	IN6[6]	IN6[7]	IN6[8]	IN6[9]
DCLK	H	H	L	L	L	H	H

Table 6 10-bit 5pair LVDS Output Format