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WM8255

Single Channel 16-bit CIS/CCD AFE with RGB LED Current Drive

DESCRIPTION

The WM8255 is a 16-bit analogue front end/digitiser IC which processes and digitises the analogue output signals from CCD sensors or Contact Image Sensors (CIS) at pixel sample rates of up to 12 MSPS.

The device includes a complete signal processing channel containing Reset Level Clamping, Correlated Double Sampling, Programmable Gain and Offset adjust functions. Internal multiplexers allow fast switching of offset and gain for line-by-line colour processing. The output from this channel is time multiplexed into a high-speed 16-bit Analogue to Digital Converter. The digital output data is available in a 2 bit or 4-bit wide multiplexed format.

An internal 4-bit DAC is supplied for internal reference level generation. This may be used during CDS to reference CIS signals or during Reset Level Clamping to clamp CCD signals. An external reference level may also be supplied. ADC references are generated internally, ensuring optimum performance from the device.

The device includes an RGB LED current drive using current and PWM functionality to control the operation of sensor LEDs.

The device typically uses an analogue supply voltage of 5.75V and a digital interface supply of 3.3V.

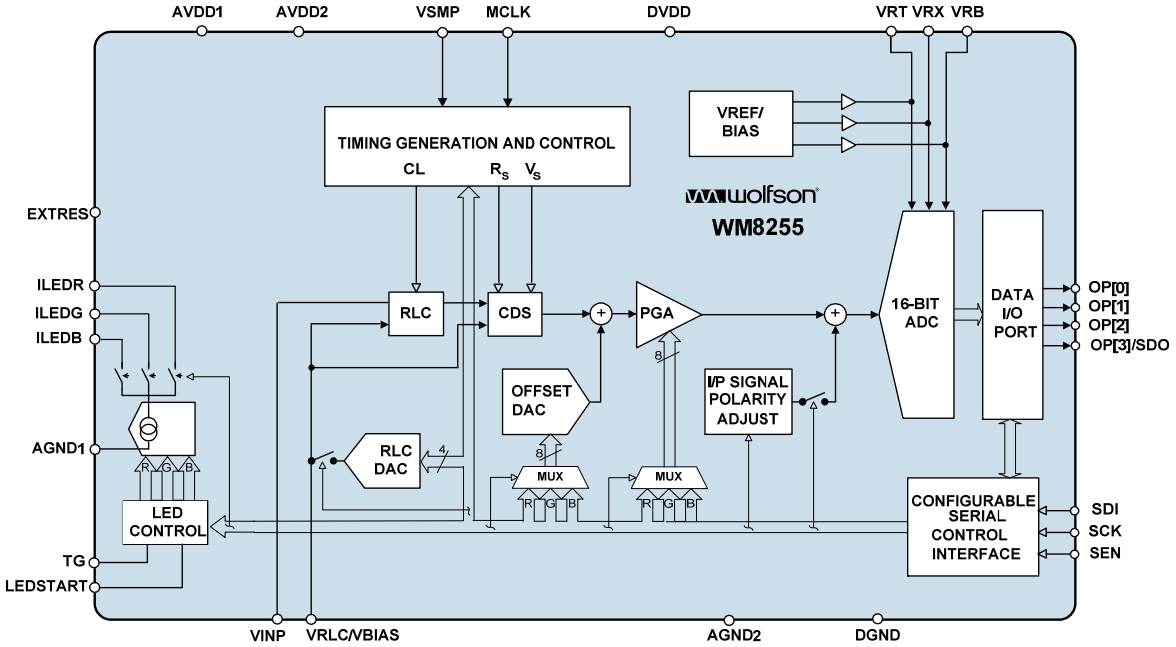
FEATURES

- 16-bit ADC
- 12 MSPS conversion rate
- Low power – 250 mW typical
- 5.75V and 3.3V supply operation
- Single channel operation
- Correlated double sampling
- Programmable gain (8-bit resolution)
- Programmable offset adjust (8-bit resolution)
- Programmable clamp voltage
- RGB LED current drive using current and PWM
- 2-bit or 4-bit wide multiplexed data output format
- Internally generated voltage references
- 28-lead QFN package
- 3 wire serial control interface

APPLICATIONS

- Flatbed and sheetfeed scanners
- USB compatible scanners
- Multi-function peripherals

BLOCK DIAGRAM



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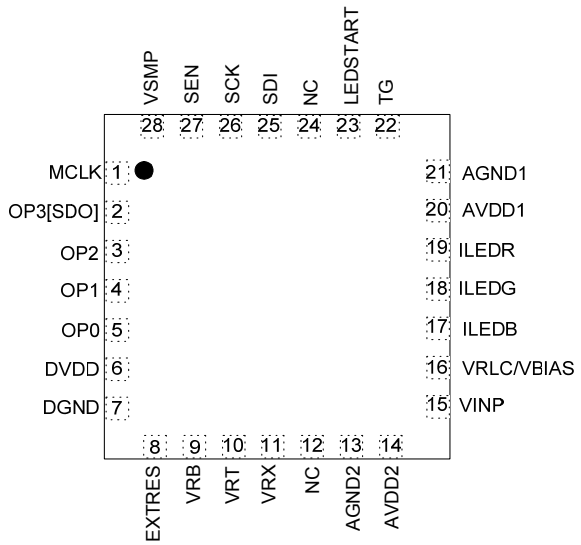
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8255BGEFL/V	0 to 85°C	4x4x0.85mm 28-lead QFN (Pb-free)	MSL3	260°C
WM8255BGEFL/RV	0 to 85°C	4x4x0.85mm 28-lead QFN (Pb-free, tape and reel)	MSL3	260°C

Note:
Reel quantity = 3,500

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION			
1	MCLK	Digital input	Master clock. This clock is applied at N times the input pixel rate (N = 2, 3, 4, 6, 8 or any multiple of 2 thereafter depending on input sample mode).			
			Digital multiplexed output data bus. ADC output data (d15:d0) is available in a 4-bit multiplexed format as shown below. A 2-bit multiplexed output is also available as described in the OUTPUT FORMATS section of this datasheet on page 18.			
			A	**B**	**C**	**D**
2	OP[3]/SDO	Digital output	d15	d11	d7	d3
3	OP[2]	Digital output	d14	d10	d6	d2
4	OP[1]	Digital output	d13	d9	d5	d1
5	OP[0]	Digital output	d12	d8	d4	d0
			Alternatively, pin OP[3]/SDO may be used to output register read-back data when address bit 4=1 and SEN has been pulsed high. See Serial Interface description in Device Description section for further details.			
6	DVDD	Supply	Digital supply (3.3V)			
7	DGND	Supply	Digital ground (0V).			
8	EXTRES	Analogue input	External resistor connection for LED absolute current control. Must be connected to ground via a suitable resistor.			
9	VRB	Analogue output	Lower reference voltage. This pin must be connected to AGND via a decoupling capacitor.			
10	VRT	Analogue output	Upper reference voltage. This pin must be connected to AGND via a decoupling capacitor.			
11	VRX	Analogue output	Input return bias voltage This pin must be connected to AGND via a decoupling capacitor.			
12	NC	No Connect	Not Connected.			
13	AGND2	Supply	Analogue ground pin (0V)			
14	AVDD2	Supply	Analogue supply (3.3V) Not required to be driven if AVDD1 is being used. A decoupling capacitor must be connected to AGND.			
15	VINP	Analogue input	Video input.			
16	VRLC/VBIAS	Analogue I/O	Selectable analogue output voltage for RLC or single-ended bias reference. This pin would typically be connected to AGND via a decoupling capacitor. VRLC can be externally driven if programmed Hi-Z.			
17	ILEDB	Analogue input	Blue LED pin			
18	ILEDG	Analogue input	Green LED pin			
19	ILEDR	Analogue input	Red LED pin			
20	AVDD1	Supply	Analogue Supply (5.75V)			
21	AGND1	Supply	Analogue ground (0V).			
22	TG	Digital input	Line synchronisation pulse			
23	LEDSTART	Digital input	LED start pulse			
24	NC	No Connect	Not Connected.			
25	SDI	Digital input	Serial data input.			
26	SCK	Digital input	Serial clock			
27	SEN	Digital input	Enables the serial interface when high.			
28	VSMP	Digital input	Video sample synchronisation pulse.			

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

The WM8255 has been classified as MSL1, which has an unlimited floor life at <30°C / 85% Relative Humidity and therefore will not be supplied in moisture barrier bags.

CONDITION	MIN	MAX
Analogue supply voltage: AVDD1	GND - 0.3V	GND + 7V
Analogue supply voltage: AVDD2	GND - 0.3V	GND + 4.2V
Digital core supply and I/O voltage: DVDD	GND - 0.3V	GND + 4.2V
Digital ground: DGND	GND - 0.3V	GND + 0.3V
Analogue grounds AGND	GND - 0.3V	GND + 0.3V
Digital inputs, digital outputs and digital I/O pins	GND - 0.3V	DVDD + 0.3V
Analogue input VINP	GND - 0.3V	AVDD + 0.3V
Other pins	GND - 0.3V	AVDD + 0.3V
Operating temperature range: T_A	0°C	+85°C

Notes:

1. GND denotes the voltage of any ground pin.
2. AGND and DGND pins are intended to be operated at the same potential. Differential voltages between these pins will degrade performance.

RECOMMENDED OPERATING CONDITIONS

CONDITION	SYMBOL	MIN	TYP	MAX	UNITS
Operating temperature range	T_A	0		85	°C
Analogue supply voltage	AVDD1	4.75	5.75	6.0	V
Analogue supply voltage [1]	AVDD2	2.97	3.3	3.63	V
Digital Core and I/O supply voltage	DVDD	2.97	3.3	3.63	V

Notes

1. AVDD2 supply not required if using AVDD1. AVDD2 would require connection to ground via a capacitor in that situation.
2. If AVDD2 is being used, both AVDD2 and DVDD should be operated at the same potential.

THERMAL PERFORMANCE

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Performance						
Thermal resistance – junction to case (5x5x0.9mm package)	$R_{\theta JC}$	$T_{ambient}$ = 25°C		10.27		°C/W
Thermal resistance – junction to ambient (5x5x0.9mm package)	$R_{\theta JA}$			29.45		°C/W
Thermal resistance – junction to ambient (4x4x0.85mm package)	$R_{\theta JA}$			24.05		°C/W

Notes:

1. Figures given are for package mounted on 4-layer FR4 according to JESD51-5 and JESD51-7.

ELECTRICAL CHARACTERISTICS

Test Conditions
AVDD1 = 5.75V, DVDD = 3.3V, AGND = DGND = AVDD2 = 0V, T_A = 25°C, MCLK = 24MHz, mode 1 unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overall System Specification (including 16-bit ADC, PGA, Offset and CDS functions)						
Full-scale input voltage range (see Note 1)		Max Gain Min Gain		0.24 2.56		Vp-p Vp-p
Input signal limits (see Note 2)	V_{IN}		0		AVDD1	V
Full-scale transition error		Gain = 0dB; PGA[7:0] = 07(hex)	-50	10	+50	mV
Zero-scale transition error		Gain = 0dB; PGA[7:0] = 07(hex)	-50	10	+50	mV
Differential non-linearity	DNL			1.5		LSB
Integral non-linearity	INL			25		LSB
Input referred noise				9		LSB rms
References						
Upper reference voltage	VRT			2.05		V
Lower reference voltage	VRB			1.05		V
Diff. reference voltage (VRT-VRB)	V_{RTB}			1.0		V
Output resistance VRT, VRB, VRX				1		Ω
VRLC/Reset-Level Clamp (RLC)						
RLC switching impedance			10	50	100	Ω
VRLC short-circuit current				8		mA
VRLC output resistance				2		Ω
VRLC Hi-Z leakage current		VRLC = 0 to AVDD1			1	μA
RLCDAC resolution				4		bits
RLCDAC step size	$V_{RLCSTEP}$			0.24		V/step
RLCDAC output voltage at code 0(hex)	V_{RLCBOT}			0.3		V
RLCDAC output voltage at code F(hex)	V_{RLCTOP}			3.9		V
Offset DAC, Monotonicity Guaranteed						
Resolution				8		bits
Differential non-linearity	DNL			0.6		LSB
Integral non-linearity	INL			2		LSB
Step size				1.96		mV/step
Output voltage		Code 00(hex) Code FF(hex)	-220 +220	-250 +250	-280 +280	mV mV

Notes:

1. **Full-scale input voltage** denotes the peak input signal amplitude that can be gained to match the ADC input range.
2. **Input signal limits** are the limits within which the full-scale input voltage signal must lie.

Test Conditions

AVDD1 = 5.75V, DVDD = 3.3V, AGND = DGND = AVDD2 = 0V, T_A = 25°C, MCLK = 24MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Programmable Gain Amplifier						
Resolution				8		bits
Gain equation				$0.78 + \frac{PGA[7:0] \times 7.57}{255}$		V/V
Max gain	G_{MAX}		8	8.35	8.7	V/V
Min gain	G_{MIN}		0.72	0.78	0.82	V/V
Internal channel offset	V_{OFF}			10		mV
Analogue to Digital Converter						
Resolution				16		bits
Maximum Speed					12	MSPS
Full-scale input range (2*(VRT-VRB))	V_{FS}			2.0		V
DIGITAL SPECIFICATIONS						
Digital Inputs						
High level input voltage	V_{IH}		0.7 * DVDD			V
Low level input voltage	V_{IL}				0.2 * DVDD	V
High level input current	I_{IH}				1	µA
Low level input current	I_{IL}				1	µA
Input capacitance	C_I			5		pF
Digital Outputs						
High level output voltage	V_{OH}	I_{OH} = 1mA	DVDD - 0.5			V
Low level output voltage	V_{OL}	I_{OL} = 1mA			0.5	V
Supply Currents (LED Current DAC switched off)						
Total supply current – active				42.5		mA
Total analogue AVDD, supply current – active	I_{AVDD}			39		mA
Total digital core, DVDD, supply current – active	I_{DVDD1}			3.5		mA
Supply current – full power down mode				500		µA

Notes:

1. Digital I/O supply current depends on the capacitive load attached to the pin. The Digital I/O supply current is measured with approximately 50pF attached to the pin.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
EXTERNAL LED CURRENT DRIVE						
Coarse Absolute LED Current Drive Range Adjust						
EXTRES = 13K7 ohm +/- 1% over process and temperature.						
Coarse LED Current Full Scale Range with External Reference including absolute and temperature tolerances	ILEDCRE0	LEDIRNG = 00	25		32	mA
	ILEDCRE1	LEDIRNG = 01	30		42.25	mA
	ILEDCRE2	LEDIRNG = 10	40		56.5	mA
	ILEDCRE3	LEDIRNG = 11	50		68	mA
Coarse LED Current Maximum Limit Range	ILEDMAX	LEDIMAX = 0	28		45	mA
	ILEDMAX	LEDIMAX = 1	35		53	mA
FINE LED ABSOLUTE CURRENT DRIVE						
Resolution	ILEDFRes			8		bits
Range	ILEDFRan		ILEDCRXX			
Zero Current					0	mA
Differential non-linearity	ILEDFDNL	No missing codes	-1		1.15	LSB
Integral non-linearity	ILEFINL				1	LSB
Compliance Voltage ILEDR	ILEDRVC	ILED=50mA	0.75+ AGND		AVDD1 - 0.5V	V
Compliance Voltage ILEDG and ILEDB	ILEDGBVC	ILED=50mA	0.25+ AGND		AVDD1 - 0.5V	V

INPUT VIDEO SAMPLING

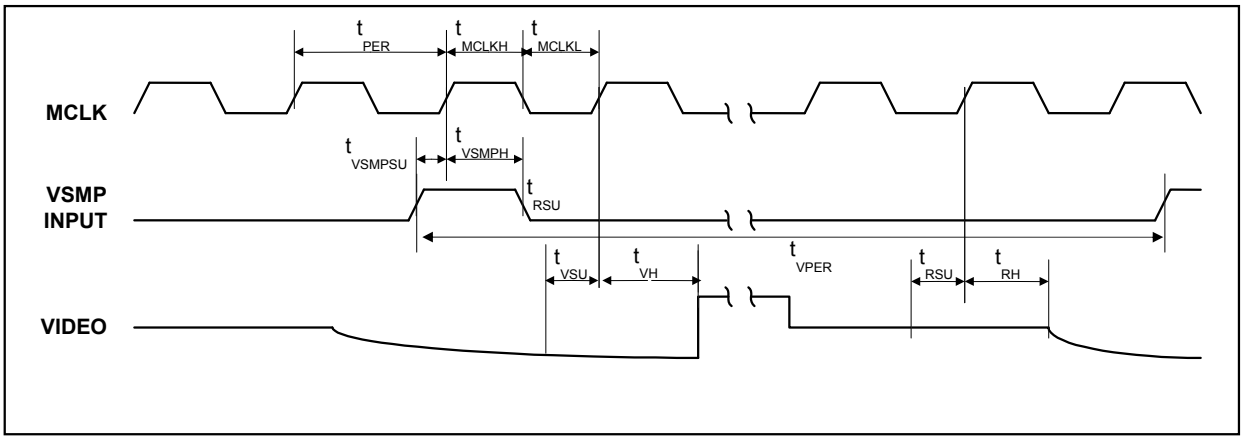


Figure 1 Input Video Timing

Note:

1. See Page 35 (Programmable VSMP Detect Circuit) for video sampling description.

Test Conditions

AVDD1 = 5.75V, DVDD = 3.3V, AGND = DGND = AVDD2 = 0V, T_A = 25°C, MCLK = 24MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
MCLK period	t_{PER}		41.5			ns
MCLK high period	t_{MCLKH}		25			ns
MCLK low period	t_{MCLKL}		25			ns
VSMP period	t_{VPER}		83			ns
VSMP set-up time	t_{VSMPSU}		6			ns
VSMP hold time	t_{VSMPH}		3			ns
Video level set-up time	t_{VSU}		10			ns
Video level hold time	t_{VH}		3			ns
Reset level set-up time	t_{RSU}		10			ns
Reset level hold time	t_{RH}		3			ns

Notes:

1. t_{VSU} and t_{RSU} denote the set-up time required after the input video signal has settled.
2. Parameters are measured at 50% of the rising/falling edge.

OUTPUT DATA TIMING

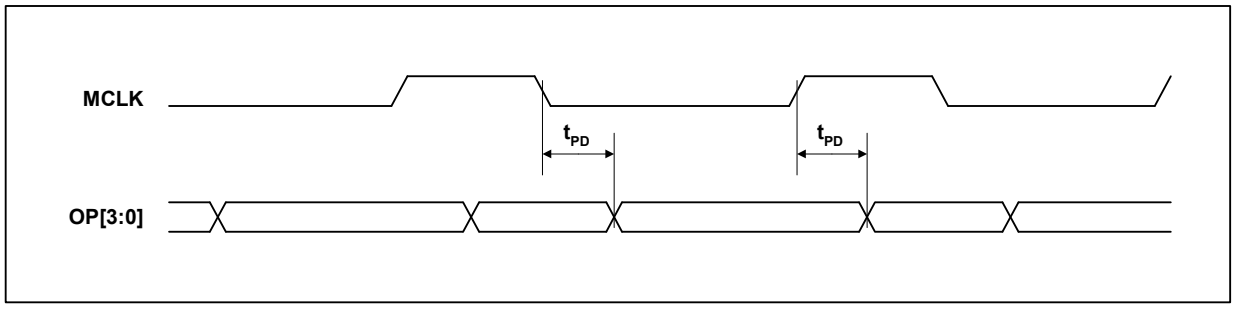


Figure 2 Output Data Timing

Test Conditions

AVDD1 = 5.75V, DVDD = 3.3V, AGND = DGND = AVDD2 = 0V, T_A = 25°C, MCLK = 24MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output propagation delay	t_{PD}	I_{OH} = 1mA, I_{OL} = 1mA	3	8	15	ns

SERIAL INTERFACE

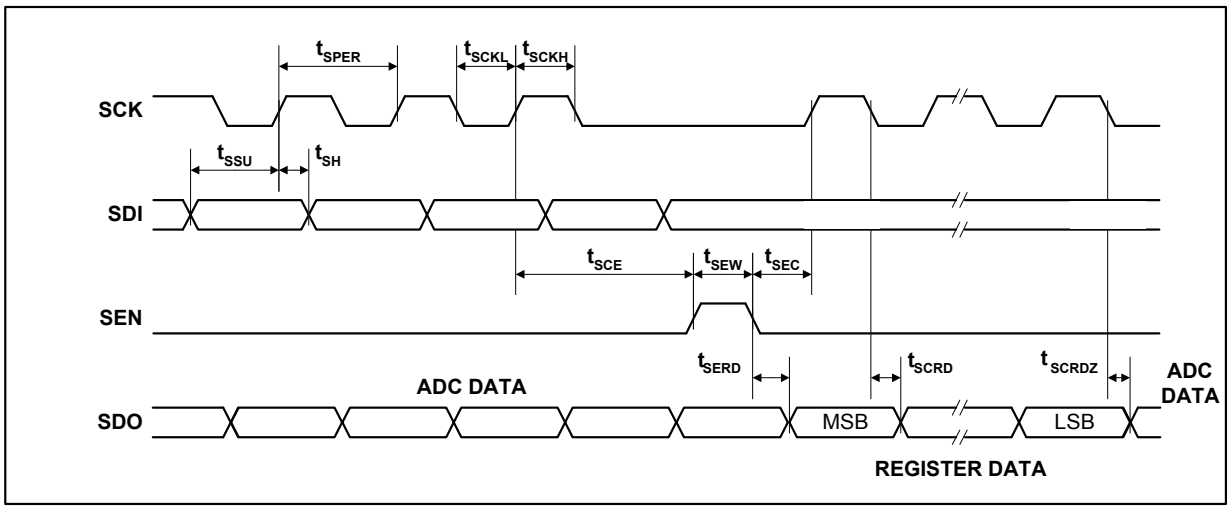


Figure 3 Serial Interface Timing

Test Conditions

AVDD1 = 5.75V, DVDD = 3.3V, AGND = DGND = AVDD2 = 0V, T_A = 25°C, MCLK = 24MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
SCK period	t_{SPER}		41.6			ns
SCK high	t_{SCKH}		18.8			ns
SCK low	t_{SCKL}		18.8			ns
SDI set-up time	t_{SSU}		6			ns
SDI hold time	t_{SH}		6			ns
SCK to SEN set-up time	t_{SCE}		12			ns
SEN to SCK set-up time	t_{SEC}		12			ns
SEN pulse width	t_{SEW}		25			ns
SEN low to SDO = Register data	t_{SERD}				30	ns
SCK low to SDO = Register data	t_{SCRD}				30	ns
SCK low to SDO = ADC data	t_{SCRDZ}				30	ns

Note:

1. Parameters are measured at 50% of the rising/falling edge

PWM TIMING

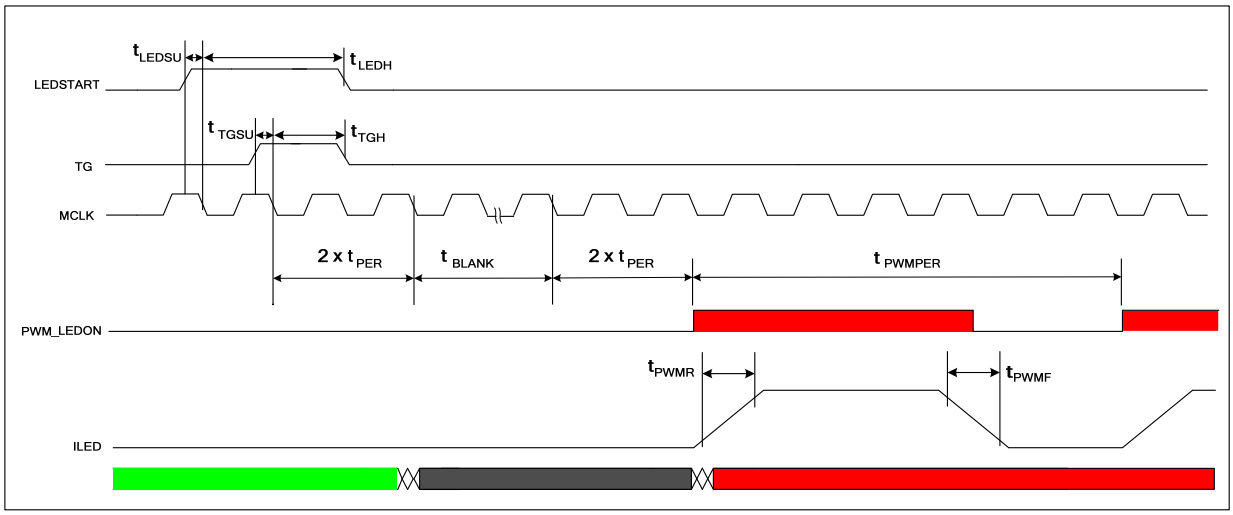


Figure 4 PWM Timing

Test Conditions

AVDD1 = 5.75V, DVDD = 3.3V, AGND = DGND = AVDD2 = 0V, T_A = 25°C, MCLK = 24MHz unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
PWM LED Current Drive Control						
PWM Period	t_{PWMPER}		(CLKDIV+1) * LEDPWMPER * t_{PER}			ns
PWM Duty Cycle			LEDPWMDC/ LEDPWMPER			-
PWM Period Resolution			(CLKDIV +1) * t_{PER}			ns
PWM Period Range			(CLKDIV +1) * 4096 * t_{PER}			ns
PWM Duty Cycle Resolution			(CLKDIV +1) * t_{PER}			ns
PWM Duty Cycle Range			(CLKDIV +1) * 4096 * t_{PER}			ns
PWM Enable Coarse Adjust	$t_{PWMMaxCount}$		t_{PWMPER}*1		t_{PWMPER} *128	ns
LEDSTART set-up time	T_{LEDSU}		6			ns
LEDSTART hold time	T_{LEDH}		3			ns
TG set-up time	t_{TGSU}		6			ns
TG hold time	t_{TGH}		3			ns
PWM Rise / Fall Time	t_{PWMR} /t_{PWMF}		1		5	us
Minimum blank period	t_{BLANK}		25			us

Notes:

1. For LED Current Drive Description refer to Page 17.
2. The Blank period starts on the 2nd falling edge of MCLK after TG goes high.
3. CLKDIV, LEDPWMPER and LEDPWMDC are register settings. For further details see Table 10.

DEVICE DESCRIPTION

INTRODUCTION

A block diagram of the device showing the signal path is presented on Page 1.

The WM8255 processes the sampled video signal on VINP with respect to the video-reset level or an internally/externally generated reference level through the analogue-processing channel.

This processing channel consists of an Input Sampling block with optional Reset Level Clamping (RLC) and Correlated Double Sampling (CDS), an 8-bit programmable offset DAC and an 8-bit Programmable Gain Amplifier (PGA).

The ADC then converts each resulting analogue signal to a 16-bit digital word. The digital output from the ADC is presented on a 4-bit wide bus.

On-chip control registers determine the configuration of the device, including the offsets and gains applied to each channel. These registers are programmable via a serial interface.

The device can control the brightness and timing of the Red, Green and Blue LEDs used in a CIS sensor. This is controlled via the serial control interface and external timing pins.

INPUT SAMPLING

The WM8255 has a single analogue processing channel and ADC, which can be used in a flexible manner to process both monochrome and line-by-line colour inputs.

Monochrome: The selected input (VINP) is sampled, processed by the analogue channel, and converted by the ADC. The same offset DAC and PGA register values are always applied.

Colour Line-by-Line: VINP is sampled and processed by the analogue channel before being converted by the ADC. The gains and offset register values applied to the PGA and offset DAC can be switched between the independent Red, Green and Blue digital registers (e.g. Red → Green→ Blue → Red…) at the start of each line in order to facilitate line-by-line colour operation. The INTM[1:0] bits determine which register contents are applied (see Table 1) to the PGA and offset DAC. By using the INTM[1:0] bits to select the desired register values only one register write is required at the start of each new colour line.

RESET LEVEL CLAMPING (RLC)

To ensure that the signal applied to the WM8255 VINP pin lies within the valid input range (0V to AVDD) the CCD output signal is usually level shifted by coupling through a capacitor, $C_{IN.}$ When active, the RLC circuit clamps the WM8255 side of this capacitor to a suitable voltage during the CCD reset period. The RLCINT register bit controls is used to activate the Reset Level Clamp circuit.

A typical input configuration is shown in Figure 5. The Timing Control Block generates a clamp pulse, CL, from MCLK and VSMP (when RLCINT is high). When CL is active the voltage on the WM8255 side of C_{IN}, at VINP, is forced to the VRLC/VBIAS voltage (V_{VRLC}) by switch 1. When the CL pulse turns off, the voltage at VINP initially remains at V_{VRLC} but any subsequent variation in sensor voltage (from reset to video level) will couple through C_{IN} to VINP.

RLC is compatible with both CDS and non-CDS operating modes, as selected by switch 2. Refer to the CDS/non-CDS Processing section.

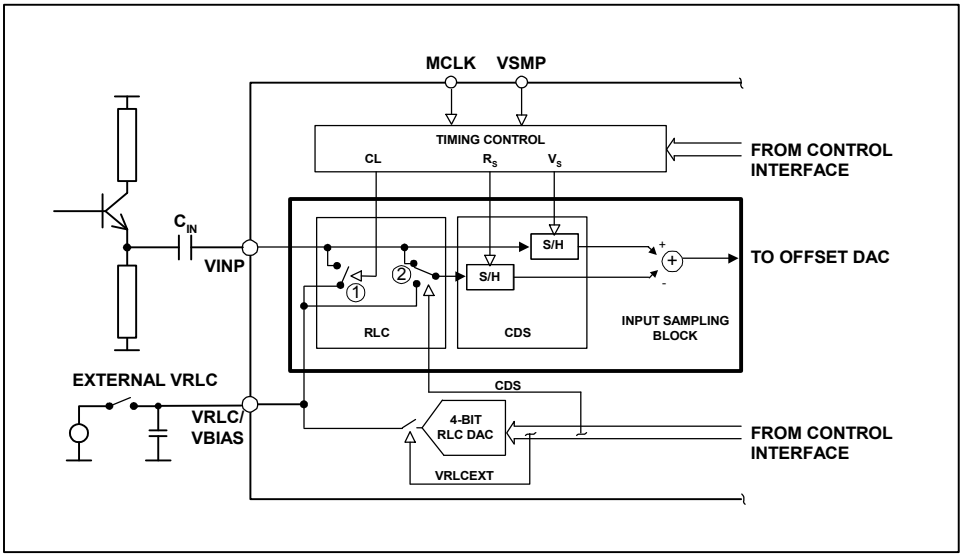


Figure 5 Reset Level Clamping and CDS Circuitry

Reset Level Clamping is controlled by register bit RLCINT. Figure 6 illustrates the effect of the RLCINT bit for a typical CCD waveform, with CL applied during the reset period.

The RLCINT register bit is sampled on the positive edge of MCLK that occurs during each VSMP pulse. The sampled level, high (or low) controls the presence (or absence) of the internal CL pulse on the next reset level. The position of CL can be adjusted by using control bits CDSREF[1:0]

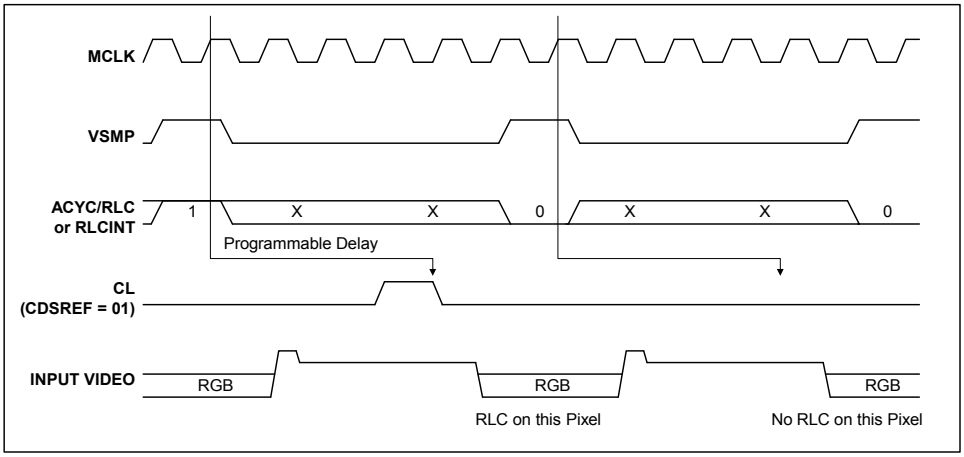


Figure 6 Relationship of RLCINT, MCLK and VSMP to Internal Clamp Pulse, CL

The VRLC/VBIAS pin can be driven internally by a 4-bit DAC (RLCDAC) by writing to control bits RLCV[3:0]. The RLCDAC range and step size may be increased by writing to control bit RLCDACRNG. Alternatively, the VRLC/VBIAS pin can be driven externally by writing to control bit VRLCEXT to disable the RLCDAC and then applying a d.c. voltage to the pin.

CDS/NON-CDS PROCESSING

For CCD type input signals, the signal may be processed using CDS, which will remove pixel-by-pixel common mode noise. For CDS operation, the video level is processed with respect to the video reset level, regardless of whether RLC has been performed. To sample using CDS, control bit CDS must be set to 1 (default), this controls switch 2 (Figure 5) and causes the signal reference to come from the video reset level. The time at which the reset level is sampled, by clock R_s/CL, is adjustable by programming control bits CDSREF[1:0].

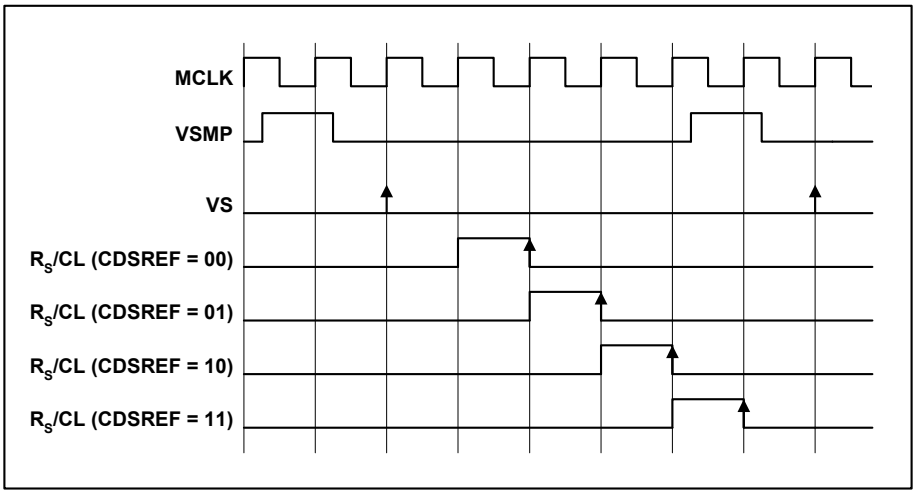


Figure 7 Reset Sample and Clamp Timing

For CIS type sensor signals, non-CDS processing is used. In this case, the video level is processed with respect to the voltage on pin VRLC/VBIAS, generated internally or externally as described above. The VRLC/VBIAS pin is sampled by R_s at the same time as V_s samples the video level in this mode.

OFFSET ADJUST AND PROGRAMMABLE GAIN

The output from the CDS block is a differential signal, which is added to the output of an 8-bit Offset DAC to compensate for offsets and then amplified by an 8-bit PGA. The gain and offset can be set for each of three colours by writing to control bits DACx[7:0] and PGAx[7:0] (where x can be R, G or B).

In colour line-by-line mode the gain and offset coefficients that are applied to the PGA and offset DAC can be multiplexed by control of the INTM[1:0] bits as shown in Table 1.

INTM[1:0]	DESCRIPTION
00	Red offset and gain registers are applied to offset DAC and PGA (DACR[7:0] and PGAR[7:0])
01	Green offset and gain registers applied to offset DAC and PGA (DACG[7:0] and PGAG[7:0])
10	Blue offset and gain registers applied to offset DAC and PGA (DACB[7:0] and PGAB[7:0])
11	Reserved.

Table 1 Offset DAC and PGA Register Control

The gain characteristic of the WM8255 PGA is shown in Figure 8. Figure 9 shows the maximum input voltage (at VINP) that can be gained up to match the ADC full-scale input range (2.0V).

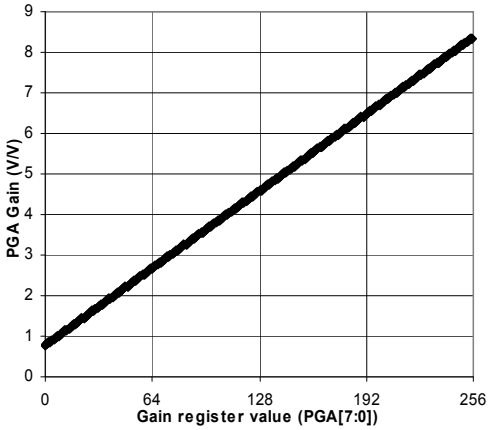


Figure 8 PGA Gain Characteristic

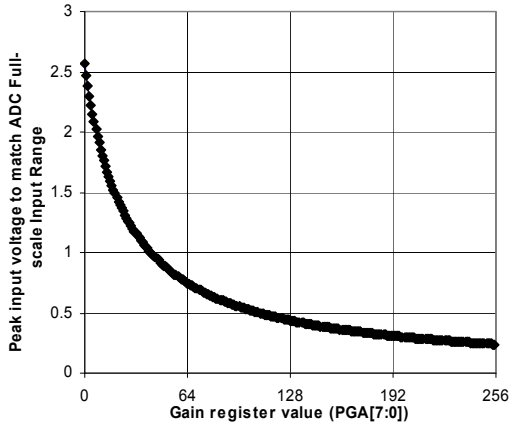


Figure 9 Peak Input Voltage to Match ADC Full-scale Range

ADC INPUT BLACK LEVEL ADJUST

The output from the PGA should be offset to match the full-scale range of the ADC (V_{FS} = 2.0V). For negative-going input video signals, a black level (zero differential) output from the PGA should be offset to the top of the ADC range by setting register bits PGAFS[1:0]=10. For positive going input signal the black level should be offset to the bottom of the ADC range by setting PGAFS[1:0]=11. Bipolar input video is accommodated by setting PGAFS[1:0]=00 or PGAFS[1:0]=01 (zero differential input voltage gives mid-range ADC output).

OVERALL SIGNAL FLOW SUMMARY

Figure 10 represents the processing of the video signal through the WM8255.

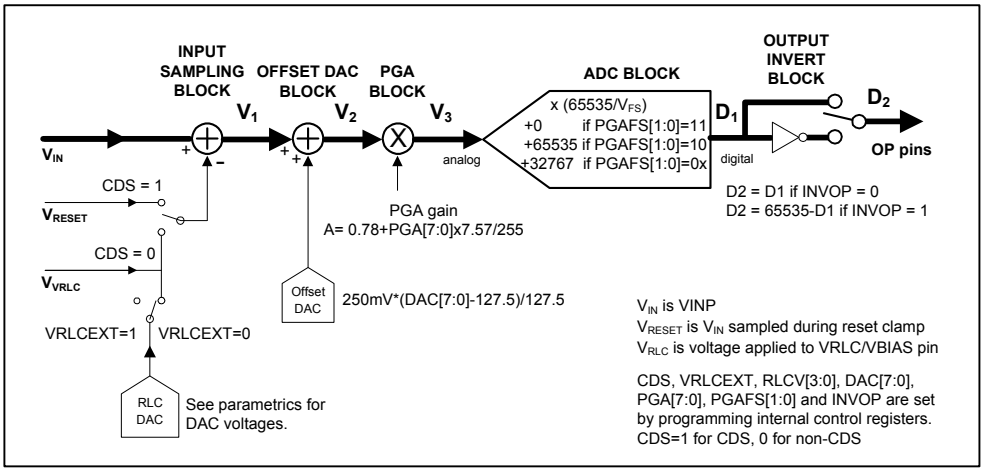


Figure 10 Overall Signal Flow

The **INPUT SAMPLING BLOCK** produces an effective input voltage $\mathbf{V_1}$. For CDS, this is the difference between the input video level V_{IN} and the input reset level V_{RESET}. For non-CDS this is the difference between the input video level V_{IN} and the voltage on the VRLC/VBIAS pin, V_{VRLC}, optionally set via the RLC DAC.

The **OFFSET DAC BLOCK** then adds the amount of fine offset adjustment required to move the black level of the input signal towards 0V, producing $\mathbf{V_2}$.

The **PGA BLOCK** then amplifies the white level of the input signal to maximise the ADC range, outputting voltage $\mathbf{V_3}$.

The **ADC BLOCK** then converts the analogue signal, $\mathbf{V_3}$, to a 16-bit unsigned digital output, $\mathbf{D_1}$.

The digital output is then inverted, if required, through the **OUTPUT INVERT BLOCK** to produce $\mathbf{D_2}$.

CALCULATING OUTPUT FOR ANY GIVEN INPUT

The following equations describe the processing of the video and reset level signals through the WM8255.

INPUT SAMPLING BLOCK: INPUT SAMPLING AND REFERENCING

If CDS = 1, (i.e. CDS operation) the previously sampled reset level, V_{RESET}, is subtracted from the input video.

$$\mathbf{V_1} = V_{IN} - V_{RESET} \quad \text{Eqn. 1}$$

If CDS = 0, (non-CDS operation) the simultaneously sampled voltage on pin VRLC is subtracted instead.

$$\mathbf{V_1} = V_{IN} - V_{VRLC} \quad \text{Eqn. 2}$$

If VRLCEXT = 1, V_{VRLC} is an externally applied voltage on pin VRLC/VBIAS.

If VRLCEXT = 0, V_{VRLC} is the output from the internal RLC DAC.

$$V_{VRLC} = (V_{RLCSTEP} * RLCV[3:0]) + V_{RLCBOT} \quad \text{Eqn. 3}$$

$V_{RLCSTEP}$ is the step size of the RLC DAC and V_{RLCBOT} is the minimum output of the RLC DAC.

OFFSET DAC BLOCK: OFFSET (BLACK-LEVEL) ADJUST

The resultant signal $\mathbf{V_1}$ is added to the Offset DAC output.

$$\mathbf{V_2} = \mathbf{V_1} + \{250mV * (DAC[7:0]-127.5)\} / 127.5 \quad \text{Eqn. 4}$$

PGA NODE: GAIN ADJUST

The signal is then multiplied by the PGA gain,

$$\mathbf{V_3} = \mathbf{V_2} * [0.78+(PGA[7:0]*7.57)/255] \quad \text{Eqn. 5}$$

ADC BLOCK: ANALOGUE-DIGITAL CONVERSION

The analogue signal is then converted to a 16-bit unsigned number, with input range configured by PGAFS[1:0].

$$\mathbf{D_1}[15:0] = INT\{ (\mathbf{V_3}/V_{FS}) * 65535\} + 32767 \quad PGAFS[1:0] = 00 \text{ or } 01 \quad \text{Eqn. 6}$$

$$\mathbf{D_1}[15:0] = INT\{ (\mathbf{V_3}/V_{FS}) * 65535\} \quad PGAFS[1:0] = 11 \quad \text{Eqn. 7}$$

$$\mathbf{D_1}[15:0] = INT\{ (\mathbf{V_3}/V_{FS}) * 65535\} + 65535 \quad PGAFS[1:0] = 10 \quad \text{Eqn. 8}$$

where the ADC full-scale range, V_{FS} = 2.0V

if $\mathbf{D_1}[15:0] < 0$ $\mathbf{D_1}[15:0] = 0$

if $\mathbf{D_1}[15:0] > 65535$ $\mathbf{D_1}[15:0] = 65535$

OUTPUT INVERT BLOCK: POLARITY ADJUST

The polarity of the digital output may be inverted by control bit INVOP.

$$\mathbf{D_2}[15:0] = \mathbf{D_1}[15:0] \quad (INVOP = 0) \quad \text{Eqn. 9}$$

$$\mathbf{D_2}[15:0] = 65535 - \mathbf{D_1}[15:0] \quad (INVOP = 1) \quad \text{Eqn. 10}$$

OUTPUT FORMATS

The digital data output from the ADC is available in a 4-bit wide multiplexed. Latency of valid output data with respect to VSMP is programmable by writing to control bits DEL[1:0]. The latency is shown in the Operating Mode Timing Diagrams section.

Figure 11 shows the output data formats for all modes. Table 2 summarises the output data obtained for each format.

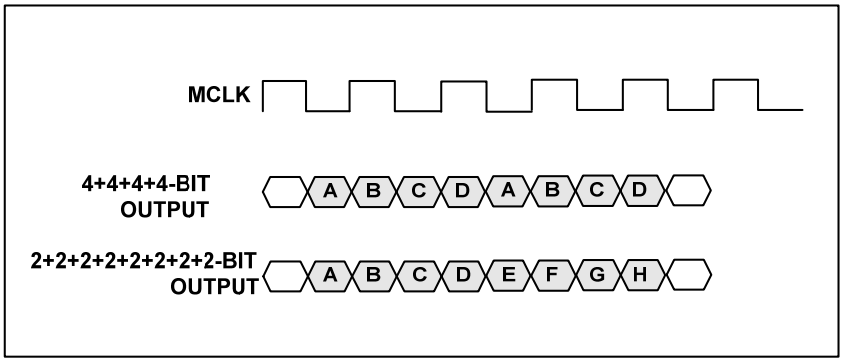


Figure 11 Output Data Formats (4 bit - Modes 1 & 3, 2 bit – Mode 1)

OUTPUT FORMAT	OUTPUT PINS	OUTPUT
4+4+4+4-bit (nibble)	OP[3:0]	A = d15, d14, d13, d12 B = d11, d10, d9, d8 C = d7, d6, d5, d4 D = d3, d2, d1, d0
2+2+2+2+2+2+2+2-bit	OP[1:0]	A = d15, d14 B = d13, d12 C = d11, d10 D = d9 , d8 E = d7 , d6 F = d5 , d4 G = d3 , d2 H = d1, d0

Table 2 Details of Output Data Shown in Figure 11

LED CURRENT DRIVE CONTROL

The WM8255 allows the user to control:

- the sequence of illumination
- the period of illumination
- the intensity of illumination

of the red, blue and green LEDs used to illuminate the image during a scan.

A sequence state machine is used to progress the sequence and control the duration of the LED selection. The progression of the sequence state machine is dependent on whether the WM8255 is in colour mode or monochromatic mode. The intensity of illumination is controlled on either control of the LED drive current or pulsing of the LED driving current.

LED CURRENT DRIVE SEQUENCE CONTROL

With reference to Figure 12, the WM8255 uses a LED sequence state machine to control the sequence and duration of the illumination of the red, green and blue LEDs.

The LED sequence state machine can progress through up to 4 states each sequence. Each of the sequence states (STATE_0 to STATE_3) may be set to one of four values to determine on whether a red, green or blue LED is illuminated or all LEDs are off. The register STATERST will determine the number of states the sequence state machine can progress through. Once the sequence state machine has reached the reset state, the LED state machine will remain in this state until again initiated.

LED CURRENT DRIVE SEQUENCE DEFINITION

Figure 13 illustrates the functionality of the sequence state mapping. The current state of the sequence machine (SEQ_STATE) is an internal register used to select one of the four register state mappings. This register increments until the value specified by STATERST at which point the sequence will hold. Figure 14 shows two examples when STATERST is set to "11_{bin}" for a 4 state sequence, and to "01_{bin}" for a 2 state sequence.

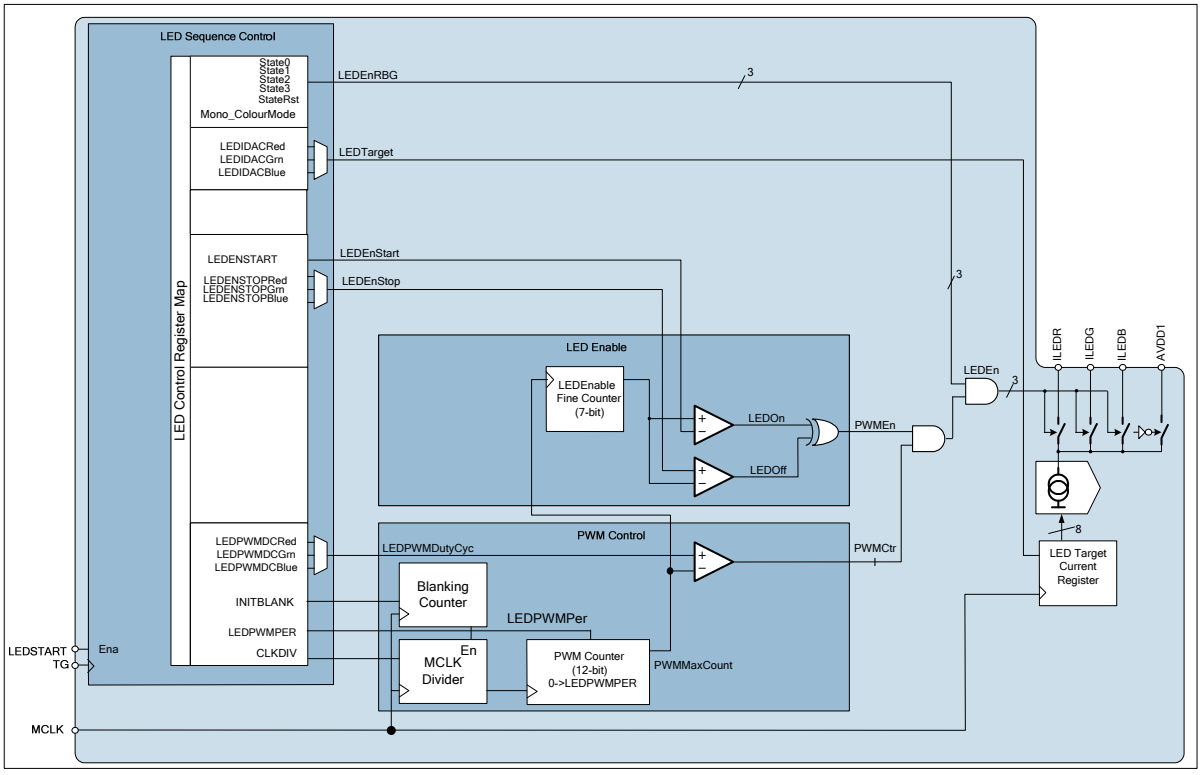


Figure 12 Block Diagram of PWM LED Control

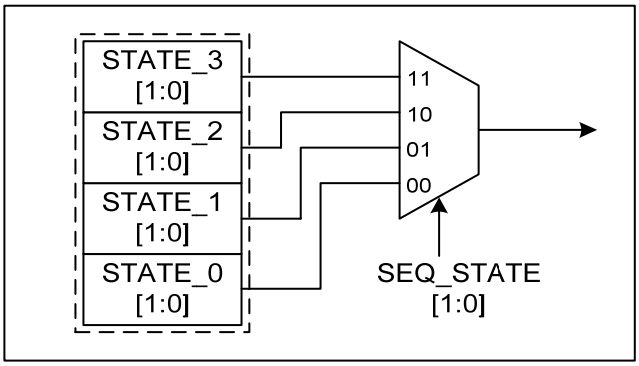


Figure 13 State Mapping Functionality

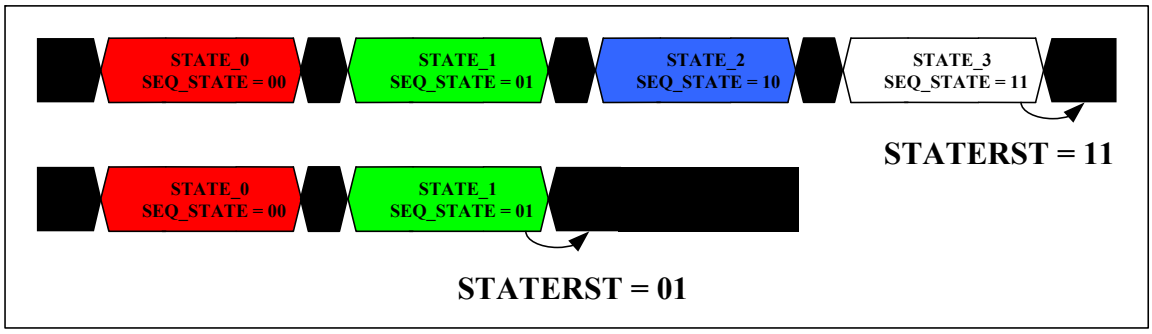


Figure 14 Setting the Sequence Length with STATERST

LED CURRENT DRIVE SEQUENCE SYNCHRONISATION AND PROGRESSION

The trigger to progress the state machine through the sequence states is dependent on whether the LED driver is operating in colour mode or monochrome mode.

COLOUR MODE

In Colour Mode operation, LEDSTART and TG are used to synchronise and progress the sequence state machine. This allows a single LED change for each line scan.

With both LEDSTART and TG high, the sequence state machine is synchronously set to STATE_0 by MCLK. With LEDSTART low and at the next high pulse of TG, the sequence state machine is progressed to the next state, STATE_1, by MCLK. This is repeated until the maximum number of states determined by STATERST has been reached. At this point the LED drive current will be switched away from the selected LED. The sequence state machine will be held in this state until restarted by LEDSTART and TG.

If at any time both TG and LEDSTART are high, the sequence is synchronously set back to STATE_0 by MCLK.

MONOCHROME (COMPOSITE) MODE

In Monochrome Mode, the progression between sequence states is triggered by the completion of the previous sequence state. This allows a complete LED sequence change for each line scan.

With both TG and LEDSTART high, the sequence state machine is synchronously set to the STATE_0 by MCLK. When the STATE_0 has reached the end of its enable period, the sequence state machine is progressed to the next state by MCLK. This is repeated until the maximum number of states determined by STATERST has been reached. At this point the LED drive current will be switched away from the selected LEDs. The sequence state machine will be held in this state until restarted by LEDSTART and TG.

If at any time both TG and LEDSTART are high, the sequence is synchronously set back to STATE_0 by MCLK.

LED CURRENT DRIVE INTENSITY CONTROL

The LED current driver is programmable to allow the LED light intensity to be adjusted independent of the LED light wavelength. Two methods are available for this:

- The absolute LED current drive may be set using a programmable 8-bit current DAC. The current DAC range for each of the LEDs may be adjusted to one of four ranges using the register LEDIRNG.
- The LED current drive may be pulsed using a pulse width modulated. The pulse width modulated period is set using the register LEDPWMPER and on time using the registers LEDPWMDCR, LEDPWMDCB and LEDPWMDCG.

Control of the absolute LED current drive and PWM modulation are independently programmable for each of the red, green and blue LEDs using the register map. The signals LEDSTART, TG and MCLK determine timing.

LED CURRENT DRIVE STATE TRANSITION AND PWM SWITCHING

The WM8255 is the combination of a LED current switching matrix and an AFE. With reference to Figure 15, during a typical line scan the video signal of the previous line scan is digitised by the AFE while the image of the current line scan is illuminated. To suppress any switching noise of the LED switching matrix coupling into the AFE, care is taken while switching the current.

Two types of current switching are available in the WM8255, state transition switching and PWM switching. State transition switching occurs when either a new LED is to be selected or the LED current DAC has to be updated. PWM transition switching occurs when the illumination intensity is controlled by pulsing the LED drive current. In colour mode, state transition switching should occur at the start of a line scan. In mono mode, state transition switching can occur during the line scan. In either colour mode or mono mode, PWM transition switching can occur during the line scan.

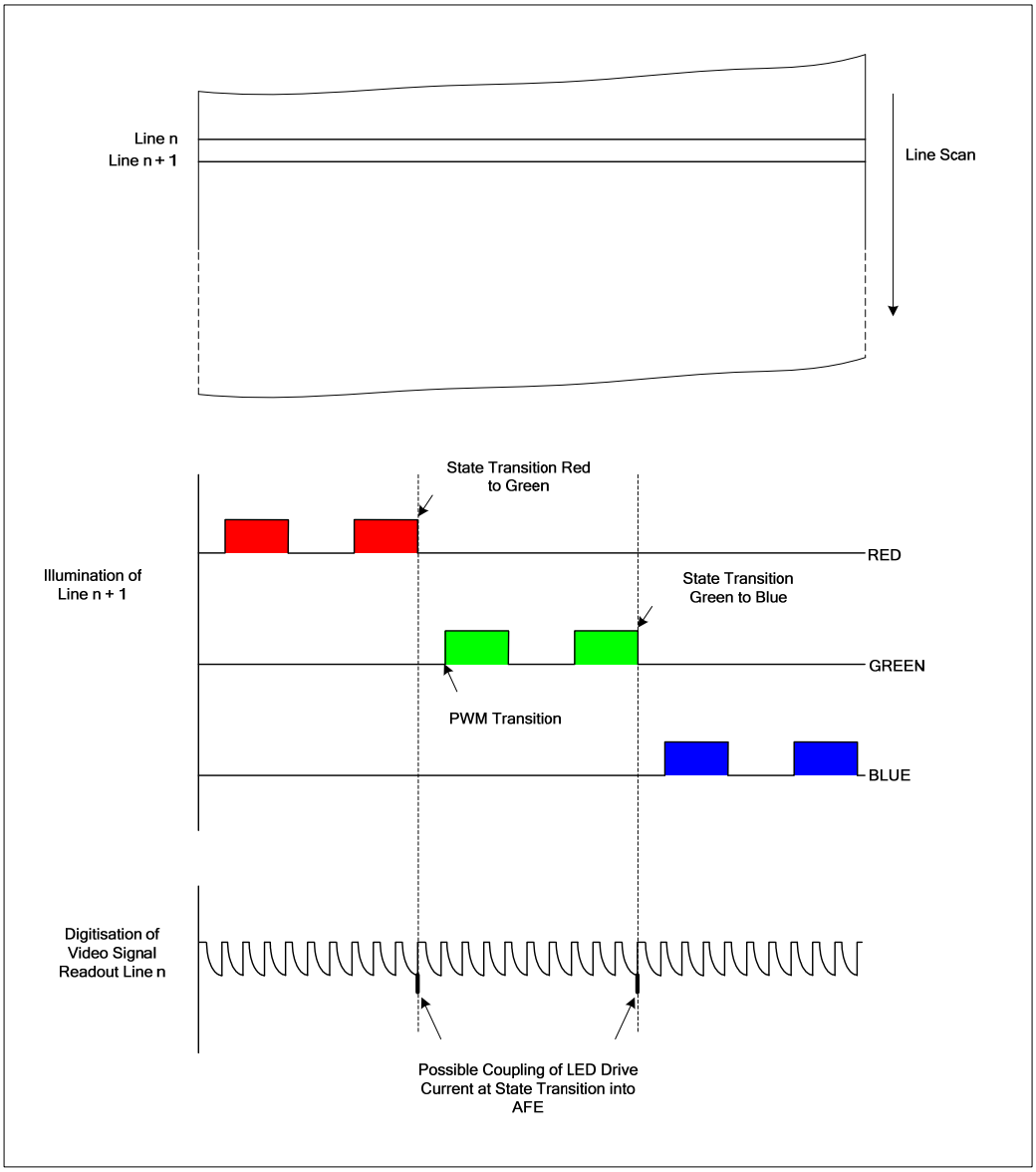


Figure 15 Relationship between Line Scan Illumination and Video Signal Readout

Two current switching techniques are used for state and PWM transition switching, slew rate controlled current switching and current steering switching.

With reference to Figure 16, the LED drive current has three blocks, the LED current DAC, the LED RGB matrix switch and a shunt current path switch.

With reference to Figure 16, for current slew rate controlled switching, the LED current DAC value is reset from the current value to zero then set to an updated value. Slew rate limited current switch may be partitioned into four operations:

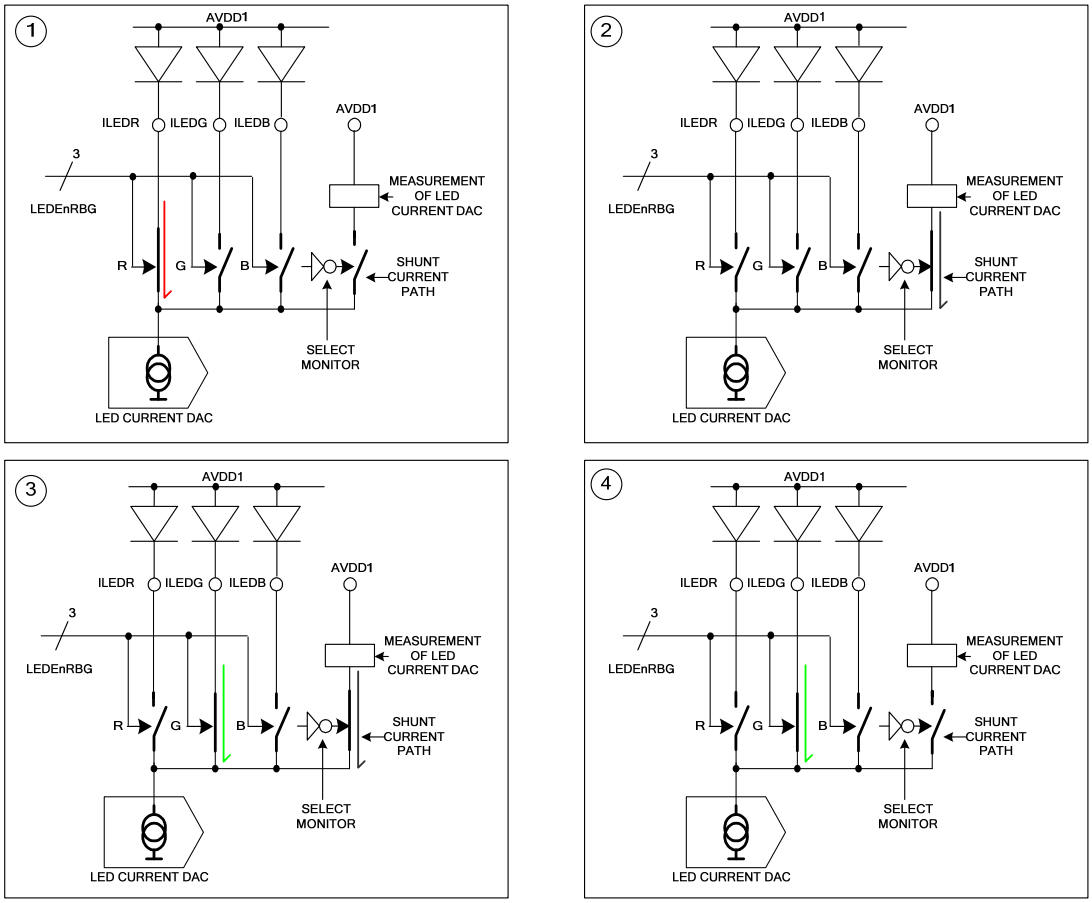


Figure 16 Current Slew Rate Controlled Switching

1. The red RGB switch is initially closed and the LED drive current will flow in the red diode

2. The Red RGB switch will open and the shunt current path switch is closed. The LED drive current will flow in the shunt current path. During this period the LED current DAC is reset to zero then updated to the next value. No current will flow in any LEDs.

3. The green RGB switch will be closed.

4. The auxiliary current path switch will be opened and LED drive current will flow in the green LED.

The finite time taken for a slew rate controlled current switch is the period necessary to change the value of the LED current DAC. The slew rate of the current change is limited by the dynamic performance of the LED current DAC. During this time the LED IDAC current will flow through the shunt current path switch and no illumination will occur. This period of time is defined by blanking period

MONO MODE REQUIREMENTS

During a slew rate limited current switch of the LED IDAC, the change of current flowing in the IDAC will couple a minor disturbance into the AFE. In colour mode this disturbance is not an issue since the state change switching will occur at the beginning of a line scan when no imaging is occurring. In mono mode a red, blue and green state switching may occur during a line scan and couple correlated switching noise into the signal path.

In mono mode to minimise switching noise into the signal path::

- The blanking period must be disabled. In this mode during a state change, no slew rate limiting switching will occur, Only the RGB switches will be switched. Table 3 defines the method to disable blanking during a state transition.

- In this mode of operation, between states the absolute value of the LED IDAC current must not change.

- In this mode of operation, setting the duty cycle to zero is an invalid state. The RGB switches should be used to switch off the LED current.

This method will have no effect on colour mode performance.

BLANKING DISABLE CODE SET		
Address	**Data**	**Comment**
0x01	0xA3	This will put the part into test configuration mode. Any address will now point to the extended page reconfiguration register
0x24	0x1C	This will: -- force the LED IDAC control state machine to stay on at all time - force the value to be held in LEDIDACR to be loaded into the LED current DAC
0x01	0x23	This will take the part back into normal operating mode.
Notes: 1. If this COMPLETE SEQUENCE of operation is not carried out TOGETHER the part may go into an unsupported mode		
To finish a mono mode scan with blanking period disabled and perform another operation, the part needs to get into a know state. Two options are available for a complete reset of the device or a reset of the LED sequence controller:		
Option 1: WM8255 global reset from blanking period disable		
Address	**Data**	**Comment**
0x04	0x00	This will reset the WM8255 into its default condition. The part should now be fully reconfigured into the user configuration.
Option 2: WM8255 LED sequence controller reset from blanking period disable		
Address	**Data**	**Comment**
0x2F	0x00	This will reset LED sequence controller WM8255. All configuration data will be held.

Table 3 Blanking Period Disable

With reference to Figure 17 for current steering,

1. The appropriate RGB matrix switch is closed allowing the LED current DAC current to flow in the LED
2. The first step to switch off the LED current is to close the shunt current path switch
3. The LED is switched off by opening the RGB switch matrix.
4. To switch on the LED, first the shunt current path switch is closed and the cycle repeats.

A make before break switch sequence is used when the LED is switched on or off. As a result the LED current DAC always has a path to flow and never changes value.

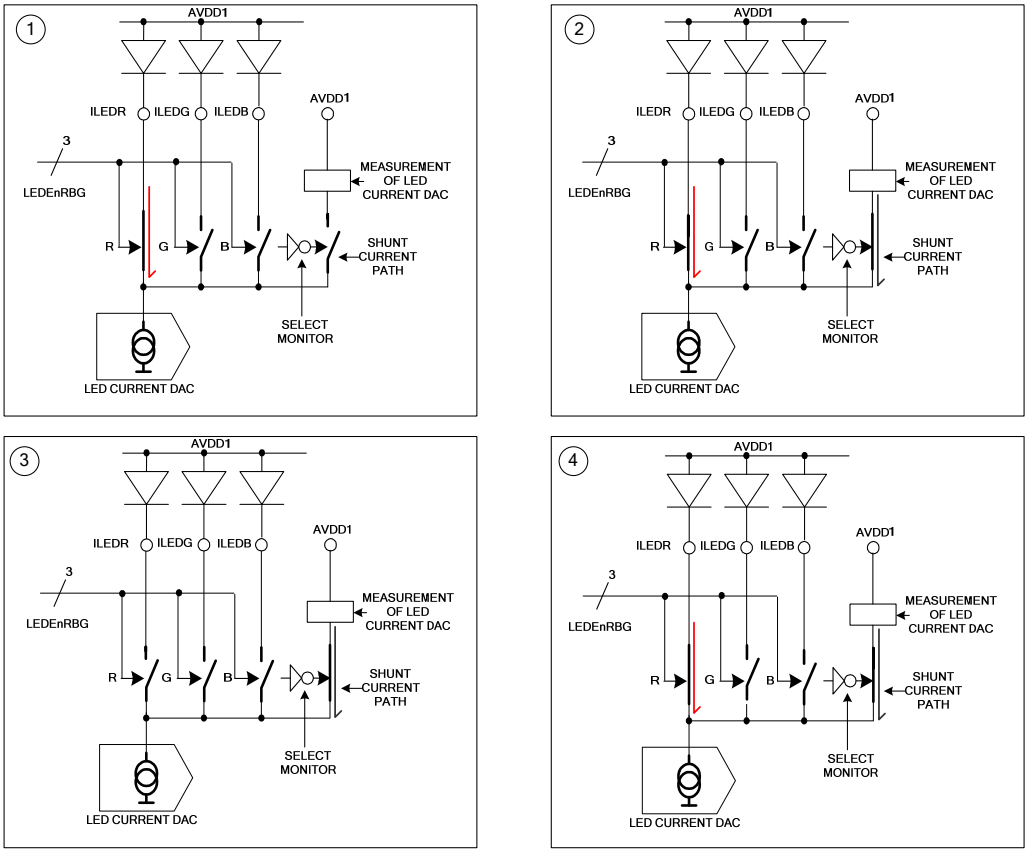


Figure 17 Current Steering Switching

LED CURRENT DRIVE CURRENT PWM CONTROL

During each sequence state, the LED control module can be pulsed by Pulse Width Modulating (PWM) the LED current drive. For each sequence state, the PWM frequency, duty cycle, and number of PWM cycles can be configured.

The PWM controller consists of two blocks; the MCLK divider and the PWM counter. The MCLK divider divides the MCLK by an amount set by the register CLKDIV.

The divided MCLK is then used to clock the PWM counter. The PWM counter will increment until it reaches its maximum count set by the register LEDPWMPER. At this point, the PWM counter will reset to zero, then continue to increment. This will set the period of the PWM control.

As the PWM counter is incremented, its state is compared with the duty cycle setting, which is set by the value in register LEDPWMDC. PWMCtrl is set while the counter value is smaller than the duty cycle setting. When the counter is larger than or equal to the duty cycle, PWMCTRL is reset for the rest of the PWM period. This will set the duty cycle of the PWM control.

The reset of the PWM counter will increment the LEDEnable counter. When the LEDEnable counter has reached LEDENSTART, PWMEn is set high, which allows PWMCtrl to control the LED current drive. The LEDEnable counter will continue to increment until it has reached LEDENSTOP. At this point PWMEn is set low, which stops PWMCtrl from controlling the LED current drive. This will set the number of cycles of the PWM control.

The PWM frequency is defined by LEDPWMPER and the divider CLKDIV. LEDPWMPER and CLKDIV may be calculated as the nearest integral of the MCLK frequency divided by the PWM frequency. If the maximum value of LEDPWMPER would reach its maximum before the desired PWM period is achieved, CLKDIV should be incremented to scale LEDPWMPER correctly.

The PWM duty cycle is defined by LEDPWMDC and CLKDIV. For a chosen PWM frequency, an integral number of PWM cycles for the period of TG may be calculated. The range of the PWM period and the duty cycle can be up to (2^4 X 2^12) MCLK cycles.