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WM8281

Low Power Audio System with Ambient Noise Cancellation and Echo Cancellation

DESCRIPTION

The WM8281 is a highly-integrated low-power audio system for smartphones, tablets and other portable audio devices. It combines an advanced DSP feature set with a flexible, high-performance audio hub CODEC.

The WM8281 digital core combines a quad-core, 600MMAC DSP system with a variety of power-efficient fixed-function audio processing blocks. The programmable DSP cores support advanced audio features, including multi-mic wideband noise reduction, high-performance acoustic echo cancellation (AEC), stereo ambient noise cancellation (ANC), speech enhancement, advanced media enhancement, and many more. The DSP cores are supported by a fully-flexible, all-digital mixing and routing engine with sample rate converters, for wide use-case flexibility.

A SLIMbus® interface supports multi-channel audio paths and host control register access. Multiple sample rates are supported concurrently via the SLIMbus interface. Three further digital audio interfaces are provided, each supporting a wide range of standard audio sample rates and serial interface formats. Automatic sample rate detection enables seamless wideband/narrowband voice call handover.

Three stereo headphone drivers each provide stereo ground-referenced or mono BTL outputs. 110dB SNR, and noise levels as low as $0.8\mu V_{RMS}$, offer hi-fi quality line or headphone output. The WM8281 also features a stereo pair of 2W Class-D outputs and four channels of stereo PDM output. A signal generator for controlling haptics devices is included; vibe actuators can connect directly to the Class-D speaker output, or via an external driver on the PDM output interface. All inputs, outputs and system interfaces can function concurrently.

The WM8281 supports up to eight microphone inputs, (up to six analogue, or up to eight PDM digital, or combinations of each). Microphone activity detection with interrupt is available. A smart accessory interface supports most standard 3.5mm accessories. Impedance sensing and measurement is provided for external accessory and push-button detection.

The WM8281 power, clocking and output driver architectures are all designed to maximise battery life in voice, music and standby modes. Low-power 'Sleep' is supported, with configurable wake-up events. The WM8281 is powered from a 1.8V external supply. A separate supply is required for the Class D speaker drivers (typically direct connection to 4.2V battery).

Two integrated FLLs provide support for a wide range of system clock frequencies. The WM8281 is configured using the I2C, SPI™ or SLIMbus interfaces. The fully-differential internal analogue architecture, minimal analogue signal paths and on-chip RF noise filters ensure a very high degree of noise immunity.

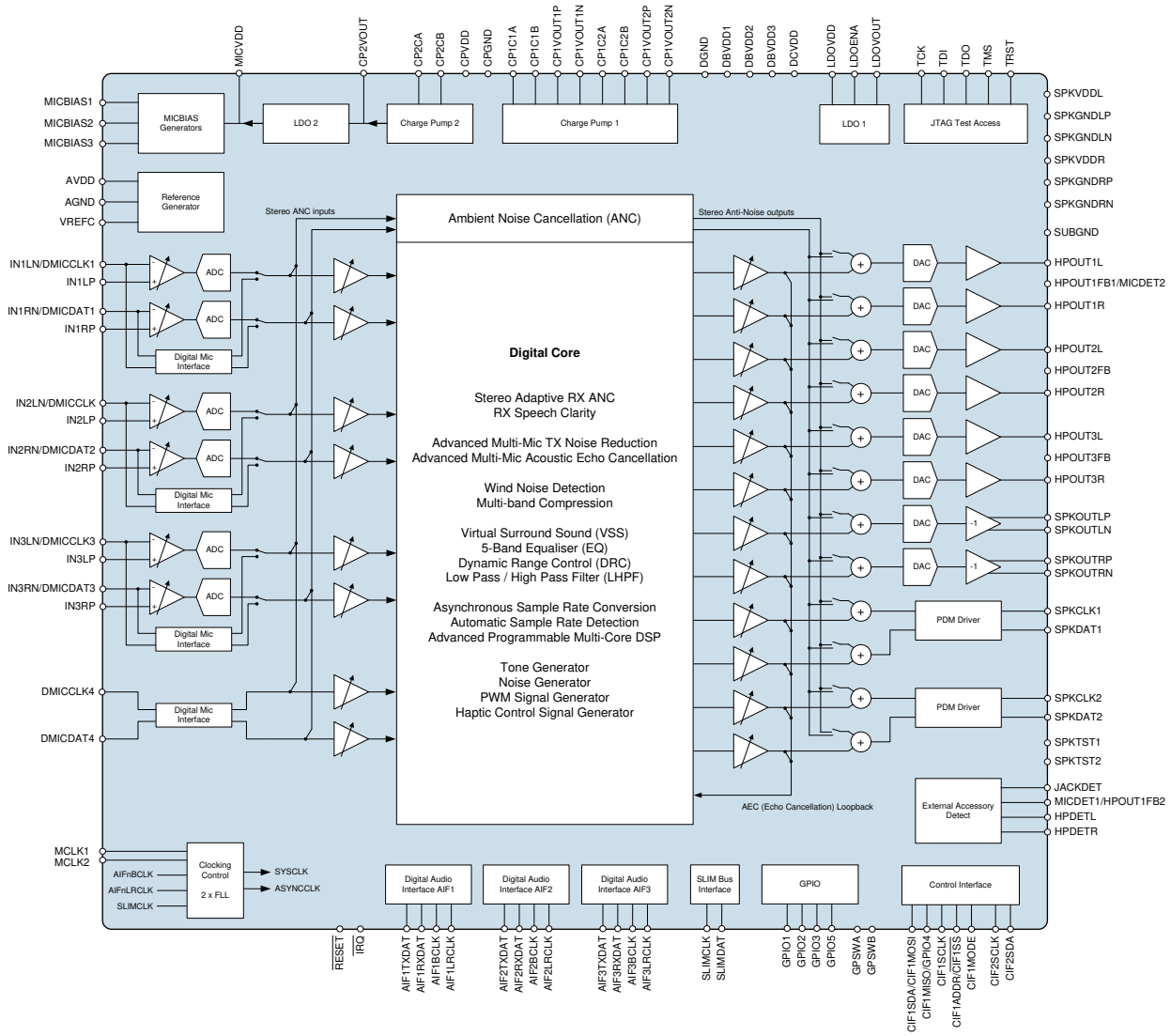
FEATURES

- 600 MIPS, 600MMAC multi-core audio-signal processor
- Programmable wideband, multi-mic audio processing
  - Cirrus Logic® stereo adaptive ambient noise cancellation
  - Transmit-path noise reduction and echo cancellation
  - Wind noise, sidetone and other programmable filters
  - Dynamic Range Control, Fully parametric EQs
  - Multiband Compression, Virtual Surround Sound
- Multi-channel asynchronous sample rate conversion
- Integrated 6/8 channel 24-bit hi-fi audio hub CODEC
  - 6 ADCs, 100dB SNR microphone input (48kHz)
  - 8 DACs, 121dB SNR headphone playback (48kHz), (48kHz, eDRE software enabled)
- Audio inputs
  - Up to 6 analogue or 8 digital microphone inputs
  - Single-ended or differential mic/line inputs
- Multi-purpose headphone / earpiece / line output drivers
  - 3 stereo output paths
  - 33mW into 32Ω load at 1% THD+N
  - 100mW into 16Ω BTL load at 5% THD+N
  - 4mW typical headphone playback power consumption
  - Pop suppression functions
  - $0.8\mu V_{RMS}$ noise floor (A-weighted)
- Stereo (2 x 2W) Class D speaker output drivers
  - Direct drive of external haptics vibe actuators
- Four-channel digital speaker (PDM) interface
- SLIMbus audio and control interface
- 3 full digital audio interfaces
  - Standard sample rates from 4kHz up to 192kHz
  - Ultrasonic accessory function support
  - TDM support on all AIFs
  - Multi-channel input/output on AIF1 and AIF2
  - Stereo input/output on AIF3
- Flexible clocking, derived from MCLKn, BCLKn, LRCLKn or SLIMbus
- 2 low-power FLLs support reference clocks down to 32kHz
- Advanced accessory detection functions
  - Low-power standby mode and configurable wake-up
- Configurable functions on 5 GPIO pins
- Integrated LDO regulators and charge pumps
- Small W-CSP package, 0.4mm pitch

APPLICATIONS

- Smartphones, tablets, and multimedia handsets

BLOCK DIAGRAM



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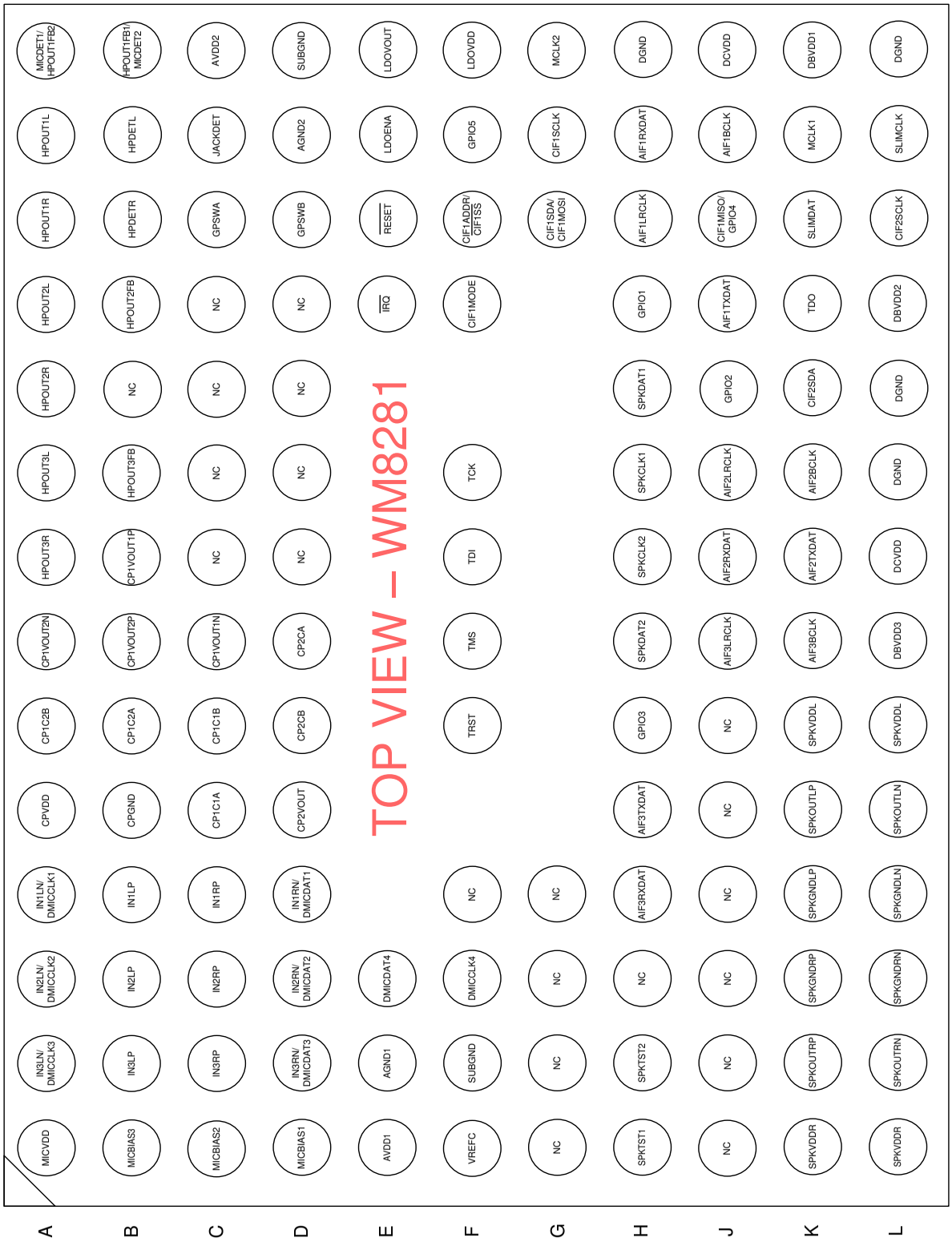
PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8281ECS/R	-40°C to +85°C	W-CSP (Pb-free, Tape and reel)	MSL1	260°C

Note:
Reel quantity = 7000

PIN DESCRIPTION

A description of each pin on the WM8281 is provided below.
Note that a table detailing the associated power domain for every input and output pin is provided on the following page.
Note that, where multiple pins share a common name, these pins should be tied together on the PCB.
All Digital Output pins are CMOS outputs, unless otherwise stated.

PIN NO	NAME	TYPE	DESCRIPTION
E2	AGND1	Supply	Analogue ground (Return path for AVDD1)
D13	AGND2	Supply	Analogue ground (Return path for AVDD2)
J13	AIF1BCLK	Digital Input / Output	Audio interface 1 bit clock
H13	AIF1RXDAT	Digital Input	Audio interface 1 RX digital audio data
H12	AIF1LRCLK	Digital Input / Output	Audio interface 1 left / right clock
J11	AIF1TXDAT	Digital Output	Audio interface 1 TX digital audio data
K9	AIF2BCLK	Digital Input / Output	Audio interface 2 bit clock
J8	AIF2RXDAT	Digital Input	Audio interface 2 RX digital audio data
J9	AIF2LRCLK	Digital Input / Output	Audio interface 2 left / right clock
K8	AIF2TXDAT	Digital Output	Audio interface 2 TX digital audio data
K7	AIF3BCLK	Digital Input / Output	Audio interface 3 bit clock
H4	AIF3RXDAT	Digital Input	Audio interface 3 RXdigital audio data
J7	AIF3LRCLK	Digital Input / Output	Audio interface 3 left / right clock
H5	AIF3TXDAT	Digital Output	Audio interface 3 TX digital audio data
E1	AVDD1	Supply	Analogue supply
C14	AVDD2	Supply	Analogue supply
F12	CIF1ADDR/ $\overline{\text{CIF1SS}}$	Digital Input	Control interface 1 (I2C) address select / Control interface 1 (SPI) Slave Select (SS)
J12	CIF1MISO/ GPIO4	Digital Input / Output	Control interface 1 Master In Slave Out data / General Purpose pin GPIO4. The CIFMISO configuration is selectable CMOS or 'Wired OR'. The GPIO4 output is selectable CMOS or Open Drain.
F11	CIF1MODE	Digital Input	Control interface 1 mode select input
G13	CIF1SCLK	Digital Input	Control interface 1 clock input
G12	CIF1SDA/ CIF1MOSI	Digital Input / Output	Control interface 1 (I2C) data input and output / Control interface 1 (SPI) Master Out Slave In data. The output functions are implemented as an Open Drain circuit.
L12	CIF2SCLK	Digital Input	Control interface 2 clock input
K10	CIF2SDA	Digital Input / Output	Control interface 2 data input and output / acknowledge output. The output function is implemented as an Open Drain circuit.
C5	CP1C1A	Analogue Output	Charge pump 1 fly-back capacitor 1 pin
C6	CP1C1B	Analogue Output	Charge pump 1 fly-back capacitor 1 pin
B6	CP1C2A	Analogue Output	Charge pump 1 fly-back capacitor 2 pin
A6	CP1C2B	Analogue Output	Charge pump 1 fly-back capacitor 2 pin
C7	CP1VOUT1N	Analogue Output	Charge pump 1 negative output 1 decoupling pin
B8	CP1VOUT1P	Analogue Output	Charge pump 1 positive output 1 decoupling pin
A7	CP1VOUT2N	Analogue Output	Charge pump 1 negative output 2 decoupling pin

PIN NO	NAME	TYPE	DESCRIPTION
B7	CP1VOUT2P	Analogue Output	Charge pump 1 positive output 2 decoupling pin
D7	CP2CA	Analogue Output	Charge pump 2 fly-back capacitor pin
D6	CP2CB	Analogue Output	Charge pump 2 fly-back capacitor pin
D5	CP2VOUT	Analogue Output	Charge pump 2 output decoupling pin / Supply for LDO2
B5	CPGND	Supply	Charge pump 1 & 2 ground (Return path for CPVDD)
A5	CPVDD	Supply	Supply for Charge Pump 1 & 2
K14	DBVDD1	Supply	Digital buffer (I/O) supply (core functions and Audio Interface 1)
L11	DBVDD2	Supply	Digital buffer (I/O) supply (for Audio Interface 2)
L7	DBVDD3	Supply	Digital buffer (I/O) supply (for Audio Interface 3)
J14, L8	DCVDD	Supply	Digital core supply
H14, L9, L10, L14	DGND	Supply	Digital ground (Return path for DCVDD, DBVDD1, DBVDD2 and DBVDD3)
F3	DMICCLK4	Digital Output	Digital MIC clock output 4
E3	DMICDAT4	Digital Input	Digital MIC data input 4
H11	GPIO1	Digital Input / Output	General Purpose pin GPIO1. The output configuration is selectable CMOS or Open Drain.
J10	GPIO2	Digital Input / Output	General Purpose pin GPIO2. The output configuration is selectable CMOS or Open Drain.
H6	GPIO3	Digital Input / Output	General Purpose pin GPIO3. The output configuration is selectable CMOS or Open Drain.
F13	GPIO5	Digital Input / Output	General Purpose pin GPIO5. The output configuration is selectable CMOS or Open Drain.
C12	GPSWA	Analogue Input / Output	General Purpose bi-directional switch contact
D12	GPSWB	Analogue Input / Output	General Purpose bi-directional switch contact
B13	HPDETL	Analogue Input	Headphone left (HPOUT1L) sense input
B12	HPDETR	Analogue Input	Headphone right (HPOUT1R) sense input
B14	HPOUT1FB1/ MICDET2	Analogue Input	HPOUT1L and HPOUT1R ground feedback pin 1/ Microphone & accessory sense input 2
A13	HPOUT1L	Analogue Output	Left headphone 1 output
A12	HPOUT1R	Analogue Output	Right headphone 1 output
B11	HPOUT2FB	Analogue Input	HPOUT2L and HPOUT2R ground loop noise rejection feedback
A11	HPOUT2L	Analogue Output	Left headphone 2 output
A10	HPOUT2R	Analogue Output	Right headphone 2 output
B9	HPOUT3FB	Analogue Input	HPOUT3L and HPOUT3R ground loop noise rejection feedback
A9	HPOUT3L	Analogue Output	Left headphone 3 output
A8	HPOUT3R	Analogue Output	Right headphone 3 output
A4	IN1LN/ DMICCLK1	Analogue Input / Digital Output	Left channel negative differential Mic/Line input / Digital MIC clock output 1
B4	IN1LP	Analogue Input	Left channel single-ended Mic/Line input / Left channel positive differential Mic/Line input
D4	IN1RN/ DMICDAT1	Analogue input / Digital Input	Right channel negative differential Mic/Line input / Digital MIC data input 1
C4	IN1RP	Analogue Input	Right channel single-ended Mic/Line input / Right channel positive differential Mic/Line input
A3	IN2LN/ DMICCLK2	Analogue Input / Digital Output	Left channel negative differential Mic/Line input / Digital MIC clock output 2
B3	IN2LP	Analogue Input	Left channel single-ended Mic/Line input / Left channel positive differential Mic/Line input
D3	IN2RN/ DMICDAT2	Analogue input / Digital Input	Right channel negative differential Mic/Line input / Digital MIC data input 2
C3	IN2RP	Analogue Input	Right channel single-ended Mic/Line input / Right channel positive differential Mic/Line input

PIN NO	NAME	TYPE	DESCRIPTION
A2	IN3LN/ DMICCLK3	Analogue Input / Digital Output	Left channel negative differential Mic/Line input / Digital MIC clock output 3
B2	IN3LP	Analogue Input	Left channel single-ended Mic/Line input / Left channel positive differential Mic/Line input
D2	IN3RN/ DMICDAT3	Analogue input / Digital Input	Right channel negative differential Mic/Line input / Digital MIC data input 3
C2	IN3RP	Analogue Input	Right channel single-ended Mic/Line input / Right channel positive differential Mic/Line input
E11	IRQ	Digital Output	Interrupt Request (IRQ) output (default is active low). The pin configuration is selectable CMOS or Open Drain.
C13	JACKDET	Analogue Input	Jack detect input
E13	LDOENA	Digital Input	Enable pin for LDO1 (generates DCVDD supply). Logic 1 input enables LDO1. If using external DCVDD supply, then LDO1 is not used, and LDOENA must be held at logic 0.
F14	LDOVDD	Supply	Supply for LDO1
E14	LDOVOUT	Analogue Output	LDO1 output. If using external DCVDD, then LDOVOUT must be left floating.
K13	MCLK1	Digital Input	Master clock 1
G14	MCLK2	Digital Input	Master clock 2
D1	MICBIAS1	Analogue Output	Microphone bias 1
C1	MICBIAS2	Analogue Output	Microphone bias 2
B1	MICBIAS3	Analogue Output	Microphone bias 3
A14	MICDET1/ HPOUT1FB2	Analogue Input	Microphone & accessory sense input 1/ HPOUT1L and HPOUT1R ground feedback pin 2
A1	MICVDD	Analogue Output	LDO2 output decoupling pin (generated internally by WM8281). (Can also be used as reference/supply for external microphones.)
E12	RESET	Digital Input	Digital Reset input (active low)
L13	SLIMCLK	Digital Input / Output	SLIM Bus Clock input / output
K12	SLIMDAT	Digital Input / Output	SLIM Bus Data input / output
H9	SPKCLK1	Digital Output	Digital speaker (PDM) 1 clock output
H8	SPKCLK2	Digital Output	Digital speaker (PDM) 2 clock output
H10	SPKDAT1	Digital Output	Digital speaker (PDM) 1 data output
H7	SPKDAT2	Digital Output	Digital speaker (PDM) 2 data output
L4	SPKGNDLN	Supply	Left speaker driver ground (Return path for SPKVDDL). See note.
K4	SPKGNDLP	Supply	Left speaker driver ground (Return path for SPKVDDL). See note.
L3	SPKGNDRN	Supply	Right speaker driver ground (Return path for SPKVDDR). See note.
K3	SPKGNDRP	Supply	Right speaker driver ground (Return path for SPKVDDR). See note.
L5	SPKOUTLN	Analogue Output	Left speaker negative output
K5	SPKOUTLP	Analogue Output	Left speaker positive output
L2	SPKOUTRN	Analogue Output	Right speaker negative output
K2	SPKOUTRP	Analogue Output	Right speaker positive output
H1	SPKTST1	Analogue Output	Test function (recommend no external connection)
H2	SPKTST2	Analogue Output	Test function (recommend no external connection)
K6, L6	SPKVDDL	Supply	Left speaker driver supply
K1, L1	SPKVDDR	Supply	Right speaker driver supply
D14, F2	SUBGND	Supply	Substrate ground
F9	TCK	Digital Input	JTAG clock input. Internal pull-down holds this pin at logic 0 for normal operation.

PIN NO	NAME	TYPE	DESCRIPTION
F8	TDI	Digital Input	JTAG data input. Internal pull-down holds this pin at logic 0 for normal operation.
K11	TDO	Digital Output	JTAG data output
F7	TMS	Digital Input	JTAG mode select input. Internal pull-down holds this pin at logic 0 for normal operation.
F6	TRST	Digital Input	JTAG Test Access Port reset (active low). Internal pull-down holds this pin at logic 0 for normal operation.
F1	VREFC	Analogue Output	Bandgap reference external components connection
B10, C8, C9, C10, C11, D8, D9, D10, D11, F4, G1, G2, G3, G4, H3, J1, J2, J3, J4, J5, J6	NC	n/a	No Connection

Note: Separate P/N ground connections are provided for each speaker driver channel; this provides flexible support for current monitoring and output protection circuits. If this option is not used, then the respective ground connections should be tied together on the PCB.

The following table identifies the power domain and ground reference associated with each of the input / output pins.

PIN NO	NAME	POWER DOMAIN	GROUND DOMAIN
J13	AIF1BCLK	DBVDD1	DGND
H13	AIF1RXDAT	DBVDD1	DGND
H12	AIF1LRCLK	DBVDD1	DGND
J11	AIF1TXDAT	DBVDD1	DGND
K9	AIF2BCLK	DBVDD2	DGND
J8	AIF2RXDAT	DBVDD2	DGND
J9	AIF2LRCLK	DBVDD2	DGND
K8	AIF2TXDAT	DBVDD2	DGND
K7	AIF3BCLK	DBVDD3	DGND
H4	AIF3RXDAT	DBVDD3	DGND
J7	AIF3LRCLK	DBVDD3	DGND
H5	AIF3TXDAT	DBVDD3	DGND
F12	CIF1ADDR/ C1F1SS	DBVDD1	DGND
J12	CIF1MISO/ GPIO4	DBVDD1	DGND
F11	CIF1MODE	DBVDD1	DGND
G13	CIF1SCLK	DBVDD1	DGND
G12	CIF1SDA/ CIF1MOSI	DBVDD1	DGND
L12	CIF2SCLK	DBVDD2	DGND
K10	CIF2SDA	DBVDD2	DGND
F3	DMICCLK4	MICVDD, MICBIAS1, MICBIAS2, MICBIAS3 The DMICCLK4 power domain is selectable using IN4_DMIC_SUP	AGND
E3	DMICDAT4	MICVDD, MICBIAS1, MICBIAS2, MICBIAS3 The DMICDAT4 power domain is selectable using IN4_DMIC_SUP	AGND
H11	GPIO1	DBVDD1	DGND
J10	GPIO2	DBVDD2	DGND
H6	GPIO3	DBVDD3	DGND
F13	GPIO5	DBVDD1	DGND
C12	GPSWA		
D12	GPSWB		
B13	HPDETL	AVDD	AGND
B12	HPDETR	AVDD	AGND
B14	HPOUT1FB1/ MICDET2	CPVDD (Ground noise rejection) / MICVDD (Microphone / Accessory detection)	CPGND
A13	HPOUT1L	CPVDD	CPGND
A12	HPOUT1R	CPVDD	CPGND
B11	HPOUT2FB	CPVDD	CPGND
A11	HPOUT2L	CPVDD	CPGND
A10	HPOUT2R	CPVDD	CPGND
B9	HPOUT3FB	CPVDD	CPGND
A9	HPOUT3L	CPVDD	CPGND
A8	HPOUT3R	CPVDD	CPGND
A4	IN1LN DMICCLK1	MICVDD (analogue) / MICVDD, MICBIAS1, MICBIAS2, MICBIAS3 (digital) The DMICCLK1 power domain is selectable using IN1_DMIC_SUP	AGND
B4	IN1LP	MICVDD	AGND
D4	IN1RN/ DMICDAT1	MICVDD (analogue) / MICVDD, MICBIAS1, MICBIAS2, MICBIAS3 (digital) The DMICDAT1 power domain is selectable using IN1_DMIC_SUP	AGND

PIN NO	NAME	POWER DOMAIN	GROUND DOMAIN
C4	IN1RP	MICVDD	AGND
A3	IN2LN/ DMICCLK2	MICVDD (analogue) / MICVDD, MICBIAS1, MICBIAS2, MICBIAS3 (digital) The DMICCLK2 power domain is selectable using IN2_DMIC_SUP	AGND
B3	IN2LP	MICVDD	AGND
D3	IN2RN/ DMICDAT2	MICVDD (analogue) / MICVDD, MICBIAS1, MICBIAS2, MICBIAS3 (digital) The DMICDAT2 power domain is selectable using IN2_DMIC_SUP	AGND
C3	IN2RP	MICVDD	AGND
A2	IN3LN/ DMICCLK3	MICVDD (analogue) / MICVDD, MICBIAS1, MICBIAS2, MICBIAS3 (digital) The DMICCLK3 power domain is selectable using IN3_DMIC_SUP	AGND
B2	IN3LP	MICVDD	AGND
D2	IN3RN/ DMICDAT3	MICVDD (analogue) / MICVDD, MICBIAS1, MICBIAS2, MICBIAS3 (digital) The DMICDAT3 power domain is selectable using IN3_DMIC_SUP	AGND
C2	IN3RP	MICVDD	AGND
E11	IRQ	DBVDD1	DGND
C13	JACKDET	AVDD	AGND
E13	LDOENA	DBVDD1	DGND
K13	MCLK1	DBVDD1	DGND
G14	MCLK2	DBVDD1	DGND
D1	MICBIAS1	MICVDD	AGND
C1	MICBIAS2	MICVDD	AGND
B1	MICBIAS3	MICVDD	AGND
A14	MICDET1/ HPOUT1FB2	MICVDD (Microphone / Accessory detection) / CPVDD (Ground noise rejection)	AGND
E12	RESET	DBVDD1	DGND
L13	SLIMCLK	DBVDD1	DGND
K12	SLIMDAT	DBVDD1	DGND
H9	SPKCLK1	DBVDD2	DGND
H8	SPKCLK2	DBVDD2	DGND
H10	SPKDAT1	DBVDD2	DGND
H7	SPKDAT2	DBVDD2	DGND
L5	SPKOUTLN	SPKVDDL	SPKGNDL
K5	SPKOUTLP	SPKVDDL	SPKGNDL
L2	SPKOUTRN	SPKVDDR	SPKGNDR
K2	SPKOUTRP	SPKVDDR	SPKGNDR
F9	TCK	DBVDD2	DGND
F8	TDI	DBVDD2	DGND
K11	TDO	DBVDD2	DGND
F7	TMS	DBVDD2	DGND
F6	TRST	DBVDD2	DGND
F1	VREFC	AVDD	AGND

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus Logic tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (DCVDD)	-0.3V	1.6V
Supply voltages (CPVDD)	-0.3V	2.5V
Supply voltages (DBVDD1, DBVDD2, DBVDD3, LDOVDD, AVDD, MICVDD)	-0.3V	5.0V
Supply voltages (SPKVDDL, SPKVDDR)	-0.3V	6.0V
Voltage range digital inputs (DBVDD1 domain)	SUBGND - 0.3V	DBVDD1 + 0.3V
Voltage range digital inputs (DBVDD2 domain)	SUBGND - 0.3V	DBVDD2 + 0.3V
Voltage range digital inputs (DBVDD3 domain)	SUBGND - 0.3V	DBVDD3 + 0.3V
Voltage range digital inputs (DMICDATn)	SUBGND - 0.3V	MICVDD + 0.3V
Voltage range analogue inputs (INnLP, INnLN)	SUBGND - 0.3V	MICVDD + 0.3V
Voltage range analogue inputs (INnRP, INnRN)	SUBGND - 0.9V	MICVDD + 0.3V
Voltage range analogue inputs (HPOUT1FB1, HPOUT1FB2, HPOUTnFB)	SUBGND - 0.3V	SUBGND + 0.3V
Voltage range analogue inputs (MICDETn, GPSWA, GPSWB)	SUBGND - 0.3V	MICVDD + 0.3V
Voltage range analogue inputs (JACKDET, HPDETL, HPDETR)	CP1VOUT2N - 0.3V	AVDD + 0.3V
Ground (AGND, DGND, CPGND, SPKGNDL, SPKGNDR)	SUBGND - 0.3V	SUBGND + 0.3V
Operating temperature range, T_A	-40ºC	+85ºC
Operating junction temperature, T_J	-40ºC	+125ºC
Storage temperature after soldering	-65ºC	+150ºC

Notes:

1. DCVDD must not be powered if AVDD is not present.
2. The AVDD1 and AVDD2 pins should be tied together. The associated power domain is referred to as AVDD.
3. The AGND1 and AGND2 pins should be tied together. The associated ground domain is referred to as AGND.
4. The HPOUT1FBn and MICDETn functions share common pins. The Absolute Maximum Rating varies according to the applicable function of each pin.
5. CP1VOUT2N is an internal supply, generated by the WM8281 Charge Pump (CP1). The CP1VOUT2N voltage may vary between AGND and -CPVDD.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core) See notes 2, 3, 4	DCVDD	1.14	1.2	1.26	V
Digital supply range (I/O) See note 5	DBVDD1, DBVDD2, DBVDD3	1.62		3.6	V
LDO supply range See note 13	LDOVDD	1.71	1.8	1.89	V
Charge Pump supply range	CPVDD	1.71	1.8	1.89	V
Speaker supply range	SPKVDDL, SPKVDDR	2.4		5.5	V
Analogue supply range See notes 2, 6, 7	AVDD	1.71	1.8	1.89	V
Microphone Bias supply See note 8	MICVDD	0.9	2.5	3.78	V
Ground See note 1	DGND, AGND, CPGND, SPKGNDL, SPKGNDR, SUBGND		0		V
Power supply rise time See notes 9, 10, 11, 12	DCVDD	10		2000	µs
	All other supplies	10			
Operating temperature range	T_A	-40		85	°C

Notes:

1. The impedance between DGND, AGND, CPGND and SUBGND should be less than 0.1Ω.The impedance between SPKGNDL, SPKGNDR and SUBGND should be less than 0.2Ω.
2. AVDD must be supplied before or simultaneously to DCVDD. DCVDD must not be powered if AVDD is not present. There are no other power sequencing requirements.
3. An internal LDO (powered by LDOVDD) can be used to provide the DCVDD supply.
4. 'Sleep' mode is supported when DCVDD is below the limits noted, provided AVDD and DBVDD1 are present.
5. If the SLIMbus interface is enabled, then the maximum DBVDD1 voltage is 1.98V.
6. The AVDD1 and AVDD2 pins should be tied together. The associated power domain is referred to as AVDD.
7. The AGND1 and AGND2 pins should be tied together. The associated ground domain is referred to as AGND.
8. An internal Charge Pump and LDO (powered by CPVDD) provide the Microphone Bias supply; the MICVDD pin should not be connected to an external supply.
9. DCVDD and MICVDD minimum rise times do not apply when these domains are powered using the internal LDOs.
10. If DCVDD is supplied externally, and the rise time exceeds 2ms, then $\overline{\text{RESET}}$ must be asserted (low) during the rise, and held asserted until after DCVDD is within the recommended operating limits.
11. The specified minimum power supply rise times assume a minimum decoupling capacitance of 100nF per pin. However, Cirrus Logic strongly advises that the recommended decoupling capacitors are present on the PCB and that appropriate layout guidelines are observed.
12. The specified minimum power supply rise times also assume a maximum PCB inductance of 10nH between decoupling capacitor and pin.
13. When the internal LDO is used to provide the DCVDD supply, then the LDOVDD supply must be suitably rated for the inrush current at start-up and wake-up. In the typical configuration, using the internal LDO, and with the LDOVDD / CPVDD / AVDD domains connected to a single supply, a peak current capability of 500mA is required on this supply.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = 1.8V,

With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Input Signal Level (IN1L, IN1R, IN2L, IN2R, IN3L, IN3R)						
Full-scale input signal level (0dBFS output)	V_{INFS}	Single-ended PGA input, 0dB PGA gain		0.5 -6		V_{RMS} dBV
		Differential PGA input, 0dB PGA gain		1 0		V_{RMS} dBV

Notes:

1. The full-scale input signal level is also the maximum analogue input level, before clipping occurs.
2. The full-scale input signal level changes in proportion with AVDD. For differential input, it is calculated as AVDD / 1.8.
3. A $1.0V_{RMS}$ differential signal equates to $0.5V_{RMS}$/-6dBV per input.
4. A sinusoidal input signal is assumed.

Test Conditions

T_A = +25°C

With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Input Pin Characteristics (IN1L, IN1R, IN2L, IN2R, IN3L, IN3R)						
Input resistance	R_{IN}	Single-ended PGA input, All PGA gain settings	9	12		kΩ
		Differential PGA input, All PGA gain settings	18	24		
Input capacitance	C_{IN}				5	pF

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Programmable Gain Amplifiers (PGAs)						
Minimum programmable gain				0		dB
Maximum programmable gain				31		dB
Programmable gain step size		Guaranteed monotonic		1		dB

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Microphone Input Signal Level (DMICDAT1, DMICDAT2, DMICDAT3, DMICDAT4)						
Full-scale input signal level (0dBFS output)		0dB gain		-6		dBFS

Notes:

5. The digital microphone input signal level is measured in dBFS, where 0dBFS is a signal level equal to the full-scale range (FSR) of the PDM input. The FSR is defined as the amplitude of a 1kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively - this is the largest 1kHz sine wave that will fit in the digital output range without clipping. Note that, because the definition of FSR is based on a sine wave, the PDM data format can support signals larger than 0dBFS.

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Line / Headphone / Earpiece Output Driver (HPOUTnL, HPOUTnR)						
Load resistance		Normal operation, Single-ended mode	6			Ω
		Normal operation, Differential (BTL) mode	15			
		Device survival with load applied indefinitely	0			
Load capacitance		Direct connection, Single-ended mode			500	pF
		Direct connection, Differential (BTL) mode			200	
		Connection via 16Ω series resistor			2	nF
Speaker Output Driver (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN)						
Load resistance		Normal operation	4			Ω
		Device survival with load applied indefinitely	0			
Load capacitance					200	pF

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 2.5V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Line / Headphone / Earpiece Output Driver (HPOUTnL, HPOUTnR)						
DC offset at Load		Single-ended mode		0.1		mV
		Differential (BTL) mode		0.2		
Speaker Output Driver (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN)						
DC offset at Load				10		mV
SPKVDD leakage current				1		µA

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 2.5V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Input Paths (INnL, INnR) to ADC (Differential Input Mode, INn_MODE = 00)						
Signal to Noise Ratio (A-weighted)	SNR	48kHz sample rate	93	100		dB
		16kHz sample rate, (wideband voice)	100	106		
Total Harmonic Distortion	THD	-1dBV input		-89	-81	dB
Total Harmonic Distortion + Noise	THD+N	-1dBV input		-88		dB
Channel separation (Left/Right)				100		dB
Input-referred noise floor		A-weighted, PGA gain = +20dB		3.2		μV_{RMS}
Common mode rejection ratio	CMRR	PGA gain = +30dB	54	60		dB
		PGA gain = 0dB	60	70		
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		85		dB
		100mV (peak-peak) 10kHz		82		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		>120		dB
		100mV (peak-peak) 10kHz		70		
Analogue Input Paths (INnLP, INnRP) to ADC (Single-Ended Input Mode, INn_MODE = 01)						
Signal to Noise Ratio (A-weighted)	SNR	48kHz sample rate	91	96		dB
		16kHz sample rate, (wideband voice)		102		
Total Harmonic Distortion	THD	-7dBV input		-85	-78	dB
Total Harmonic Distortion + Noise	THD+N	-7dBV input		-84		dB
Channel separation (Left/Right)				100		dB
Input-referred noise floor		A-weighted, PGA gain = +20dB		3.2		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		77		dB
		100mV (peak-peak) 10kHz		50		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		90		dB
		100mV (peak-peak) 10kHz		50		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 2.5V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Line Output (HPOUTnL, HPOUTnR; Load = 10kΩ, 50pF)						
Full-scale output signal level	V_{OUT}	0dBFS input	1 0			Vrms dBV
Signal to Noise Ratio (A-weighted)	SNR	Output signal = 1Vrms	107	115		dB
		Output signal = 1Vrms, eDRE software enabled		120		
Total Harmonic Distortion	THD	0dBFS input		-92	-84	dB
Total Harmonic Distortion + Noise	THD+N	0dBFS input		-90		dB
Channel separation (Left/Right)				110		dB
Output noise floor		A-weighted, eDRE software enabled		0.8		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		80		dB
		100mV (peak-peak) 10kHz		72		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		>120		dB
		100mV (peak-peak) 10kHz		>120		
DAC to Headphone Output (HPOUTnL, HPOUTnR, R_L = 32Ω, Short Circuit Protection disabled)						
Maximum output power	P_O	0.1% THD+N		32		mW
Signal to Noise Ratio (A-weighted)	SNR	Output signal = 1Vrms	107	115		dB
		Output signal = 1Vrms, eDRE software enabled		121		
Total Harmonic Distortion	THD	P_O = 20mW		-89		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 20mW		-88		dB
Total Harmonic Distortion	THD	P_O = 5mW		-91	-84	dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 5mW		-88		dB
Channel separation (Left/Right)				94		dB
Output noise floor		A-weighted, eDRE software enabled		0.8		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		89		dB
		100mV (peak-peak) 10kHz		72		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		>120		dB
		100mV (peak-peak) 10kHz		>120		
DAC to Headphone Output (HPOUTnL, HPOUTnR, R_L = 16Ω, Short Circuit Protection disabled)						
Maximum output power	P_O	0.1% THD+N		42		mW
Signal to Noise Ratio (A-weighted)	SNR	Output signal = 1Vrms	107	115		dB
		Output signal = 1Vrms, eDRE software enabled		121		
Total Harmonic Distortion	THD	P_O = 20mW		-88		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 20mW		-87		dB
Total Harmonic Distortion	THD	P_O = 5mW		-88	-84	dB
Total Harmonic Distortion + Noise	THD+N	P_O = 5mW		-87		dB
Channel separation (Left/Right)				92		dB
Output noise floor		A-weighted, eDRE software enabled		0.8		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		89		dB
		100mV (peak-peak) 10kHz		72		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		>120		dB
		100mV (peak-peak) 10kHz		>120		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 2.5V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Earpiece Output (HPOUTnL, HPOUTnR, Mono Mode, R_L = 32Ω BTL, Short Circuit Protection disabled)						
Maximum output power	P_O	0.1% THD+N		106		mW
Signal to Noise Ratio (A-weighted)	SNR	Output signal = 1.41Vrms		117		dB
		Output signal = 1.41Vrms, eDRE software enabled		126		
Total Harmonic Distortion	THD	P_O = 75mW		-88		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 75mW		-86		dB
Total Harmonic Distortion	THD	P_O = 5mW		-89		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 5mW		-88		dB
Output noise floor		A-weighted		2.25		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		105		dB
		100mV (peak-peak) 10kHz		107		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		>120		dB
		100mV (peak-peak) 10kHz		>120		
DAC to Earpiece Output (HPOUTnL, HPOUTnR, Mono Mode, R_L = 16Ω BTL, Short Circuit Protection disabled)						
Maximum output power	P_O	0.1% THD+N		105		mW
Signal to Noise Ratio (A-weighted)	SNR	Output signal = 1.41Vrms		117		dB
		Output signal = 1.41Vrms, eDRE software enabled		126		
Total Harmonic Distortion	THD	P_O = 75mW		-86		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 75mW		-85		dB
Total Harmonic Distortion	THD	P_O = 5mW		-86		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 5mW		-85		dB
Output noise floor		A-weighted		2.25		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		105		dB
		100mV (peak-peak) 10kHz		112		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		>120		dB
		100mV (peak-peak) 10kHz		>120		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 2.5V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Speaker Output (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN; Load = 8Ω, 22µH, BTL)						
Maximum output power	P_O	SPKVDD = 5.0V, 1% THD+N		1.4		W
		SPKVDD = 4.2V, 1% THD+N		1.0		
		SPKVDD = 3.6V, 1% THD+N		0.7		
Signal to Noise Ratio	SNR	A-weighted, Output signal = 2.83Vrms	85	95		dB
Total Harmonic Distortion	THD	P_O = 1.0W		-40		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 1.0W		-40		dB
Total Harmonic Distortion	THD	P_O = 0.5W		-70	-59	dB
Total Harmonic Distortion + Noise	THD+N	P_O = 0.5W		-69		dB
Channel separation (Left/Right)				80		dB
Output noise floor		A-weighted		51.2	177	μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		76		dB
		100mV (peak-peak) 10kHz		68		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		72		dB
		100mV (peak-peak) 10kHz		55		
DAC to Speaker Output (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN; Load = 4Ω, 15µH, BTL)						
Maximum output power	P_O	SPKVDD = 5.0V, 1% THD+N		2.5		W
		SPKVDD = 4.2V, 1% THD+N		1.8		
		SPKVDD = 3.6V, 1% THD+N		1.3		
Signal to Noise Ratio	SNR	A-weighted, Output signal = 2.83Vrms		95		dB
Total Harmonic Distortion	THD	P_O = 1.0W		-70		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 1.0W		-69		dB
Total Harmonic Distortion	THD	P_O = 0.5W		-69		dB
Total Harmonic Distortion + Noise	THD+N	P_O = 0.5W		-68		dB
Channel separation (Left/Right)				80		dB
Output noise floor		A-weighted		51.2		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		76		dB
		100mV (peak-peak) 10kHz		68		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		72		dB
		100mV (peak-peak) 10kHz		55		

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input / Output (except DMICDATn and DMICCLKn) **Digital I/O is referenced to DBVDD1, DBVDD2 or DBVDD3. See "Pin Description" for the domain applicable to each pin.**						
Input HIGH Level	V_{IH}	V_{DBVDDn} = 1.8V ±10%	0.75 × V_{DBVDDn}			V
		V_{DBVDDn} = 2.5V ±10%	0.8 × V_{DBVDDn}			
		V_{DBVDDn} = 3.3V ±10%	0.7 × V_{DBVDDn}			
Input LOW Level	V_{IL}	V_{DBVDDn} = 1.8V ±10%			0.3 × V_{DBVDDn}	V
		V_{DBVDDn} = 2.5V ±10%			0.25 × V_{DBVDDn}	
		V_{DBVDDn} = 3.3V ±10%			0.2 × V_{DBVDDn}	
Note that digital input pins should not be left unconnected or floating.						
Output HIGH Level (I_{OH} = 1mA)	V_{OH}	V_{DBVDDn} = 1.8V ±10%	0.75 × V_{DBVDDn}			V
		V_{DBVDDn} = 2.5V ±10%	0.65 × V_{DBVDDn}			
		V_{DBVDDn} = 3.3V ±10%	0.7 × V_{DBVDDn}			
Output LOW Level (I_{OL} = 1mA)	V_{OL}	V_{DBVDDn} = 1.8V ±10%			0.25 × V_{DBVDDn}	V
		V_{DBVDDn} = 2.5V ±10%			0.3 × V_{DBVDDn}	
		V_{DBVDDn} = 3.3V ±10%			0.15 × V_{DBVDDn}	
Input capacitance					5	pF
Input leakage			-10		10	µA
Pull-up / pull-down resistance (where applicable)			36		50	kΩ
Digital Microphone Input / Output (DMICDATn and DMICCLKn) **DMICDATn and DMICCLKn are each referenced to a selectable supply, V_{SUP}, according to the INn_DMIC_SUP registers**						
DMICDATn input HIGH Level	V_{IH}		0.65 × V_{SUP}			V
DMICDATn input LOW Level	V_{IL}				0.35 × V_{SUP}	V
DMICCLKn output HIGH Level	V_{OH}	I_{OH} = 1mA	0.8 × V_{SUP}			V
DMICCLKn output LOW Level	V_{OL}	I_{OL} = -1mA			0.2 × V_{SUP}	V
Input capacitance				25		pF
Input leakage			-1		1	µA
General Purpose Input / Output (GPIOn)						
Clock output frequency		GPIO pin configured as OPCLK or FLL output			50	MHz
General Purpose Switch The GPSWA pin should be positive-biased with respect to GPSWB. The GPSWB pin voltage must not exceed GPSWA + 0.3V.						
Switch resistance	$R_{DS(ON)}$	Switch closed, I=1mA			40	Ω
Switch resistance	$R_{DS(OFF)}$	Switch open	100			MΩ

Test Conditions

fs ≤ 48kHz

With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Decimation Filters						
Passband		+/- 0.05dB	0		0.454 fs	
		-6dB		0.5 fs		
Passband ripple					+/- 0.05	dB
Stopband			0.546 fs			
Stopband attenuation		f > 0.546 fs	85			dB
Group delay					2	ms
DAC Interpolation Filters						
Passband		+/- 0.05dB	0		0.454 fs	
		-6dB		0.5 fs		
Passband ripple					+/- 0.05	dB
Stopband			0.546 fs			
Stopband attenuation		f > 0.546 fs	85			dB
Group delay					1.5	ms

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 2.5V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Bias (MICBIAS1, MICBIAS2, MICBIAS3) Note - No capacitor on MICBIASn Note - In regulator mode, it is required that V_{MICVDD} - $V_{MICBIAS}$ > 200mV						
Minimum Bias Voltage	$V_{MICBIAS}$	Regulator mode (MICBn_BYPASS=0) Load current ≤ 1.0mA		1.5		V
Maximum Bias Voltage				2.8		V
Bias Voltage output step size				0.1		V
Bias Voltage accuracy			-5%		+5%	V
Bias Current		Regulator mode (MICBn_BYPASS=0), V_{MICVDD} - $V_{MICBIAS}$ >200mV			2.4	mA
		Bypass mode (MICBn_BYPASS=1)			5.0	
Output Noise Density		Regulator mode (MICBn_BYPASS=0), MICBn_LVL = 4h, Load current = 1mA, Measured at 1kHz		100		nV/√Hz
Integrated noise voltage		Regulator mode (MICBn_BYPASS=0), MICBn_LVL = 4h, Load current = 1mA, 100Hz to 7kHz, A-weighted		5		µVrms
Power Supply Rejection Ratio (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz	100			dB
		100mV (peak-peak) 10kHz	80			
Load capacitance		Regulator mode (MICBn_BYPASS=0), MICBn_EXT_CAP=0			50	pF
		Regulator mode (MICBn_BYPASS=0), MICBn_EXT_CAP=1	1.8	4.7		µF
Output discharge resistance		MICBn_ENA=0, MICBn_DISCH=1		2		kΩ

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 2.5V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
External Accessory Detect						
Load impedance detection range Detection via HPDETL pin (ACCDET_MODE=001) or HPDETR pin (ACCDET_MODE=010)		HP_IMPEDANCE_ RANGE=00	4		30	Ω
		HP_IMPEDANCE_ RANGE=01	8		100	
		HP_IMPEDANCE_ RANGE=10	100		1000	
		HP_IMPEDANCE_ RANGE=11	1000		10000	
Load impedance detection range Detection via MICDET1 or MICDET2 pin (ACCDET_MODE=100)			400		6000	Ω
Load impedance detection accuracy (result derived from HP_DACVAL, ACCDET_MODE=001 or 010)		HP_IMPEDANCE_ RANGE=01 or 10	-5		+5	%
		HP_IMPEDANCE_ RANGE=00 or 11	-10		+10	
Load impedance detection accuracy (result derived from HP_LVL, ACCDET_MODE= 001, 010 or 100)			-20		+20	%
Load impedance detection range Detection via MICDET1 or MICDET2 pin (ACCDET_MODE=000). 2.2kΩ (2%) MICBIAS resistor. Note these characteristics assume no other component is connected to MICDETn. See "Applications Information" for recommended external components when a typical microphone is present.		for MICD_LVL[0] = 1	0		3	Ω
		for MICD_LVL[1] = 1	17		21	
		for MICD_LVL[2] = 1	36		44	
		for MICD_LVL[3] = 1	62		88	
		for MICD_LVL[4] = 1	115		160	
		for MICD_LVL[5] = 1	207		381	
		for MICD_LVL[8] = 1	475		30000	
Jack Detection input threshold voltage (JACKDET)	$V_{JACKDET}$	Jack insertion		0.5 x AVDD		V
		Jack removal		0.85 x AVDD		