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WM8310

Processor Power Management Subsystem

DESCRIPTION

The WM8310 is an integrated power-management subsystem which provides a cost-effective, flexible, single-chip solution for power management. It is specifically targeted at the requirements of a range of low-power portable consumer products, but is suitable to any application with a multimedia processor. The WM8310 is designed to operate as a system PMIC supporting a variety of industry-standard processors and accessories in a wide range of consumer multimedia applications.

The start-up behaviour and configuration is fully programmable in an integrated OTP non-volatile memory. This highly flexible solution helps reduce time-to-market, as changing application requirements can be very easily accommodated in the OTP. The InstantConfig™ interface enables an external EEPROM to configure the WM8310.

The WM8310 power management subsystem comprises of four programmable DC-DC converters, eleven LDO regulators (four of which are low-noise for supplying sensitive analogue subsystems). The integrated OTP bootstrap circuitry controls the start-up sequencing and voltages of the converters and regulators as well as the sequencing of system clocks.

WM8310 can be powered from a battery, a wall adaptor or from a USB power source. An on-chip regulator provides power for always-on PMIC functions such as register map and the RTC. The device provides autonomous backup battery switchover. A low-power LDO is included to support 'Alive' processor power domains external to the WM8310.

A linear on-chip battery charger supports trickle charging and constant current / constant voltage charging of single-cell lithium-ion / lithium-polymer batteries. The charge current, termination voltage, and charger time-out are programmable. WM8310 detects and handles battery fault conditions with a minimum of system software involvement.

A 12-bit Auxiliary ADC supports a wide range of applications for internal as well as external analogue sampling, such as voltage detection and temperature measurement.

WM8310 includes a crystal oscillator, an internal RC oscillator and Frequency Locked Loop (FLL) to generate clock signals for autonomous system start-up and processor clocking. A Secure Real-time Clock (S-RTC) and alarm function is included, capable of system wake-up from low-power modes. A watchdog function is provided to ensure system integrity.

To maximise battery life, highly-granular power management enables each function in the WM8310 subsystem to be independently powered down through a control interface or alternatively through register and OTP-configurable GPIOs. The device offers a standby power consumption of <10uA, making it particularly suitable for portable applications.

The WM8310 is supplied in a 7x7mm 169-ball BGA package, ideal for use in portable systems. The WM8310 forms part of the Wolfson series of audio and power management solutions.

FEATURES

Power Management

- 2 x DC-DC synchronous buck converters (0.6V - 1.8V, 1.2A, DVS)
- 1 x DC-DC synchronous buck converter (0.85V - 3.4V, 1A)
- 1 x DC-DC boost converter (up to 30V, up to 90mA)
- 1 x LDO regulator (0.9V - 3.3V, 300mA, 1Ω)
- 2 x LDO regulators (0.9V - 3.3V, 200mA, 1Ω)
- 3 x LDO regulators (0.9V - 3.3V, 100mA, 2Ω)
- 2 x Low-noise LDO regulators (1.0V - 3.5V, 200mA, 1Ω)
- 2 x Low-noise LDO regulators (1.0V - 3.5V, 150mA, 2Ω)
- 1 x 'Alive' LDO regulator (0.8V – 1.55V, up to 25mA)

Backlight LED Current Sinks

- 2 x programmable constant current sinks, suitable for multi-LED display backlight control

Battery Charger

- Programmable single-cell lithium-ion / lithium-polymer battery charger (1A max charge current)
- Battery monitoring for temperature and voltage
- Autonomous backup battery charging and switching

System Control

- I^2C or SPI compatible primary control interface
- Interrupt based feedback communication scheme
- Watchdog timer and system reset control
- Autonomous power sequencing and fault detection
- Intelligent power path and power source selection
- OTP memory bootstrap configuration function

Additional Features

- Auxiliary ADC for multi-function analogue measurement
- 128-bit pseudo-random unique ID
- Secure Real-Time Clock with wake-up alarm
- 12 x configurable multi-function (GPIO) pins
- Comprehensive clocking scheme: low-power 32kHz RTC crystal oscillator, Frequency Locked Loop, GPIO clock output and 4MHz RC clock for power management
- System LED outputs indicating power state, battery charger or fault status
- Selectable USB current limiting up to 1.8A (in accordance with USB Battery Charging specification Rev 1.1)

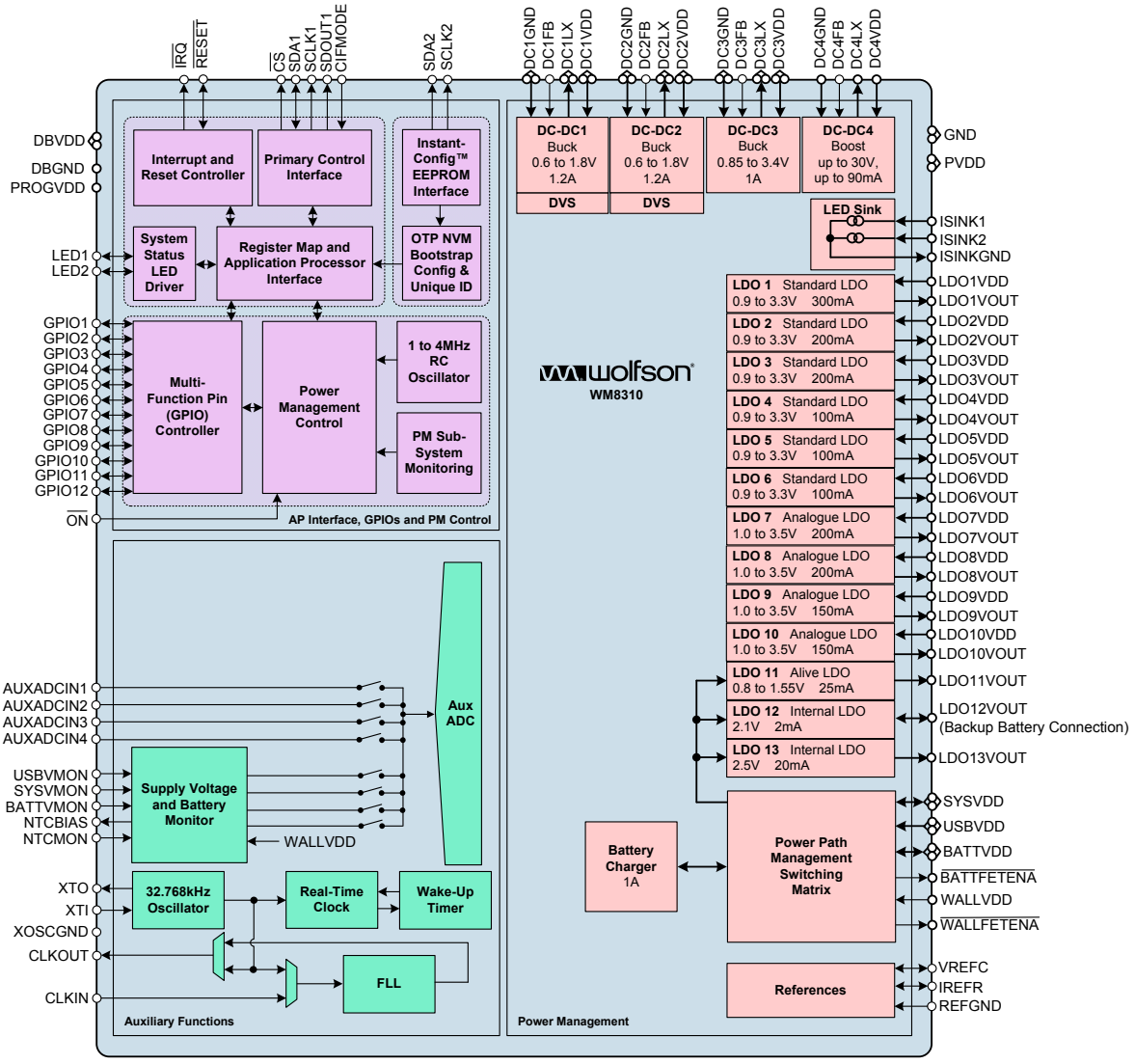
Package Options

- 7x7mm, 169-ball BGA package, 0.5mm ball pitch

APPLICATIONS

- Portable Media Players
- Portable Navigation Devices
- Cellular Handsets
- Electronic Books
- Electronic Gaming Devices

BLOCK DIAGRAM



TYPICAL APPLICATIONS

The WM8310 is designed as a system PMIC device that manages multiple power supply paths (wall adapter, USB, battery) and generates configurable DC supplies to power processors and associated peripherals within a system. The WM8310 provides three DC-DC synchronous buck (step-down) converters and one DC-DC boost (step-up) converter. Eleven LDO regulators provide a high degree of flexibility to provide power to multiple devices, with the capability to power-up and power-down different circuits independently.

Two of the DC-DC buck converters incorporate Wolfson's BuckWise™ technology specifically designed to handle rapid changes in load current; programmable slew rate DVS is also provided, as required by modern application processors. Selectable operating modes on all of the DC-DC converters allow each converter to be optimally configured for light, heavy or transient load conditions. Flexible operating configurations allow the converters to be tailored for minimum PCB area, maximum performance, or for maximum efficiency. The analogue LDOs provide low-noise outputs suitable for powering sensitive circuits such as RF / Wi-Fi / bluetooth radio applications.

The WM8310 powers up the converters and LDOs according to a programmable sequence. A configurable 'SLEEP' state is also available, providing support for an alternate configuration, typically for low-power / standby operation. The power control sequences and many other parameters can be stored in an integrated user-configurable OTP (One-Time Programmable) memory or may be loaded from an external memory. The WM8310 supports the programming and verification of the integrated OTP memory.

The WM8310 provides power path management which seamlessly switches between wall adapter, USB and battery power sources according to the prevailing conditions. A backup power source is also supported in order to maintain the Real Time Clock (RTC) in the absence of any other supplies. The WM8310 provides a configurable battery charger for the main battery, powered from either the wall adapter or USB supplies. The backup power source is maintained using a constant-voltage output from the WM8310.

Programmable GPIO pins may be configured as hardware inputs for general use or for selecting different power management configurations. As outputs, the GPIOs can provide indications of the device status, or may be used as control signals for other power management circuits. The WM8310 also provides two LED drivers, which can be controlled manually or configured as status indicators for the OTP memory programmer, operating power state or battery charger.

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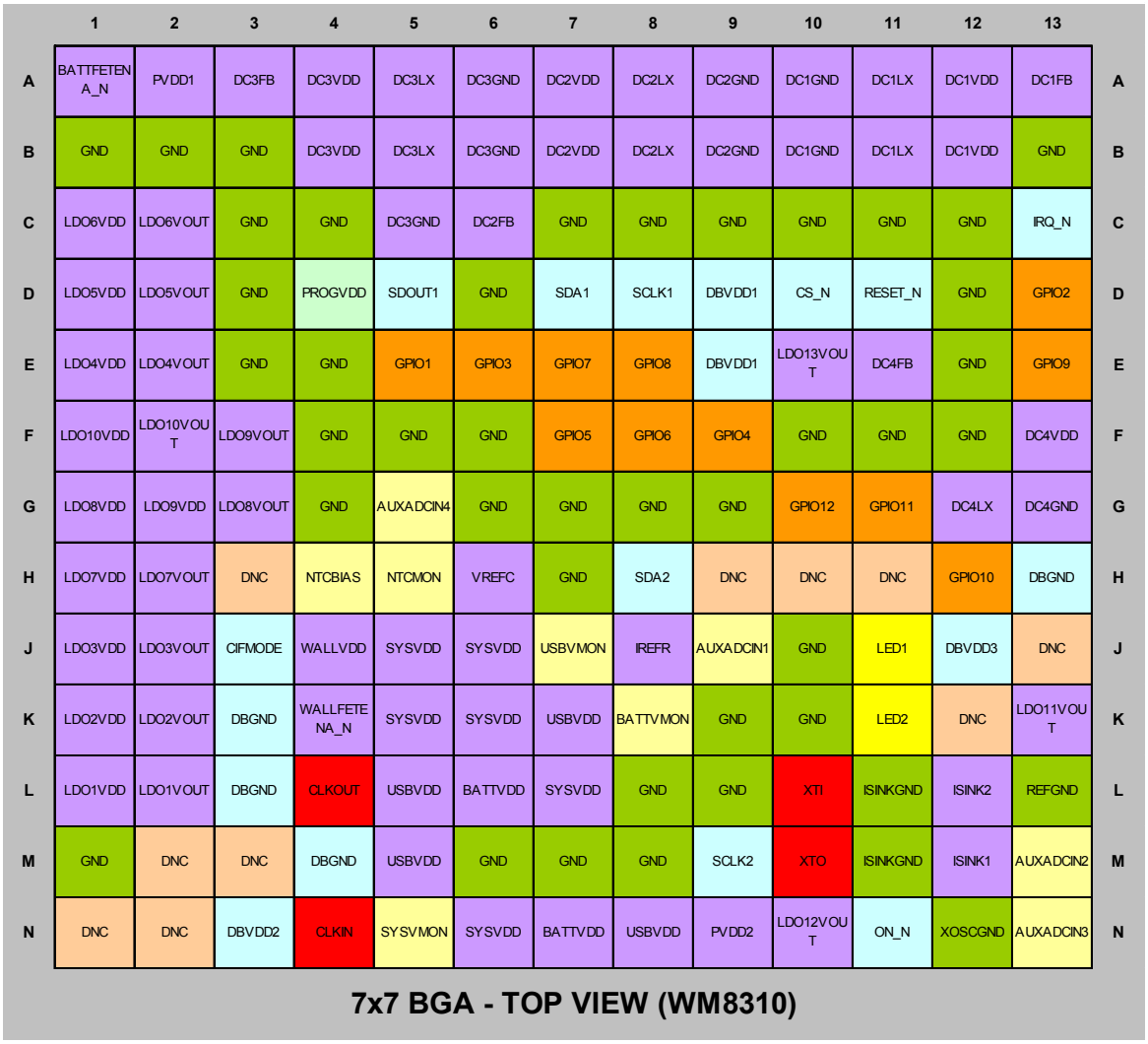
1 PIN CONFIGURATION



	1	2	3	4	5	6	7	8	9	10	11	12	13	
A	BATTFETENA_N	PVDD1	DC3FB	DC3VDD	DC3LX	DC3GND	DC2VDD	DC2LX	DC2GND	DC1GND	DC1LX	DC1VDD	DC1FB	A
B	GND	GND	GND	DC3VDD	DC3LX	DC3GND	DC2VDD	DC2LX	DC2GND	DC1GND	DC1LX	DC1VDD	GND	B
C	LDO6VDD	LDO6VOUT	GND	GND	DC3GND	DC2FB	GND	GND	GND	GND	GND	GND	IRQ_N	C
D	LDO5VDD	LDO5VOUT	GND	PROGVDD	SDOUT1	GND	SDA1	SCLK1	DBVDD1	CS_N	RESET_N	GND	GPIO2	D
E	LDO4VDD	LDO4VOUT	GND	GND	GPIO1	GPIO3	GPIO7	GPIO8	DBVDD1	LDO13VOUT	DC4FB	GND	GPIO9	E
F	LDO10VDD	LDO10VOUT	LDO9VOUT	GND	GND	GND	GPIO5	GPIO6	GPIO4	GND	GND	GND	DC4VDD	F
G	LDO8VDD	LDO9VDD	LDO8VOUT	GND	AUXADCIN4	GND	GND	GND	GND	GPIO12	GPIO11	DC4LX	DC4GND	G
H	LDO7VDD	LDO7VOUT	DNC	NTCBIAS	NTCMON	VREFC	GND	SDA2	DNC	DNC	DNC	GPIO10	DBGND	H
J	LDO3VDD	LDO3VOUT	CIFMODE	WALLVDD	SYSVDD	SYSVDD	USBVMON	IREFR	AUXADCIN1	GND	LED1	DBVDD3	DNC	J
K	LDO2VDD	LDO2VOUT	DBGND	WALLFETENA_N	SYSVDD	SYSVDD	USBVDD	BATTVMON	GND	GND	LED2	DNC	LDO11VOUT	K
L	LDO1VDD	LDO1VOUT	DBGND	CLKOUT	USBVDD	BATTVDD	SYSVDD	GND	GND	XTI	ISINKGND	ISINK2	REFGND	L
M	GND	DNC	DNC	DBGND	USBVDD	GND	GND	GND	SCLK2	XTO	ISINKGND	ISINK1	AUXADCIN2	M
N	DNC	DNC	DBVDD2	CLKIN	SYSVMON	SYSVDD	BATTVDD	USBVDD	PVDD2	LDO12VOUT	ON_N	XOSCGND	AUXADCIN3	N

7x7 BGA - TOP VIEW (WM8310)

2 ORDERING INFORMATION

ORDER CODE	OTP	TEMPERATURE RANGE (T_A)	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8310CGEB/V	Unprogrammed	-40°C to +85°C	169-ball (7 x 7mm) (Pb-free)	MSL3	260°C
WM8310CGEB/RV	Unprogrammed	-40°C to +85°C	169-ball (7 x 7mm) (Pb-free, tape and reel)	MSL3	260°C
WM8310CGEBxxx/RV*	Custom	-40°C to +85°C	169-ball (7 x 7mm) (Pb-free, tape and reel) **	MSL3	260°C

Note:

Reel quantity = 2200

* xxx = Unique OTP part number

* Custom OTP minimum order quantity 22,000

3 PIN DESCRIPTION

Notes:

1. Pins are sorted by functional groups.
2. The power domain associated with each pin is noted; VPMIC is the domain powered by LDO12 for the 'always-on' functions internal to the WM8310.
3. Note that an external level-shifter may be required when interfacing between different power domains.

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION
Auxiliary ADC				
J7	USBVMON	Analogue Input	USBVDD	USBVDD Supply Voltage Monitor
N5	SYSVMON	Analogue Input	SYSVDD	SYSVDD Supply Voltage Monitor
K8	BATTVMON	Analogue Input	BATTVDD	BATTVDD Supply Voltage Monitor
J9	AUXADCIN1	Analogue Input/Output	SYSVDD	Auxiliary Analogue Input 1 / Battery Charge Current Monitor Output
M13	AUXADCIN2	Analogue Input		Auxiliary Analogue Input 2
N13	AUXADCIN3	Analogue Input		Auxiliary Analogue Input 3
G5	AUXADCIN4	Analogue Input	DBVDD	Auxiliary Analogue Input 4
Clocking and Real Time Clock				
M10	XTO	Analogue Output	VPMIC	Crystal Drive Output
L10	XTI	Analogue Input		Crystal Drive Input or 32.768kHz CMOS Clock Input
N12	XOSCGND	Supply		Crystal Oscillator Ground
L4	CLKOUT	Digital Output	DBVDD	CMOS Clock Output Configurable Open Drain / CMOS mode. (External 4.7kΩ pull-up recommended in Open Drain mode.)
N4	CLKIN	Digital Input		CMOS FLL Clock Input
General Purpose Input / Output				
E5	GPIO1	Digital I/O	DBVDD or VPMIC	GPIO Pin 1 Selectable pull-up/pull-down.
D13	GPIO2	Digital I/O		GPIO Pin 2 Selectable pull-up/pull-down.
E6	GPIO3	Digital I/O		GPIO Pin 3 Selectable pull-up/pull-down.
F9	GPIO4	Digital I/O	DBVDD or SYSVDD	GPIO Pin 4 Selectable pull-up/pull-down.
F7	GPIO5	Digital I/O		GPIO Pin 5 Selectable pull-up/pull-down.
F8	GPIO6	Digital I/O		GPIO Pin 6 Selectable pull-up/pull-down.
E7	GPIO7	Digital I/O	DBVDD or VPMIC	GPIO Pin 7 Selectable pull-up/pull-down.
E8	GPIO8	Digital I/O		GPIO Pin 8 Selectable pull-up/pull-down.
E13	GPIO9	Digital I/O		GPIO Pin 9 Selectable pull-up/pull-down.
H12	GPIO10	Digital I/O	DBVDD or SYSVDD	GPIO Pin 10 Selectable pull-up/pull-down.
G11	GPIO11	Digital I/O		GPIO Pin 11 Selectable pull-up/pull-down.
G10	GPIO12	Digital I/O		GPIO Pin 12 Selectable pull-up/pull-down.

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION	
Processor Interface and IC Control					
N11	$\overline{ON}$	Digital Input	VPMIC	ON Request Pin (Internal pull-up)	
D11	$\overline{RESET}$	Digital I/O	DBVDD	System Reset Input and Open Drain Output. (Internal pull-up)	
C13	$\overline{IRQ}$	Digital Output	DBVDD	PMIC Interrupt Flag Output. Configurable Open Drain / CMOS mode. (Internal pull-up in Open Drain mode.)	
J3	CIFMODE	Digital Input	DBVDD	Primary Control Interface Mode Select: 0 = I^2C Compatible Control Interface Mode 1 = SPI Compatible Control Interface Mode	
				SPI Compatible Control Interface Mode	*I^2C Compatible Control Interface Mode*
D5	SDOUT1	Digital Output	DBVDD	Control Interface Serial Data Out. Open Drain output; external 4.7kΩ pull-up recommended.	No Function
D8	SCLK1	Digital Input		Control Interface Serial Clock	Control Interface Serial Clock
D7	SDA1	Digital I/O		Control Interface Serial Data In	Control Interface Serial Data Input and Open Drain Output. External 4.7kΩ pull-up recommended. (Output can extend above DBVDD domain.)
D10	$\overline{CS}$	Digital Input		Control Interface Chip Select	I^2C Address Select: 0 = 68h 1 = 6Ch
M9	SCLK2	Digital I/O	VPMIC	Control Interface Serial Clock for external InstantConfig™ EEPROM (ICE) (Internal pull-down)	
H8	SDA2	Digital I/O		Control Interface Serial Data to/from external InstantConfig™ EEPROM (ICE (Internal pull-down)	
D9, E9	DBVDD1	Supply		Digital Buffer Supply	
N3	DBVDD2	Supply		Digital Buffer Supply	
J12	DBVDD3	Supply		Digital Buffer Supply	
H13, K3, L3, M4	DBGND	Supply		Digital Buffer Ground	
OTP Memory					
D4	PROGVDD	Supply		High-voltage input for OTP programming.	

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION
DC-DC Converters and LDO Regulators				
B1, B2, B3, B13, C3, C4, C7, C8, C9, C10, C11, C12, D3, D6, D12, E3, E4, E12, F4, F5, F6, F10, F11, F12, G4, G6, G7, G8, G9, H7, J10, K9, K10, L8, L9, M1, M6, M7, M8	GND	Supply		Ground
A2	PVDD1	Supply		Internal VDD supply; Connect to SYSVDD
N9	PVDD2	Supply		
A10, B10	DC1GND	Supply		DC-DC1 Power Ground
A13	DC1FB	Analogue Input	DC1VDD	DC-DC1 Feedback Pin
A11, B11	DC1LX	Analogue I/O		DC-DC1 Inductor Connection
A12, B12	DC1VDD	Supply		DC-DC1 Power Input (connect to SYSVDD supply)
A9, B9	DC2GND	Supply		DC-DC2 Power Ground
C6	DC2FB	Analogue Input	DC2VDD	DC-DC2 Feedback Pin
A8, B8	DC2LX	Analogue I/O		DC-DC2 Inductor Connection
A7, B7	DC2VDD	Supply		DC-DC2 Power Input (connect to SYSVDD supply)
A6, B6, C5	DC3GND	Supply		DC-DC3 Power Ground
A3	DC3FB	Analogue Input	DC3VDD	DC-DC3 Feedback Pin
A5, B5	DC3LX	Analogue I/O		DC-DC3 Inductor Connection
A4, B4	DC3VDD	Supply		DC-DC3 Power Input (connect to SYSVDD supply)
G13	DC4GND	Supply		DC-DC4 Power Ground
E11	DC4FB	Analogue Input	DC4VDD	DC-DC4 Feedback Connection
G12	DC4LX	Analogue I/O		DC-DC4 Inductor Connection
F13	DC4VDD	Supply		DC-DC4 Power Input (connect to SYSVDD supply)
L1	LDO1VDD	Supply		LDO1 Power Input (must be ≤ SYSVDD supply)
L2	LDO1VOUT	Analogue Output	LDO1VDD	LDO1 Power Output
K1	LDO2VDD	Supply		LDO2 Power Input (must be ≤ SYSVDD supply)
K2	LDO2VOUT	Analogue Output	LDO2VDD	LDO2 Power Output
J1	LDO3VDD	Supply		LDO3 Power Input (must be ≤ SYSVDD supply)
J2	LDO3VOUT	Analogue Output	LDO3VDD	LDO3 Power Output
E1	LDO4VDD	Supply		LDO4 Power Input (must be ≤ SYSVDD supply)
E2	LDO4VOUT	Analogue Output	LDO4VDD	LDO4 Power Output
D1	LDO5VDD	Supply		LDO5 Power Input (must be ≤ SYSVDD supply)
D2	LDO5VOUT	Analogue Output	LDO5VDD	LDO5 Power Output
C1	LDO6VDD	Supply		LDO6 Power Input (must be ≤ SYSVDD supply)
C2	LDO6VOUT	Analogue Output	LDO6VDD	LDO6 Power Output
H1	LDO7VDD	Supply		LDO7 Power Input
H2	LDO7VOUT	Analogue Output	LDO7VDD	LDO7 Power Output
G1	LDO8VDD	Supply		LDO8 Power Input

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION
G3	LDO8VOUT	Analogue Output	LDO8VDD	LDO8 Power Output
G2	LDO9VDD	Supply		LDO9 Power Input
F3	LDO9VOUT	Analogue Output	LDO9VDD	LDO9 Power Output
F1	LDO10VDD	Supply		LDO10 Power Input
F2	LDO10VOUT	Analogue Output	LDO10VDD	LDO10 Power Output
K13	LDO11VOUT	Analogue Output	PVDD	LDO11 (Alive) Power Output
N10	LDO12VOUT	Analogue I/O	PVDD	LDO12 (Internal VPMIC) Output; Backup battery supply input / output
E10	LDO13VOUT	Analogue I/O	PVDD	LDO13 (Internal INTVDD) Output; not for general use
Current Sinks				
M12	ISINK1	Analogue Output	SYSVDD	LED String Current Sink 1
L12	ISINK2	Analogue Output		LED String Current Sink 2
L11, M11	ISINKGND	Supply		LED String Current Sink Ground
Voltage and Current References				
H6	VREFC	Analogue I/O	VPMIC	Voltage Reference capacitor connection point
J8	IREFR	Analogue I/O		Current Reference resistor connection point
L13	REFGND	Supply		Reference Ground
Power Path Management				
J5, J6 K5, K6, L7, N6	SYSVDD	Supply		System VDD Supply
K7, L5, M5, N8	USBVDD	Supply		USB VDD Supply
L6, N7	BATTVDD	Supply		Primary Battery Supply
A1	$\overline{\text{BATTFETENA}}$	Digital Output	PVDD	External Battery FET Driver
J4	WALLVDD	Supply		Wall VDD Supply/Sense
K4	$\overline{\text{WALLFETENA}}$	Digital Output	highest VDD supply	External Wall FET Driver. Power domain is the highest out of WALLVDD, USBVDD or BATTVDD.
H4	NTCBIAS	Analogue Output	VPMIC	Battery NTC Temperature Monitor Supply
H5	NTCMON	Analogue Input		Battery NTC Temperature Monitor Voltage Sense Input
Status LED Drivers				
J11	LED1	Digital Output	SYSVDD	Status LED Driver 1. Open Drain Output
K11	LED2	Digital Output		Status LED Driver 2. Open Drain Output
Do Not Connect				
H3, H9, H10, H11, J13, K12, M2, M3, N1, N2	DNC			Do Not Connect

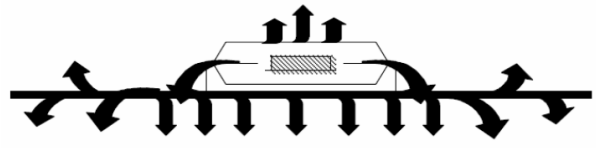
4 THERMAL CHARACTERISTICS

Thermal analysis must be performed in the intended application to prevent the WM8310 from exceeding maximum junction temperature. Several contributing factors affect thermal performance most notably the physical properties of the mechanical enclosure, location of the device on the PCB in relation to surrounding components and the number of PCB layers. Connecting the GND balls through thermal vias and into a large ground plane will aid heat extraction.

Three main heat transfer paths exist to surrounding air:

- Package top to air (convection and radiation).
- Package bottom to PCB (convection and radiation).
- Package leads to PCB (conduction).

(Note that radiation is not normally significant at the moderate temperatures experienced in typical applications.)



The temperature rise T_R is given by $T_R = P_D * \Theta_{JA}$

- P_D is the power dissipated by the device.
- Θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature and is therefore a measure of heat transfer from the die to surrounding air.
- For WM8310, Θ_{JA} = 45°C/W
- The quoted Θ_{JA} is based on testing to the EIA/JEDEC-51-2 test environment (ie. $1ft^3$ box, still air, with specific PCB stack-up and tracking rules). Note that this is not guaranteed to reflect all typical end applications.

The junction temperature T_J is given by $T_J = T_A + T_R$

- T_A, is the ambient temperature.

The worst case conditions are when the WM8310 is operating in a high ambient temperature, and under conditions which cause high power dissipation, such as the DC-DC converters operating at low supply voltage, high duty cycle and high output current. Under such conditions, it is possible that the heat dissipated could cause the maximum junction temperature of the device to be exceeded. Care must be taken to avoid this situation. An example calculation of the junction temperature is given below.

- P_D = 500mW (example figure)
- Θ_{JA} = 45°C/W
- $T_R = P_D * \Theta_{JA}$ = 22.5°C
- T_A = 85°C (example figure)
- $T_J = T_A + T_R$ = 107.5°C

The minimum and maximum operating junction temperatures for the WM8310 are quoted in Section 5. The maximum junction temperature is 125°C. Therefore, the junction temperature in the above example is within the operating limits of the WM8310.

5 ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The WM8310 has been classified as MSL3.

CONDITION	MIN	MAX
OTP Programming Supply (PROGVDD)	-0.3V	7.0V
BATTVDD, WALLVDD and USBVDD supplies	-0.3V	7.0V
Input voltage for LDO regulators	-0.3V	7.0V
Input voltage for DC-DC converters	-0.3V	7.0V
Digital buffer supply (DBVDD1, DBVDD2, DBVDD3)	-0.3V	4.5V
Voltage range for digital inputs	-0.3V	DBVDD + 0.3V
Operating Temperature Range, T_A	-40°C	+85°C
Junction Temperature, T_J	-40°C	+125°C
Thermal Impedance Junction to Ambient, θ_{JA}		45°C/W
Storage temperature prior to soldering	30°C max / 60% RH max	
Storage temperature after soldering	-65°C	+150°C
Soldering temperature (10 seconds)		+260°C
Note: These ratings assume that all ground pins are at 0V.		

6 RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Wall Input power source	WALLVDD	4.3		5.5	V
Battery Input power source	BATTVDD	2.7		5.5	V
USB Input power source	USBVDD	4.3		5.5	V
Digital buffer supply	DBVDD1, DBVDD2, DBVDD3	1.71		3.6	V
OTP Programming Supply (see note)	PROGVDD	6.25	6.5	6.75	V
	LDO12VOUT		3.3		V
Ground	GND, DC1GND, DC2GND, DC3GND, DC4GND, DBGND, XOSCGND, REFGND		0		V

Note:
The OTP Programming Supply PROGVDD should only be present when programming the OTP. At other times, this pin should be left unconnected. The LDO12VOUT must be overdriven by an external supply when programming the OTP. At other times, the voltage at this pin is driven by the internal circuits of the WM8310.

7 ELECTRICAL CHARACTERISTICS

7.1 DC-DC SYNCHRONOUS BUCK CONVERTERS

DC-DC1 and DC-DC2

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.2V, MODE = FCCM[1], T_J = -40°C to +125°C; typical values are at T_J = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}	V_{IN} = SYSVDD	2.7		5.5	V
Programmable Output Voltage	V_{OUT}	F_{SW} = 2MHz	0.6		1.8	V
		F_{SW} = 4MHz	0.6		1.4	
V_{OUT} Step Size	V_{OUT_STEP}			12.5		mV
V_{OUT} Accuracy	V_{OUT_ACC}	V_{IN} = 2.7V to 5.5V, I_{OUT} = 0mA to 1200mA	-3		3	%
Undervoltage margin		0.6V ≤ V_{OUT} < 0.9V		50		mV
		0.9V ≤ V_{OUT} < 1.3V		80		
		1.3V ≤ V_{OUT} ≤ 1.8V		100		
Overvoltage margin		0.6V ≤ V_{OUT} ≤ 1.8V		100		mV
Output Current	I_{OUT}	FCCM[1] and Auto (CCM/DCM with PS[2]) Modes	0		1200	mA
		Hysteretic Mode	0		150	
		LDO Mode	0		10	
P-channel Current Limit	I_{P_LIM}	F_{SW} = 2MHz		1800		mA
		F_{SW} = 4MHz		2000		
Quiescent Current	I_Q	I_{OUT} = 0mA, FCCM[1] and Auto (CCM/DCM with PS[2]) Modes (excluding switching losses)		500		µA
		I_{OUT} = 0mA, Hysteretic Mode		70		
		I_{OUT} = 0mA, LDO Mode		25		
Shutdown Current	I_{SD}	DC*m*_ENA = 0		0.01		µA
P-channel On Resistance	R_{DSP}	V_{IN} = V_{GS} = 3.8V, I_{DCmLX} = 100mA		140		mΩ
N-channel On Resistance	R_{DSN}	V_{IN} = V_{GS} = 3.8V, I_{DCmLX} = -100mA		130		mΩ
Switching Frequency	F_{SW}	DC*m*_FREQ = 01		2		MHz
		DC*m*_FREQ = 11		4		

Notes:

1. Forced Continuous Conduction Mode

2. Continuous / Discontinuous Conduction with Pulse-Skipping Mode

DC-DC3

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.2V, MODE = FCCM[1], T_J = -40°C to +125°C; typical values are at T_J = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}	V_{IN} = SYSVDD	2.7		5.5	V
Programmable Output Voltage	V_{OUT}		0.85[4]		3.4	V
V_{OUT} Step Size	V_{OUT_STEP}			25		mV
V_{OUT} Accuracy	V_{OUT_ACC}	V_{IN} = 2.7V to 5.5V, I_{OUT} = 0mA to 1000mA	-4		4	%
Undervoltage margin		0.85V ≤ V_{OUT} ≤ 3.4V		50		mV
Output Current	I_{OUT}	FCCM[1] and Auto (CCM/DCM with PS[2]) Modes	0		1000	mA
		Hysteretic Mode, DC3_STNBY_LIM=01	0		200[3]	
		LDO Mode	0		10	
P-channel Current Limit	I_{P_LIM}			1600		mA
Quiescent Current	I_Q	I_{OUT} = 0mA, FCCM[1] and Auto (CCM/DCM with PS[2]) Modes (excluding switching losses)		330		µA
		I_{OUT} = 0mA, Hysteretic Mode		110		
		I_{OUT} = 0mA, LDO Mode		30		
Shutdown Current	I_{SD}	DC3_ENA = 0		0.01		µA
P-channel On Resistance	R_{DSP}	V_{IN} = V_{GS} = 3.8V, I_{DC3LX} = 100mA		165		mΩ
N-channel On Resistance	R_{DSN}	V_{IN} = V_{GS} = 3.8V, I_{DC3LX} = -100mA		155		mΩ
Switching Frequency	F_{SW}			2		MHz

Notes:

1. Forced Continuous Conduction Mode
2. Continuous / Discontinuous Conduction with Pulse-Skipping Mode
3. The maximum output current in Hysteretic Mode can be adjusted using the DC*m*_STNBY_LIM registers
4. In FCCM mode, the minimum V_{OUT} is 1.2V

7.2 DC-DC STEP UP CONVERTER

DC-DC4

Unless otherwise noted: V_{IN} = 3.8V, T_J = -40°C to +125°C; typical values are at T_J = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}	V_{IN} = SYSVDD	2.7		5.5	V
Output Voltage	V_{OUT}		6.5		30	V
Load Current	I_{LOAD}	V_{OUT} ≤ 8V	0		90	mA
		V_{OUT} = 6.5V to 20V	0		40	
		V_{OUT} = 20V to 30V	0		25	
Quiescent Current	I_Q	DC4_ENA=1		330		µA
Shutdown Current	I_{SD}	DC4_ENA=0		0.1	1	µA
N-channel On Resistance	R_{DSN}			150		mΩ
Regulated feedback voltage	V_{ISINKn}			500		mV
Out of regulation level	V_{ISINKn}			440		mV
Overvoltage detection	V_{DC4FB}			500		mV
Switching frequency	F_{SW}			1		MHz
N-channel Current limit	I_{N_LIM}			800		mA

7.3 CURRENT SINKS

Unless otherwise noted: T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Sink Current	I_{ISINKn}	0.3 <= V_{ISINKn} <= SYSVDD	2		28000	µA
Current Accuracy	I_{ISINKn}	I_{ISINKn} =12mA, V_{ISINKn} = 0.5V		TBD		V
Current matching	I_{ISINKn}	I_{ISINKn} =12mA, V_{ISINKn} = 0.5V		TBD		

7.4 LDO REGULATORS

LDO1

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.8V, T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}	V_{IN} ≤ SYSVDD	1.5		5.5	V
Programmable Output Voltage	V_{OUT}		0.9		3.3	V
V_{OUT} Step Size	V_{OUT_STEP}	V_{OUT} = 0.9V to 1.6V		50		mV
		V_{OUT} = 1.7V to 3.3V		100		
Output Current	I_{OUT}	Normal mode	0		300	mA
		Low power mode, LDO*n*_LP_MODE=0	0		50	
		Low power mode, LDO*n*_LP_MODE=1	0		20	
V_{OUT} Accuracy	V_{OUT_ACC}	I_{LOAD} = 1mA	-3		+3	%
Line Regulation	$V_{OUT\ LINE}$	V_{IN} = (V_{OUT} + 0.5) to 5.5V, I_{LOAD} = 150mA Note that V_{IN} must be >= 1.5V		0.1		%/V
Load Regulation	$V_{OUT\ LOAD}$	I_{LOAD} =1mA to 300mA		0.015		%/mA
Dropout Voltage	V_{IN} - V_{OUT}	I_{LOAD} =150mA, V_{OUT} > 2.7V		250		mV
		I_{LOAD} =150mA, V_{OUT} 1.8V to 2.7V		300		
		I_{LOAD} =150mA, V_{OUT} < 1.8V		500		
Undervoltage level	V_{OUT}	V_{OUT} Falling		88		%
Quiescent Current	I_Q	Normal mode, no load		30		µA
		Low power mode, LDO*n*_LP_MODE=0, no load		10		
		Low power mode, LDO*n*_LP_MODE=1, no load		5		
		I_{LOAD} = 1mA to 300mA		I_Q (no load) + 1% of load		
Power Supply Rejection Ratio	PSRR	I_{LOAD} = 150mA, <= 1kHz		53		dB
		I_{LOAD} = 150mA, 10kHz		53		
		I_{LOAD} = 150mA, 100kHz		32		
On Resistance (Switch mode)	R_{DSON}	V_{IN} = 1.5V, I_{LOAD} = 100mA		1.5		Ω
		V_{IN} = 1.8V, I_{LOAD} = 100mA		1.2		
		V_{IN} = 2.5V, I_{LOAD} = 100mA		0.85		
		V_{IN} = 3.3V, I_{LOAD} = 100mA		0.7		
Current Limit (Switch mode)	I_{CL}	V_{OUT} = 0V		600		mA
Start-up time	t_{start_up}	No load, Output cap 2.2 µF, 90% of V_{OUT}		10		µs
Shutdown time	t_{shut_down}	No load, Output cap 2.2 µF, 10% of V_{OUT}			10	ms

LDO2, LDO3

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.8V, T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}	V_{IN} ≤ SYSVDD	1.5		5.5	V
Programmable Output Voltage	V_{OUT}		0.9		3.3	V
V_{OUT} Step Size	V_{OUT_STEP}	V_{OUT} = 0.9V to 1.6V		50		mV
		V_{OUT} = 1.7V to 3.3V		100		
Output Current	I_{OUT}	Normal mode	0		200	mA
		Low power mode, LDO*n*_LP_MODE=0	0		50	
		Low power mode, LDO*n*_LP_MODE=1	0		20	
V_{OUT} Accuracy	V_{OUT_ACC}	I_{LOAD} = 1mA	-3		+3	%
Line Regulation	$V_{OUT\ LINE}$	V_{IN} = (V_{OUT} + 0.5) to 5.5V, I_{LOAD} = 100mA Note that V_{IN} must be >= 1.5V		0.1		%/V
Load Regulation	$V_{OUT\ LOAD}$	I_{LOAD} =1mA to 200mA		0.015		%/mA

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dropout Voltage	V_{IN} - V_{OUT}	I_{LOAD} =100mA, V_{OUT} > 2.7V		200		mV
		I_{LOAD} =100mA, V_{OUT} 1.8V to 2.7V		250		
		I_{LOAD} =100mA, V_{OUT} < 1.8V		400		
Undervoltage level	V_{OUT}	V_{OUT} Falling		88		%
Quiescent Current	I_Q	Normal mode, no load		30		µA
		Low power mode, LDO*n*_LP_MODE=0, no load		10		
		Low power mode, LDO*n*_LP_MODE=1, no load		5		
		I_{LOAD} = 1mA to 200mA		I_Q (no load) + 1% of load		
Power Supply Rejection Ratio	PSRR	I_{LOAD} = 100mA, <= 1kHz		55		dB
		I_{LOAD} = 100mA, 10kHz		55		
		I_{LOAD} = 100mA, 100kHz		32		
On Resistance (Switch mode)	R_{DSON}	V_{IN} = 1.5V, I_{LOAD} = 100mA		1.5		Ω
		V_{IN} = 1.8V, I_{LOAD} = 100mA		1.2		
		V_{IN} = 2.5V, I_{LOAD} = 100mA		0.85		
		V_{IN} = 3.3V, I_{LOAD} = 100mA		0.7		
Current Limit (Switch mode)	I_{CL}	V_{OUT} = 0V		400		mA
Start-up time	t_{start_up}	No load, Output cap 2.2 µF, 90% of V_{OUT}		10		µs
Shutdown time	t_{shut_down}	No load, Output cap 2.2 µF, 10% of V_{OUT}			10	ms

LDO4, LDO5, LDO6

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.8V, T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}	V_{IN} ≤ SYSVDD	1.5		5.5	V
Programmable Output Voltage	V_{OUT}		0.9		3.3	V
V_{OUT} Step Size	V_{OUT_STEP}	V_{OUT} = 0.9V to 1.6V		50		mV
		V_{OUT} = 1.7V to 3.3V		100		
Output Current	I_{OUT}	Normal mode	0		100	mA
		Low power mode, LDO*n*_LP_MODE=0	0		50	
		Low power mode, LDO*n*_LP_MODE=1	0		20	
V_{OUT} Accuracy	V_{OUT_ACC}	I_{LOAD} = 1mA	-3		+3	%
Line Regulation	$V_{OUT\ LINE}$	V_{IN} = (V_{OUT} + 0.5) to 5.5V, I_{LOAD} = 50mA Note that V_{IN} must be >= 1.5V		0.1		%/V
Load Regulation	$V_{OUT\ LOAD}$	I_{LOAD} =1mA to 100mA		0.025		%/mA
Dropout Voltage	V_{IN} - V_{OUT}	I_{LOAD} =100mA, V_{OUT} > 2.7V		200		mV
		I_{LOAD} =100mA, V_{OUT} 1.8V to 2.7V		250		
		I_{LOAD} =100mA, V_{OUT} < 1.8V		400		
Undervoltage level	V_{OUT}	V_{OUT} Falling		88		%
Quiescent Current	I_Q	Normal mode, no load		30		µA
		Low power mode, LDO*n*_LP_MODE=0, no load		10		
		Low power mode, LDO*n*_LP_MODE=1, no load		5		
		I_{LOAD} = 1mA to 100mA		I_Q (no load) + 1% of load		
Power Supply Rejection Ratio	PSRR	I_{LOAD} = 50mA, <= 1kHz		55		dB
		I_{LOAD} = 50mA, 10kHz		55		
		I_{LOAD} = 50mA, 100kHz		32		
On Resistance (Switch mode)	R_{DSON}	V_{IN} = 1.5V, I_{LOAD} = 100mA		3.2		Ω
		V_{IN} = 1.8V, I_{LOAD} = 100mA		2.1		
		V_{IN} = 2.5V, I_{LOAD} = 100mA		1.35		
		V_{IN} = 3.3V, I_{LOAD} = 100mA		1.1		

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Limit (Switch mode)	I_{CL}	V_{OUT} = 0V		230		mA
Start-up time	t_{start_up}	No load, Output cap 2.2 µF, 90% of V_{OUT}		10		µs
Shutdown time	t_{shut_down}	No load, Output cap 2.2 µF, 10% of V_{OUT}			10	ms

LDO7, LDO8

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.8V, T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}		1.71		5.5	V
Programmable Output Voltage	V_{OUT}		1.0		3.5	V
V_{OUT} Step Size	V_{OUT_STEP}	V_{OUT} = 1.0V to 1.6V		50		mV
		V_{OUT} = 1.7V to 3.5V		100		
Output Current	I_{OUT}	Normal mode	0		200	mA
		Low Power mode	0		50	
V_{OUT} Accuracy	V_{OUT_ACC}	I_{LOAD} = 1mA	-2.5		+2.5	%
Line Regulation	$V_{OUT\ LINE}$	V_{IN} = (V_{OUT} + 0.5) to 5.5V, I_{LOAD} = 100mA Note that V_{IN} must be >= 1.71V		0.025		%/V
Load Regulation	$V_{OUT\ LOAD}$	I_{LOAD} =1mA to 200mA		0.003		%/mA
Dropout Voltage	V_{IN} - V_{OUT}	I_{LOAD} =100mA, V_{OUT} =1.8V		95		mV
		I_{LOAD} =100mA, V_{OUT} =2.5V		65		
		I_{LOAD} =100mA, V_{OUT} =3.3V		60		
Undervoltage level	V_{OUT}	V_{OUT} Falling		93		%
Quiescent Current	I_Q	Normal mode, no load		110		µA
		Low Power mode, no load		70		
		I_{LOAD} = 1mA to 200mA		I_Q (no load) + 0.1% of load		
Power Supply Rejection Ratio	PSRR	I_{LOAD} = 100mA, <= 1kHz		70		dB
		I_{LOAD} = 100mA, 10kHz		67		
		I_{LOAD} = 100mA, 100kHz		48		
Output noise voltage	V_{OUT}	f=10Hz to 100kHz; V_{OUT}=2.8V, I_{LOAD} = 1mA		30		μV_{RMS}
		f=10Hz to 100kHz; V_{OUT}=2.8V, I_{LOAD} = 10mA		32		
		f=10Hz to 100kHz; V_{OUT}=2.8V, I_{LOAD} = 100mA		32		
On Resistance (Switch mode)	R_{DSON}	V_{IN} = 1.71V, I_{LOAD} = 100mA		550		mΩ
		V_{IN} = 1.8V, I_{LOAD} = 100mA		500		
		V_{IN} = 2.5V, I_{LOAD} = 100mA		330		
		V_{IN} = 3.5V, I_{LOAD} = 100mA		250		
Current Limit (Switch mode)	I_{CL}	V_{OUT} = 0V		320		mA
Start-up time	t_{start_up}	No load, Output cap 4.7 µF, 90% of V_{OUT}		50		µs
Shutdown time	t_{shut_down}	No load, Output cap 4.7 µF, 10% of V_{OUT}			10	ms

LDO9, LDO10

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.8V, T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}		1.71		5.5	V
Programmable Output Voltage	V_{OUT}		1.0		3.5	V
V_{OUT} Step Size	V_{OUT_STEP}	V_{OUT} = 1.0V to 1.6V		50		mV
		V_{OUT} = 1.7V to 3.5V		100		
Output Current	I_{OUT}	Normal mode	0		150	mA
		Low Power mode	0		50	

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT} Accuracy	V_{OUT_ACC}	I_{LOAD} = 1mA	-2.5		+2.5	%
Line Regulation	$V_{OUT\ LINE}$	V_{IN} = (V_{OUT} + 0.5) to 5.5V, I_{LOAD} = 75mA Note that V_{IN} must be >= 1.71V		0.025		%/V
Load Regulation	$V_{OUT\ LOAD}$	I_{LOAD} =1mA to 150mA		0.004		%/mA
Dropout Voltage	V_{IN} - V_{OUT}	I_{LOAD} =100mA, V_{OUT} =1.8V		135		mV
		I_{LOAD} =100mA, V_{OUT} =2.5V		100		
		I_{LOAD} =100mA, V_{OUT} =3.3V		90		
Undervoltage level	V_{OUT}	V_{OUT} Falling		93		%
Quiescent Current	I_Q	Normal mode, no load		110		µA
		Low Power mode, no load		70		
		I_{LOAD} = 1mA to 150mA		I_Q (no load) + 0.1% of load		
Power Supply Rejection Ratio	PSRR	I_{LOAD} = 75mA, <= 1kHz		73		dB
		I_{LOAD} = 75mA, 10kHz		69		
		I_{LOAD} = 75mA, 100kHz		49		
Output noise voltage	V_{OUT}	f=10Hz to 100kHz; V_{OUT}=2.8V, I_{LOAD} = 1mA		30		μV_{RMS}
		f=10Hz to 100kHz; V_{OUT}=2.8V, I_{LOAD} = 10mA		32		
		f=10Hz to 100kHz; V_{OUT}=2.8V, I_{LOAD} = 100mA		32		
On Resistance (Switch mode)	R_{DSON}	V_{IN} = 1.71V, I_{LOAD} = 100mA		1000		mΩ
		V_{IN} = 1.8V, I_{LOAD} = 100mA		930		
		V_{IN} = 2.5V, I_{LOAD} = 100mA		610		
		V_{IN} = 3.5V, I_{LOAD} = 100mA		430		
Current Limit (Switch mode)	I_{CL}	V_{OUT} = 0V		250		mA
Start-up time	t_{start_up}	No load, Output cap 4.7 µF, 90% of V_{OUT}		70		µs
Shutdown time	t_{shut_down}	No load, Output cap 4.7 µF, 10% of V_{OUT}			10	ms

LDO11

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.2V, T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Programmable Output Voltage	V_{OUT}		0.8		1.55	V
V_{OUT} Step Size	V_{OUT_STEP}			50		mV
Output Current	I_{OUT}	SYSVDD < 3.1V	0		10	mA
		SYSVDD ≥ 3.1V	0		25	
V_{OUT} Accuracy	V_{OUT}	V_{IN} = 2.7 to 5.5V ; I_{LOAD} = 100µA	-4		+4	%
Line Regulation	$V_{OUT\ LINE}$	V_{IN} = 2.7 to 5.5V; I_{LOAD} = 1mA		0.4		%/V
Load Regulation	$V_{OUT\ LOAD}$	I_{LOAD} = 100µA to 10mA		0.2		%/mA
Quiescent Current	I_Q	No load		2.5		µA
Start-up time	t_{start_up}	No load, Output cap 0.1 µF, 90% of V_{OUT}		0.3	1	ms
Shutdown time	t_{shut_down}	No load, Output cap 0.1 µF, 10% of V_{OUT}		0.3	1	ms

7.5 RESET THRESHOLDS

Unless otherwise noted: T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power On Reset						
Power on Reset threshold VPMIC (LDO12VOUT) voltage at which device transitions between NO POWER and BACKUP states	$V_{POR, DE-ASSERT}$	VPMIC rising		1.18		V
	$V_{POR, ASSERT}$	VPMIC falling		1.08		V
Power on Reset hysteresis	$V_{POR, HYST}$			100		mV
Device Reset Control						
Device Reset threshold VPMIC (LDO12VOUT) voltage at which device transitions between BACKUP and OFF states	$V_{RES, DE-ASSERT}$	VPMIC rising		1.94		V
	$V_{RES, ASSERT}$	VPMIC falling		1.85		V
Device Reset hysteresis	$V_{RES, HYST}$			92		mV
Device Shutdown						
Shutdown threshold SYSVDD voltage at which the device forces an OFF transition	$V_{SHUTDOWN}$	SYSVDD falling		2.7		V
SYSLO threshold accuracy SYSVDD voltage at which SYSLO is asserted	V_{SYSLO}	SYSVDD falling, V_{SYSLO} set by SYSLO_THR (2.8V to 3.5V)	-3.5		+3.5	%
SYSOK threshold accuracy SYSVDD voltage at which SYSOK is asserted.	V_{SYSOK}	SYSVDD rising, V_{SYSOK} set by SYSOK_THR (2.8V to 3.5V) Note the SYSOK hysteresis margin ($V_{SYSOK, HYST}$) is added to SYSOK_THR.	-3.5		+3.5	%
SYSOK hysteresis	$V_{SYSOK, HYST}$			40		mV

7.6 REFERENCES

Unless otherwise noted: T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage Reference	V_{VREFC}			0.8		V
Current Reference	V_{IREFR}	100kΩ to REFGND		0.5		V

7.7 BATTERY CHARGER

Unless otherwise noted: T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General						
Supply voltage (Voltage required to commence charging; note that charging can continue at lower supply voltages, eg. under current throttling conditions)	V_{SYSVDD}		4.3		5.5	V
Target voltage	V_{BATT_TGT}	CHG_VSEL = 00	4.0	4.05	4.1	V
		CHG_VSEL = 01	4.05	4.10	4.15	
		CHG_VSEL = 10	4.1	4.15	4.2	
		CHG_VSEL = 11	4.15	4.20	4.25	
Charger re-start threshold (Trickle charging starts when battery voltage is below this threshold)	V_{BATT_RSTRT}			V_{BATT_TGT} - 100mV		V
Defective battery threshold	V_{BATT_DEF}			2.85		V
Defective battery timeout	t_{BATT_DEF}			30		mins
Overvoltage threshold	V_{BATT_OV}			4.5		V
End of Charge Current	I_{EOC}	Set by CHG_ITERM		20 to 90		mA
Maximum trickle charge current	I_{TRKL_LIM}	Set by CHG_TRKL_ILIM		50 to 200		mA
Fast charge threshold (Fast charging fast-charge is only possible when battery voltage is above this threshold)	V_{FAST_CHG}			2.85		V
Maximum fast charge current	I_{FAST_LIM}	Set by CHG_FAST_ILIM		50 to 1000		mA
Supply voltage regulation level (Current throttling is applied if supply drops to this level)	V_{SYS_REG}					
Internal Battery FET 'On' Resistance	R_{CHG_SW}	$V_{BATTVDD}$ = 3.8V		90		mΩ
		$V_{BATTVDD}$ = 3.3V		100		
Battery Temperature Monitoring						
Battery temperature monitor source (NTCBIAS)	$V_{NTCBIAS}$			2.1		V
NTCMON voltage for high battery temperature detection	V_{BTEMP_H}	V_{NTCMON} falling		0.344 × $V_{NTCBIAS}$		V
		V_{NTCMON} rising		0.365 × $V_{NTCBIAS}$		
NTCMON voltage for low battery temperature detection	V_{BTEMP_L}	V_{NTCMON} rising		0.767 × $V_{NTCBIAS}$		V
		V_{NTCMON} falling		0.743 × $V_{NTCBIAS}$		
NTCMON voltage for 'no NTC' detection	V_{NO_NTC}	V_{NTCMON} rising		0.961 × $V_{NTCBIAS}$		V
		V_{NTCMON} falling		0.931 × $V_{NTCBIAS}$		

7.8 USB POWER CONTROL

Unless otherwise noted: T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage	V_{USBVDD}		4.3		5.5	V
USB FET 'On' Resistance	R_{USB_SW}	USB_ILIM = 010		230		mΩ
		USB_ILIM = 011 or greater		96		
Current limit	I_{USBVDD}	USB_ILIM = 010		91	100	mA
		USB_ILIM = 011		454	500	
		USB_ILIM = 100		805	900	
		USB_ILIM = 101		1343	1500	
		USB_ILIM = 110		1609	1800	
		USB_ILIM = 111		496	550	
Current limit response time				10		µs

7.9 GENERAL PURPOSE INPUTS / OUTPUTS (GPIO)

Unless otherwise noted: T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIO1, GPIO2, GPIO3, GPIO7, GPIO8, GPIO9						
Input HIGH Level	V_{IH}		0.75 x VDD			V
Input LOW Level	V_{IL}				0.25 x VDD	V
Output HIGH Level	V_{OH}	I_{OH} = 1mA	0.8 x VDD			V
Output LOW Level	V_{OL}	I_{OL} = -1mA			0.2 x VDD	V
Pull-up resistance to VDD	R_{PU}	GPn_PWR_DOM=0 and DBVDD=1.8V or GPn_PWR_DOM=1		180		kΩ
Pull-down resistance	R_{PD}			180		kΩ
GPIO4, GPIO5, GPIO6, GPIO10, GPIO11, GPIO12						
Input HIGH Level	V_{IH}		0.85 x VDD			V
Input LOW Level	V_{IL}				0.2 x VDD	V
Output HIGH Level	V_{OH}	I_{OH} = 1mA	0.8 x VDD			V
Output LOW Level	V_{OL}	I_{OL} = -1mA			0.2 x VDD	V
Pull-up resistance to VDD	R_{PU}	GPn_PWR_DOM=0 and DBVDD=1.8V or GPn_PWR_DOM=1 and SYSVDD=3.8V		180		kΩ
Pull-down resistance	R_{PD}			180		kΩ

Notes:

1. 'VDD' is the voltage of the applicable power domain for each pin (selected by the corresponding GPn_PWR_DOM register).
2. Pull-up / pull-down resistance only applies when enabled using the GPn_PULL registers.
3. Pull-up / pull-down resistors are disabled when the GPIO pin is tri-stated.
4. Pull-up / pull-down resistance may change with the applicable power domain (as selected by GPn_PWR_DOM).

7.10 DIGITAL INTERFACES

Unless otherwise noted: T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{ON}$, $\overline{RESET}$, $\overline{IRQ}$, CIFMODE, SDOUT1, SCLK1, SDA1, $\overline{CS}$, SCLK2, SDA2						
Input HIGH Level	V_{IH}		0.75 x VDD			V
Input LOW Level	V_{IL}				0.2 x VDD	V
Output HIGH Level	V_{OH}	I_{OH} = 1mA	0.8 x VDD			V
Output LOW Level	V_{OL}	I_{OL} = -1mA			0.2 x VDD	V
'VDD' is the voltage of the applicable power domain for each pin, as defined in Section 3.						
ON pin pull-up resistance	R_{PU}			140		kΩ
RESET pin pull-up resistance	R_{PU}	DBVDD=1.8V		180		kΩ
		DBVDD=3.6V		85		
IRQ pin pull-up resistance	R_{PU}	DBVDD=1.8V		180		kΩ
		DBVDD=3.6V		85		
SCLK2 pin pull-down resistance	R_{PD}			100		kΩ
SDA2 pin pull-down resistance	R_{PD}			100		kΩ

7.11 AUXILIARY ADC

Unless otherwise noted: T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input resistance	$R_{AUXADCINn}$	During measurement		400		kΩ
Input voltage range	$V_{AUXADCIN1, 2, 3}$		0		V_{SYSVDD}	V
	$V_{AUXADCIN4}$		0		V_{DBVDD}	
Input capacitance	$C_{AUXADCINn}$			2		pF
AUXADC Resolution				12		bits
AUXADC Conversion Time				39		µs
AUXADC accuracy		Input voltage = 3V	-2.5		+2.5	%

7.12 SYSTEM STATUS LED DRIVERS

Unless otherwise noted: T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LED1 and LED2						
Sink current				10		mA

7.13 CLOCKING

Unless otherwise noted: T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
FLL input reference	32.768kHz	FLL_CLK_SRC=00		32.768		kHz
	CLKIN	FLL_CLK_SRC=01	32		25000	kHz
FLL output frequency	CLKOUT	CLKOUT_SRC=0	32		25000	kHz