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WM8326

Processor Power Management Subsystem

DESCRIPTION

The WM8326 is an integrated power-management subsystem which provides a cost-effective, flexible, single-chip solution for power management. It is specifically targeted at the requirements of a range of low-power portable consumer products, but is suitable to any application with a multimedia processor. The WM8326 is designed to operate as a system PMIC supporting the ARM9™, ARM11™ and ARM Cortex-A™ processors, but is also capable of supporting the majority of application and mobile processors at the heart of a wide range of low-power consumer multimedia applications.

The start-up behaviour and configuration is fully programmable in an integrated OTP non-volatile memory. This highly flexible solution helps reduce time-to-market, as changing application requirements can be very easily accommodated in the OTP. The InstantConfig™ interface enables an external EEPROM to configure the WM8326.

The WM8326 power management subsystem comprises four programmable DC-DC converters and eleven LDO regulators (four of which are low-noise for supplying sensitive analogue subsystems). The integrated OTP bootstrap circuitry controls the start-up sequencing and voltages of the converters and regulators as well as the sequencing of system clocks.

The DC-DC converters deliver high performance and high efficiency across a wide range of operating conditions. They are optimised to support the high load current transients seen in modern processor core domains. DC-DC3 / DC-DC4 can be connected together and operated in 'dual' mode to support an increased current load of up to 1.6A

An on-chip regulator provides power for always-on PMIC functions such as register map and the RTC. The device provides autonomous backup battery switchover. A low-power LDO is included to support 'Alive' processor power domains external to the WM8326.

A 12-bit Auxiliary ADC supports a wide range of applications for internal as well as external analogue sampling, such as voltage detection and temperature measurement.

WM8326 includes a crystal oscillator and an internal RC oscillator to generate all clock signals for autonomous system start-up and processor clocking. A Secure Real-time Clock (S-RTC) and alarm function is included, capable of waking up the system from low-power modes. A watchdog function is provided to ensure system integrity.

To maximise battery life, highly-granular power management enables each function in the WM8326 subsystem to be independently powered down through a control interface or alternatively through register and OTP-configurable GPIOs. The device offers a standby power consumption of <7uA, making it particularly suitable for portable applications.

The WM8326 is supplied in an 8x8mm 81-lead QFN package, ideal for use in portable systems. The WM8326 forms part of the Wolfson series of audio and power management solutions, and is widely register compatible with the WM831X devices.

FEATURES

Power Management

- 2 x DC-DC synchronous buck converters (0.6V - 1.8V, 2.5A, DVS)
- 2 x DC-DC synchronous buck converters (0.85V - 3.4V, 1A)
- 1 x LDO regulator (0.9V - 3.3V, 300mA, 1Ω)
- 2 x LDO regulators (0.9V - 3.3V, 200mA, 1Ω)
- 3 x LDO regulators (0.9V - 3.3V, 100mA, 2Ω)
- 2 x Low-noise LDO regulators (1.0V - 3.5V, 200mA, 1Ω)
- 2 x Low-noise LDO regulators (1.0V - 3.5V, 150mA, 2Ω)
- 1 x 'Alive' regulator (0.8V – 1.55V, up to 25mA)

System Control

- I^2C or SPI compatible primary control interface
- Comprehensive interrupt scheme
- Watchdog timer and system reset control
- Autonomous power sequencing and fault detection
- OTP memory bootstrap configuration function

Additional Features

- Auxiliary ADC for multi-function analogue measurement
- 128-bit pseudo-random unique ID
- Secure Real-Time Clock with wake-up alarm
- 12 x configurable multi-function (GPIO) pins
- Comprehensive clocking scheme: low-power 32kHz RTC crystal oscillator, GPIO clock output and 4MHz RC clock for power management
- System LED outputs indicating device power state, and fault status

Package Options

- 8 x 8 x 0.85mm, 81-lead QFN package

APPLICATIONS

- Cellular Handsets
- Smartphones
- Electronic Books
- Portable Media Players
- Mobile Internet Devices
- Electronic Gaming Devices
- Netbooks
- Smartbooks
- Set Top Box
- Digital Picture Frames

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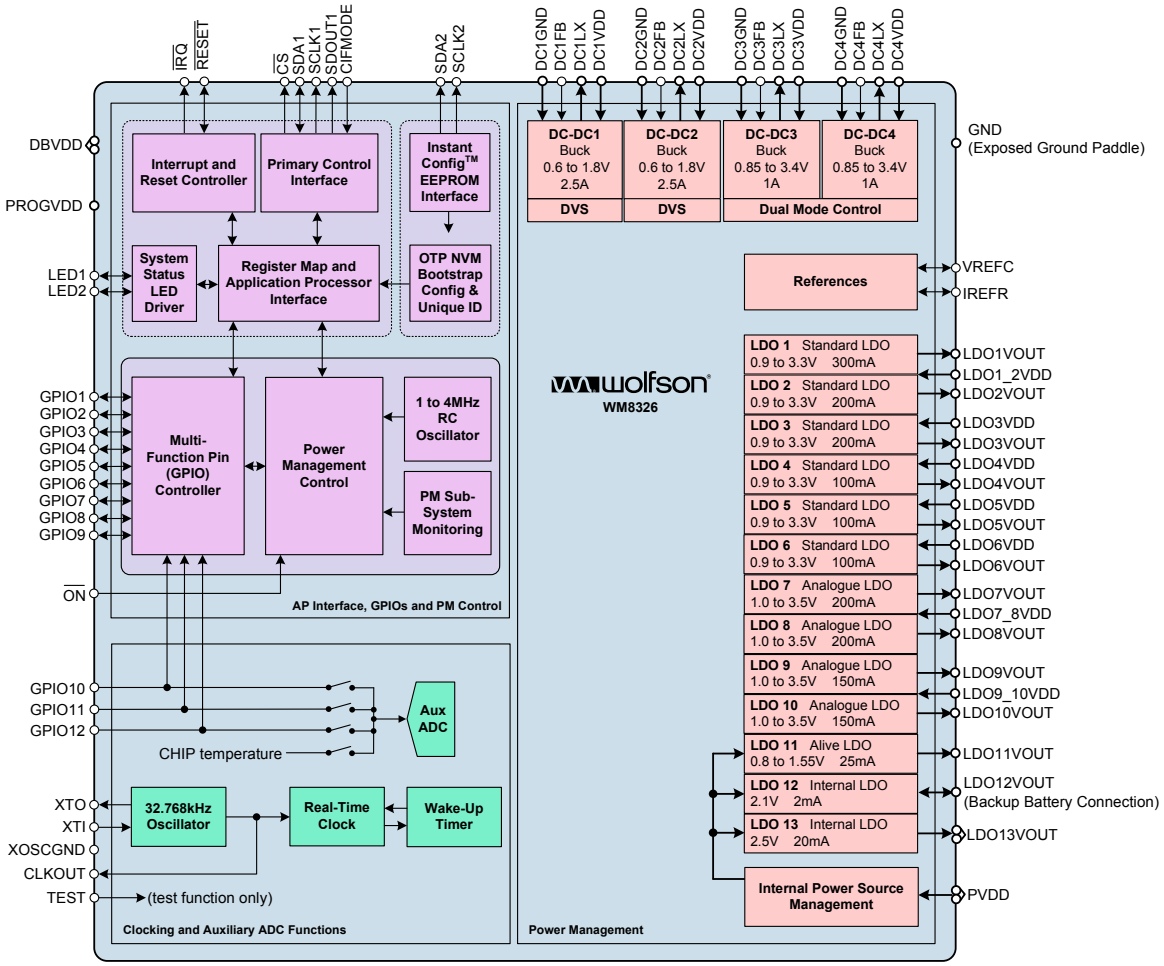
BLOCK DIAGRAM



TYPICAL APPLICATIONS

The WM8326 is designed as a system PMIC device that generates configurable DC supplies to power processors and associated peripherals within a system. The WM8326 provides four DC-DC synchronous buck (step-down) converters. Two of these can operate in dual mode, providing an increased current capability. Eleven LDO regulators provide a high degree of flexibility to provide power to multiple devices, with the capability to power-up and power-down different circuits independently.

Two of the DC-DC buck converters incorporate Wolfson's BuckWise™ technology specifically designed to handle rapid changes in load current; programmable slew rate DVS is also provided, as required by modern application processors. Selectable operating modes on all of the DC-DC converters allow each converter to be optimally configured for light, heavy or transient load conditions. Flexible operating configurations allow the converters to be tailored for minimum PCB area, maximum performance, or for maximum efficiency. The analogue LDOs provide low-noise outputs suitable for powering sensitive circuits such as RF / Wi-Fi / cellular handset applications.

The WM8326 powers up the converters and LDOs according to a programmable sequence. A configurable 'SLEEP' state is also available, providing support for an alternate configuration, typically for low-power / standby operation. The power control sequences and many other parameters can be stored in an integrated user-configurable OTP (One-Time Programmable) memory or may be loaded from an external memory. The WM8326 supports the programming and verification of the integrated OTP memory.

A backup battery supply can be connected to the WM8326 in order to maintain the Real Time Clock (RTC) in the absence of the primary supply.

Programmable GPIO pins may be configured as hardware inputs for general use or for selecting different power management configurations. As outputs, the GPIOs can provide indications of the device status, or may be used as control signals for other power management circuits. The WM8326 also provides two LED drivers, which can be controlled manually or configured as status indicators for the OTP memory programmer or operating power state.

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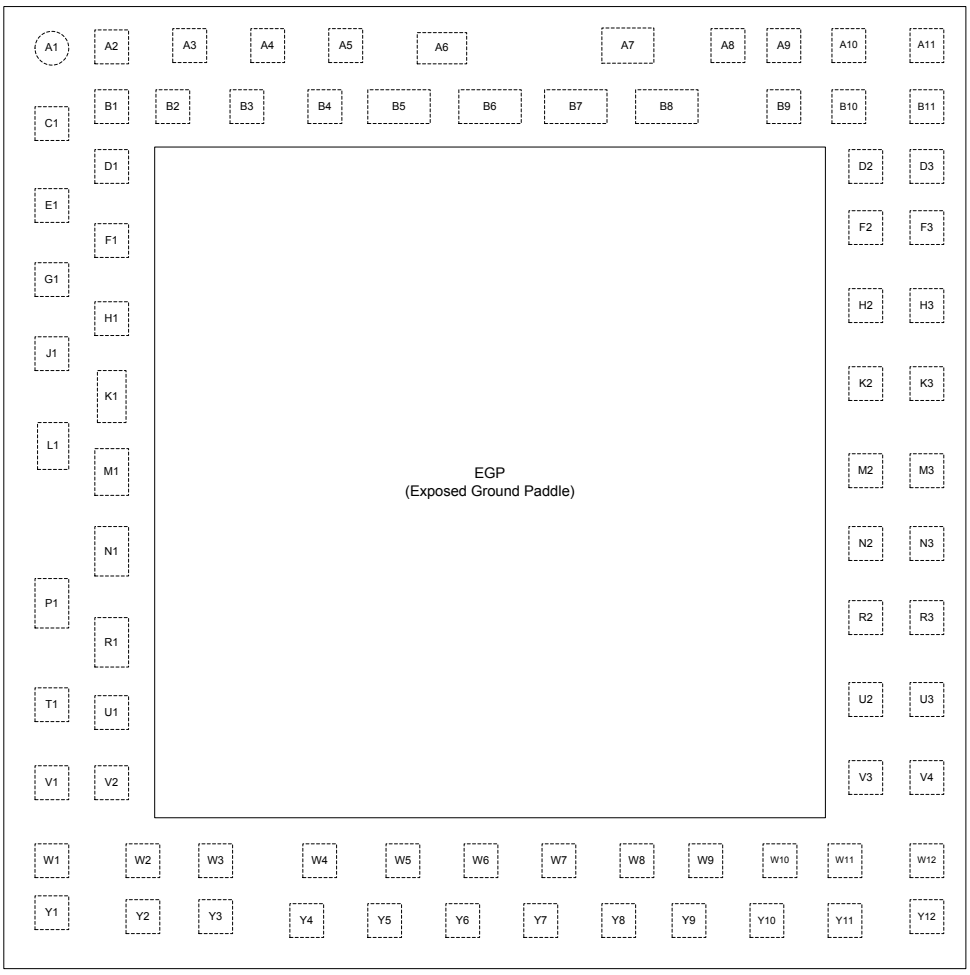
1 PIN CONFIGURATION



Top View – WM8326

2 ORDERING INFORMATION

ORDER CODE	OTP	TEMPERATURE RANGE (T_A)	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8326GEFL/V	Unprogrammed	-40°C to +85°C	81-lead QFN (8 x 8mm) (Pb-free)	MSL3	260°C
WM8326GEFL/RV	Unprogrammed	-40°C to +85°C	81-lead QFN (8 x 8mm) (Pb-free, tape and reel)	MSL3	260°C
WM8326GEFLxxx/RV*	Custom	-40°C to +85°C	81-lead QFN (8 x 8mm) (Pb-free, tape and reel) **	MSL3	260°C

Note:

Reel quantity = 2200

* xxx = Unique OTP part number

** Custom OTP minimum order quantity 22,000.

3 PIN DESCRIPTION

Notes:

1. Pins are sorted by functional groups.
2. The power domain associated with each pin is noted; VPMIC is the domain powered by LDO12 for the 'always-on' functions internal to the WM8326.
3. Note that an external level-shifter may be required when interfacing between different power domains.

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION
Clocking and Real Time Clock				
Y12	XTO	Analogue Output	VPMIC	Crystal Drive Output
Y11	XTI	Analogue Input		Crystal Drive Input or 32.768kHz CMOS Clock Input
W11	XOSCGND	Supply		Crystal Oscillator Ground
H1	CLKOUT	Digital Output	DBVDD	CMOS Clock Output Configurable Open Drain / CMOS mode. (External 4.7kΩ pull-up recommended in Open Drain mode.)
General Purpose Input / Output and Auxiliary ADC				
D3	GPIO1	Digital I/O	DBVDDor VPMIC	GPIO Pin 1 Selectable pull-up/pull-down.
F2	GPIO2	Digital I/O		GPIO Pin 2 Selectable pull-up/pull-down.
F3	GPIO3	Digital I/O		GPIO Pin 3 Selectable pull-up/pull-down.
W4	GPIO4	Digital I/O	DBVDDor PVDD	GPIO Pin 4 Selectable pull-up/pull-down.
Y4	GPIO5	Digital I/O		GPIO Pin 5 Selectable pull-up/pull-down.
W5	GPIO6	Digital I/O		GPIO Pin 6 Selectable pull-up/pull-down.
H2	GPIO7	Digital I/O	DBVDDor VPMIC	GPIO Pin 7 Selectable pull-up/pull-down.
H3	GPIO8	Digital I/O		GPIO Pin 8 Selectable pull-up/pull-down.
K3	GPIO9	Digital I/O		GPIO Pin 9 Selectable pull-up/pull-down.
Y5	GPIO10	Digital I/O	DBVDDor PVDD	GPIO Pin 10 / Auxiliary ADC input Selectable GPIO pull-up/pull-down.
Y6	GPIO11	Digital I/O		GPIO Pin 11 / Auxiliary ADC input Selectable GPIO pull-up/pull-down.
W6	GPIO12	Digital I/O		GPIO Pin 12 / Auxiliary ADC input Selectable GPIO pull-up/pull-down.

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION	
Processor Interface and IC Control					
W9	$\overline{ON}$	Digital Input	VPMIC	ON Request Pin (Internal pull-up)	
B10	$\overline{RESET}$	Digital I/O	DBVDD	System Reset Input and Open Drain Output. (Internal pull-up)	
A11	$\overline{IRQ}$	Digital Output	DBVDD	PMIC Interrupt Flag Output. Configurable Open Drain / CMOS mode. (Internal pull-up in Open Drain mode.)	
E1	CIFMODE	Digital Input	DBVDD	Primary Control Interface Mode Select: 0 = I^2C Compatible Control Interface Mode 1 = SPI Compatible Control Interface Mode	
				SPI Compatible Control Interface Mode	*I^2C Compatible Control Interface Mode*
D2	SDOUT1	Digital Output	DBVDD	Control Interface Serial Data Out. Open Drain output; external 4.7kΩ pull-up recommended.	No Function
B9	SCLK1	Digital Input		Control Interface Serial Clock	Control Interface Serial Clock
A9	SDA1	Digital I/O		Control Interface Serial Data In	Control Interface Serial Data Input and Open Drain Output. External 4.7kΩ pull-up recommended. (Output can extend above DBVDD domain.)
A10	$\overline{CS}$	Digital Input		Control Interface Chip Select	I^2C Address Select: 0 = 68h 1 = 6Ch
Y10	SCLK2	Digital I/O	VPMIC	Control Interface Serial Clock for external InstantConfig™ EEPROM (ICE) (Internal pull-down)	
W10	SDA2	Digital I/O		Control Interface Serial Data to/from external InstantConfig™ EEPROM (ICE) (Internal pull-down)	
B11	DBVDD1	Supply		Digital Buffer Supply	
F1	DBVDD2	Supply		Digital Buffer Supply	
OTP Memory					
Y3	PROGVDD	Supply		High-voltage input for OTP programming.	

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION
DC-DC Converters and LDO Regulators				
B7	DC1GND	Supply		DC-DC1 Power Ground
A8	DC1FB	Analogue Input	DC1VDD	DC-DC1 Feedback Pin
A7	DC1LX	Analogue I/O		DC-DC1 Inductor Connection
B8	DC1VDD	Supply		DC-DC1 Power Input (connect to PVDD system supply)
B6	DC2GND	Supply		DC-DC2 Power Ground
A5	DC2FB	Analogue Input	DC2VDD	DC-DC2 Feedback Pin
A6	DC2LX	Analogue I/O		DC-DC2 Inductor Connection
B5	DC2VDD	Supply		DC-DC2 Power Input (connect to PVDD system supply)
M1	DC3GND	Supply		DC-DC3 Power Ground
J1	DC3FB	Analogue Input	DC3VDD	DC-DC3 Feedback Pin
L1	DC3LX	Analogue I/O		DC-DC3 Inductor Connection
K1	DC3VDD	Supply		DC-DC3 Power Input (connect to PVDD system supply)
N1	DC4GND	Supply		DC-DC4 Power Ground
T1	DC4FB	Analogue Input	DC4VDD	DC-DC4 Feedback Pin
P1	DC4LX	Analogue I/O		DC-DC4 Inductor Connection
R1	DC4VDD	Supply		DC-DC4 Power Input (connect to PVDD system supply)
A3	LDO1_2VDD	Supply		LDO1 & LDO2 Power Input
B2	LDO1VOUT	Analogue Output	LDO1VDD	LDO1 Power Output
B3	LDO2VOUT	Analogue Output	LDO2VDD	LDO2 Power Output
B4	LDO3VDD	Supply		LDO3 Power Input
A4	LDO3VOUT	Analogue Output	LDO3VDD	LDO3 Power Output
W3	LDO4VDD	Supply		LDO4 Power Input
Y2	LDO4VOUT	Analogue Output	LDO4VDD	LDO4 Power Output
Y1	LDO5VDD	Supply		LDO5 Power Input
W2	LDO5VOUT	Analogue Output	LDO5VDD	LDO5 Power Output
W1	LDO6VDD	Supply		LDO6 Power Input
V1	LDO6VOUT	Analogue Output	LDO6VDD	LDO6 Power Output
R3	LDO7_8VDD	Supply		LDO7 & LDO8 Power Input
N2	LDO7VOUT	Analogue Output	LDO7VDD	LDO7 Power Output
R2	LDO8VOUT	Analogue Output	LDO8VDD	LDO8 Power Output
M2	LDO9_10VDD	Supply		LDO9 Power Input
M3	LDO9VOUT	Analogue Output	LDO9VDD	LDO9 Power Output
N3	LDO10VOUT	Analogue Output	LDO10VDD	LDO10 Power Output
V3	LDO11VOUT	Analogue Output	PVDD	LDO11 (Alive) Power Output
Y8	LDO12VOUT	Analogue I/O	PVDD	LDO12 (Internal VPMIC) Output; Backup battery supply input / output
W7	LDO13VOUT1	Analogue I/O	PVDD	LDO13 (Internal INTVDD) Output; not for general use
K2	LDO13VOUT2	Analogue I/O	PVDD	LDO13 - Connect to LDO13VOUT1 (W7)
Voltage and Current References				
W8	VREFC	Analogue I/O	VPMIC	Voltage Reference capacitor connection point
Y9	IREFR	Analogue I/O		Current Reference resistor connection point
System LED Drivers				
U3	LED1	Digital Output	PVDD	Status LED Driver 1. Open Drain Output
U2	LED2	Digital Output		Status LED Driver 2. Open Drain Output

PIN	NAME	TYPE	POWER DOMAIN	DESCRIPTION
System Power				
U1	PVDD1	Supply		System VDD Supply
Y7	PVDD2	Supply		System VDD Supply
V4	PVDD3	Supply		System VDD Supply
EGP	Exposed Ground Paddle	Analogue Ground		Ground
Miscellaneous				
A1, A2, B1, C1, D1, V2, W12	DNC			Do Not Connect
G1, W12	TEST			Test function (connect to GND)

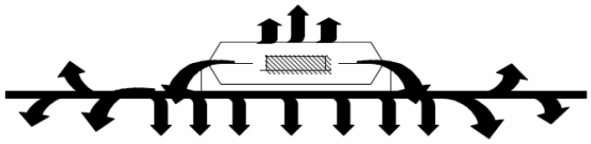
4 THERMAL CHARACTERISTICS

Thermal analysis must be performed in the intended application to prevent the WM8326 from exceeding maximum junction temperature. Several contributing factors affect thermal performance most notably the physical properties of the mechanical enclosure, location of the device on the PCB in relation to surrounding components and the number of PCB layers. Connecting the GND balls through thermal vias and into a large ground plane will aid heat extraction.

Three main heat transfer paths exist to surrounding air:

- Package top to air (convection and radiation).
- Package bottom to PCB (convection and radiation).
- Package leads to PCB (conduction).

(Note that radiation is not normally significant at the moderate temperatures experienced in typical applications.)



The temperature rise T_R is given by $T_R = P_D * \Theta_{JA}$

- P_D is the power dissipated by the device.
- Θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature and is therefore a measure of heat transfer from the die to surrounding air.
- For WM8326, Θ_{JA} = 24°C/W
- The quoted Θ_{JA} is based on testing to the EIA/JEDEC-51-2 test environment (ie. $1ft^3$ box, still air, with specific PCB stack-up and tracking rules). Note that this is not guaranteed to reflect all typical end applications.

The junction temperature T_J is given by $T_J = T_A + T_R$

- T_A, is the ambient temperature.

The worst case conditions are when the WM8326 is operating in a high ambient temperature, and under conditions which cause high power dissipation, such as the DC-DC converters operating at low supply voltage, high duty cycle and high output current. Under such conditions, it is possible that the heat dissipated could cause the maximum junction temperature of the device to be exceeded. Care must be taken to avoid this situation. An example calculation of the junction temperature is given below.

- P_D = 500mW (example figure)
- Θ_{JA} = 24°C/W
- $T_R = P_D * \Theta_{JA}$ = 12°C
- T_A = 85°C (example figure)
- $T_J = T_A + T_R$ = 97°C

The minimum and maximum operating junction temperatures for the WM8326 are quoted in Section 5. The maximum junction temperature is 125°C. Therefore, the junction temperature in the above example is within the operating limits of the WM8326.

5 ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The WM8326 has been classified as MSL3.

CONDITION	MIN	MAX
OTP Programming Supply (PROGVDD)	-0.3V	7.0V
System supply (PVDD1, PVDD2, PVDD3)	-0.3V	7.0V
Input voltage for LDO regulators	-0.3V	7.0V
Input voltage for DC-DC converters	-0.3V	7.0V
Digital buffer supply (DBVDD1, DBVDD2)	-0.3V	4.5V
Voltage range for digital inputs	-0.3V	DBVDD + 0.3V
Operating Temperature Range, T_A	-40°C	+85°C
Junction Temperature, T_J	-40°C	+125°C
Thermal Impedance Junction to Ambient, θ_{JA}		24°C/W
Storage temperature prior to soldering	30°C max / 60% RH max	
Storage temperature after soldering	-65°C	+150°C
Soldering temperature (10 seconds)		+260°C
Note: These ratings assume that all ground pins are at 0V.		

6 RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
System power source	PVDD1, PVDD2, PVDD3	2.7		5.5	V
Digital buffer supply	DBVDD1, DBVDD2	1.71		3.6	V
OTP Programming Supply (see note)	PROGVDD	6.25	6.5	6.75	V
	LDO12VOUT		3.3		V
Ground	Exposed Ground Paddle (EGP), DC1GND, DC2GND, DC3GND, DC4GND, XOSCGND		0		V

Note:

The OTP Programming Supply PROGVDD should only be present when programming the OTP. At other times, this pin should be left unconnected. The LDO12VOUT must be overdriven by an external supply when programming the OTP. At other times, the voltage at this pin is driven by the internal circuits of the WM8326.

7 ELECTRICAL CHARACTERISTICS

7.1 DC-DC SYNCHRONOUS BUCK CONVERTERS

DC-DC1 and DC-DC2

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.2V, MODE = FCCM[1], T_J = -40°C to +125°C; typical values are at T_J = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}			2.7		5.5	V
Programmable Output Voltage	V_{OUT}	F_{SW} = 2MHz		0.6		1.8	V
		F_{SW} = 4MHz		0.6		1.4	
V_{OUT} Step Size	V_{OUT_STEP}				12.5		mV
V_{OUT} Accuracy	V_{OUT_ACC}	V_{IN} = 2.7V to 5.5V, I_{OUT} = 0mA to 2500mA		-2.5		+2.5	%
Undervoltage margin	V_{UV}	0.6V ≤ V_{OUT} < 0.9V			50		mV
		0.9V ≤ V_{OUT} < 1.3V			80		
		1.3V ≤ V_{OUT} ≤ 1.8V			100		
Overvoltage margin	V_{OV}	0.6V ≤ V_{OUT} ≤ 1.8V			100		mV
Output Current	I_{OUT}	FCCM[1] and Auto (CCM/DCM with PS[2]) Modes	F_{SW} = 2MHz	0		2500	mA
			F_{SW} = 4MHz	0		1250	
		Hysteretic Mode		0		150	
		LDO Mode		0		10	
P-channel Current Limit	I_{P_LIM}				3650		mA
Quiescent Current	I_Q	I_{OUT} = 0mA, FCCM[1] and Auto (CCM/DCM with PS[2]) Modes (excluding switching losses)			585		µA
		I_{OUT} = 0mA, Hysteretic Mode			100		
		I_{OUT} = 0mA, LDO Mode			25		
Shutdown Current	I_{SD}	DC*m*_ENA = 0			0.01		µA
P-channel On Resistance	R_{DSP}	V_{IN} = V_{GS} = 3.8V, I_{DCmLX} = 100mA			115		mΩ
N-channel On Resistance	R_{DSN}	V_{IN} = V_{GS} = 3.8V, I_{DCmLX} = -100mA			105		mΩ
Switching Frequency	F_{SW}	DC*m*_FREQ = 01			2		MHz
		DC*m*_FREQ = 10			4		

Notes:

1. Forced Continuous Conduction Mode
2. Continuous / Discontinuous Conduction with Pulse-Skipping Mode

DC-DC3 and DC-DC4

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.8V, MODE = FCCM[1], T_J = -40°C to +125°C; typical values are at T_J = 25°C

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}			2.7		5.5	V
Programmable Output Voltage	V_{OUT}			0.85[4]		3.4	V
V_{OUT} Step Size	V_{OUT_STEP}				25		mV
V_{OUT} Accuracy	V_{OUT_ACC}	V_{IN} = 2.7V to 5.5V, I_{OUT} = 0mA to 1000mA		-4		+4	%
Undervoltage margin	V_{UV}	0.85V ≤ V_{OUT} ≤ 3.4V			50		mV
Output Current	I_{OUT}	FCCM[1] and Auto (CCM/DCM with PS[2]) Modes	Independent operation (DC4_SLV=0)	0		1000	mA
			Dual mode operation (DC4_SLV=1)	0		800[5]	
		Hysteretic Mode, DC*m*_STNBY_LIM=01		0		100[3]	
		LDO Mode		0		10	
P-channel Current Limit	I_{P_LIM}				1600		mA
Quiescent Current	I_Q	I_{OUT} = 0mA, FCCM[1] and Auto (CCM/DCM with PS[2]) Modes (excluding switching losses)			330		µA
		I_{OUT} = 0mA, Hysteretic Mode			110		
		I_{OUT} = 0mA, LDO Mode			20		
Shutdown Current	I_{SD}	DC*m*_ENA = 0			0.01		µA
P-channel On Resistance	R_{DSP}	V_{IN} = V_{GS} = 3.8V, I_{DCmLX} = 100mA			165		mΩ
N-channel On Resistance	R_{DSN}	V_{IN} = V_{GS} = 3.8V, I_{DCmLX} = -100mA			155		mΩ
Switching Frequency	F_{SW}				2		MHz

Notes:

1. Forced Continuous Conduction Mode
2. Continuous / Discontinuous Conduction with Pulse-Skipping Mode
3. The maximum output current in Hysteretic mode can be adjusted using the DCm_STNBY_LIM registers
4. In FCCM mode, the minimum V_{OUT} is 1.2V
5. In Dual mode operation, the ratings are 'per converter'. The combined maximum output current is 1600mA

7.2 LDO REGULATORS

LDO1

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.8V, T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}		1.5		5.5	V
Programmable Output Voltage	V_{OUT}		0.9		3.3	V
V_{OUT} Step Size	V_{OUT_STEP}	V_{OUT} = 0.9V to 1.6V		50		mV
		V_{OUT} = 1.7V to 3.3V		100		
Output Current	I_{OUT}	Normal mode	0		300	mA
		Low power mode, LDO*n*_LP_MODE=0	0		50	
		Low power mode, LDO*n*_LP_MODE=1	0		20	
V_{OUT} Accuracy	V_{OUT_ACC}	I_{LOAD} = 1mA	-3		+3	%
Line Regulation	$V_{OUT\ LINE}$	V_{IN} = (V_{OUT} + 0.5) to 5.5V, I_{LOAD} = 150mA Note that V_{IN} must be >= 1.5V		0.1		%/V
Load Regulation	$V_{OUT\ LOAD}$	I_{LOAD} =1mA to 300mA		0.011		%/mA
Dropout Voltage	V_{IN} - V_{OUT}	I_{LOAD} =150mA, V_{OUT} > 2.7V		250		mV
		I_{LOAD} =150mA, V_{OUT} 1.8V to 2.7V		300		
		I_{LOAD} =150mA, V_{OUT} < 1.8V		500		
Undervoltage level	V_{OUT}	V_{OUT} Falling		88		%
Quiescent Current	I_Q	Normal mode, no load		30		µA
		Low power mode, LDO*n*_LP_MODE=0, no load		10		
		Low power mode, LDO*n*_LP_MODE=1, no load		5		
		I_{LOAD} = 1mA to 300mA		I_Q (no load) + 1% of load		
Power Supply Rejection Ratio	PSRR	I_{LOAD} = 150mA, <= 1kHz		53		dB
		I_{LOAD} = 150mA, 10kHz		53		
		I_{LOAD} = 150mA, 100kHz		32		
On Resistance (Switch mode)	R_{DSON}	V_{IN} = 1.5V, I_{LOAD} = 100mA		1.5		Ω
		V_{IN} = 1.8V, I_{LOAD} = 100mA		1.2		
		V_{IN} = 2.5V, I_{LOAD} = 100mA		0.85		
		V_{IN} = 3.3V, I_{LOAD} = 100mA		0.7		
Current Limit (Switch mode)	I_{CL}	V_{OUT} = 0V		600		mA
Start-up time	t_{start_up}	No load, Output cap 2.2 µF, 90% of V_{OUT}		10		µs
Shutdown time	t_{shut_down}	No load, Output cap 2.2 µF, 10% of V_{OUT}			10	ms

LDO2, LDO3

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.8V, T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}		1.5		5.5	V
Programmable Output Voltage	V_{OUT}		0.9		3.3	V
V_{OUT} Step Size	V_{OUT_STEP}	V_{OUT} = 0.9V to 1.6V		50		mV
		V_{OUT} = 1.7V to 3.3V		100		
Output Current	I_{OUT}	Normal mode	0		200	mA
		Low power mode, LDO*n*_LP_MODE=0	0		50	
		Low power mode, LDO*n*_LP_MODE=1	0		20	
V_{OUT} Accuracy	V_{OUT_ACC}	I_{LOAD} = 1mA	-3		+3	%
Line Regulation	$V_{OUT\ LINE}$	V_{IN} = (V_{OUT} + 0.5) to 5.5V, I_{LOAD} = 100mA Note that V_{IN} must be >= 1.5V		0.1		%/V
Load Regulation	$V_{OUT\ LOAD}$	I_{LOAD} =1mA to 200mA		0.011		%/mA

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Dropout Voltage	V_{IN} - V_{OUT}	I_{LOAD} =100mA, V_{OUT} > 2.7V		200		mV
		I_{LOAD} =100mA, V_{OUT} 1.8V to 2.7V		250		
		I_{LOAD} =100mA, V_{OUT} < 1.8V		400		
Undervoltage level	V_{OUT}	V_{OUT} Falling		88		%
Quiescent Current	I_Q	Normal mode, no load		30		µA
		Low power mode, LDO*n*_LP_MODE=0, no load		10		
		Low power mode, LDO*n*_LP_MODE=1, no load		5		
		I_{LOAD} = 1mA to 200mA		I_Q (no load) + 1% of load		
Power Supply Rejection Ratio	PSRR	I_{LOAD} = 100mA, <= 1kHz		55		dB
		I_{LOAD} = 100mA, 10kHz		55		
		I_{LOAD} = 100mA, 100kHz		32		
On Resistance (Switch mode)	R_{DSON}	V_{IN} = 1.5V, I_{LOAD} = 100mA		1.5		Ω
		V_{IN} = 1.8V, I_{LOAD} = 100mA		1.2		
		V_{IN} = 2.5V, I_{LOAD} = 100mA		0.85		
		V_{IN} = 3.3V, I_{LOAD} = 100mA		0.7		
Current Limit (Switch mode)	I_{CL}	V_{OUT} = 0V		400		mA
Start-up time	t_{start_up}	No load, Output cap 2.2 µF, 90% of V_{OUT}		10		µs
Shutdown time	t_{shut_down}	No load, Output cap 2.2 µF, 10% of V_{OUT}			10	ms

LDO4, LDO5, LDO6

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.8V, T_J = -40°C to +125°C; Typical values are at T_J = +25ºC.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}		1.5		5.5	V
Programmable Output Voltage	V_{OUT}		0.9		3.3	V
V_{OUT} Step Size	V_{OUT_STEP}	V_{OUT} = 0.9V to 1.6V		50		mV
		V_{OUT} = 1.7V to 3.3V		100		
Output Current	I_{OUT}	Normal mode	0		100	mA
		Low power mode, LDO*n*_LP_MODE=0	0		50	
		Low power mode, LDO*n*_LP_MODE=1	0		20	
V_{OUT} Accuracy	V_{OUT_ACC}	I_{LOAD} = 1mA	-3		+3	%
Line Regulation	$V_{OUT\ LINE}$	V_{IN} = (V_{OUT} + 0.5) to 5.5V, I_{LOAD} = 50mA Note that V_{IN} must be >= 1.5V		0.1		%/V
Load Regulation	$V_{OUT\ LOAD}$	I_{LOAD} =1mA to 100mA		0.022		%/mA
Dropout Voltage	V_{IN} - V_{OUT}	I_{LOAD} =100mA, V_{OUT} > 2.7V		200		mV
		I_{LOAD} =100mA, V_{OUT} 1.8V to 2.7V		250		
		I_{LOAD} =100mA, V_{OUT} < 1.8V		400		
Undervoltage level	V_{OUT}	V_{OUT} Falling		88		%
Quiescent Current	I_Q	Normal mode, no load		30		µA
		Low power mode, LDO*n*_LP_MODE=0, no load		10		
		Low power mode, LDO*n*_LP_MODE=1, no load		5		
		I_{LOAD} = 1mA to 100mA		I_Q (no load) + 1% of load		
Power Supply Rejection Ratio	PSRR	I_{LOAD} = 50mA, <= 1kHz		55		dB
		I_{LOAD} = 50mA, 10kHz		55		
		I_{LOAD} = 50mA, 100kHz		32		
On Resistance (Switch mode)	R_{DSON}	V_{IN} = 1.5V, I_{LOAD} = 100mA		3.2		Ω
		V_{IN} = 1.8V, I_{LOAD} = 100mA		2.1		
		V_{IN} = 2.5V, I_{LOAD} = 100mA		1.35		
		V_{IN} = 3.3V, I_{LOAD} = 100mA		1.1		

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Limit (Switch mode)	I_{CL}	V_{OUT} = 0V		230		mA
Start-up time	t_{start_up}	No load, Output cap 2.2 µF, 90% of V_{OUT}		10		µs
Shutdown time	t_{shut_down}	No load, Output cap 2.2 µF, 10% of V_{OUT}			10	ms

LDO7, LDO8

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.8V, T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}		1.71		5.5	V
Programmable Output Voltage	V_{OUT}		1.0		3.5	V
V_{OUT} Step Size	V_{OUT_STEP}	V_{OUT} = 1.0V to 1.6V		50		mV
		V_{OUT} = 1.7V to 3.5V		100		
Output Current	I_{OUT}	Normal mode	0		200	mA
		Low Power mode	0		50	
V_{OUT} Accuracy	V_{OUT_ACC}	I_{LOAD} = 1mA	-2.5		+2.5	%
Line Regulation	$V_{OUT\ LINE}$	V_{IN} = (V_{OUT} + 0.5) to 5.5V, I_{LOAD} = 100mA Note that V_{IN} must be >= 1.71V		0.025		%/V
Load Regulation	$V_{OUT\ LOAD}$	I_{LOAD} =1mA to 200mA		0.003		%/mA
Dropout Voltage	V_{IN} - V_{OUT}	I_{LOAD} =100mA, V_{OUT} =1.8V		95		mV
		I_{LOAD} =100mA, V_{OUT} =2.5V		65		
		I_{LOAD} =100mA, V_{OUT} =3.3V		60		
Undervoltage level	V_{OUT}	V_{OUT} Falling		93		%
Quiescent Current	I_Q	Normal mode, no load		110		µA
		Low Power mode, no load		70		
		I_{LOAD} = 1mA to 200mA		I_Q (no load) + 0.1% of load		
Power Supply Rejection Ratio	PSRR	I_{LOAD} = 100mA, <= 1kHz		70		dB
		I_{LOAD} = 100mA, 10kHz		67		
		I_{LOAD} = 100mA, 100kHz		48		
Output noise voltage	V_{OUT}	f=10Hz to 100kHz; V_{OUT}=2.8V, I_{LOAD} = 1mA		30		μV_{RMS}
		f=10Hz to 100kHz; V_{OUT}=2.8V, I_{LOAD} = 10mA		32		
		f=10Hz to 100kHz; V_{OUT}=2.8V, I_{LOAD} = 100mA		32		
On Resistance (Switch mode)	R_{DSON}	V_{IN} = 1.71V, I_{LOAD} = 100mA		550		mΩ
		V_{IN} = 1.8V, I_{LOAD} = 100mA		500		
		V_{IN} = 2.5V, I_{LOAD} = 100mA		330		
		V_{IN} = 3.5V, I_{LOAD} = 100mA		250		
Current Limit (Switch mode)	I_{CL}	V_{OUT} = 0V		320		mA
Start-up time	t_{start_up}	No load, Output cap 4.7 µF, 90% of V_{OUT}		50		µs
Shutdown time	t_{shut_down}	No load, Output cap 4.7 µF, 10% of V_{OUT}			10	ms

LDO9, LDO10

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.8V, T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Voltage	V_{IN}		1.71		5.5	V
Programmable Output Voltage	V_{OUT}		1.0		3.5	V
V_{OUT} Step Size	V_{OUT_STEP}	V_{OUT} = 1.0V to 1.6V		50		mV
		V_{OUT} = 1.7V to 3.5V		100		
Output Current	I_{OUT}	Normal mode	0		150	mA
		Low Power mode	0		50	

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT} Accuracy	V_{OUT_ACC}	I_{LOAD} = 1mA	-2.5		+2.5	%
Line Regulation	$V_{OUT\ LINE}$	V_{IN} = (V_{OUT} + 0.5) to 5.5V, I_{LOAD} = 75mA Note that V_{IN} must be >= 1.71V		0.025		%/V
Load Regulation	$V_{OUT\ LOAD}$	I_{LOAD} =1mA to 150mA		0.004		%/mA
Dropout Voltage	V_{IN} - V_{OUT}	I_{LOAD} =100mA, V_{OUT} =1.8V		135		mV
		I_{LOAD} =100mA, V_{OUT} =2.5V		100		
		I_{LOAD} =100mA, V_{OUT} =3.3V		90		
Undervoltage level	V_{OUT}	V_{OUT} Falling		93		%
Quiescent Current	I_Q	Normal mode, no load		110		µA
		Low Power mode, no load		70		
		I_{LOAD} = 1mA to 150mA		I_Q (no load) + 0.1% of load		
Power Supply Rejection Ratio	PSRR	I_{LOAD} = 75mA, <= 1kHz		73		dB
		I_{LOAD} = 75mA, 10kHz		69		
		I_{LOAD} = 75mA, 100kHz		49		
Output noise voltage	V_{OUT}	f=10Hz to 100kHz; V_{OUT}=2.8V, I_{LOAD} = 1mA		30		μV_{RMS}
		f=10Hz to 100kHz; V_{OUT}=2.8V, I_{LOAD} = 10mA		32		
		f=10Hz to 100kHz; V_{OUT}=2.8V, I_{LOAD} = 100mA		32		
On Resistance (Switch mode)	R_{DSON}	V_{IN} = 1.71V, I_{LOAD} = 100mA		1000		mΩ
		V_{IN} = 1.8V, I_{LOAD} = 100mA		930		
		V_{IN} = 2.5V, I_{LOAD} = 100mA		610		
		V_{IN} = 3.5V, I_{LOAD} = 100mA		430		
Current Limit (Switch mode)	I_{CL}	V_{OUT} = 0V		250		mA
Start-up time	t_{start_up}	No load, Output cap 4.7 µF, 90% of V_{OUT}		70		µs
Shutdown time	t_{shut_down}	No load, Output cap 4.7 µF, 10% of V_{OUT}			10	ms

LDO11

Unless otherwise noted: V_{IN} = 3.8V, V_{OUT} = 1.2V, T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Programmable Output Voltage	V_{OUT}		0.8		1.55	V
V_{OUT} Step Size	V_{OUT_STEP}			50		mV
Output Current	I_{OUT}	PVDD < 3.1V	0		10	mA
		PVDD ≥ 3.1V	0		25	
V_{OUT} Accuracy	V_{OUT}	V_{IN} = 2.7 to 5.5V ; I_{LOAD} = 100µA	-4		+4	%
Line Regulation	$V_{OUT\ LINE}$	V_{IN} = 2.7 to 5.5V; I_{LOAD} = 1mA		0.4		%/V
Load Regulation	$V_{OUT\ LOAD}$	I_{LOAD} = 100µA to 10mA		0.2		%/mA
Quiescent Current	I_Q	No load		2.5		µA
Start-up time	t_{start_up}	No load, Output cap 0.1 µF, 90% of V_{OUT}		0.3	1	ms
Shutdown time	t_{shut_down}	No load, Output cap 0.1 µF, 10% of V_{OUT}		0.3	1	ms

7.3 RESET THRESHOLDS

Unless otherwise noted: T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power On Reset						
Power on Reset threshold VPMIC (LDO12VOUT) voltage at which device transitions between NO POWER and BACKUP states	$V_{POR, DE-ASSERT}$	VPMIC rising		1.18		V
	$V_{POR, ASSERT}$	VPMIC falling		1.08		V
Power on Reset hysteresis	$V_{POR, HYST}$			100		mV
Device Reset Control						
Device Reset threshold VPMIC (LDO12VOUT) voltage at which device transitions between BACKUP and OFF states	$V_{RES, DE-ASSERT}$	VPMIC rising		1.89		V
	$V_{RES, ASSERT}$	VPMIC falling		1.80		V
Device Reset hysteresis	$V_{RES, HYST}$			90		mV
Device Shutdown						
Shutdown threshold PVDD voltage at which the device forces an OFF transition	$V_{SHUTDOWN}$	PVDD falling		2.7		V
SYSLO threshold accuracy PVDD voltage at which SYSLO is asserted.	V_{SYSLO}	PVDD falling, V_{SYSLO} set by SYSLO_THR (2.8V to 3.5V)	-3		+3	%
SYSOK threshold accuracy PVDD voltage at which SYSOK is asserted.	V_{SYSOK}	PVDD rising, V_{SYSOK} set by SYSOK_THR (2.8V to 3.5V) Note the SYSOK hysteresis margin ($V_{SYSOK, HYST}$) is added to SYSOK_THR.	-3		+3	%
SYSOK hysteresis	$V_{SYSOK, HYST}$			40		mV

7.4 REFERENCES

Unless otherwise noted: T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voltage Reference	V_{VREFC}			0.8		V
Current Reference	V_{IREFR}	100kΩ to GND		0.5		V

7.5 GENERAL PURPOSE INPUTS / OUTPUTS (GPIO)

Unless otherwise noted: T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIO1, GPIO2, GPIO3, GPIO7, GPIO8, GPIO9						
Input HIGH Level	V_{IH}		0.75 x VDD			V
Input LOW Level	V_{IL}				0.25 x VDD	V
Output HIGH Level	V_{OH}	I_{OH} = 1mA	0.8 x VDD			V
Output LOW Level	V_{OL}	I_{OL} = -1mA			0.2 x VDD	V
Pull-up resistance to VDD	R_{PU}	GPn_PWR_DOM=0 and DBVDD=1.8V or GPn_PWR_DOM=1		180		kΩ
Pull-down resistance	R_{PD}			180		kΩ
GPIO4, GPIO5, GPIO6, GPIO10, GPIO11, GPIO12						
Input HIGH Level	V_{IH}		0.85 x VDD			V
Input LOW Level	V_{IL}				0.2 x VDD	V
Output HIGH Level	V_{OH}	I_{OH} = 1mA	0.75 x VDD			V
Output LOW Level	V_{OL}	I_{OL} = -1mA			0.2 x VDD	V
Pull-up resistance to VDD	R_{PU}	GPn_PWR_DOM=0 and DBVDD=1.8V or GPn_PWR_DOM=1 and PVDD=3.8V		180		kΩ
Pull-down resistance	R_{PD}			180		kΩ

Notes:

1. 'VDD' is the voltage of the applicable power domain for each pin (selected by the corresponding GPn_PWR_DOM register).
2. Pull-up / pull-down resistance only applies when enabled using the GPn_PULL registers.
3. Pull-up / pull-down resistors are disabled when the GPIO pin is tri-stated.
4. Pull-up / pull-down resistance may change with the applicable power domain (as selected by GPn_PWR_DOM).

7.6 DIGITAL INTERFACES

Unless otherwise noted: T_J = -40°C to +125°C; Typical values are at T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{ON}$, $\overline{RESET}$, $\overline{IRQ}$, CIFMODE, SDOUT1, SCLK1, SDA1, $\overline{CS}$, SCLK2, SDA2						
Input HIGH Level	V_{IH}		0.75 x VDD			V
Input LOW Level	V_{IL}				0.2 x VDD	V
Output HIGH Level	V_{OH}	I_{OH} = 1mA	0.8 x VDD			V
Output LOW Level	V_{OL}	I_{OL} = -1mA			0.2 x VDD	V
'VDD' is the voltage of the applicable power domain for each pin, as defined in Section 3.						
ON pin pull-up resistance	R_{PU}			140		kΩ
RESET pin pull-up resistance	R_{PU}	DBVDD=1.8V		180		kΩ
		DBVDD=3.6V		85		
IRQ pin pull-up resistance	R_{PU}	DBVDD=1.8V		180		kΩ
		DBVDD=3.6V		85		
SCLK2 pin pull-down resistance	R_{PD}			100		kΩ
SDA2 pin pull-down resistance	R_{PD}			100		kΩ

7.7 AUXILIARY ADC

Unless otherwise noted: T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input resistance	$R_{GPIO10, 11, 12}$	During measurement		400		kΩ
Input voltage range	$V_{GPIO10, 11, 12}$	GPn_PWR_DOM = 0	0		V_{DBVDD}	V
		GPn_PWR_DOM = 1	0		V_{PVDD}	
Input capacitance	$C_{GPIO10, 11, 12}$			2		pF
AUXADC Resolution				12		bits
AUXADC Conversion Time				39		µs
AUXADC accuracy		Input voltage = 3V	-2.5		+2.5	%

7.8 SYSTEM STATUS LED DRIVERS

Unless otherwise noted: T_J = +25ºC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LED1 and LED2						
Sink current		$V_{LED1/2}$ = 1V		10		mA

8 TYPICAL POWER CONSUMPTION

Data to follow