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WM8351

Wolfson AudioPlus™ Stereo CODEC with Power Management

DESCRIPTION

The WM8351 is an integrated audio and power management subsystem which provides a cost effective, single-chip solution for portable audio and multimedia systems.

The integrated audio CODEC provides all the necessary functions for high-quality stereo recording and playback. Programmable on-chip amplifiers allow for the direct connection of headphones and microphones with a minimum of external components. A programmable low-noise bias voltage is available to feed one or more electret microphones. Additional audio features include programmable high-pass filter in the ADC input path.

The WM8351 includes four programmable DC-DC converters, four low-dropout (LDO) regulators and a current limit switch to generate suitable supply voltages for each part of the system, including the integrated audio CODEC as well as off-chip components such as a digital core and I/O supplies, and LED lighting. An additional on-chip regulator maintains the backup power for always-on functions. The WM8351 can be powered by a lithium battery, by a wall adaptor or USB.

An on-chip battery charger supports both trickle charging and fast (constant current, constant voltage) charging of single-cell lithium batteries. The charge current, termination voltage, and charger time-out are programmable to suit different types of batteries.

Internal power management circuitry controls the start-up and shutdown sequencing of clocks and supply voltages. It also detects and handles conditions such as under-voltage, extreme temperatures, and deeply discharged or defective batteries, with a minimum of software involvement.

A programmable constant-current sink is available for driving LED strings, e.g. for display backlights or photo-flash applications, in a highly power-efficient way. Additional RGB LEDs can be driven through GPIO pins.

The WM8351 includes a 32.768kHz crystal oscillator, an internal RC oscillator, a real-time clock (RTC) and an alarm function capable of waking up the system. Internal circuitry can generate all clock signals required to start up the device.

The master clock for the audio CODEC can be input directly, or may be generated internally using an integrated, low power Frequency Locked Loop (FLL).

To extend battery life, fine-grained power management enables each function in the WM8351 to be independently powered down through the control interface. The WM8351 forms part of the Wolfson AudioPlus™ series of audio and power management solutions.

FEATURES

Stereo Hi-Fi CODEC

- DAC SNR 95dB ('A' weighted @ 48kHz), THD –81dB
- ADC SNR 95dB ('A' weighted @ 48kHz), THD –83dB
- 40mW on-chip headphone driver with 'capless' option
- 16Ω headphone load: THD -72dB, Po = 20mW
- 2 differential microphone inputs with low-noise bias voltage and programmable preamps
- Programmable high-pass filter for ADC
- Microphone and Headphone detection
- Auxiliary inputs for analogue signals
- Sample rates: 8, 11.025, 16, 22.05, 24, 32, 44.1 or 48kHz

System Control

- Support for 2-wire or 3-/4-wire Control Interface
- Handles power sequencing, reset signals and fault conditions
- Autonomous power source selection (battery, wall adaptor or USB bus)
- Total current drawn from USB bus is limited to comply with USB 2.0 standard and USB OTG supplement

Supply Generation

- 1 x DC-DC Buck Converter (0.85V - 3.4V, Up to 1A)
- 2 x DC-DC Buck Converters (0.85V - 3.4V, Up to 500mA)
- 1 x DC-DC Boost Converter (5V - 20V, 40 to 200mA)
- 4 x LDO voltage regulators (0.9V - 3.3V, 150mA)

LED Drivers

- Programmable constant-current sink, suitable for screen backlight or white LED photo flash
- 3 open-drain outputs for RGB LEDs

Battery Charger

- Single-cell Li-Ion / Li-Pol battery charger
- Thermal protection for charge control; temperature monitoring available for thermal regulation
- LED outputs to indicate charge status and fault conditions

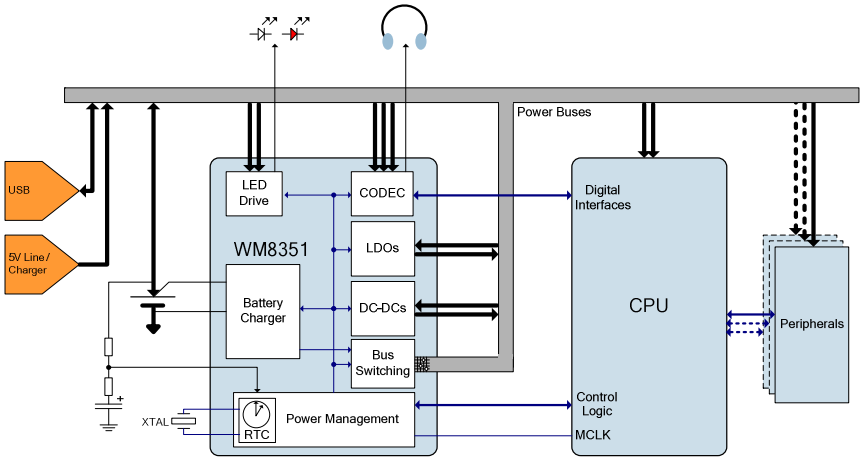
Additional Features

- "Always on" RTC with wake-up alarm
- Watchdog timer
- Up to 13 configurable GPIO pins
- On-chip crystal oscillator and internal RC oscillator
- Low power FLL supporting wide range of input clocks
- 7x7mm, 129 BGA package, 0.5mm ball pitch

APPLICATIONS

- Portable Audio and Media players
- Portable Navigation Devices
- Portable systems powered by single-cell lithium batteries

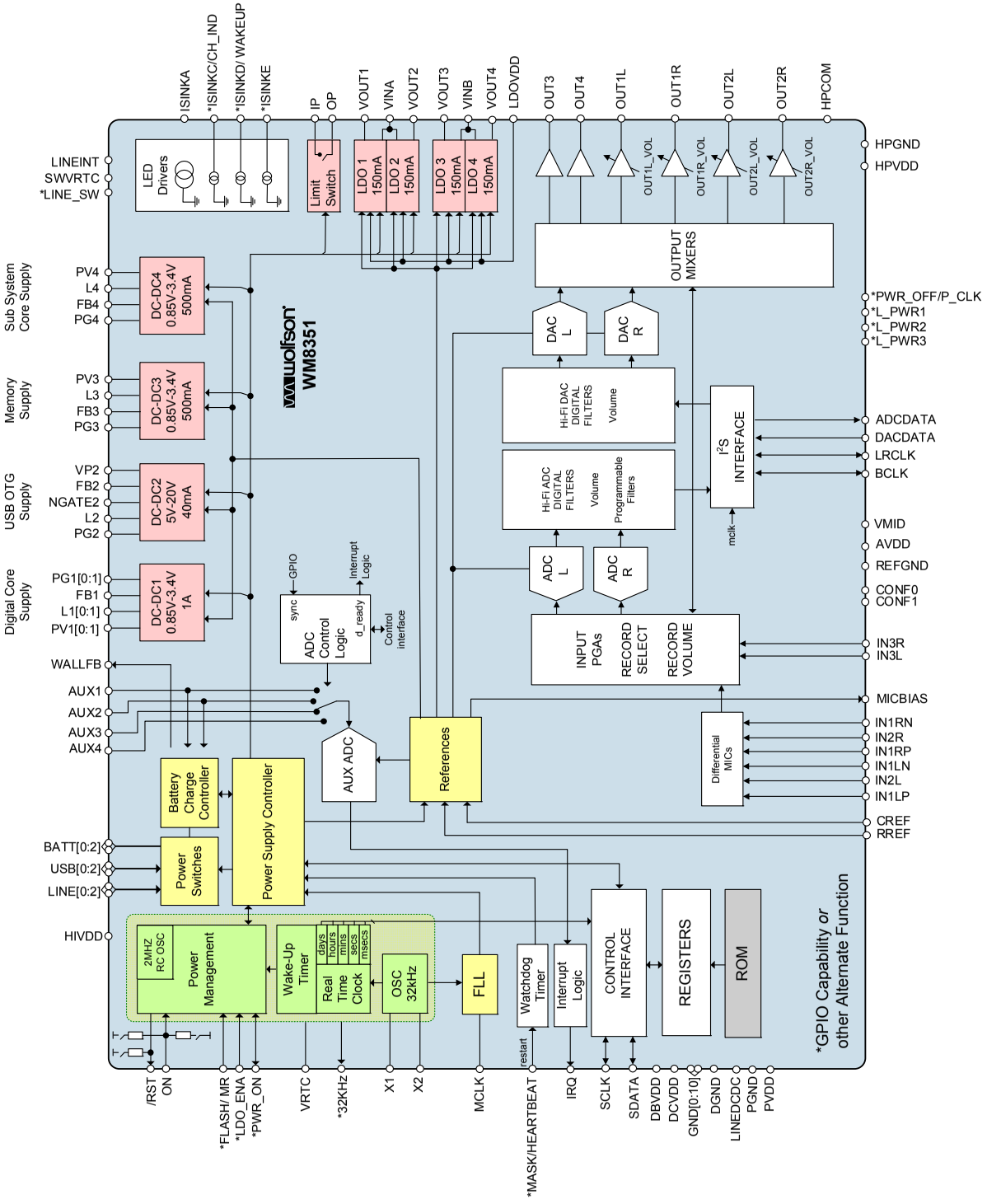
TYPICAL APPLICATIONS



The WM8351 is a complete audio and power management solution for portable media devices. The device incorporates three programmable step-down switching regulators, a step-up switching regulator, a full-featured battery charger, four Low Drop-Out (LDO) voltage regulators which can also serve as hot-swap outputs, a backup supply regulator, a programmable white LED driver, a Real-Time Clock (RTC) alongside a 32.768kHz (32kHz) oscillator capable of operating from a backup battery, a 12-bit auxiliary ADC for precise measurements, a ROM-programmable power management state machine and numerous protection features all in a single 7x7mm BGA package. When only battery power is available, a battery switch provides power to all switching regulators (and some other internal modules). When external power is applied (eg. from USB or Wall adapter), the WM8351 seamlessly transitions from battery power (a single-cell Lithium battery) to the applicable external supply. The battery charger is then activated, all internal power for the device is drawn from the appropriate external power source and the battery is disconnected from the load. Maximum battery charge current and charge time are programmable. The USB power manager provides accurate current limiting for the USB pin under all conditions. The hot-swap outputs (LDOs in current-limited 'Switch Mode' operation) are ideal for powering memory cards and other devices that can be inserted while the system is fully powered.

The integrated Hi-Fi stereo CODEC incorporates preamps and a low-noise bias voltage for differential microphones, and flexible pseudo-differential drivers for headphone and differential/single-ended line outputs. External component requirements are reduced as no separate microphone or headphone amplifiers are required. Digital filter options are available in the ADC and DAC paths, to cater for application filtering. The WM8351 is capable of operating without any external clock, as it can derive all required clocks from its internal crystal oscillator, RC clock, and Frequency Locked Loop. An external low jitter clock may be required in some applications for high performance audio.

BLOCK DIAGRAM



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1 PIN CONFIGURATION

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	DNC	DNC	OP	PV1	L1	PG1	DNC	DNC	DNC	DNC	GPIO12	FB2	PG2
B	DNC	DNC	IP	PV1	L1	PG1	DNC	DNC	DNC	PVDD	GPIO10	NGATE2	VP2
C	L4	PG4	FB4	DNC	LINEDCDC	FB1	GND	GND	AUX4	GPIO11	PGND	PG3	L2
D	PV4	BATT	HIVDD	N/A	N/A	N/A	N/A	N/A	N/A	N/A	FB3	PV3	L3
E	BATT	BATT	WALLFB	N/A	N/A	N/A	N/A	N/A	N/A	N/A	ISINKA	DNC	SINKGND
F	LINE	LINE	LINE	N/A	N/A	GND	GND	GND	N/A	N/A	VOUT4	LDOVDD	VINB
G	USB	USB	USB	N/A	N/A	GND	GND	GND	N/A	N/A	VOUT2	VOUT3	VINA
H	VRTC	LINEINT	CREF	N/A	N/A	GND	GND	GND	N/A	N/A	AUX1	VOUT1	AUX3
J	CONF0	X1	RREF	N/A	N/A	N/A	N/A	N/A	N/A	N/A	OUT1R	HPCOM	AUX2
K	CONF1	ON	X2	N/A	N/A	N/A	N/A	N/A	N/A	N/A	OUT1L	OUT4	HPVDD
L	GPIO0	/RST	SWVRTC	IRQ	GPIO5	GPIO8	GPIO9	BCLK	LRCLK	IN3L	IN1LN	OUT3	HPGND
M	GPIO2	GPIO1	SDA	GPIO6	DGND	MCLK	ADCDATA	AVDD	IN3R	INL2	MICBIAS	OUT2R	OUT2L
N	GPIO3	SCL	GPIO4	GPIO7	DCVDD	DBVDD	DACDATA	REFGND	VMID	IN1LP	INR2	IN1RP	IN1RN

7mm x 7mm BGA, Z

Notes: Pin names beginning with a lower-case "n" indicate that the pin is active low.
Colour coding indicates function of pins in typical usage:

- DC-DC converters
- LDO voltage regulators
- Power management functions
- Analogue pins for audio codec
- Digital pins for audio codec
- Quiet ground
- Others

2 ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8351GEB/V	-25°C to +85°C	129-ball BGA (7 x 7 mm) (Pb-free)	MSL3	260°C
WM8351GEB/RV	-25°C to +85°C	129-ball BGA (7 x 7 mm) (Pb-free, tape and reel)	MSL3	260°C

Note:

Reel quantity = 2,200

3 PIN DESCRIPTION

Notes:

Pins are listed in alphabetical order by name.

NAME	LOCATION(S)	TYPE	POWER DOMAIN	DESCRIPTION
ADCDATA	M7	Digital Output	DBVDD	Digital audio output (typically from on-chip audio ADC to external IC)
AUX1	H11	Analogue Input	LINE	Auxiliary ADC input AUX1 (Special function for connection to temperature-sensing NTC resistor in battery pack)
AUX2	J13	Analogue Input	LINE	Auxiliary ADC input AUX2
AUX3	H13	Analogue Input	LINE	Auxiliary ADC input AUX3
AUX4	C9	Analogue Input	LINE	Auxiliary ADC input AUX4
AVDD	M8	Supply		Analogue supply for audio CODEC
BATT	E1, E2, D2	Analogue I/O		Main battery power connection (can draw power or charge battery)
BCLK	L8	Digital I/O	DBVDD	Bit clock signal for digital audio interface
CREF	H3	Analogue Output	VRTC	Decoupling for VREF reference voltage (connect capacitor here)
CONF0	J1	Digital Input	VRTC	Start-up configuration pin 0
CONF1	K1	Digital Input	VRTC	Start-up configuration pin 1
DACDATA	N7	Digital Input	DBVDD	Digital audio input (typically from external IC to on-chip audio DAC)
DCVDD	N5	Supply		Digital core supply; powers digital core of audio CODEC
DBVDD	N6	Supply		Digital I/O buffer supply; powers digital audio interface, control interface and pins GPIO4 to GPIO9
DGND	M5	Supply		Digital ground; return path for DCVDD and DBVDD supplies
FB1	C6	Analogue Input	PV1	DC-DC1 feedback pin
FB2	A12	Analogue Input	VP2	DC-DC2 feedback pin
FB3	D11	Analogue Input	PV3	DC-DC3 feedback pin
FB4	C3	Analogue Input	PV4	DC-DC4 feedback pin
GND	F6, F7, F8, G6, G7, G8, H6, H7 H8, C7, C8	Supply		Quiet ground connection for audio CODEC. Note that DC-DC Converters use a separate ground connection.
GPIO0	L1	Digital I/O	VRTC	General Purpose Input/Output pin 0
GPIO1	M2	Digital I/O	VRTC	General Purpose Input/Output pin 1
GPIO2	M1	Digital I/O	VRTC	General Purpose Input/Output pin 2
GPIO3	N1	Digital I/O	VRTC	General Purpose Input/Output pin 3
GPIO4	N3	Digital I/O	DBVDD	General Purpose Input/Output pin 4
GPIO5	L5	Digital I/O	DBVDD	General Purpose Input/Output pin 5
GPIO6	M4	Digital I/O	DBVDD	General Purpose Input/Output pin 6
GPIO7	N4	Digital I/O	DBVDD	General Purpose Input/Output pin 7
GPIO8	L6	Digital I/O	DBVDD	General Purpose Input/Output pin 8
GPIO9	L7	Digital I/O	DBVDD	General Purpose Input/Output pin 9
GPIO10	B11	Digital I/O	LINE	General Purpose Input/Output pin 10
GPIO11	C10	Digital I/O	LINE	General Purpose Input/Output pin 11
GPIO12	A11	Digital I/O	LINE	General Purpose Input/ Output pin 12
HIVDD	D3	Analogue Output		Analogue output from power management unit which determines highest supply from Line, Battery or USB.
HPCOM	J12	Analogue Input	HPVDD	Headphone output amplifier noise compensation input
HPGND	L13	Supply	HPVDD	Headphone ground; return path for HPVDD supply
HPVDD	K13	Supply		Headphone supply – powers the analogue outputs OUT1L, OUT1R, OUT2L, OUT2R, OUT3 and OUT4
IN1LN	L11	Analogue Input	AVDD	Inverting input for left microphone channel

NAME	LOCATION(S)	TYPE	POWER DOMAIN	DESCRIPTION
IN1LP	N10	Analogue Input	AVDD	Non-inverting input 1 for left microphone channel
IN1RN	N13	Analogue Input	AVDD	Inverting input for right microphone channel
IN1RP	N12	Analogue Input	AVDD	Non-inverting input 1 for right microphone channel
IN2L	M10	Analogue Input	AVDD	Non-inverting input 2 for left microphone channel
IN2R	N11	Analogue Input	AVDD	Non-inverting input 2 for right microphone channel
IN3L	L10	Analogue Input	AVDD	Auxiliary input for analogue audio signals (left channel)
IN3R	M9	Analogue Input	AVDD	Auxiliary input for analogue audio signals (right channel)
IP	B3	Analogue Input		Power input to current limit switch
ISINKA	E11	Analogue Output	LDOVDD	Constant-current LED driver A
L1	A5, B5	Analogue I/O	PV1	DC-DC1 inductor connection
L2	C13	Analogue I/O	VP2	DC-DC2 inductor connection
L3	D13	Analogue I/O	PV3	DC-DC3 inductor connection
L4	C1	Analogue I/O	PV4	DC-DC4 inductor connection
LDOVDD	F12	Supply		LDO amplifier supply voltage
LINEDCDC	C5	Supply		Supply connection for DC-DC 1 and 4 control circuits
LINEINT	H2	Supply		Supply connection for Internal Reference circuits
LINE	F1, F2, F3	Supply		LINE supply connection
LRCLK	L9	Digital I/O	DBVDD	Word clock (left/right clock) signal for digital audio interface
MCLK	M6	Digital I/O	DBVDD	Master Clock (may be generated internally or externally)
MICBIAS	M11	Analogue Output	AVDD	Low-noise bias voltage for condenser microphones (connect decoupling capacitor here)
NGATE2	B12	Analogue Output	VP2	DC-DC2 connection to gate of external power FET
IRQ	L4	Digital Output open-drain	DBVDD	Interrupt signal from WM8351 to host processor
ON	K2	Digital Input	VRTC	Connection for power-on switch
/RST	L2	Digital Output open-drain	DBVDD	System Reset Signal (active low)
OP	A3	Analogue Output		Power output from current limit switch
OUT1L	K11	Analogue Output	AVDD	Left channel analogue audio output 1
OUT2L	M13	Analogue Output	AVDD	Left channel analogue audio output 2
OUT1R	J11	Analogue Output	AVDD	Right channel analogue audio output 1
OUT2R	M12	Analogue Output	AVDD	Right channel analogue audio output 2
OUT3	L12	Analogue Output	AVDD	Analogue audio output 3 (or pseudo-ground output for capacitor-less headphone outputs)
OUT4	K12	Analogue Output	AVDD	Analogue audio output 4
PG1	A6, B6	Supply		DC-DC1 power ground
PG2	A13	Supply		DC-DC2 power ground
PG3	C12	Supply		DC-DC3 power ground
PG4	C2	Supply		DC-DC4 power ground
PGND	C11	Supply		Ground connection
PV1	A4, B4,	Supply		DC-DC1 line or battery power input
PV3	D12	Supply		DC-DC3 line or battery power input
PV4	D1	Supply		DC-DC4 line or battery power input
PVDD	B10	Supply		Supply connection for DC-DC 2 and 3 control circuits
REFGND	N8	Supply		Reference ground for audio ADC and DAC
RREF	J3	Analogue Output		Connection for external 100kΩ current reference resistor
SCLK	N2	Digital Input	DBVDD	Clock signal for 2-wire serial control interface (5V Tolerant)
SDATA	M3	Digital I/O	DBVDD	Data line for 2-wire serial control interface (5V Tolerant)
SINKGND	E13	Supply		Ground connection for ISINKA
SWVRTC	L3	Analogue Output	VRTC	Switchable VRTC output. Typically used for battery temperature monitoring

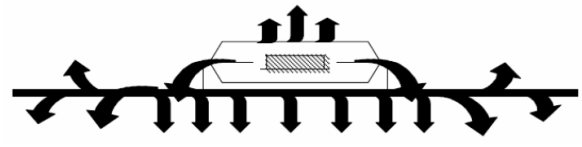
NAME	LOCATION(S)	TYPE	POWER DOMAIN	DESCRIPTION
USB	G1, G2, G3	Supply		Connection to USB power rail
VINA	G13	Supply		Input to voltage regulators LDO1 and LDO2
VINB	F13	Supply		Input to voltage regulators LDO3 and LDO4
VMID	N9	Analogue I/O	AVDD	Reference voltage (normally AVDD/2) for audio CODEC (connect capacitor here)
VOUT1	H12	Analogue Output	VINA	Output of voltage regulator LDO1
VOUT2	G11	Analogue Output	VINA	Output of voltage regulator LDO2
VOUT3	G12	Analogue Output	VINB	Output of voltage regulator LDO3
VOUT4	F11	Analogue Output	VINB	Output of voltage regulator LDO4
VP2	B13	Supply		DC-DC2 power input
VRTC	H1	Supply		Backup power connection (WM8351 can draw power from this pin or re-charge the backup power source)
WALLFB	E3	Analogue Input	LINE	Connection to Wall feedback
X1	J2	Analogue Input	VRTC	Connection for 32.768kHz crystal (input to oscillator from crystal) or 32.768kHz external clock input (when not using crystal)
X2	K3	Analogue Output	VRTC	Connection for 32.768kHz crystal (output from oscillator to crystal)
DNC	A1, A2, A7, A8, A9, A10, B1, B2, B7, B8, B9, C4, E12			Do Not Connect

4 THERMAL CHARACTERISTICS

Thermal analysis must be performed in the intended application to prevent the WM8351 from exceeding maximum junction temperature. Several contributing factors affect thermal performance most notably the physical properties of the mechanical enclosure, location of the device on the PCB in relation to surrounding components and the number of PCB layers. Connecting the nine central GND balls through thermal vias and into a large ground plane will aid heat extraction.

Three main heat transfer paths exist to surrounding air:

- Package top to air (radiation).
- Package bottom to PCB (radiation).
- Package leads to PCB (conduction).



The temperature rise T_R is given by $T_R = P_D * \Theta_{JA}$

- P_D is the power dissipated by the device.
- Θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature and is therefore a measure of heat transfer from the die to surrounding air.
- For WM8351, Θ_{JA} = 32°C/W

The junction temperature T_J is given by $T_J = T_A + T_R$

1. T_A, is the ambient temperature.

The worst case conditions are when the WM8351 is operating in a high ambient temperature, with low supply voltage, high duty cycle and high output current. Under such conditions, it is possible that the heat dissipated could exceed the maximum junction temperature of the device. Care must be taken to avoid this situation. An example calculation of the junction temperature is given below.

- P_D = 1W (example figure)
- Θ_{JA} = 32°C/W
- $T_R = P_D * \Theta_{JA}$ = 32°C
- T_A = 85°C (example figure)
- $T_J = T_A + T_R$ = 117°C

The minimum and maximum operating junction temperatures for the WM8351 are quoted in Section 5. The maximum junction temperature is 125°C. Therefore, the junction temperature in the above example is within the operating limits of the WM8351.

5 ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The WM8351 has been classified as MSL3.

CONDITION	MIN	MAX
BATT, LINE and USB voltage	-0.3V	+7V
Input voltage for LDO regulators (pins VINA, VINB)	-0.3V	+7V
Analogue supply voltages (AVDD, HPVDD)	-0.3V	+4.5V
Digital supply voltages (DCVDD, DBVDD)	-0.3V	+4.5V
Voltage range for CODEC analogue inputs	-0.3V	AVDD + 0.3V
Voltage range for digital inputs	-0.3V	DBVDD + 0.3V
Master Clock Frequency (When MCLK_DIV set to divide by 2)		37MHz
Operating Temperature Range, T_A	-25°C	+85°C
Junction Temperature, T_J	-20°C	+125°C
Thermal Impedance Junction to Ambient, θ_{JA}		32°C/W
Storage temperature prior to soldering	30°C max / 60% RH max	
Storage temperature after soldering	-65°C	+150°C
Soldering temperature (10 seconds)		+260°C
Note: These ratings assume that all ground pins are at 0V.		

6 RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Digital Supply Range (Core)	DCVDD	1.71		3.6	V
Digital Supply Range (Buffer)	DBVDD	1.71		3.6	V
Headphone Supply Range	HPVDD	2.5		3.6	V
Analogue Supply Range	AVDD	2.5		3.6	V
Line Input Source	LINE	2.95		5.5	V
Battery Input Source	BATT	2.95		4.2	V
USB Input Source	USB	4.75		5.25	V
LDO Input Source	VINA, VINB	0		5.5	V
Ground	GND, PGND, DGND, HPGND, REFGND, PG1, PG2, PG3, PG4		0		V

7 ELECTRICAL CHARACTERISTICS

7.1 HI-FI AUDIO CODEC

Test Conditions

DCVDD = 1.8V, AVDD = HPVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Preamp Inputs (IN1LP, IN1LN, IN1RP, IN1RN)						
Full-scale Input Signal Level (0dB) – note this changes with AVDD	V_{INFS}			1 0		V rms dBV
Mic preamp equivalent input noise	At 35.25dB gain			150		µV
Input resistance	R_{MICIN}	Gain set to 35.25dB		2.3		kΩ
Input resistance	R_{MICIN}	Gain set to 0dB		64		kΩ
Input resistance	R_{MICIN}	Gain set to -12dB		101		kΩ
Input Capacitance	C_{MICIN}			2		pF
Recommended decoupling cap	C_{DECOUP}			0.33		µF
MIC Programmable Gain Amplifier (PGA)						
Programmable Gain			-12		35.25	dB
Programmable Gain Step Size		Monotonic		0.75		dB
Mute Attenuation				-90		dB
Selectable Input Gain Boost (0/+20dB)						
Gain Boost			0		20	dB
Auxiliary Analogue Inputs (IN3L, IN3R)						
Full-scale Input Signal Level (0dB) – note this changes with AVDD	V_{INFS}			1.0 0		Vrms dBV
PGA gain range to summer			-12		+6	dB
PGA step size to summer				3		dB
Input Resistance	R_{AUXIN}			32		kΩ
Input Capacitance	C_{AUXIN}			10		pF
Analogue to Digital Converter (ADC)						
Signal to Noise Ratio (Note 1, 2)		A-weighted, 0dB gain	86	95		dB
Total Harmonic Distortion (Note 4)		-2dBV Input	-75	-83		dB
Digital to Analogue Converter (DAC) to Line-Out (OUT1L, OUT1R with 10kΩ / 50pF load)						
Full-scale output		PGA gains set to 0dB		HPVDD/3.3		Vrms
Signal to Noise Ratio (Note 1, 2)	SNR	A-weighted	90	95		dB
Total Harmonic Distortion (Note 3)	THD+N	R_L = 10kΩ full-scale signal	-75	-81		dB
Channel Separation (Note 4)		1kHz signal		89		dB
Output Mixers						
PGA gain range into mixer			-15	0	+6	dB
PGA gain step into mixer				3		dB
Analogue Output PGAs (OUT1L, OUT1R, OUT2L, OUT2R)						
Programmable Gain range			-57	0	+6	dB
Programmable Gain step size		Monotonic		1		dB
Mute attenuation		1kHz, full scale signal		78		dB
Headphone Output (OUT1L, OUT1R, OUT2L, OUT2R)						
0dB full scale output voltage				HPVDD/3.3		Vrms
Signal to Noise Ratio	SNR	A-weighted	87	96		dB
Total Harmonic Distortion (Note 3)	THD+N	R_L = 16Ω, Po=20mW HPVDD=3.3V	-65	-72		dB
		R_L = 32Ω, Po=20mW HPVDD=3.3V		-71		dB

Test Conditions

DCVDD = 1.8V, AVDD = HPVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUT3/OUT4 outputs (with 10kΩ / 50pF load)						
Full-scale output				HPVDD/3.3		Vrms
Signal to Noise Ratio (Note 1, 2)	SNR	A-weighted	90	97		dB
Total Harmonic Distortion (Note 3)	THD	R_L = 10kΩ full-scale signal	-77	-83		dB
Channel Separation (Note 4)		5kHz signal		80		dB
Microphone Bias						
Bias Voltage	$V_{MICBIAS}$	MBVSEL=0		0.9*AVDD		V
		MBVSEL=1		0.75*AVDD		V
Bias Current Source	$I_{MICBIAS}$			3		mA
Output Noise Voltage	Vn	1kHz to 20kHz		24		nV/√Hz
Digital Input / Output						
Input HIGH Level	V_{IH}		0.7×DBVDD			V
Input LOW Level	V_{IL}				0.3×DBVDD	V
Output HIGH Level	V_{OH}	I_{OL}=1mA	0.9×DBVDD			V
Output LOW Level	V_{OL}	I_{OH}-1mA			0.1xDBVDD	V
Frequency Locked Loop (FLL)						
Reference clock frequency	F_{REF}		0.032		22	MHz
Jack Detect						
Detection switch threshold	V_{IH}		0.7xAVDD			V
	V_{IL}				0.3xAVDD	V
HPCOM						
Ground noise rejection	V_{IH}			40		dB
	V_{IL}			40		dB

TERMINOLOGY

1. Signal-to-noise ratio (dB) = SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) = DR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (E.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) = THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Channel Separation (dB) = Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.

7.2 DC-DC STEP UP CONVERTER ELECTRICAL CHARACTERISTICS

Test Conditions
T_A = +25ºC unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC-DC2						
Input voltage range	V_{IN}	when used as converter	2.7	3.7	5.5	V
		when used as switch	1.2			
Output voltage range	V_{OUT}	by default (needs external component configuration)	V_{IN}		20 (30)	V
USB OTG output voltage	$V_{OUT,USB}$	V_{IN}<4.5V; I_{OUT}<100mA; DC2_FBSRC [1:0]=11		5.0		V
Output current	I_{OUT}	V_{OUT}=30V	0		25	mA
		V_{OUT}=20V (DC2_ILIM_=1)			40 (18)	
		V_{OUT}=5.0V (DC2_ILIM_=1)			170 (100)	
Switch resistance	R_{ON}	V_{IN}=3.3V; V_{OUT}=3.2V; +25°C		0.26		Ω
		V_{IN}=1.8V; V_{OUT}=1.7V; +25°C		0.41		
		V_{IN}=1.2V; V_{OUT}=1.1V; +25°C		0.84		
Maximum switch current	$I_{SW,MAX}$				700	mA
Switching frequency	f_{CLK}			1.0		MHz
Maximum duty cycle	D_{MAX}	V_{IN}=3V; f_{CLK}=1.0MHz		90		%
Efficiency	H	V_{IN}=3.8V; V_{OUT}=20V; I_{OUT}=20mA		75		%
		V_{IN}=3.8V; V_{OUT}=5.0V; I_{OUT}=100mA		88		
Quiescent current	I_{DD}	Shutdown or switch configuration		0.1		uA
		active; no switching		260		
		active; pulse skipping		260		
Regulated feedback voltage	V_{FB}	DC2_FBSRC [1:0] = 00		0.5		V
	V_{CURR}	DC2_FBSRC [1:0] = 01 or 10		0.5		
Undervoltage detect	$V_{FB,UV}$	below feedback voltage		12		%
	$V_{USB,UV}$	DC2_FBSRC [1:0] = 11		4.6		V
Overvoltage detect	$V_{FB,OV}$	above feedback voltage		8		%
	$V_{USB,OV}$	DC2_FBSRC [1:0] = 11		5.4		V
Peak inductor current limit	I_{PK}	V_{IN}=3V; V_{OUT}=90%;		700		mA
		DC2_ILIM_=1		450		
On resistance of NGATE driver	R_{NGATE}	P-Channel FET (I_{PFET}=100mA)		4.6		Ω
		N-Channel FET (I_{NFET}=100mA)		4.9		
Input capacitor	C_{IN}	X5R/X7R dielectric	1.0	2.2		µF
Inductor	L_F		-30%	10	+30%	µH
Inductor current rating	$I_{SAT,Lf}$		500			mA
		DC2_ILIM_=1	320			
Output capacitor	C_{OUT}	DC2_FBSRC [1:0]= 00 or 11; V_{OUT}=5V	3.7	10	22	µF
		DC2_FBSRC [1:0]= 00; V_{OUT}=10V	0.84	2.2	4.7	
		DC2_FBSRC [1:0]= 00; V_{OUT}=20V	0.18	0.47	1.0	
		DC2_FBSRC [1:0]= 01 or 10; V_{OUT}=10V	2.0	4.7	10	
		DC2_FBSRC [1:0]= 01 or 10; V_{OUT}=15V	1.5	2.2	10	
		DC2_FBSRC [1:0]= 01 or 10; V_{OUT}=20V	0.9	1.5	4.7	

7.3 DC-DC STEP DOWN CONVERTER ELECTRICAL CHARACTERISTICS

Test Conditions

V_{IN} = 3.7, V_{OUT} = 1.8V, T_A = +25ºC unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
DC-DC1								
Input Voltage	V_{IN}				2.7	3.7	5.5	V
Output Voltage	V_{OUT}				0.85		3.4	V
VOUT Accuracy	V_{OUT}	V_{IN} = 3.7V V_{OUT} = 0.85V / 1.8V / 3.4V	I_{OUT} = 0.5A	Active		+/- 3.0		%
			I_{OUT} = 0.005A	Sleep		-1.5 +4.5		
Line Regulation	$V_{OUT\ LINE}$	V_{IN} = 2.7V to 5.5V V_{OUT} = 1.8V	I_{OUT} = 0.5A	Active		+/- 0.5		%
			I_{OUT} = 0.1A	Standby		+/- 0.25		
			I_{OUT} = 0.005A	Sleep		+/- 0.4	+/- 0.5	
Load Regulation	$V_{OUT\ LOAD}$	I_{OUT} = 0.001A to 1A		Active		+/- 0.2		%
		I_{OUT} = 0A to 0.1A		Standby		+/- 0.2		
		I_{OUT} = 0A to 0.01A		Sleep		+/- 0.3	+/- 0.5	
Quiescent Current	$I_{Q\ ACTIVE}$	Active (excluding switching losses)				265		µA
	$I_{Q\ STANDBY}$	Standby (excluding switching losses)				115		
	I_{QSLEEP}	Sleep				25		
Shutdown current	I_{SD}					0.01		µA
P-channel On Resistance	R_{DSP}	V_{IN} = 3.7V, $I_{L(n)}$ = 100mA				0.09		Ω
N-channel On Resistance	R_{DSN}	V_{IN} = 3.7V, $I_{L(n)}$ = 100mA				0.167		Ω
P-channel leakage current	I_{LXP}	V_{IN} = 3.7V, L(n) = GND				0.01		µA
N-channel leakage current	I_{LXN}	V_{IN} = 3.7V, L(n) = 3.7V				2.8		µA
Switching Frequency	f_{SW}					2.0		MHz

Test Conditions
T_A = +25ºC unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS			MIN	TYP	MAX	UNITS
DC-DC3 and DC-DC4								
Input Voltage	V_{IN}				2.7	3.7	5.5	V
Output Voltage	V_{OUT}				0.85		3.4	V
VOUT Accuracy	V_{OUT}	V_{IN} = 3.7V V_{OUT} = 0.85V / 1.8V / 3.4V	I_{OUT} = 0.5A	Active		+/- 3.0		%
			I_{OUT} = 0.005A	Sleep		-1.5 +4.5		
Line Regulation	$V_{OUT\ LINE}$	V_{IN} = 2.7V to 5.5V V_{OUT} = 1.8V	I_{OUT} = 0.25A	Active		+/- 0.4		%
			I_{OUT} = 0.025A (100mA lim)	Standby		+/- 0.18		
			I_{OUT} = 0.005A	Sleep		+/- 0.4	+/- 0.5	
Load Regulation	$V_{OUT\ LOAD}$	I_{OUT} = 1mA to 500mA		Active		+/- 0.5		%
		I_{OUT} = 0A to 0.05A		Standby		+/- 0.2		
		I_{OUT} = 0A to 0.010A		Sleep		+/- 0.3	+/- 0.5	
Quiescent Current	$I_{Q\ ACTIVE}$	Active (excluding switching losses)				318		µA
	$I_{Q\ STANDBY}$	Standby (excluding switching losses)				120		
	$I_{Q\ SLEEP}$	Sleep				25		
Shutdown current	I_{SD}					0.01		µA
P-channel On Resistance	R_{DSP}	V_{IN} = 3.7V, $I_{L(n)}$ = 100mA				0.29		Ω
N-channel On Resistance	R_{DSN}	V_{IN} = 3.7V, $I_{L(n)}$ = 100mA				0.2		Ω
P-channel leakage current	I_{LXP}	V_{IN} = 3.7V, L(n) = GND				0.02		µA
N-channel leakage current	I_{LXN}	V_{IN} = 3.7V, L(n) = 3.7V				1.4		µA
Switching Frequency	f_{SW}					2.0		MHz

7.4 LDO REGULATOR ELECTRICAL CHARACTERISTICS

Test Conditions

V_{IN} = 3.7, V_{OUT} = 1.8V, T_A = +25ºC unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDO1 to LDO4 (WM8351 in ACTIVE State)						
Input Voltage	VIN	After start-up	1.6	3.7	5.5	V
Output voltage	VOUT*n*		0.9		3.3	V
Regulation Accuracy				+/-3.3%		%
Dropout Voltage		100mA, V_{IN} < 1.8V		200		mV
		100mA, V_{IN} <2.7V		700		
Load current				100	150	mA
Quiescent Current			27		1% of load	µA
Leakage Current				<2.5		µA
Power Supply Rejection Ratio	PSRR	1kHz, V_{OUT} =1.8V, 25mA load		-50		dB
		100Hz				
ON Resistance in switch mode	R_{ON}	LDOn_SWI = 1		2	3.5	Ω
LDO1 (WM8351 in OFF State)						
Output Voltage	VOUT1			0.95 × VOUT1 in ACTIVE		V

7.5 BATTERY CHARGER

Test Conditions

T_A = +25ºC unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General						
Wall adaptor voltage	LINE	When charging from wall adaptor	4.0		5.5	V
USB voltage	USB	When charging from USB power rail	4.0		5.5	V
Target voltage		CHG_VSEL=00	4.0	4.05	4.1	V
		CHG_VSEL=01	4.05	4.1	4.15	
		CHG_VSEL=10	4.1	4.15	4.2	
		CHG_VSEL=11	4.15	4.2	4.25	
Defective battery threshold				2.85		V
End of Charge Current	EOC	Programmable in register R168 CHG_EOC_SEL bits		20 to 90		mA
Trickle Charging						
Trickle charge initiation threshold (WM8351 starts trickle charging when battery is below this threshold)				CHG_VSEL - 100mV		V
50mA trickle charge current		CHG_TRICKLE_SEL = 0 (default)		35.9		mA
100mA trickle charge current		CHG_TRICKLE_SEL = 1		78.6		mA
Fast Charging						
Fast charge threshold (WM8351 can only fast-charge if battery is above this threshold)				3.1		V
Maximum fast-charge current	I_{MAX}			750		mA
Backup Battery (VRTC)						
Backup battery charger output. (Note that this backup charger voltage also determines the UVLO threshold.)			2.5	2.7	2.9	V

7.6 CURRENT LIMIT SWITCH

Test Conditions

T_A = +25ºC unless otherwise noted.

PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
Maximum input voltage		2.7		LINE	V
On resistance (at 3.3V)			2.0		Ω
Current limit flag threshold			180		mA
Current limit			215		mA
Quiescent current (EN but not ON)			7		µA
Quiescent current (EN and ON)					µA

7.7 LED DRIVERS

Test Conditions

T_A = +25ºC unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ISINKA						
Sink Current		duty cycle = 20%			200	mA
		continuous			40	
ISINKC, ISINKD, ISINKE						
Sink Current					20	mA
Output voltage drop		10mA load		0.8		V

7.8 GENERAL PURPOSE INPUTS / OUTPUTS (GPIO)

Test Conditions

T_A = +25ºC unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIO0 to GPIO3						
Input HIGH Level	V_{IH}		0.7×VRTC			V
Input LOW Level	V_{IL}				0.3×VRTC	V
Output HIGH Level	V_{OH}	sinking 2 mA	0.9×VRTC			V
Output LOW Level	V_{OL}	sourcing 2 mA			0.1×VRTC	V
Sink / source current						mA
Pull-up resistance to VRTC	R_{PU}	GPn_PU = 1		310		kΩ
Pull-down resistance	R_{PD}	GPn_PD = 1		225		kΩ
GPIO4 to GPIO9						
Logic levels	See Section 7.9					
Sink / source current						mA
Pull-up resistance to DBVDD	R_{PU}	GPn_PU= 1		220		kΩ
Pull-down resistance	R_{PD}	GPn_PD = 1		144		kΩ
GPIO10 to GPIO12						
Input HIGH Level	V_{IH}		2.0			V
Input LOW Level	V_{IL}				0.9	V
Output HIGH Level	V_{OH}	sinking 2 mA	0.9× LINE			V
Output LOW Level	V_{OL}	sourcing 2 mA			0.1× GPIO_VDD	V
Sink / source current						mA
Pull-up resistance to LINE	R_{PU}	GPn_PU = 1		250		kΩ
Pull-down resistance	R_{PD}	GPn_PD = 1		135		kΩ

7.9 DIGITAL INTERFACES

Test Conditions

T_A = +25ºC unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDA, SCLK, MCLK, BCLK, LRCLK, ADCDATA, DACDATA, GPIO4 to GPIO9						
Input HIGH Level	V_{IH}		0.7×DBVDD			V
Input LOW Level	V_{IL}				0.3×DBVDD	V
Output HIGH Level	V_{OH}	sinking 1mA	0.9×DBVDD			V
Output LOW Level	V_{OL}	sourcing 1mA			0.1xDBVDD	V

7.10 AUXILIARY ADC

Test Conditions

T_A = +25ºC unless otherwise noted.

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNITS
Input resistance (AUX1,2,3,4, USB, LINE, BATT and CHIPTEMP)	AUXADC_SCALEn [1:0] = 00		∞	∞	∞	Ω
	AUXADC_SCALEn [1:0] = 01			2.2		kΩ
	AUXADC_SCALEn [1:0]= 10		330		660	kΩ
	AUXADC_SCALEn [1:0] = 11		330		440	kΩ
Input Voltage range. AUX1,2,3,4,USB,LINE,BATT and CHIPTEMP (V_{RTC} = 2.7V & V_{LINE} (max)= 5.5V, V_{BG}=1.25V)	AUXADC_SCALEn [1:0] = 01 AUXADC_REF = 0				V_{BG}	V
	AUXADC_SCALEn [1:0] = 01 AUXADC_REF = 1				V_{RTC}	V
	AUXADC_SCALEn [1:0] = 10 AUXADC_REF = 0				2 x V_{BG}	V
	AUXADC_SCALEn [1:0] = 10 AUXADC_REF = 1				2 x V_{RTC}	V
	AUXADC_SCALEn [1:0] = 11 AUXADC_REF = 0				V_{LINE}	V
	AUXADC_SCALEn [1:0] = 11 AUXADC_REF = 1				4 x V_{BG}	V
Input capacitance (AUX1,2,3,4, USB, LINE, BATT and CHIPTEMP)	Input is selected (INPUT_SELECT) and AUXADC_SCALEn [1:0] not = 00			2.08		pF
VRTC quiescent current	AUX_RBMODE = 0, AUXADC_ENA = 1			140		µA
VRTC quiescent current	AUX_RBMODE = 1 AUXADC_ENA = 1			151		µA
LINE_INT quiescent current					<<1	mA
ADCCLK frequency		f_{AUXCLK}	400	470/512	800	kHz
ADC Resolution				12		bits
ADC Conversion Time				13		CLK periods
Aux ADC accuracy	Non-calibrated (calibration possible using the VBG input on AUX3). 1% of this variation due to BG variation over temperature.			2.2		%

8 TYPICAL POWER CONSUMPTION

ADC Master Mode

48kHz

AVDD (V)	HPVDD (V)	DBVDD (V)	DCVDD (V)	IAVDD (mA)	IHPVDD (mA)	IDB (mA)	IDC (mA)	Power Consumption (mW)
2.5	2.5	1.71	1.71	3.6	0.000014	0.55	2.3	13.87
3.3	3.3	3.3	1.8	4.46	0.00003	1.085	2.4	22.62
3.6	3.6	3.6	3.6	4.79	0.000028	1.18	5.67	41.90

ADC Master Mode

1kHz Tone 100mVpk-pk

AVDD (V)	HPVDD (V)	DBVDD (V)	DCVDD (V)	IAVDD (mA)	IHPVDD (mA)	IDB (mA)	IDC (mA)	Power Consumption (mW)
2.5	2.5	1.71	1.71	3.6	0.00009	0.5	2.14	13.51
3.3	3.3	3.3	1.8	4.4	0.00016	1.02	2.3	22.03
3.6	5.5	3.6	3.6	4.8	0.00008	1.12	5.3	40.39

ADC Master Mode

Pink Noise

AVDD (V)	HPVDD (V)	DBVDD (V)	DCVDD (V)	IAVDD (mA)	IHPVDD (mA)	IDB (mA)	IDC (mA)	Power Consumption (mW)
2.5	2.5	1.71	1.71	3.58	0.000004	0.51	2.1	13.41
3.3	3.3	3.3	1.8	4.43	0.00026	1	2.2	21.88
3.6	5.5	3.6	3.6	4.8	0.000085	1.1	5.2	39.96

ADC Slave Mode

44.1kHz

AVDD (V)	HPVDD (V)	DBVDD (V)	DCVDD (V)	IAVDD (mA)	IHPVDD (mA)	IDB (mA)	IDC (mA)	Power Consumption (mW)
2.5	2.5	1.71	1.71	3.4	0.00002	0.02	2.2	12.30
3.3	3.3	3.3	1.8	4.2	0.00041	0.05	2.3	18.17
3.6	3.6	3.6	3.6	4.4	0.0004	0.05	5.33	35.21

DAC OUT1 Master Mode

44.1kHz, 10kΩ Load

AVDD (V)	HPVDD (V)	DBVDD (V)	DCVDD (V)	IAVDD (mA)	IHPVDD (mA)	IDB (mA)	IDC (mA)	Power Consumption (mW)
2.5	2.5	1.71	1.71	2.97	0.299	0.193	1.69	11.39
3.3	3.3	3.3	1.8	4.14	0.432	0.39	1.78	19.58
3.6	3.6	3.6	3.6	4.54	0.486	0.461	4.28	35.16

48kHz,10kΩ Load

AVDD (V)	HPVDD (V)	DBVDD (V)	DCVDD (V)	IAVDD (mA)	IHPVDD (mA)	IDB (mA)	IDC (mA)	Power Consumption (mW)
2.5	2.5	1.71	1.71	2.82	0.3	0.2	2	11.56
3.3	3.3	3.3	1.8	3.94	0.45	0.42	2.12	19.69
3.6	3.6	3.6	3.6	4.33	0.51	0.46	4.9	36.72