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WM8523

24-bit 192kHz Stereo DAC with 2Vrms Ground Referenced Line Output

DESCRIPTION

The WM8523 is a stereo DAC with integral charge pump and software control interface. This provides 2Vrms line driver outputs using a single 3.3V power supply rail.

The device features ground-referenced outputs and the use of a DC servo to eliminate the need for line driving coupling capacitors and effectively eliminate power on pops and clicks.

The device is controlled and configured either via the I2C/SPI compliant serial control interface or a hardware control interface.

The device supports all common audio sampling rates between 8kHz and 192kHz using all common MCLK fs rates. Master and Slave modes are available and de-emphasis is also supported.

The WM8523 has a 3.3V tolerant digital interface, allowing logic up to 3.3V to be connected.

The device is available in a 20-lead TSSOP package.

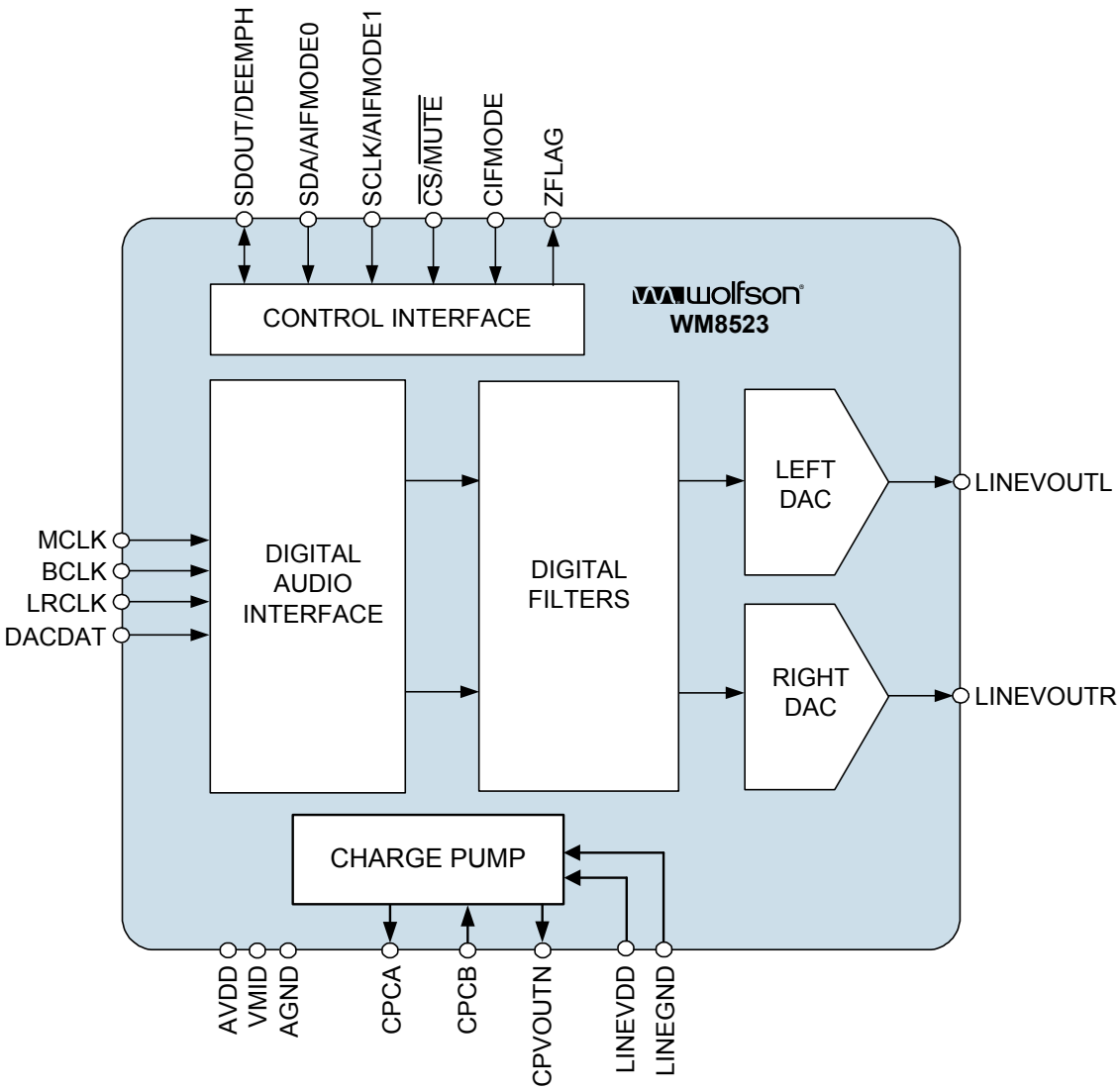
FEATURES

- High performance stereo DAC with ground referenced line driver
- Audio Performance
  - 106dB SNR ('A-weighted')
  - -89dB THD @ -1dBFS
- Digital Volume control ranging from -100dB to +12dB
- 120dB mute attenuation
- All common sample rates from 8kHz to 192kHz supported
- I^2C/SPI compatible and hardware control modes
- Data formats: LJ, RJ, I^2S, DSP
- De-emphasis supported
- Maximum 1mV DC offset on Line Outputs
- Pop/Click suppressed Power Up/Down Sequencer
- AVDD and LINEVDD +3.3V ±10% allowing single supply
- 20-lead TSSOP package
- Operating temperature range: -40°C to 85°C

APPLICATIONS

- Consumer digital audio applications requiring 2Vrms output
  - Set Top Box
  - Digital TV
  - DVD Players
  - Games Consoles
  - A/V Receivers

BLOCK DIAGRAM



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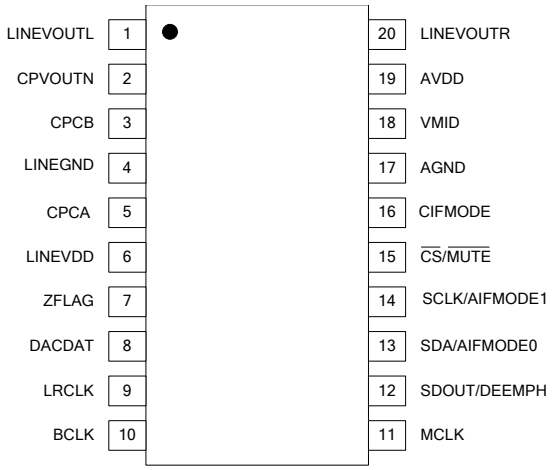
PIN CONFIGURATION



20-LEAD TSSOP

ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8523GEDT	−40°C to +85°C	20-lead TSSOP (pb-free)	MSL1	260°C
WM8523GEDT/R	−40°C to +85°C	20-lead TSSOP (pb-free, tape and reel)	MSL1	260°C

Note:

Reel quantity = 2000

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION		
1	LINEVOUTL	Analogue Out	Left line output		
2	CPVOUTN	Analogue Out	Charge Pump negative rail decoupling pin		
3	CPCB	Analogue Out	Charge Pump fly back capacitor pin		
4	LINEGND	Supply	Charge Pump ground		
5	CPCA	Analogue Out	Charge Pump fly back capacitor pin		
6	LINEVDD	Supply	Charge Pump supply		
7	ZFLAG	Digital Out	Zero flag output		
8	DACDAT	Digital In	Digital audio interface data input		
9	LRCLK	Digital I/O	Digital audio interface left/right clock		
10	BCLK	Digital I/O	Digital audio interface bit clock		
11	MCLK	Digital In	Master clock		
			I^2C SOFTWARE MODE	**SPI SOFTWARE MODE**	**HARDWARE MODE**
12	SDOUT/ DEEMPH	Digital I/O	I^2C address select bit[1]	Serial control interface data output pin	0 – No de-emphasis 1 – De-emphasis
13	SDA/ AIFMODE0	Digital I/O Internal pull-down	Serial control interface data input pin	Serial control interface data input pin	**AIFMODE[1:0]** 00 – LJ 24 bits 01 – I2S 24 bits 10 – RJ 16 bits 11 – RJ 24 bits
14	SCLK/ AIFMODE1	Digital I/O Internal pull-down	Serial control interface clock input pin	Serial control interface clock input pin	
15	$\overline{CS}$/ $\overline{MUTE}$	Digital In	I^2C address select bit[0]	Serial control interface chip select	0 – Mute enabled 1 – Mute disabled
16	CIFMODE	Digital In Tri-level	0 – I^2C compatible mode select	1 – SPI compatible mode select	Z – Hardware mode
17	AGND	Supply	Analogue ground		
18	VMID	Analogue Out	Analogue midrail decoupling pin		
19	AVDD	Supply	Analogue supply		
20	LINEVOUTR	Analogue Out	Right line output		

Note: Tri-level pins which require the 'Z' state to be selected should be left floating (open)

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
AVDD, LINEVDD	-0.3V	+4.5V
Voltage range digital inputs	LINEGND -0.3V	LINEVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Temperature range, T_A	-40°C	+125°C
Storage temperature after soldering	-65°C	+150°C

Notes

1. Analogue grounds must always be within 0.3V of each other.
2. LINEVDD and AVDD must always be within 0.3V of each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue supply range	AVDD, LINEVDD		2.97	3.3	3.63	V
Ground	AGND, LINEGND			0		V

ELECTRICAL CHARACTERISTICS

Test Conditions

LINEVDD=AVDD=3.3V, LINEGND=AGND=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Output Levels						
Output Level		0dBFS	1.89	2.1	2.31	Vrms
Load Impedance			1			kΩ
Load Capacitance		No external RC filter			300	pF
		With filter shown in Figure 39.			1	µF
DAC Performance						
Signal to Noise Ratio	SNR	R_L = 10kΩ A-weighted	100	106		dB
		R_L = 10kΩ Un-weighted		104		dB
Dynamic Range	DNR	R_L = 10kΩ A-weighted		104		dB
Total Harmonic Distortion	THD	R_L = 10kΩ -1dBFS		-89		dB
		R_L = 10kΩ 0dBFS		-86		dB
AVDD + LINEVDD Power Supply Rejection Ratio	PSRR	100Hz		54		dB
		1kHz		54		dB
		20kHz		50		dB
Channel Separation		1kHz		100		dB
		20Hz to 20kHz		95		dB
System Absolute Phase				0		degrees
Channel Level Matching				0.1		dB
Mute Attenuation				-120		dB
DC Offset at LINEVOUTL and LINEVOUTR			-1	0	1	mV
Digital Logic Levels						
Input HIGH Level	V_{IH}		0.7× LINEVDD			V
Input LOW Level	V_{IL}				0.3× LINEVDD	V
Output HIGH Level	V_{OH}	I_{OL} = 1mA	0.9× LINEVDD			V
Output LOW Level	V_{OL}	I_{OH} = -1mA			0.1× LINEVDD	V
Input Capacitance				10		pF
Input Leakage			-0.9		0.9	µA

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum theoretical full scale output signal and the output with no input signal applied.
2. Total Harmonic Distortion (dB) – THD is the level of the rms value of the sum of harmonic distortion products relative to the amplitude of the measured output signal.
3. All performance measurements carried out with 20kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
4. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.

POWER CONSUMPTION MEASUREMENTS

Test Conditions LINEVDD=AVDD=3.3V, LINEGND=AGND=0V, T_A=+25°C, Slave Mode, quiescent (no signal)				
	TEST CONDITIONS	**IAVDD (mA)**	**ILINEVDD (mA)**	**TOTAL (mA)**
Off	No clocks applied SYS_ENA[1:0]=00	0.8	1.1	1.9
fs=48kHz, MCLK=256fs				
Standby	SYS_ENA[1:0]=01	0.2	2.2	2.4
Playback	SYS_ENA[1:0]=11	4.8	6.0	10.8
fs=96kHz, MCLK=256fs				
Standby	SYS_ENA[1:0]=01	0.2	2.9	3.1
Playback	SYS_ENA[1:0]=11	5.5	8.5	14.0
fs=192kHz, MCLK=128fs				
Standby	SYS_ENA[1:0]=01	0.2	2.9	3.1
Playback	SYS_ENA[1:0]=11	5.5	8.5	14.0

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

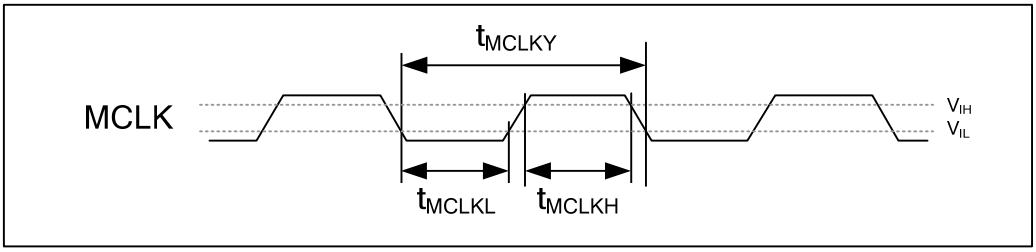


Figure 1 System Clock Timing Requirements

Test Conditions

LINEVDD=AVDD=2.97~3.63V, LINEGND=AGND=0V, T_A=+25°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Master Clock Timing Information					
MCLK cycle time	t_{MCLKY}	27		500	ns
MCLK high time	t_{MCLKH}	11			ns
MCLK low time	t_{MCLKL}	11			ns
MCLK duty cycle (t_{MCLKH}/t_{MCLKL})		40:60		60:40	%

AUDIO INTERFACE TIMING – MASTER MODE

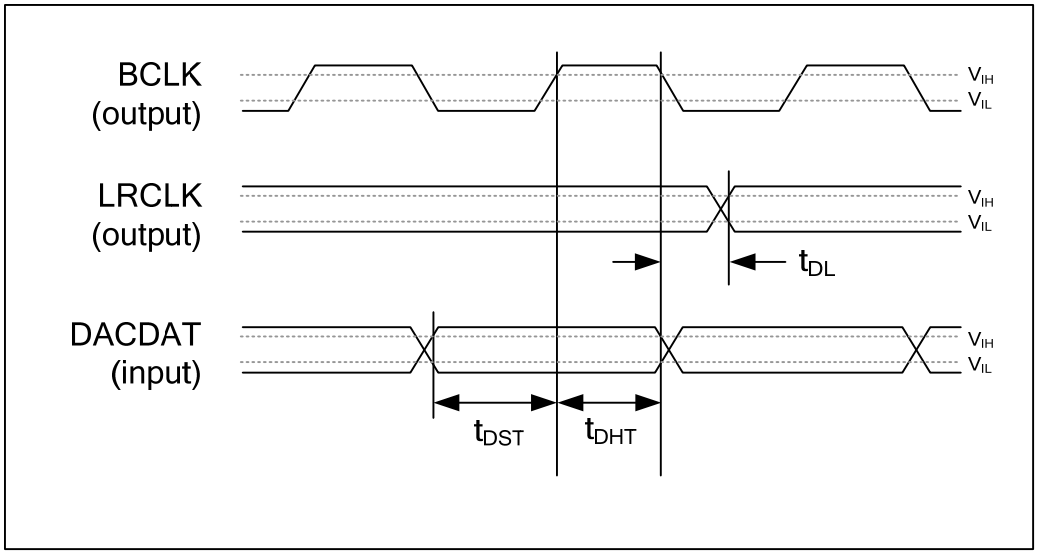


Figure 2 Master Mode Digital Audio Data Timing

Test Conditions

LINEVDD=AVDD=2.97~3.63, LINEGND=AGND=0V, T_A=+25°C, Master Mode

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
LRCLK propagation delay from BCLK falling edge	t_{DL}	4		16	ns
DACDAT setup time to BCLK rising edge	t_{DST}	22			ns
DACDAT hold time to BCLK falling edge	t_{DHT}	25			ns

Table 1 Master Mode Audio Interface Timing

AUDIO INTERFACE TIMING – SLAVE MODE

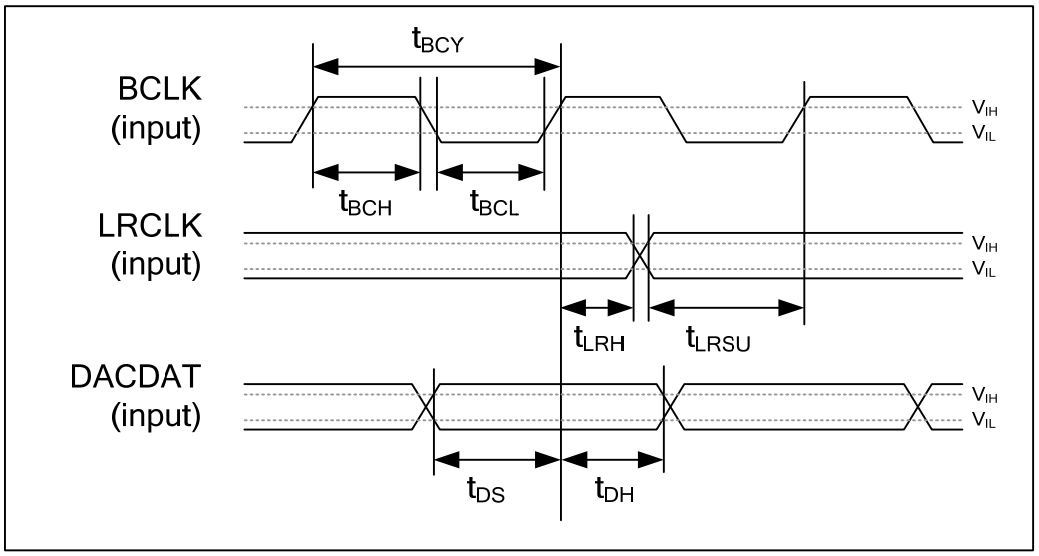


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

LINEVDD=AVDD=2.97~3.63V, LINEGND=AGND=0V, T_A=+25°C, Slave Mode

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t_{BCY}	27			ns
BCLK pulse width high	t_{BCH}	11			ns
BCLK pulse width low	t_{BCL}	11			ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}	7			ns
LRCLK hold time from BCLK rising edge	t_{LRH}	5			ns
DACDAT hold time from LRCLK rising edge	t_{DH}	5			ns
DACDAT set-up time to BCLK rising edge	t_{DS}	7			ns

Table 2 Slave Mode Audio Interface Timing

Note:

BCLK period should always be greater than or equal to MCLK period.

CONTROL INTERFACE TIMING – I²C MODE

I²C mode is selected by driving the CIFMODE pin low.

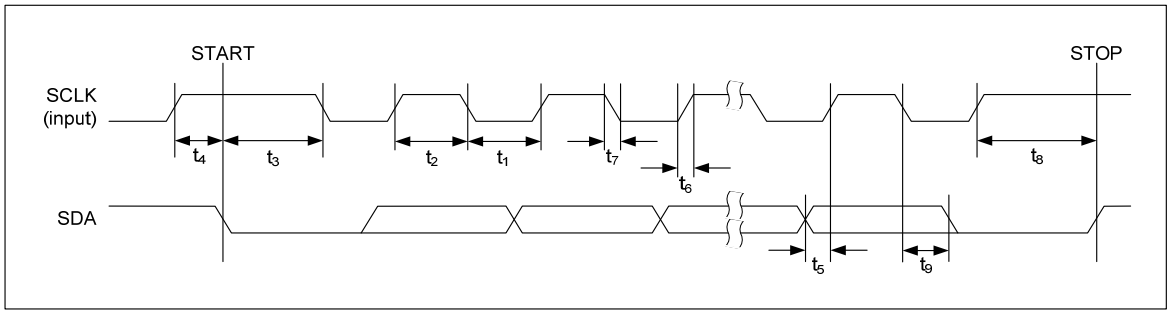


Figure 4 Control Interface Timing – I²C Control Mode

Test Conditions

LINEVDD=AVDD=2.97~3.63V, LINEGND=AGND=0V, T_A=+25°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency				400	kHz
SCLK Low Pulse-Width	t_1	100			ns
SCLK High Pulse-Width	t_2	100			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDA, SCLK Rise Time	t_6			300	ns
SDA, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed		2		8	ns

Table 3 Control Interface Timing – I²C Control Mode

CONTROL INTERFACE TIMING – SPI MODE

SPI mode is selected by connecting the CIFMODE pin high.

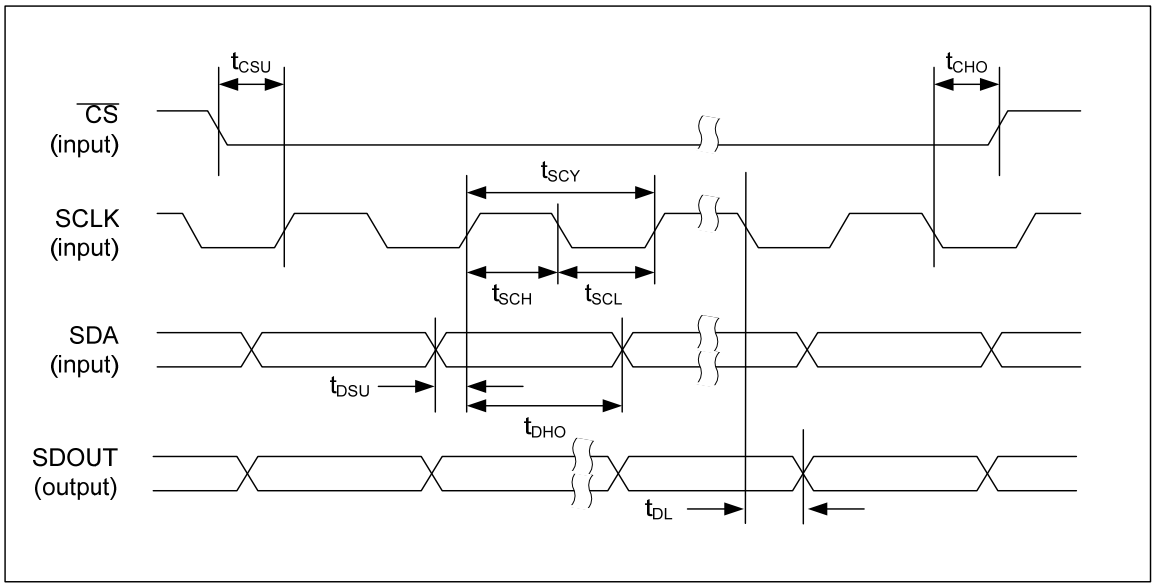


Figure 5 Control Interface Timing – SPI Control Mode (Read Cycle)

Test Conditions

LINEVDD=AVDD=2.97~3.63V, LINEGND=AGND=0V, T_A=+25°C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB falling edge	t_{CSU}	40			ns
SCLK falling edge to CSB rising edge	t_{CHO}	40			ns
SCLK pulse cycle time	t_{SCY}	160			ns
SCLK pulse width low	t_{SCL}	64			ns
SCLK pulse width high	t_{SCH}	64			ns
SDA to SCLK set-up time	t_{DSU}	20			ns
SDA to SCLK hold time	t_{DHO}	40			ns
SDOUT propagation delay from SCLK falling edge	t_{DL}			5	ns
Pulse width of spikes that will be suppressed	t_{ps}	2		8	ns

Table 4 Control Interface Timing –SPI Control Mode

POWER ON RESET CIRCUIT

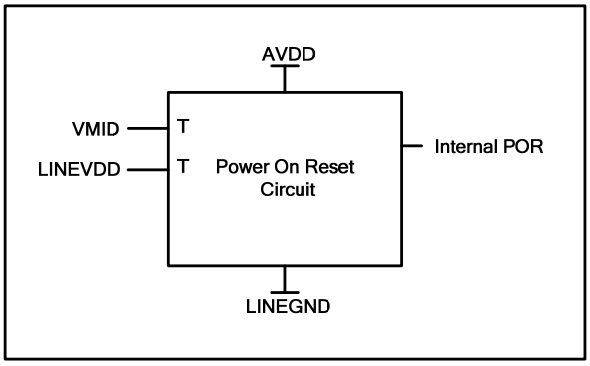


Figure 6 Internal Power on Reset Circuit Schematic

The WM8523 includes an internal Power-On-Reset circuit, as shown in Figure 6, which is used to reset the DAC digital logic into a default state after power up. The POR circuit is powered by AVDD and has as its inputs VMID and LINEVDD. It asserts POR low if VMID or LINEVDD are below a minimum threshold.

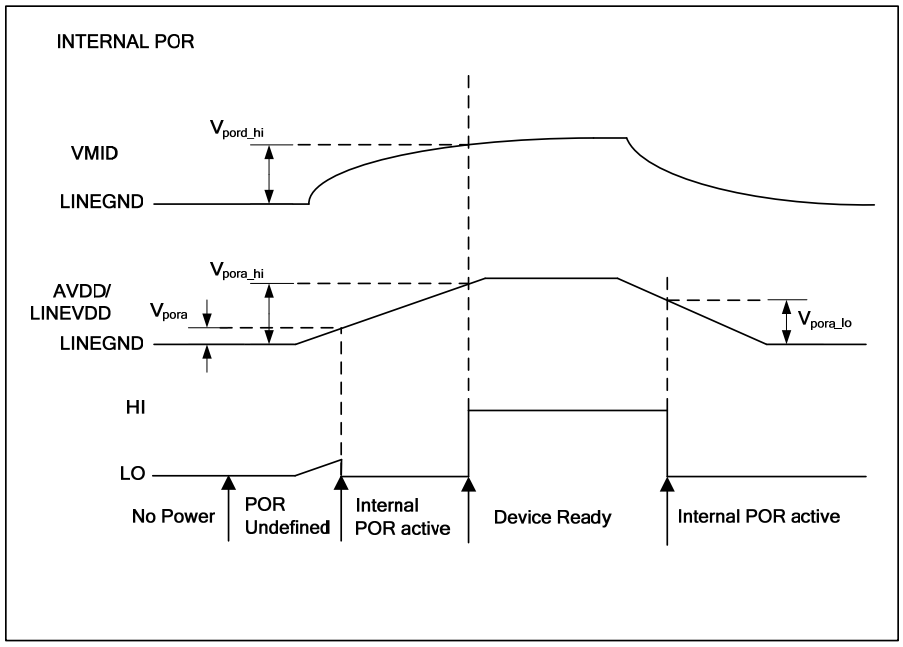


Figure 7 Typical Power Timing Requirements

Figure 7 shows a typical power-up sequence where LINEVDD comes up with AVDD. When AVDD goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee POR is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. After VMID rises to V_{pord_hi} and AVDD rises to $V_{pora\_hi,}$ POR is released high and all registers are in their default state and writes to the control interface may take place.

On power down, PORB is asserted low whenever LINEVDD or AVDD drop below the minimum threshold V_{pora_low}.

Test Conditions

LINEVDD = AVDD = 3.3V AGND = LINEGND = 0V, T_A = +25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Input Timing Information						
VDD level to POR defined (LINEVDD/AVDD rising)	V_{pora}	Measured from LINEGND		158		mV
VDD level to POR rising edge (VMID rising)	V_{pord_hi}	Measured from LINEGND	0.63	0.8	1	V
VDD level to POR rising edge (LINEVDD/AVDD rising)	V_{pora_hi}	Measured from LINEGND	1.44	1.8	2.18	V
VDD level to POR falling edge (LINEVDD/AVDD falling)	V_{pora_lo}	Measured from LINEGND	0.96	1.46	1.97	V

Table 5 Power on Reset

Note: All values are simulated results

DEVICE DESCRIPTION

INTRODUCTION

The WM8523 provides high fidelity, $2V_{rms}$ ground referenced stereo line output from a single supply line with minimal external components. The integrated DC servo eliminates the requirement for external mute circuitry by minimising DC transients at the output during power up/down. The device is well-suited to both stereo and multi-channel systems.

The device supports all common audio sampling rates between 8kHz and 192kHz using common MCLK fs rates. Master and slave modes are available.

The WM8523 supports both hardware and software control modes.

In hardware control mode, the digital audio interface format is switchable between 16 to 24bits LJ, RJ and I^2S. Mute and de-emphasis control pins are also available.

In software control modes the digital audio interface is highly programmable, with four control interface addresses to allow multiple WM8523 devices to be configured independently.

SOFTWARE CONTROL INTERFACE

Software Control Mode is selected by logic 1 or 0 on the CIFMODE pin. The logic level is referenced to the LINEVDD power domain. When software mode is selected, the associated multi-function control pins are defined as described in Table 6.

PIN NAME	PIN NUMBER	DESCRIPTION
SDOUT	12	I^2C Mode - Device Address[1] SPI Mode - Serial Data Output
SDA	13	Serial Data Input
SCLK	14	Serial Data Clock
$\overline{CS}$	15	I^2C Mode - Device Address[0] SPI Mode - Chip Select
CIFMODE	16	Control Interface Mode 0 = I^2C Mode 1 = SPI Mode Z = Hardware Mode

Table 6 Software Control Pin Configuration

In software control mode, the WM8523 is controlled by writing to its control registers. Readback is available for all registers, including device ID and power management status bits. The control interface can operate as an I^2C or SPI control interface: register read-back is provided on the bi-directional pin SDA in I^2C mode, and on the SDOUT pin in SPI mode. The WM8523 software control interface is supplied by the LINEVDD power domain.

The available software control interface modes are summarised as follows:

- I^2C mode uses pins SCLK and SDA.
- SPI mode uses pins $\overline{CS}$, SCLK and SDA and SDOUT.

I^2C mode is selected by setting the CIFMODE pin to logic 0. When CIFMODE is set to logic 1, SPI mode is selected.

I²C CONTROL MODE

In I²C mode, the WM8523 is a slave device on the control interface; SCLK is a clock input, while SDA is a bi-directional data pin. To allow arbitration of multiple slaves (and/or multiple masters) on the same interface, the WM8523 transmits logic 1 by tri-stating the SDA pin, rather than pulling it high. An external pull-up resistor is required to pull the SDA line high so that the logic 1 can be recognised by the master.

In order to allow many devices to share a single I²C control bus, every device on the bus has a unique 7-bit device address (this is not the same as the 8-bit address of each register in the WM8523). The device address is determined by the logic level on the SDOUT and $\overline{CS}$ pins as shown in Table 7. The LSB of the device address is the R/$\overline{W}$ bit; this bit is set to logic 1 for "Read" and logic 0 for "Write".

SDOUT ADDR1	$\overline{CS}$ ADDR0	DEVICE ADDRESS
0	0	0011 0100 (34h)
0	1	0011 0110 (36h)
1	0	0011 1100 (3Ch)
1	1	0011 1110 (3Eh)

Table 7 Control Interface Device Address Selection

The WM8523 operates as an I²C slave device only. The controller indicates the start of data transfer with a high to low transition on SDA while SCLK remains high. This indicates that a device address, register address and data will follow. All devices on the I²C bus respond to the start condition and shift in the next eight bits on SDA (7-bit device address + Read/Write bit, MSB first). If the device address received matches the device address of the WM8523, then the WM8523 responds by pulling SDA low on the next clock pulse (ACK). If the device address is not recognised or the R/$\overline{W}$ bit is '1' when operating in write only mode, the WM8523 returns to the idle condition and waits for a new start condition and valid address.

If the device address matches the device address of the WM8523, the data transfer continues as described below. The controller indicates the end of data transfer with a low to high transition on SDA while SCLK remains high. After receiving a complete address and data sequence the WM8523 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDA changes while SCLK is high), the device returns to the idle condition.

The WM8523 supports the following read and write operations:

- Single write
- Single read

The sequence of signals associated with a single register write operation is illustrated in Figure 8.

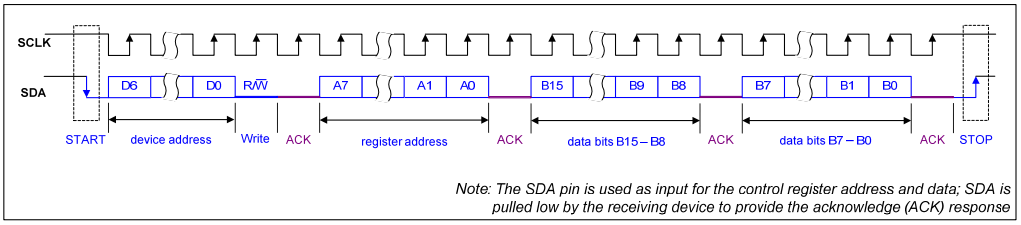


Figure 8 Control Interface I²C Register Write

The sequence of signals associated with a single register read operation is illustrated in Figure 9.

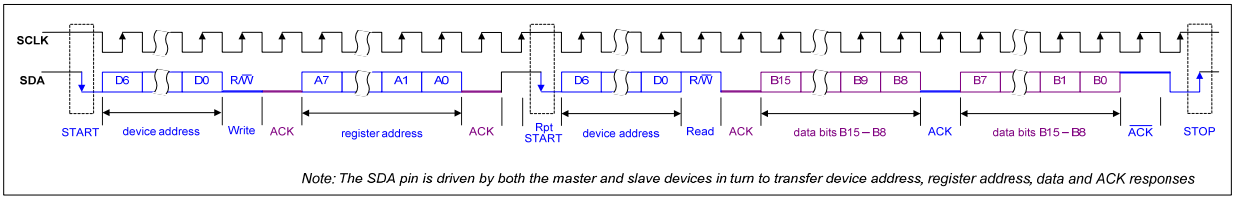


Figure 9 Control Interface I²C Register Read

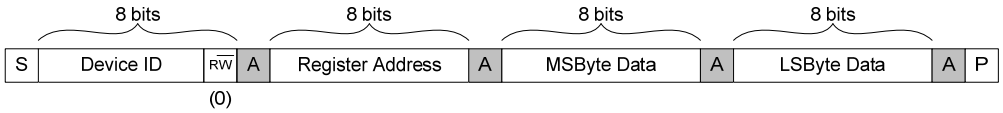


Figure 10 Single Register Write to Specified Address

Figure 11 Single Register Read from Specified Address

SPI CONTROL MODE

The WM8523 can also be controlled by writing to registers through a SPI control interface. A control word consists of 24 bits. The first bit is the read/write bit (R/$\overline{W}$), which is followed by 7 address bits (A6 to A0) that determine which control register is accessed. The remaining 16 bits (B15 to B0) are data bits, corresponding to the 16 bits in each control register.

Volume update registers R06h and R07h are unavailable in SPI control mode. To use volume update in software control mode, I^2C mode must be used.

In SPI mode, every rising edge of SCLK clocks in one data bit from the SDA pin. A rising edge on $\overline{CS}$ latches in a complete control word consisting of the last 24 bits.

The SPI mode write operation protocol is illustrated in Figure 12.

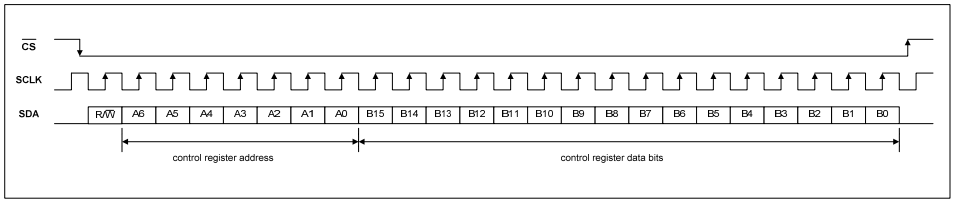


Figure 12 SPI Control Interface – write operation

In Write operations (R/$\overline{W}$=0), all SDA bits are driven by the controlling device.

In Read operations (R/$\overline{W}$=1), the SDA pin is ignored following receipt of the valid register address. The data bits are output by the WM8523 on the SDOUT pin.

The SPI mode read operation protocol is illustrated in Figure 13.

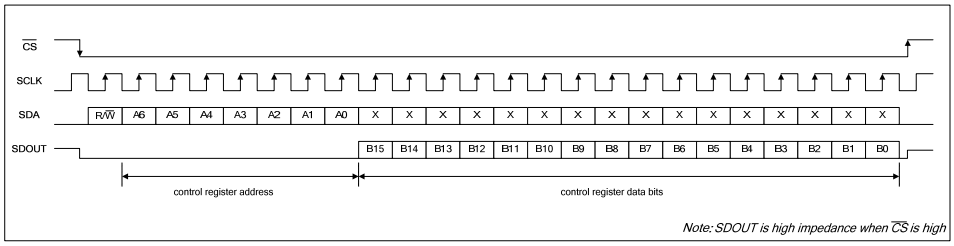


Figure 13 SPI Control Interface – read operation

REGISTER RESET

Any write to register R0 (00h) will reset the WM8523. All register bits are reset to their default values.

DEVICE ID AND REVISION

Reading from register R0 (00h) returns the device ID. Reading from register R1 returns the device revision number.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 DEVICE_ID 00h	15:0	DEVICE_ID [15:0]	10000101 00100011	**Device ID** A read of this register will return the device ID, 0x8523.
R1 REVISION 01h	2:0	CHIP_REV [2:0]	N/A	**Device Revision** A read of this register will return the device revision number. This number is sequentially incremented if the device design is updated.

Table 8 Device ID and Revision Number

DIGITAL AUDIO INTERFACE

The digital audio interface is used for inputting audio data to the WM8523. The digital audio interface uses three pins:

- DACDAT: DAC data input
- LRCLK: Left/Right data alignment clock
- BCLK: Bit clock, for synchronisation

In software control mode, all interface data formats and modes of operation can be selected. In hardware control mode, only a subset of formats and modes are supported – see the Hardware Interface Control section on page 30 for details.

MASTER AND SLAVE MODE OPERATION

The WM8523 digital audio interface can operate as a master or as a slave as shown in Figure 14 and Figure 15.

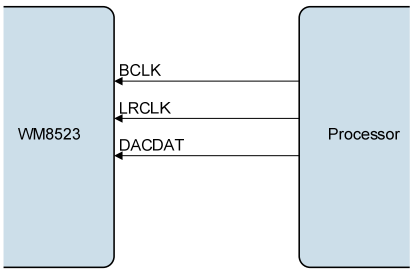


Figure 14 Slave Mode

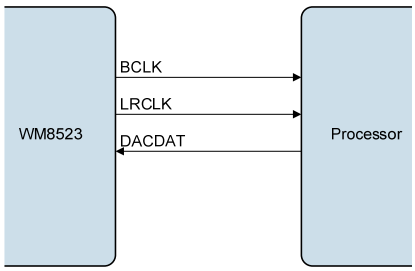


Figure 15 Master Mode

INTERFACE FORMATS

The WM8523 supports five different audio data formats:

- Left justified
- Right justified
- I^2S
- DSP Mode A
- DSP Mode B

PCM operation is supported using the DSP mode. All seven of these modes are MSB first. They are described in Audio Data Formats on page 20. Refer to the "Electrical Characteristics" section for timing information. Refer to Table 10 for interface control format register settings.

AUDIO DATA FORMATS

In Right Justified mode, the LSB is available on the last rising edge of BCLK before a LRCLK transition. All other bits are transmitted before (MSB first). Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles after each LRCLK transition.

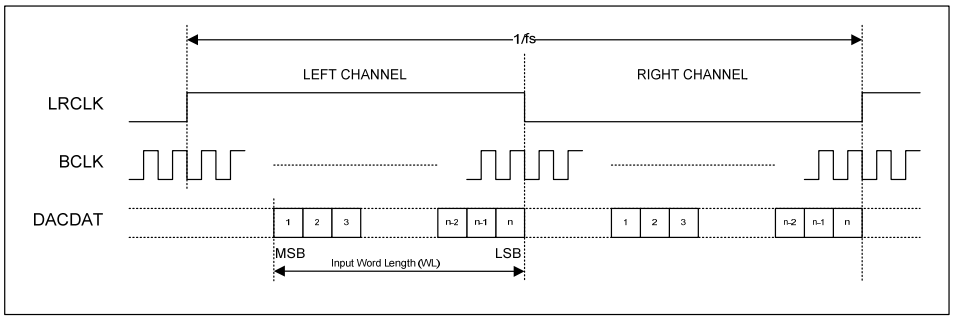


Figure 16 Right Justified Audio Interface (assuming n-bit word length)

In Left Justified mode, the MSB is available on the first rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles before each LRCLK transition.

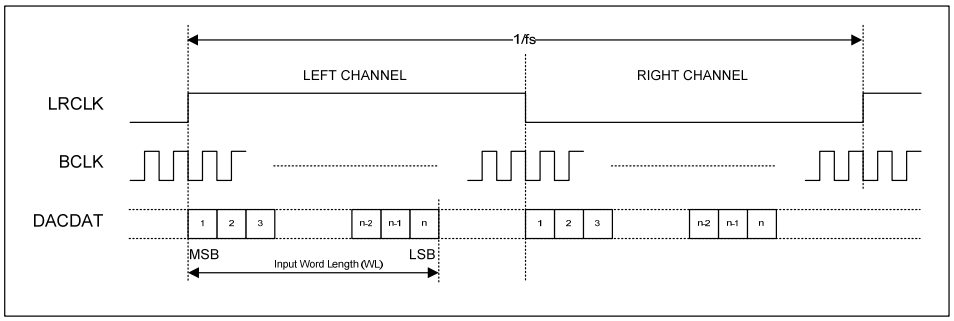


Figure 17 Left Justified Audio Interface (assuming n-bit word length)

In I^2S mode, the MSB is available on the second rising edge of BCLK following a LRCLK transition. The other bits up to the LSB are then transmitted in order. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of one sample and the MSB of the next.

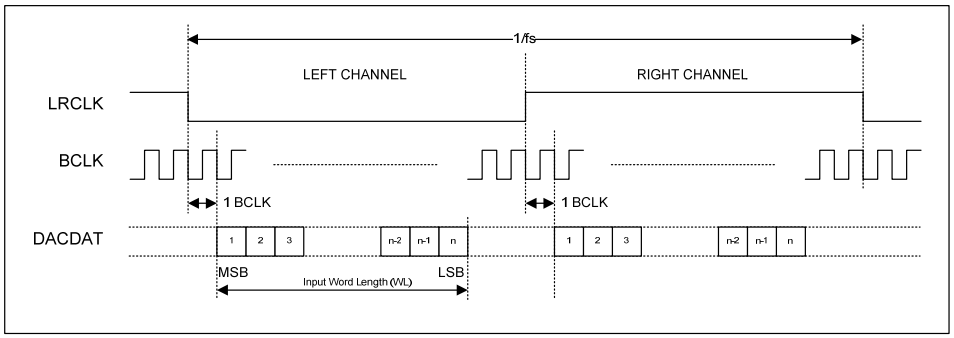


Figure 18 I^2S Justified Audio Interface (assuming n-bit word length)

In DSP mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK (selectable by AIF_LRCLK_INV) following a rising edge of LRCLK. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In device master mode, the LRCLK output will resemble the frame pulse shown in Figure 19 and Figure 20. In device slave mode, Figure 21 and Figure 22, it is possible to use any length of frame pulse less than 1/fs, providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.

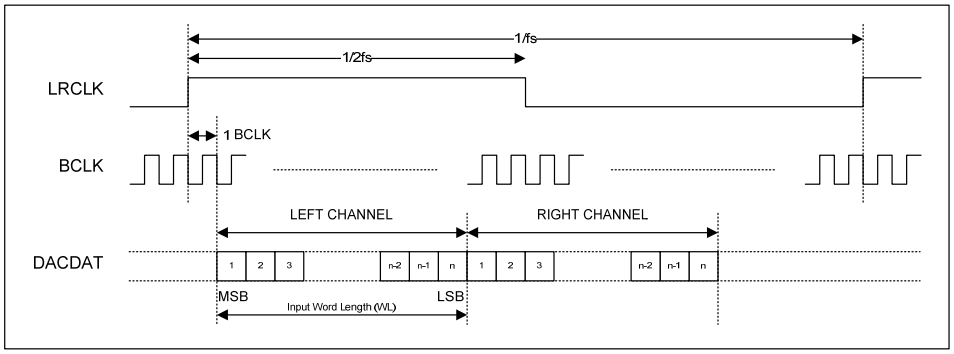


Figure 19 DSP Mode Audio Interface (mode A, AIF_LRCLK_INV=0, Master)

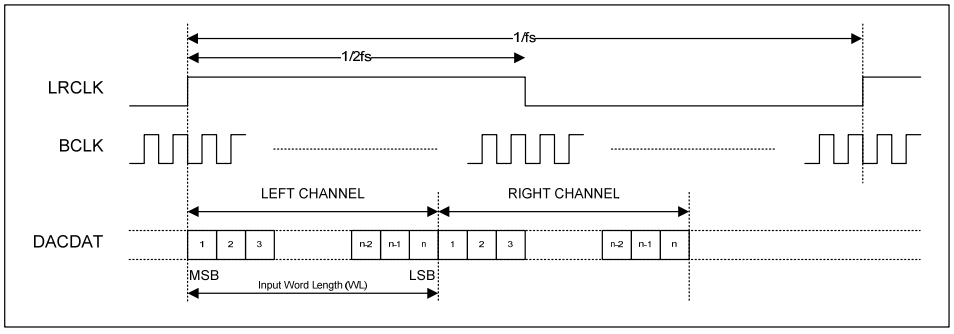


Figure 20 DSP Mode Audio Interface (mode B, AIF_LRCLK_INV=1, Master)

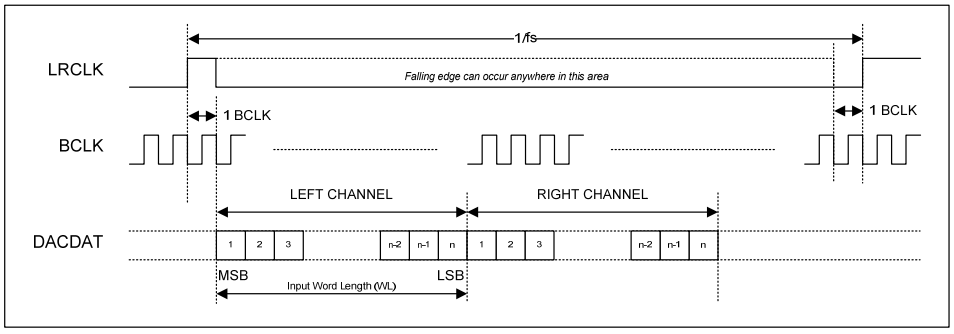


Figure 21 DSP Mode Audio Interface (mode A, AIF_LRCLK_INV=0, Slave)

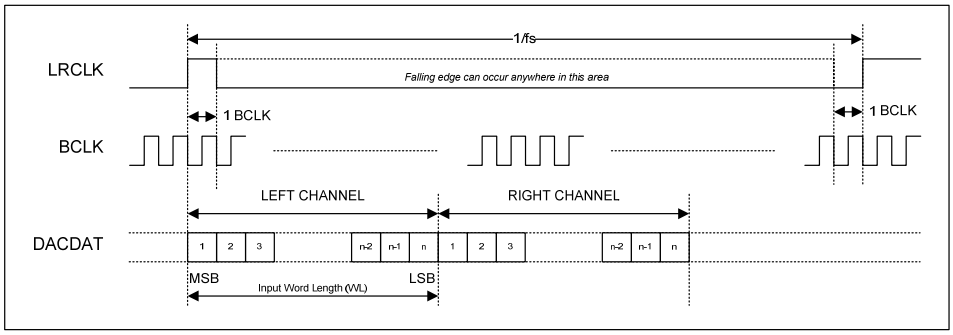


Figure 22 DSP Mode Audio Interface (mode B, AIF_LRCLK_INV=1, Slave)

DIGITAL AUDIO INTERFACE CONTROL

The control of the audio interface in software mode is achieved by register write. Dynamically changing the audio data format may cause erroneous operation and is not recommended.

Digital audio data is transferred to the WM8523 via the digital audio interface. The DAC operates in master or slave mode.

The DAC audio interface requires left/right frame clock (LRCLK) and bit clock (BCLK). These can be supplied externally (slave mode) or they can be generated internally (master mode). Selection of master and slave mode is achieved by setting AIF_MSTR bit in Register 3.

The frequency of LRCLK in master mode is dependent upon the DAC master clock frequency and the AIF_SR[2:0] bits. The frequency of BCLK in master mode can be selected by AIF_BCLKDIV[2:0]. In slave mode, the MCLK to LRCLK ratio can be auto-detected or set manually using the AIF_SR[2:0] bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 AIF_CTRL1 03h	7	AIF_MSTR	0	**Master/Slave Select** 0 = Slave 1 = Master
R4 AIF_CTRL2 04h	2:0	AIF_SR[2:0	000	**MCLK:LRCLK Ratio** 000 = Auto detect 001 = 128fs 010 = 192fs 011 = 256fs 100 = 384fs 101 = 512fs 110 = 768fs 111 = 1152fs
	5:3	AIF_BCLKDIV[2:0]	000	**BCLK Divider Control (Master Mode)** 000 = MCLK/4 001 = MCLK/8 010 = 32fs 011 = 64fs 100 = 128fs 101 - 111 reserved

Table 9 DAC Clocking Mode Control

Interface timing is such that the input data and left/right clock are sampled on the rising edge of BCLK. By setting the appropriate BCLK and LRCLK polarity bits, the WM8523 DAC can sample data on the opposite clock edges.

The control of audio interface formats and clock polarities is summarised in Table 10.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 AIF_CTRL1 03h	1:0	AIF_FMT	10	**Audio Data Interface Format** 00 = Right justified 01 = Left justified 10 = I2S format 11 = DSP mode
	2	Reserved	0	Reserved
	4:3	AIF_WL	10	**Audio Data Word Length** 00 = 16 bits 01 = 20 bits 10 = 24 bits 11 = 32 bits
	5	AIF_BCLK_INV	0	**BCLK Inversion Control** Slave mode: 0 = use rising edge 1 = use falling edge Master mode: 0 = BCLK normal 1 = BCLK inverted
	6	AIF_LRCLK_INV	0	**LRCLK Inversion Control** 0 = normal polarity 1 = inverted polarity When AIF_FMT[2:0]=011 (DSP Mode): 0 = mode A (2nd clock) 1 = mode B (1st clock)

Table 10 Audio Interface Control

DIGITAL AUDIO DATA SAMPLING RATES

The external master clock is applied directly to the MCLK input pin. In a system where there are a number of possible sources for the reference clock, it is recommended that the clock source with the lowest jitter be used for the master clock to optimise the performance of the WM8523.

In slave mode the WM8523 has a detection circuit that automatically determines the relationship between the master clock frequency (MCLK) and the sampling rate (LRCLK), to within ±32 system clock periods. The MCLK must be synchronised with the LRCLK, although the device is tolerant of phase variations or jitter on the MCLK.

If the device is configured in slave mode using auto-detect or in hardware mode, and during sample rate change the ratio between MCLK and LRCLK varies more than once within 1026 LRCLK periods, then it is recommended that the device be taken into the standby state or the off state before the sample rate change and held in standby until the sample rate change is complete. This will ensure correct operation of the detection circuit on the return to the enabled state. For details on the standby state, please refer to the Software Control Interface (software mode, page 15) and Power Up and Down Control In Hardware Mode section of the datasheet (hardware mode, on page 31).

The DAC supports MCLK to LRCLK ratios of 128fs to 1152fs and sampling rates of 8kHz to 192kHz, provided the internal signal processing of the DAC is programmed to operate at the correct rate.

Table 11 shows typical master clock frequencies and sampling rates supported by the WM8523 DAC.

SAMPLING RATE LRCLK	MASTER CLOCK FREQUENCY (MHz)						
	128fs	192fs	256fs	384fs	512fs	768fs	1152fs
8kHz	Unavailable	Unavailable	2.048	3.072	4.096	6.144	9.216
32kHz	Unavailable	Unavailable	8.192	12.288	16.384	24.576	36.864
44.1kHz	Unavailable	Unavailable	11.2896	16.9344	22.5792	33.8688	Unavailable
48kHz	Unavailable	Unavailable	12.288	18.432	24.576	36.864	Unavailable
88.2kHz	11.2896	16.9344	22.5792	33.8688	Unavailable	Unavailable	Unavailable
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable	Unavailable
176.4kHz	22.5792	33.8688	Unavailable	Unavailable	Unavailable	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable	Unavailable

Table 11 MCLK Frequencies and Audio Sample Rates

DAC FEATURES

SYSTEM ENABLE

The WM8523 includes a number of enable and disable mechanisms to allow the device to be powered on and off in a pop-free manner. The SYS_ENA[1:0] control bits enable the DAC and analogue paths.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 PSCTRL1 02h	1:0	SYS_ ENA[1:0]	00	**System Power Control** 00 = Off 01 = Power down 10 = Power up and mute 11 = Power up and unmute

Table 12 System Enable Control

Note: MCLK must be present at all times when using the SYS_ENA[1:0] bits. If MCLK is stopped at any point the device will power down to the 'off' state, but all register settings will remain. Restarting MCLK will start the device internal power sequence and the device will return to the power state set by the SYS_ENA[1:0] bits.

The power up and power down sequences are summarised in Figure 23. There is no requirement to manually cycle the device through the sequence via register writes, as the device will always automatically step through each stage in the sequence.

Power Up

When SYS_ENA[1:0]=00, the internal clocks are stopped and all analogue and digital blocks are disabled for maximum power saving. The device starts up in this state in software mode. Setting SYS_ENA[1:0]=01 enables the internal charge pump and required control circuitry, but the signal path remains powered down. When SYS_ENA[1:0]=10 all blocks are powered up sequentially and full system configuration is achieved. Once this is complete, the device is ready to pass audio but is muted. Setting SYS_ENA[1:0]=11 releases the mute and audio playback begins.

Power Down

When SYS_ENA[1:0]=11 the device is powered up and passing audio. Changing SYS_ENA[1:0]=10 applies a digital softmute to the output. Setting SYS_ENA[1:0]=01 sequentially powers down all circuit blocks but leaves the charge pump and required control circuitry enabled. This can be considered the low-power standby state. Finally, setting SYS_ENA[1:0]=00 will disable all circuit blocks including the charge pump, and full system initialisation will be required to restart the device.