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WM8594

24-bit 192kHz 2Vrms Multi-Channel CODEC

DESCRIPTION

The WM8594 is a high performance multi-channel audio CODEC with flexible input/output selection and digital and analogue volume control. Features include a 24-bit stereo ADC with digital gain control, two 24-bit DACs with independent volume control and clocking, and a range of input/output channel selection options with analogue volume control for flexible routing within current and future audio systems.

The WM8594 has a five stereo input selector which accepts input levels up to 2Vrms. One stereo input can be routed to the ADC. All inputs can be routed to an output selector.

The WM8594 outputs three stereo audio channels at line levels up to 2Vrms, which can be selected from any of the analogue inputs and DAC outputs. Additionally, one stereo output is available with a headphone driver. The DAC channels include independent digital volume control, and all three stereo output channels include analogue volume control with soft ramp.

The WM8594 supports up to 2Vrms analogue inputs, 2Vrms outputs, with sampling rates from 32kHz to 192kHz for the DACs, and 32kHz to 96kHz for the ADC.

The WM8594 is controlled via a serial interface with support for 2-wire and 3-wire control with full readback. Control of mute, powerdown and reset can also be achieved by pin selection.

The WM8594 is ideal for audio applications requiring high performance and flexible routing options, including flat panel digital TV and DVD recorder.

The WM8594 is available in a 48-lead TQFP package.

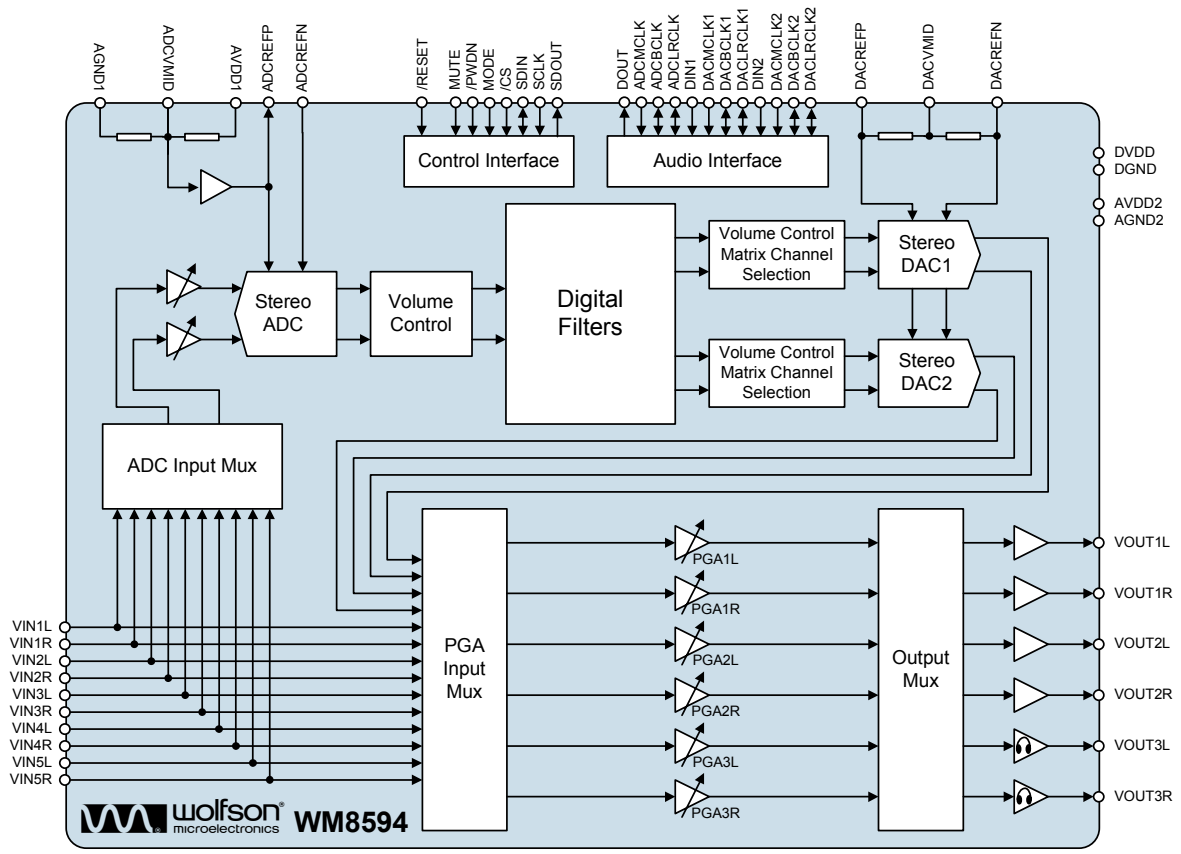
FEATURES

- Multi-channel CODEC with 5 stereo input selector and 3 stereo output selector
- 4-channel DAC, 2-channel ADC
- 5x2Vrms stereo input selector with 3x2 channel analogue bypass to output selector
- 3x2Vrms stereo output selector
- Stereo headphone driver
- Audio performance
  - DAC: 100dB SNR typical ('A' weighted @ 48kHz)
  - DAC: -87dB THD typical
  - ADC: 96dB SNR typical ('A' weighted @ 48kHz)
  - ADC: -80dB THD typical
- Independent sampling rate for ADC and DACs
- Independent sampling rate for DAC1 and DAC2
- DACs sampling frequency 32kHz – 192kHz
- ADC sampling frequency 32kHz – 96kHz
- DAC digital volume control +12dB to -100dB in 0.5dB steps
- ADC digital volume control from +30dB to -97dB in 0.5dB steps
- ADC input analogue boost control, selectable from 0dB, +3dB, +6dB and +12dB
- Output analogue volume control +6dB to -73.5dB in 0.5dB steps with zero cross or soft ramp to prevent pops and clicks
- Headphone drive capability on one stereo output with jack detect
- 2 and 3-wire serial control interface with readback and hardware reset, mute and powerdown pins
- Independent master or slave clocking modes
- Programmable format audio data interface modes
  - I^2S, LJ, RJ, DSP
- 3.3V / 9V analogue, 3.3V digital supply operation
- 48-lead TQFP package

APPLICATIONS

- Digital Flat Panel TV
- DVD-RW

BLOCK DIAGRAM



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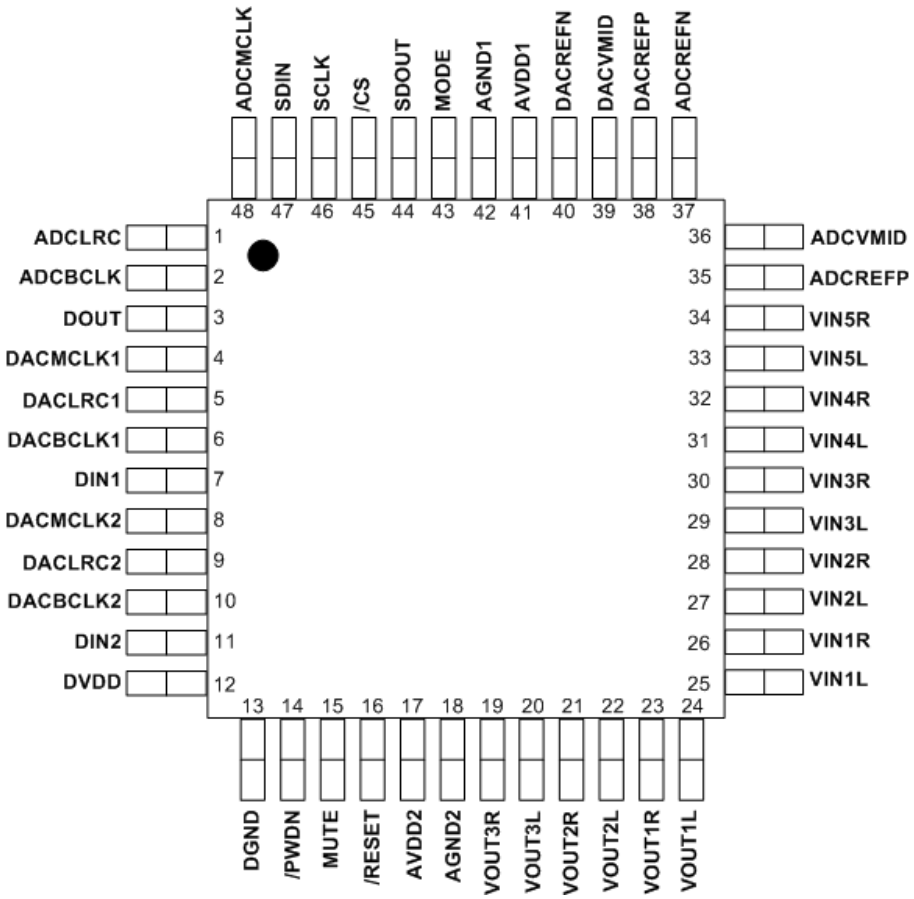
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8594SEFT/V	-40 to +85°C	48-lead TQFP (Pb-free)	MSL3	260˚C
WM8594SEFT/RV	-40 to +85°C	48-lead TQFP (Pb-free, tape and reel)	MSL3	260˚C

Note:

Reel quantity = 2,200

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	ADCLRC	Digital Input/Output	ADC audio interface left/right clock input/output
2	ADCBCLK	Digital Input/Output	ADC audio interface bit clock input/output
3	DOUT	Digital Output	ADC data output
4	DACMCLK1	Digital Input	DAC1 master clock
5	DACLRC1	Digital input	DAC1 audio interface left/right clock input
6	DACBCLK1	Digital Input	DAC1 audio interface bit clock input
7	DIN1	Digital Input	DAC 1 data input
8	DACMCLK2	Digital Input	DAC2 master clock
9	DACLRC2	Digital input	DAC2 audio interface left/right clock input
10	DACBCLK2	Digital Input	DAC2 audio interface bit clock input
11	DIN2	Digital Input	DAC 2 data input
12	DVDD	Supply	Digital supply
13	DGND	Supply	Digital ground
14	/PWDN	Digital Input	Hardware standby mode
15	MUTE	Digital Input	Hardware DAC mute
16	/RESET	Digital Input	Hardware reset
17	AVDD2	Supply	Analogue 9V supply
18	AGND2	Supply	Analogue ground
19	VOUT3R	Analogue Output	Output selector channel 3 right output
20	VOUT3L	Analogue Output	Output selector channel 3 left output
21	VOUT2R	Analogue Output	Output selector channel 2 right output
22	VOUT2L	Analogue Output	Output selector channel 2 left output
23	VOUT1R	Analogue Output	Output selector channel 1 right output
24	VOUT1L	Analogue Output	Output selector channel 1 left output
25	VIN1L	Analogue Input	Input selector channel 1 left input
26	VIN1R	Analogue Input	Input selector channel 1 right input
27	VIN2L	Analogue Input	Input selector channel 2 left input
28	VIN2R	Analogue Input	Input selector channel 2 right input
29	VIN3L	Analogue Input	Input selector channel 3 left input
30	VIN3R	Analogue Input	Input selector channel 3 right input
31	VIN4L	Analogue Input	Input selector channel 4 left input
32	VIN4R	Analogue Input	Input selector channel 4 right input
33	VIN5L	Analogue Input	Input selector channel 5 left input
34	VIN5R	Analogue Input	Input selector channel 5 right input
35	ADCREFP	Analogue Input	Positive reference for ADC
36	ADCVMID	Analogue Output	Midrail divider decoupling pin for ADC
37	ADCREFN	Analogue Input	Ground reference for ADC
38	DACREFP	Analogue Input	Positive reference for DACs
39	DACVMID	Analogue Output	Midrail divider decoupling pin for DACs
40	DACREFN	Analogue Input	Ground reference for DACs
41	AVDD1	Supply	Analogue 3.3V supply
42	AGND1	Supply	Analogue ground
43	MODE	Digital Input	Software mode select (High = 3-wire, Low = 2-wire)
44	SDOUT	Digital Output	Software mode: serial control interface data output
45	/CS	Digital Input	Software mode: serial control interface chip select
46	SCLK	Digital Input	Software mode: serial control interface clock signal
47	SDIN	Digital Input	Software mode: serial control interface data signal
48	ADCMCLK	Digital Input	ADC master clock input

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Digital supply voltage, DVDD	-0.3V	+4.5V
Analogue supply voltage, AVDD1	-0.3V	+7V
Analogue supply voltage, AVDD2	-0.3V	+15V
Voltage range digital inputs	DGND -0.3V	DVDD + 0.3V
Voltage range analogue inputs	AGND – 2.4V	AVDD1 + 2.4V
Master Clock Frequency		38.462MHz
Ambient temperature (supplies applied)	-55°C	+125°C
Storage temperature	-65°C	+150°C
Pb free package body temperature (reflow 10 seconds)		+260°C
Package body temperature (soldering 2 minutes)		+183°C

Note:

1. Analogue and digital grounds must always be within 0.3V of each other.

THERMAL PERFORMANCE

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal resistance – junction to ambient	$R_{\theta JA}$			56.5 See note 1		°C/W

Notes:

1. Figure given for package mounted on 4-layer FR4 according to JESD51-7. (No forced air flow is assumed).
2. Thermal performance figures are estimated.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital power supply	DVDD		2.97	3.3	3.6	V
Analogue power supply	AVDD1		2.97	3.3	3.6	V
Analogue power supply	AVDD2		8.1	9	9.9	V
Ground	DGND/AGND1/ AGND2			0		V
Operating temperature range	T_A		-40		+85	°C

Notes:

1. Digital supply (DVDD) must never be more than 0.3V greater than AVDD1 in normal operation.
2. Digital ground (DGND) and analogue grounds (AGND1, AGND2) must never be more than 0.3V apart.

SUPPLY CURRENT CONSUMPTION

Test Conditions

AVDD2=9V, AVDD1=DVDD=3.3V, AGND1=AGND2=0V, DGND=0V, T_A=+25˚C, fs=48kHz, MCLK=256fs unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Record (DACs disabled)						
Digital supply current	I_{DVDD}	fs=48kHz, 256fs Quiescent		8.6		mA
Analogue supply 1 current	I_{AVDD1}			9.2		mA
Analogue supply 2 current	I_{AVDD2}			0.01		mA
DAC Playback (ADC disabled, one DAC disabled)						
Digital supply current	I_{DVDD}	fs=48kHz, 256fs Quiescent		5.5		mA
Analogue supply 1 current	I_{AVDD1}			6.5		mA
Analogue supply 2 current	I_{AVDD2}			2.0		mA
Digital supply current	I_{DVDD}	fs=96kHz, 256fs Quiescent		9.5		mA
Analogue supply 1 current	I_{AVDD1}			7.0		mA
Analogue supply 2 current	I_{AVDD2}			2.0		mA
Digital supply current	I_{DVDD}	fs=192kHz, 256fs Quiescent		10.0		mA
Analogue supply 1 current	I_{AVDD1}			7.0		mA
Analogue supply 2 current	I_{AVDD2}			2.0		mA
ADC Record, DAC Playback (all circuit blocks enabled)						
Digital supply current	I_{DVDD}	fs=48kHz, 256fs Quiescent		17.0		mA
Analogue supply 1 current	I_{AVDD1}			20.0		mA
Analogue supply 2 current	I_{AVDD2}			11.0		mA
Power Down (all circuit blocks disabled)						
Digital supply current	I_{DVDD}	No inputs		160		µA
Analogue supply 1 current	I_{AVDD1}			0.1		µA
Analogue supply 2 current	I_{AVDD2}			0.1		µA

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD2=9V, AVDD1=DVDD=3.3V, AGND1=AGND2=0V, DGND=0V, TA=+25˚C, 1kHz signal, fs=48kHz, MCLK=256fs unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital logic levels						
Input low level	V_{IL}				0.3xDVDD	V
Input high level	V_{IH}		0.7xDVDD			V
Output low level	V_{OL}				0.1 x DVDD	V
Output high level	V_{OH}		0.9 x DVDD			V
Digital input leakage current				±0.2		µA
Digital input leakage capacitance				5		pF
Analogue Reference Levels						
ADC Midrail Voltage	ADCVMID			AVDD1/2		V
ADC Buffered Positive Reference Voltage	ADCREFP			ADCVMID		V
DAC Midrail Voltage	DACVMID			DACREFP/2		V
Potential divider resistance		AVDD1 to ADCVMID ADCVMID to AGND1		100		kΩ
		DACVREFP to DACVMID DACVMID to DACVREFN VMID_SEL[1:0] = 01		75 (Note 2)		kΩ
Analogue Line Outputs						
Output signal level (0dB)		R_L = 10kΩ	-10%	2.0x AVDD2 / 9	+10%	Vrms
Maximum capacitance load					11	nF
Minimum resistance load			1			kΩ
Analogue Headphone Outputs						
Output signal level (0dB)		R_L = 32Ω, P_O=20mW		0.8x AVDD2 / 9		Vrms
Minimum resistance load			16			Ω
Analogue Inputs						
Input signal level (0dB)				2.0 x AVDD1/3.3		Vrms
Input impedance			10	12	14	kΩ
Extended input impedance (Note 3)		External resistor = 10kΩ		21		kΩ
Input capacitance				5		pF

Test Conditions

AVDD2=9V, AVDD1=DVDD=3.3V, AGND1=AGND2=0V, DGND=0V, TA=+25°C, 1kHz signal, fs=48kHz, MCLK=256fs unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC Performance						
Signal to Noise Ratio[1,5]	SNR	A-weighted @ fs = 48kHz	90	100		dB
		A-weighted @ fs = 96kHz		100		dB
		A-weighted @ fs = 192kHz		100		dB
Dynamic Range[2,5]	DNR	A-weighted, -60dB full scale input	90	100		dB
Total Harmonic Distortion[3,5]	THD	1kHz, 0dBFS @ fs = 48kHz		-87	-80	dB
		1kHz, 0dBFS @ fs = 96kHz		-86		dB
		1kHz, 0dBFS @ fs = 192kHz		-85		dB
Channel Separation[4,5]		1kHz		110		dB
Channel Level Matching				0.1		dB
Channel Phase Deviation				0.05		Degree
Power supply rejection ratio	PSRR	1kHz, 100mVpp		50		dB
		20Hz to 20kHz, 100mVpp		45		dB
ADC Performance						
Signal to Noise Ratio[1,5]	SNR	A-weighted, 0dB gain @ fs = 48kHz	85	96		dB
		A-weighted, 0dB gain @ fs = 96kHz		98		dB
Dynamic Range[2,5]	DNR	A-weighted, -60dB full scale input	85	96		dB
Total Harmonic Distortion[3,5]	THD	1kHz, -1dBFS @ fs = 48kHz		-80	-70	dB
		1kHz, -1dBFS @ fs = 96kHz		-78		dB
Channel Separation[4,5]				110		dB
Channel Level Matching				0.1		dB
Channel Phase Deviation				0.05		Degree
Power Supply Rejection Ratio	PSRR			70		dB
				52		dB
Analogue Bypass Paths						
Signal to Noise Ratio[1,5]	SNR	A-weighted		103		dB
Dynamic Range[2,5]	DNR	A-weighted		103		dB
Total Harmonic Distortion[3,5]	THD			90		dB
Channel Separation[4,5]				110		dB
Channel Level Matching				0.1		dB
Channel Phase Deviation				0.05		Degree
Headphone Amplifier						
Output signal level (0dB)		R_L=32Ω P_O=20mW		0.8		Vrms
Signal to Noise Ratio[1,5]	SNR	A-weighted		98		dB
Total Harmonic Distortion	THD	P_O=10mW, R_L=16Ω		-66		dB
		P_O=20mW, R_L=32Ω		-70		dB
Channel Separation[4,5]		1kHz		92		dB
Power Supply Rejection Ratio	PSRR	1kHz, 100mVpp		50		dB

Test Conditions

AVDD2=9V, AVDD1=DVDD=3.3V, AGND1=AGND2=0V, DGND=0V, TA=+25˚C, 1kHz signal, fs=48kHz, MCLK=256fs unless otherwise stated

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Volume Control						
ADC minimum digital volume				-97		dB
ADC maximum digital volume				+30		dB
ADC volume step size				0.5		dB
DAC minimum digital volume				-100		dB
DAC maximum digital volume				+12		dB
DAC volume step size				0.5		dB
Analogue Volume Control						
Minimum gain				-73.5		dB
Maximum gain				+6		dB
Step size				0.5		dB
Mute attenuation				120		dB
Crosstalk						
DAC to ADC		1kHz signal, ADC fs=48kHz, DAC fs=44.1kHz		100		dB
		20kHz signal, ADC fs=48kHz, DAC fs=44.1kHz		100		dB
ADC to DAC		1kHz signal, ADC fs=48kHz, DAC fs=44.1kHz		100		dB
		20kHz signal, ADC fs=48kHz, DAC fs=44.1kHz		100		dB

TERMINOLOGY

1. Signal-to-noise ratio (dBFS) – SNR is the difference in level between a reference full scale output signal and the device output with no signal applied. This ratio is also called idle channel noise. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dBFS) – DNR is a measure of the difference in level between the highest and lowest components of a signal. Normally a THD measurement at -60dBFS. The measured signal is then corrected by adding 60dB to the result, e.g. THD @ -60dBFS = -30dB, DNR = 90dB.
3. Total Harmonic Distortion (dBFS) – THD is the difference in level between a reference full scale output signal and the first seven odd harmonics of the output signal. To calculate the ratio, the fundamental frequency of the output signal is notched out and an RMS value of the next seven odd harmonics is calculated.
4. Channel Separation (dB) – Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
5. All performance measurements carried out with 20kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.

Notes:

1. All minimum and maximum values are subject to change.
2. This resistance is selectable using VMID_SEL[1:0] – see Figure 52 for full details.
3. See p77 for details of extended input impedance configuration.

MASTER CLOCK TIMING

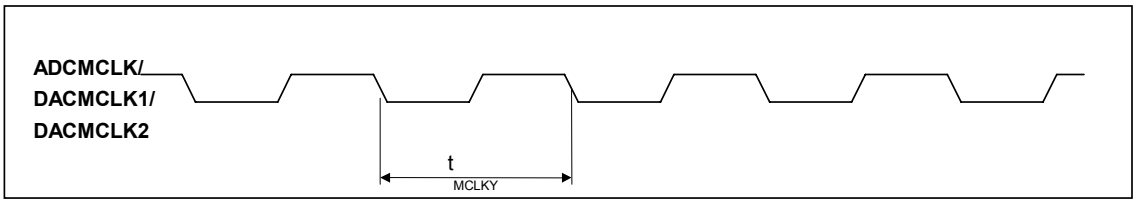


Figure 1 MCLK Timing

Test Conditions

AVDD1, DVDD = 3.3V, AVDD2 = 9V, AGND1, AGND2, DGND = 0V, T_A = +25^{O}C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Master Clock Timing Information					
MCLK System clock cycle time	t_{MCLKY}	27		120	ns
MCLK Duty cycle		40:60		60:40	%
MCLK Period Jitter				200	ps
MCLK Rise/Fall times				10	ns

Table 1 Master Clock Timing Requirements

/RESET TIMING

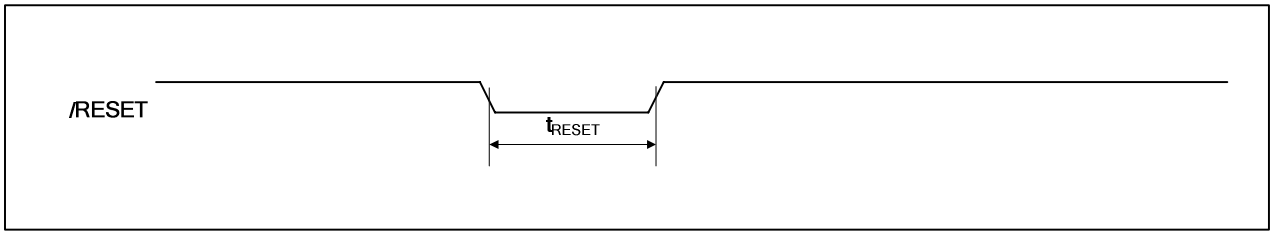


Figure 2 /RESET Timing

Test Conditions

AVDD1, DVDD = 3.3V, AVDD2 = 9V, AGND1, AGND2, DGND = 0V, T_A = +25^{O}C

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
/RESET Timing Information					
/RESET pulsewidth low	T_{RESET}	10			ns

Table 2 /RESET Timing Requirements

DIGITAL AUDIO INTERFACE TIMING – SLAVE MODE

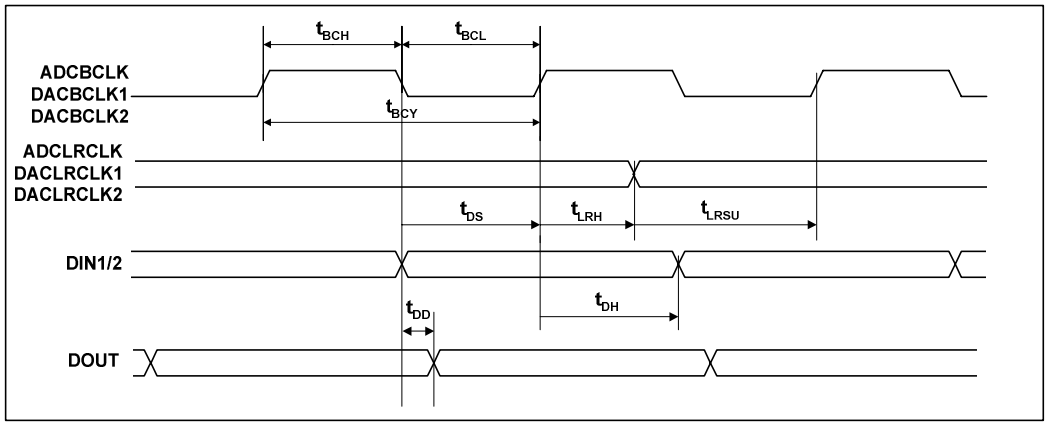


Figure 3 Slave Mode Digital Audio Data Timing

Test Conditions

AVDD1, DVDD = 3.3V, AVDD2 = 9V, AGND1, AGND2, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, ADCMCLK, DACMCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
ADCBCLK / DACBCLK1 / DACBCLK2 cycle time	t_{BCY}	80			ns
ADCBCLK / DACBCLK1 / DACBCLK2 pulse width high	t_{BCH}	30			ns
ADCBCLK / DACBCLK1 / DACBCLK2 pulse width low	t_{BCL}	30			ns
ADCBCLK / DACBCLK1 / DACBCLK2 rise/fall times				5	ns
ADCLRCLK / DACLRCLK1 / DACLRCLK2 set-up time to ADCBCLK / DACBCLK1 / DACLRCLK2 rising edge	t_{LRSU}	22			ns
ADCLRCLK / DACLRCLK1 / DACLRCLK2 hold time from ADCBCLK / DACBCLK1 / DACBCLK2 rising edge	t_{LRH}	25			ns
ADCLRCLK / DACLRCLK1 / DACLRCLK2 rise/fall times				5	ns
DIN1/2 hold time from DACBCLK1 / DACBCLK2 rising edge	t_{DH}	25			ns
DOUT propagation delay from ADCBCLK falling edge	t_{DD}	4		16	ns

Table 3 Slave Mode Audio Interface Timing

DIGITAL AUDIO INTERFACE TIMING – MASTER MODE

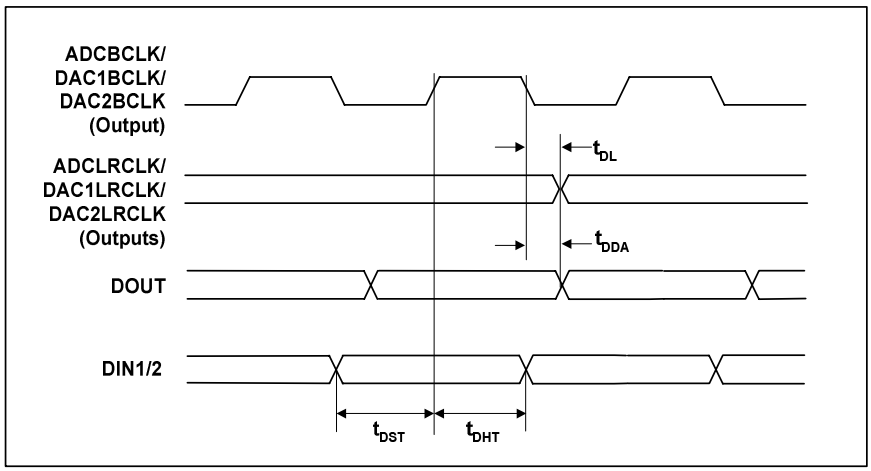


Figure 4 Master Mode Digital Audio Data Timing

Test Conditions

AVDD1, DVDD = 3.3V, AVDD2 = 9V, AGND1, AGND2, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, ADCMCLK, DACMCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
ADCLRCLK / DACLRCLK1 / DACLRCLK2 propagation delay from ADCBCLK / DACBCLK1 / DACLRCLK2 falling edge	t_{DL}	4		16	ns
DOUT propagation delay from ADCBCLK falling edge	t_{DDA}	4		16	ns
DIN1 / DIN2 setup time to DACBCLK1 / DACBCLK2 rising edge	t_{DST}	22			ns
DIN1 / DIN2 hold time to DACBCLK1 / DACBCLK2 rising edge	t_{DHT}	25			ns

Table 4 Master Mode Audio Interface Timing

CONTROL INTERFACE TIMING – 2-WIRE MODE

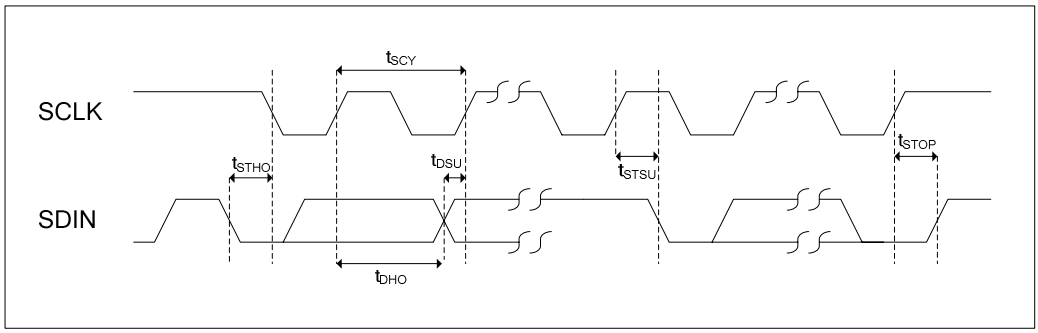


Figure 5 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

AVDD1, DVDD = 3.3V, AVDD2 = 9V, AGND1, AGND2, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, ADCMCLK, DACMCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK pulse cycle time	t_{SCY}	2500			ns
SCLK duty cycle		40/60		60/40	%
SCLK frequency				400	kHz
Hold Time (Start Condition)	t_{STHO}	600			ns
Setup Time (Start Condition)	t_{STSU}	600			ns
Data Setup Time	t_{DSU}	100			ns
SDIN, SCLK Rise Time				300	ns
SDIN, SCLK Fall Time				300	ns
Setup Time (Stop Condition)	t_{STOP}	600			ns
Data Hold Time	t_{DHO}			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	2		8	ns

Table 5 Control Interface Timing – 2-Wire Serial Control Mode

CONTROL INTERFACE TIMING – 3-WIRE MODE

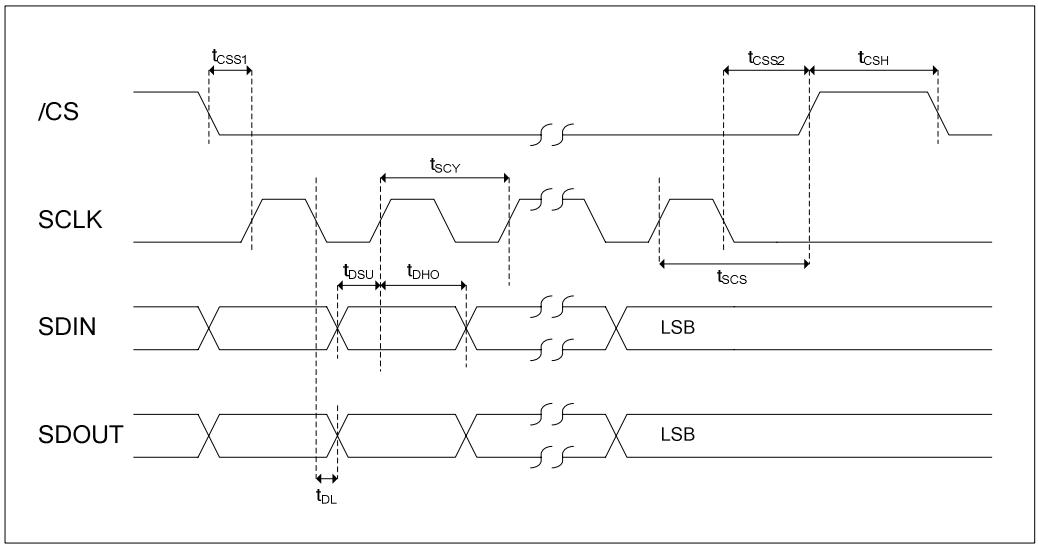


Figure 6 Control Interface Timing – 3-Wire Serial Control Mode

Test Conditions

AVDD1, DVDD = 3.3V, AVDD2 = 9V, AGND1, AGND2, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, ADCMCLK, DACMCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB rising edge	t_{SCS}	80			ns
SCLK pulse cycle time	t_{SCY}	160			ns
SCLK duty cycle		40/60		60/40	%
SDIN to SCLK set-up time	t_{DSU}	20			ns
SDIN hold time from SCLK rising edge	t_{DHO}	40			ns
SDOUT propagation delay from SCLK rising edge	t_{DL}			5	ns
/CS pulse width high	t_{CSH}	40			ns
/CS rising/falling to SCLK rising	t_{CSS1}	40			ns
SCLK falling to /CS rising	t_{CSS2}	40			ns
Pulse width of spikes that will be suppressed	t_{ps}	2		8	ns

Table 6 Control Interface Timing – 3-Wire Serial Control Mode

POWER ON RESET (POR)

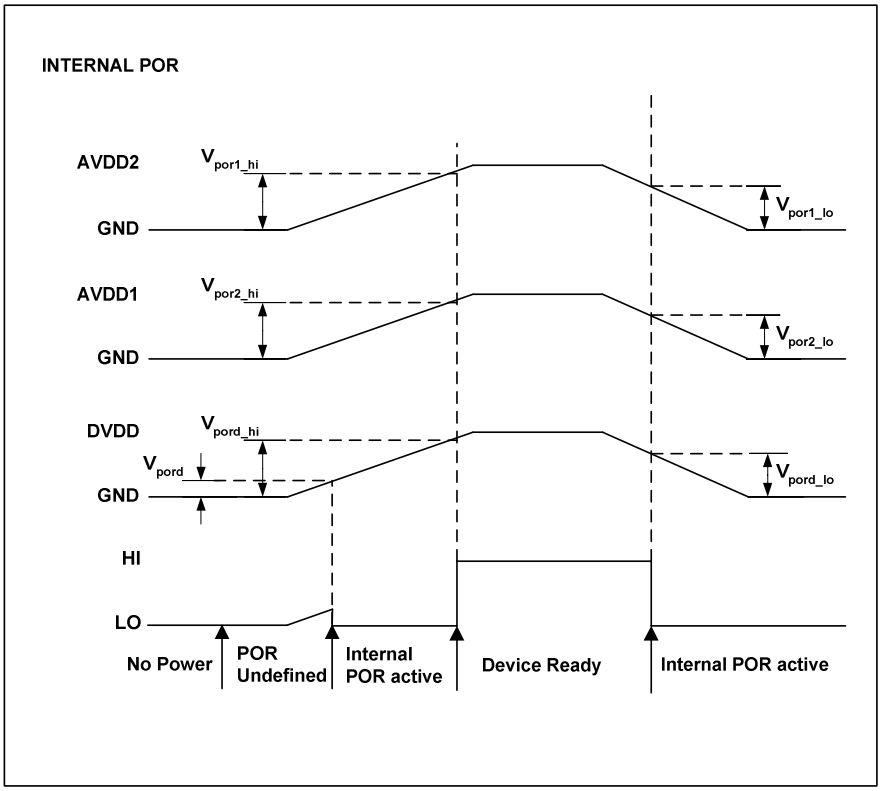


Figure 1 Power Supply Timing Requirements

Test Conditions

DVDD = 3.3V, AVDD1 = 3.3V, AVDD2 = 9V DGND = AGND1 = AGND2 = 0V, T_A = +25°C, T_{A_max} = +125°C, T_{A_min} = -25°C
$AVDD1_{max}$ = $DVDD_{max}$ = 3.63V, $AVDD1_{min}$ = $DVDD_{mim}$= 2.97V, $AVDD2_{max}$ = 9.9V, $AVDD2_{min}$ = 8.1V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Input Timing Information						
VDD level to POR defined (DVDD rising)	V_{pord}	Measured from DGND	0.27	0.36	0.60	V
VDD level to POR rising edge (DVDD rising)	V_{pord_hi}	Measured from DGND	1.34	1.88	2.32	V
VDD level to POR falling edge (DVDD falling)	V_{pord_lo}	Measured from DGND	1.32	1.86	2.30	V
VDD level to POR rising edge (AVDD1 rising)	V_{por1_hi}	Measured from DGND	1.65	1.68	1.85	V
VDD level to POR falling edge (AVDD1 falling)	V_{por1_lo}	Measured from DGND	1.63	1.65	1.83	V
VDD level to POR rising edge (AVDD2 rising)	V_{por2_hi}	Measured from DGND	1.80	1.86	2.04	V
VDD level to POR falling edge (AVDD2 falling)	V_{por2_lo}	Measured from DGND	1.76	1.8	2.02	V

Table 7 Power on Reset

DEVICE DESCRIPTION

INTRODUCTION

The WM8594 is a high performance multi-channel audio CODEC with 2Vrms line level inputs and outputs and flexible analogue input / output switching. The device comprises a 24-bit stereo ADC, two 24-bit stereo DACs with independent sampling rates and digital volume control, and a flexible analogue input and output multiplexer. Analogue inputs and outputs are all at 2Vrms line level, minimising external component count.

The DACs can operate from independent left/right clocks, bit clocks and master clocks with independent data inputs. Alternatively, the DACs can be synchronised to use the same clocks with independent data inputs. Each of the DAC audio interfaces can be configured to operate in ether master or slave clocking modes. In master mode, left/right clocks and bit clocks are all outputs. In slave mode, left/right clocks and bit clocks are all inputs.

The ADC uses a separate left/right clock, bit clock and master clock, allowing independent recording and playback in audio applications. The ADC audio interface can be configured to operate in either master or slave clocking mode. In master mode, left/right clocks and bit clocks are all outputs. In slave mode, left/right clocks and bit clocks are all inputs.

The ADC includes digital gain control, allowing signals to be gained and attenuated between +30dB and -97dB in 0.5dB steps.

The DACs include independent digital volume control, which is adjustable between +12dB and -100 dB in 0.5dB steps. The DACs can be configured to output stereo audio data and a range of mono audio options.

The input multiplexer accepts five stereo line level inputs at up to 2Vrms. One stereo input can be routed to the ADC, and all five stereo inputs can be routed to the output multiplexer.

The output multiplexer includes analogue volume control with zero cross, adjustable between +6dB and -73.5dB in 0.5dB steps, and configurable soft ramp rate. Analogue audio is output at 2Vrms line level.

Control of the internal functionality of the device is by 2-wire serial control interface with readback. The interface may be asynchronous to the audio data interface as control data will be re-synchronised to the audio processing internally. In addition, control of mute, power-down and reset may also be achieved by pin selection.

Operation using system clocks of 128fs, 192fs, 256fs, 384fs, 512fs, 768fs or 1152fs is provided. ADC and both DACs may be clocked independently. Sampling rates from 32kHz to 192kHz are supported for both DACs provided the appropriate master clocks are input. Sampling rates from 32kHz to 96kHz are supported for the ADC provided the appropriate master clock is input.

The audio data interface supports right justified, left justified, and I^2S interface formats along with a highly flexible DSP serial port interface format.

CONTROL INTERFACE

Control of the WM8594 is achieved by a 2-wire SM-bus-compliant or 3-wire SPI compliant serial interface with readback. Software interface mode is selected using the MODE pin as shown in Table 8 below:

MODE	INTERFACE FORMAT
Low	2 wire
High	3 wire

Table 8 Control Interface Mode Selection

2-WIRE (SM-BUS COMPATIBLE) SERIAL CONTROL INTERFACE MODE

Many devices can be controlled by the same bus, and each device has a unique 7-bit address.

REGISTER WRITE

The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address and read/write bit, MSB first). If the device address received matches the address of the WM8594, the WM8594 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised, the WM8594 returns to the idle condition and waits for a new start condition with valid address.

When the WM8594 has acknowledged a correct address, the controller sends the first byte of control data (B23 to B16, i.e. the WM8594 register address). The WM8594 then acknowledges the first data byte by pulling SDIN low for one SCLK pulse. The controller then sends a second byte of control data (B15 to B8, i.e. the first 8 bits of register data), and the WM8594 acknowledges again by pulling SDIN low for one SCLK pulse. Finally, the controller sends a third byte of control data (B7 to B0, i.e. the final 8 bits of register data), and the WM8594 acknowledges again by pulling SDIN low for one SCLK pulse.

The transfer of data is complete when there is a low to high transition on SDIN while SCLK is high. After receiving a complete address and data sequence the WM8594 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the WM8594 reverts to the idle condition.

The WM8594 device 2-wire write address is 34h (00110100) or 36h (00110110), selectable by control of /CS.

/CS (PIN 45)	2-WIRE BUS ADDRESS (B[7:1])
0	34h (0011010)
1	36h (0011011)

Table 9 2-Wire Control Interface Bus Address Selection

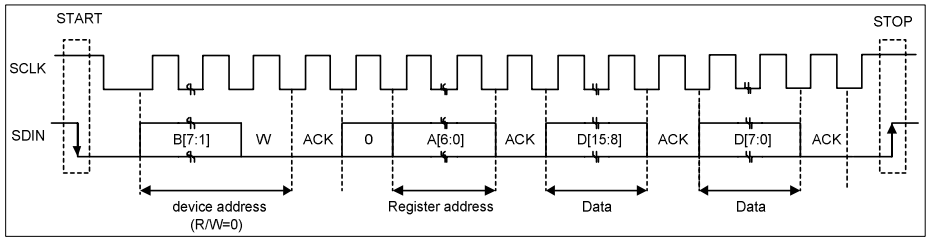


Figure 7 2-Wire Write Protocol

AUTO-INCREMENT REGISTER WRITE

It is possible to write to multiple consecutive registers using the auto-increment feature. When AUTO_INC is set, the register write protocol follows the method shown in Figure 8. As with normal register writes, the controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high, and all devices on the bus receive the device address.

When the WM8594 has acknowledged a correct address, the controller sends the first byte of control data (A6 to A0, i.e. the WM8594 initial register address). The WM8594 then acknowledges the first control data byte by pulling SDIN low for one SCLK pulse. The controller then sends a byte of register data. The WM8594 acknowledges the first byte of register data, auto-increments the register address to be written to, and waits for the next byte of register data. Subsequent bytes of register data can be written to consecutive registers of the WM8594 without setting up the device and register address.

The transfer of data is complete when there is a low to high transition on SDIN while SCLK is high.

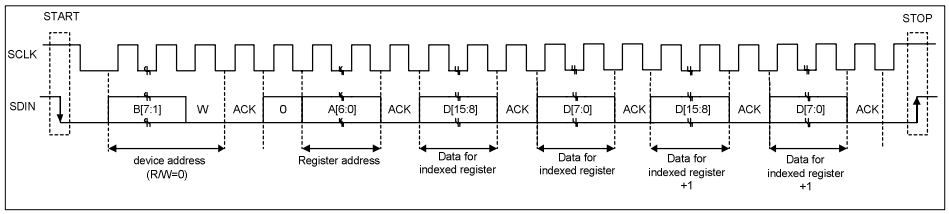


Figure 8 2-Wire Auto-Increment Register Write

REGISTER READBACK

The WM8594 allows readback of all registers with data output on the bidirectional SDIN pin. The protocol is similar to that used to write to the device. The controller will issue the device address followed by a write bit, and the register index will then be passed to the WM8594.

At this point the controller will issue a repeated start condition and resend the device address along with a read bit. The WM8594 will acknowledge this and the WM8594 will become a slave transmitter.

The WM8594 will place the data from the indexed register onto SDIN MSB first. When the controller receives the first byte of data, it acknowledges it. When the controller receives the second and final byte of data it will not acknowledge receipt of the data indicating that it will resume master transmitter control of SDIN. The controller will then issue a stop command completing the read cycle.

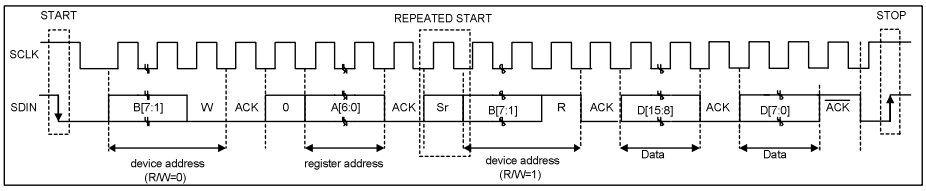


Figure 9 2-wire Read Protocol

AUTO-INCREMENT REGISTER READBACK

It is possible to read from multiple consecutive registers in continuous readback mode. Continuous readback mode is selected by setting AUTO_INC.

In continuous readback mode, the WM8594 will return the indexed register first, followed by consecutive registers in increasing index order until the controller issues a stop sequence.

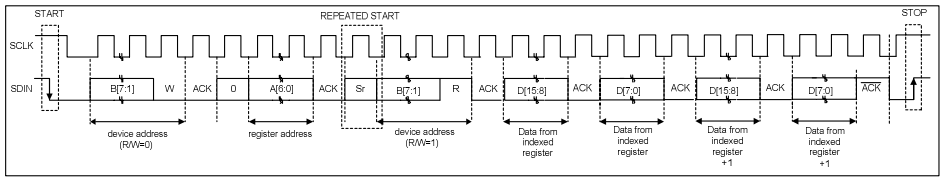


Figure 10 2-Wire Auto-Increment Register Readback

3-WIRE (SPI COMPATIBLE) SERIAL CONTROL INTERFACE MODE

REGISTER WRITE

SDIN is used for the program data, SCLK is used to clock in the program data and /CS is use to latch in the program data. SDIN is sampled on the rising edge of SCLK. The 3-wire interface write protocol is shown in Figure 11.

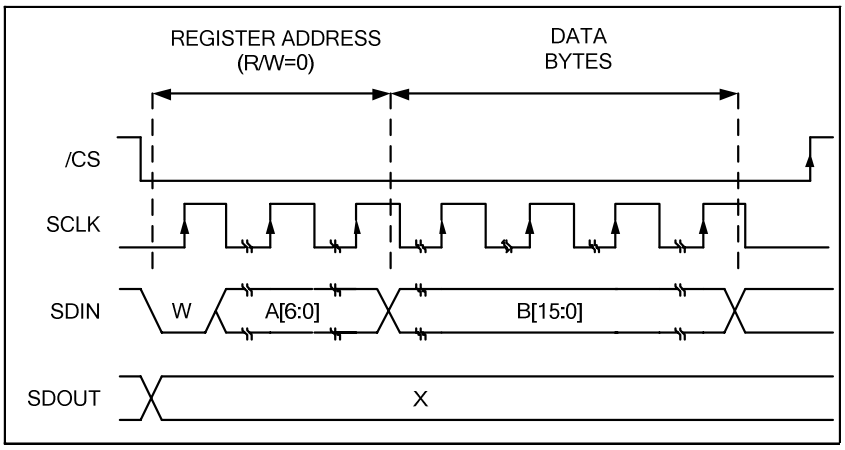


Figure 11 3-Wire Serial Interface Write Protocol

- W indicates write operation.
- A[6:0] is the register index.
- B[15:0] is the data to be written to the register indexed.
- /CS is edge sensitive – the data is latched on the rising edge of /CS.

REGISTER READ-BACK

The read-only status registers can be read back via the SDOUT pin. Read Back is enabled when the R/W bit is high. The data can then be read by writing to the appropriate register address, to which the device will respond with data.

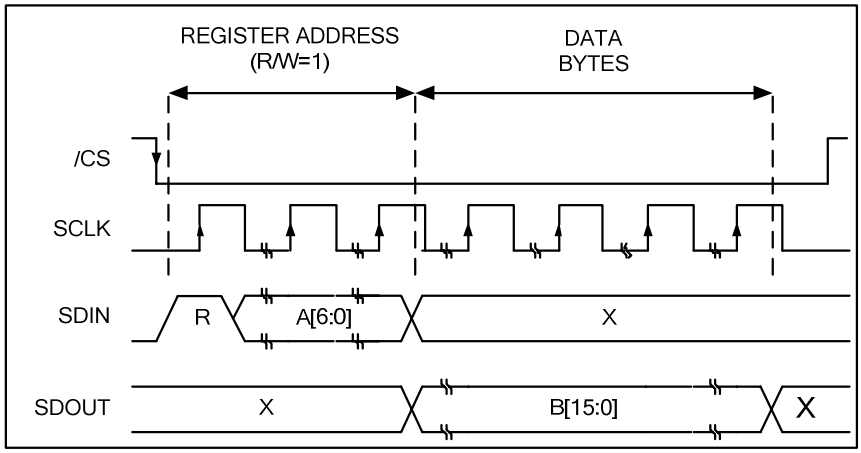


Figure 12 3-Wire Serial Interface Readback Protocol

REGISTER RESET

Any write to register R0 (00h) will reset the WM8594. All register bits are reset to their default values.

DEVICE ID AND REVISION

Reading from register R0 returns the device ID. Reading from register R1 returns the device revision number.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 DEVICE_ID 00h	15:0	DEVICE_ID [15:0]	10000101 10010100	**Device ID** A read of this register will return the device ID, 0x8594.
R1 REVISION 01h	7:0	REVNUM [7:0]	N/A	**Device Revision** A read of this register will return the device revision number. This number is sequentially incremented if the device design is updated.

Table 10 Device ID and Revision Number

DIGITAL AUDIO DATA FORMATS

The WM8594 supports a range of common audio interface formats:

- I^2S
- Left Justified (LJ)
- Right Justified (RJ)
- DSP Mode A
- DSP Mode B

All formats send the MSB first and support word lengths of 16, 20, 24 and 32 bits, with the exception of 32 bit RJ mode, which is not supported.

Audio data for each stereo channel is time multiplexed with the interface's left/right clock indicating whether the left or right channel is present. The left/right clock is also used as a timing reference to indicate the beginning or end of the data words.

In LJ, RJ and I^2S modes, the minimum number of bit clock periods per left/right clock period is two times the selected word length. The left/right clock must be high for a minimum of bit clock periods equivalent to the word length, and low for the same period. For example, for a word length of 24 bits, the left/right clock must be high for a minimum of 24 bit clock periods and low for a minimum of 24 bit clock periods. Any mark to space ratio is acceptable for the left/right clock provided these requirements are met.

In DSP modes A and B, left and right channels must be time multiplexed and input on DIN1. LRCLK is used as a frame synchronisation signal to identify the MSB of the first input word. The minimum number of bit clock periods per left/right clock period is two times the selected word length. Any mark to space ratio is acceptable for the left/right clock provided the rising edge is correctly positioned.

I2S MODE

In I^2S mode, the MSB of input data is sampled on the second rising edge of bit clock following a left/right clock transition. The MSB of output data changes on the first falling edge of bit clock following a left/right clock transition, and may be sampled on the next rising edge of bit clock. Left/right clocks are low during the left channel audio data samples and high during the right channel audio data samples.

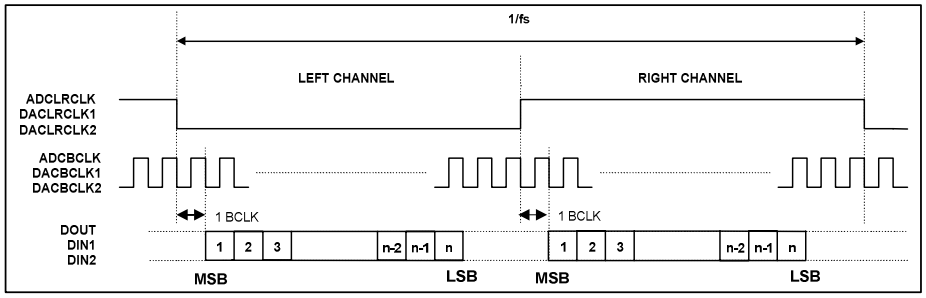


Figure 13 I2S Mode Timing

LEFT JUSTIFIED (LJ) MODE

In LJ mode, the MSB of the input data is sampled by the WM8594 on the first rising edge of bit clock following a left/right clock transition. The MSB of output data changes on the same falling edge of bit clock as left/right clock and may be sampled on the next rising edge of bit clock. Left/right clock is high during the left channel audio data samples and low during the right channel audio data samples.

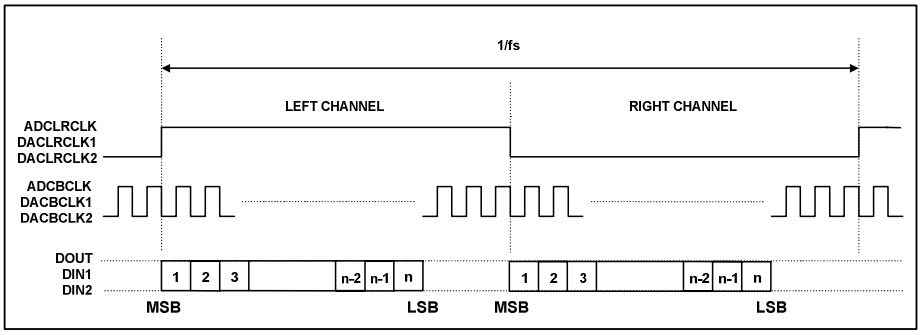


Figure 14 LJ Mode Timing

RIGHT JUSTIFIED (RJ) MODE

In RJ mode the LSB of input data is sampled on the rising edge of bit clock preceding a left/right clock transition. The LSB of output data changes on the falling edge of bit clock preceding a left/right clock transition, and may be sampled on the next rising edge of bit clock. Left/right clock is high during the left channel audio data samples and low during the right channel audio data samples.

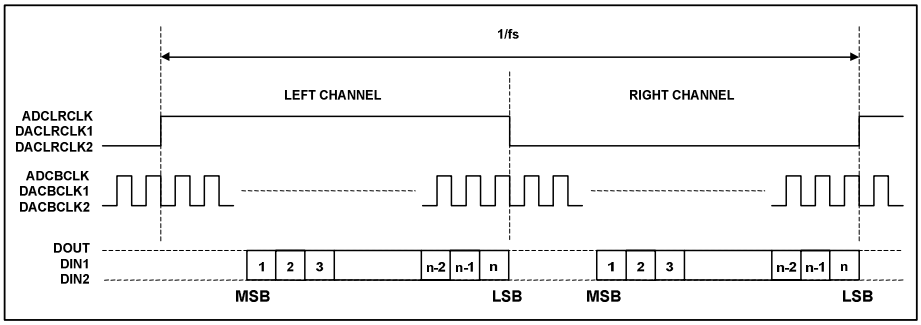


Figure 15 RJ Mode Timing

DSP MODE A

In DSP Mode A, the MSB of channel 1 left data input is sampled on the second rising edge of bit clock following a left/right clock rising edge. Channel 1 right data then follows. The MSB of output data changes on the first falling edge of bit clock following a left/right clock transition and may be sampled on the rising edge of bit clock. The right channel data is contiguous with the left channel data.

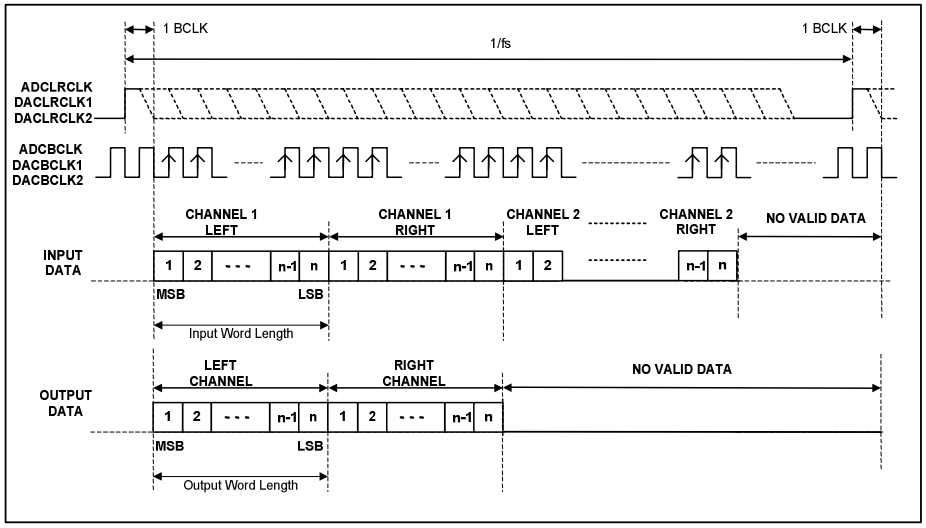


Figure 16 DSP Mode A Timing

DSP MODE B

In DSP Mode B, the MSB of channel 1 left data input is sampled on the first bit clock rising edge following a left/right clock rising edge. Channel 1 right data then follows. The MSB of output data changes on the same falling edge of BCLK as the low to high left/right clock transition and may be sampled on the rising edge of bit clock. The right channel data is contiguous with the left channel data.

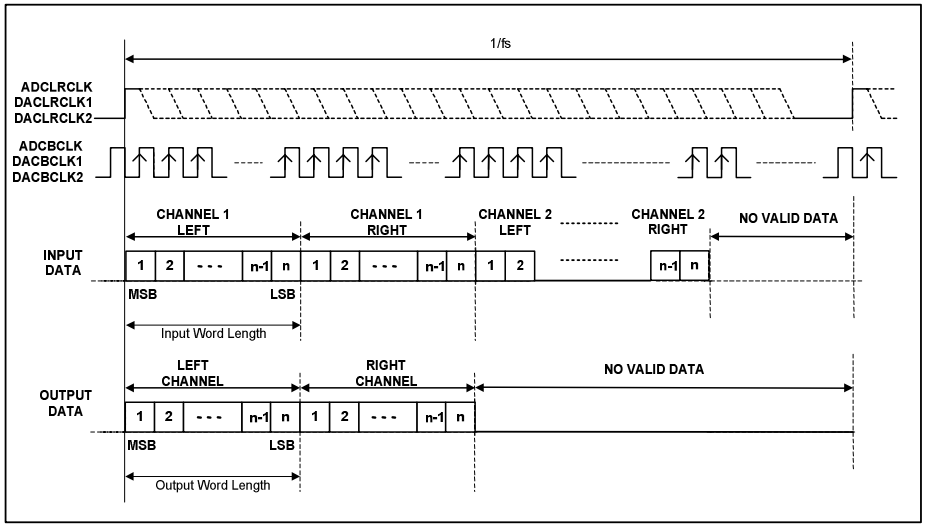


Figure 17 DSP Mode B Timing

DIGITAL AUDIO INTERFACE CONTROL

The control of the audio interface formats is achieved by register write. Dynamically changing the audio data format may cause erroneous operation and is not recommended.

Interface timing is such that the input data and left/right clock are sampled on the rising edge of the interface bit clock. Output data changes on the falling edge of the interface bit clock. By setting the appropriate bit clock and left/tight clock polarity bits, the WM8594 ADC and DACs can sample data on the opposite clock edges.

The control of audio interface formats and clock polarities is summarised in Table 11.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 DAC1_CTRL1 02h	1:0	DAC1_ FMT[1:0]	10	**DAC1 Audio Interface Format** 00 = Right Justified 01 = Left Justified 10 = I^2S 11 = DSP
	3:2	DAC1_ WL[1:0]	10	**DAC1 Audio Interface Word Length** 00 = 16-bit 01 = 20-bit 10 = 24-bit 11 = 32-bit (not available in Right Justified mode)
	4	DAC1_BCP	0	**DAC1 BCLK Polarity** 0 = DACBCLK not inverted - data latched on rising edge of BCLK 1 = DACBCLK inverted - data latched on falling edge of BCLK

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	5	DAC1_LRP	0	**DAC1 LRCLK Polarity** 0 = DACLRCLK not inverted 1 = DACLRCLK inverted
R7 DAC2_CTRL1 07h	1:0	DAC2_ FMT[1:0]	10	**DAC2 Audio Interface Format** 00 = Right Justified 01 = Left Justified 10 = I^2S 11 = DSP
	3:2	DAC2_ WL[1:0]	10	**DAC2 Audio Interface Word Length** 00 = 16-bit 01 = 20-bit 10 = 24-bit 11 = 32-bit (not available in Right Justified mode)
	4	DAC2_BCP	0	**DAC2 BCLK Polarity** 0 = DACBCLK not inverted - data latched on rising edge of BCLK 1 = DACBCLK inverted - data latched on falling edge of BCLK
	5	DAC2_LRP	0	**DAC2 LRCLK Polarity** 0 = DACLRCLK not inverted 1 = DACLRCLK inverted
R13 ADC_CTRL1 0Dh	1:0	ADC_ FMT[1:0]	10	**ADC Audio Interface Format** 00 = Right Justified 01 = Left Justified 10 = I^2S 11 = DSP
	3:2	ADC_ WL[1:0]	10	**ADC Audio Interface Word Length** 00 = 16-bit 01 = 20-bit 10 = 24-bit 11 = 32-bit (not available in Right Justified mode)
	4	ADC_BCP	0	**ADC BCLK Polarity** 0 = ADCBCLK not inverted - data latched on rising edge of BCLK 1 = ADCBCLK inverted - data latched on falling edge of BCLK
	5	ADC_LRP	0	**ADC LRCLK Polarity** 0 = ADCLRCLK not inverted 1 = ADCLRCLK inverted

Table 11 Audio Interface Control