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WM8731 / WM8731L

Portable Internet Audio CODEC with Headphone Driver and Programmable Sample Rates

DESCRIPTION

The WM8731 or WM8731L (WM8731/L) are low power stereo CODECs with an integrated headphone driver. The WM8731/L is designed specifically for portable MP3 audio and speech players and recorders. The WM8731 is also ideal for MD, CD-RW machines and DAT recorders.

Stereo line and mono microphone level audio inputs are provided, along with a mute function, programmable line level volume control and a bias voltage output suitable for an electret type microphone.

Stereo 24-bit multi-bit sigma delta ADCs and DACs are used with oversampling digital interpolation and decimation filters. Digital audio input word lengths from 16-32 bits and sampling rates from 8kHz to 96kHz are supported.

Stereo audio outputs are buffered for driving headphones from a programmable volume control, line level outputs are also provided along with anti-thump mute and power up/down circuitry.

The device is controlled via a 2 or 3 wire serial interface. The interface provides access to all features including volume controls, mutes, de-emphasis and extensive power management facilities. The device is available in a small 28-lead SSOP package or the smaller 28 lead quad flat leadless package (QFN).

FEATURES

- Highly Efficient Headphone Driver
- Audio Performance
  - ADC SNR 90dB ('A' weighted) at 3.3V, 85dB at 1.8V
  - DAC SNR 100dB ('A' weighted) at 3.3V, 95dB at 1.8V
- Low Power
  - Playback only 22mW, 8mW ('L' Variant)
  - Analogue Pass Through 12mW, 3.5mW ('L' variant)
  - 1.42 – 3.6V Digital Supply Operation
  - 2.7 – 3.6V Analogue Supply Operation
  - 1.8 – 3.6V Analogue Supply Operation ('L' Variant)
- ADC and DAC Sampling Frequency: 8kHz – 96kHz
- Selectable ADC High Pass Filter
- 2 or 3-Wire MPU Serial Control Interface
- Programmable Audio Data Interface Modes
  - I^2S, Left, Right Justified or DSP
  - 16/20/24/32 bit Word Lengths
  - Master or Slave Clocking Mode
- Microphone Input and Electret Bias with Side Tone Mixer
- Available in 28-lead SSOP or 28-lead QFN package

APPLICATIONS

- Portable MP3 Players and Recorders
- CD and Minidisc Recorders
- PDAs / smartphones

BLOCK DIAGRAM

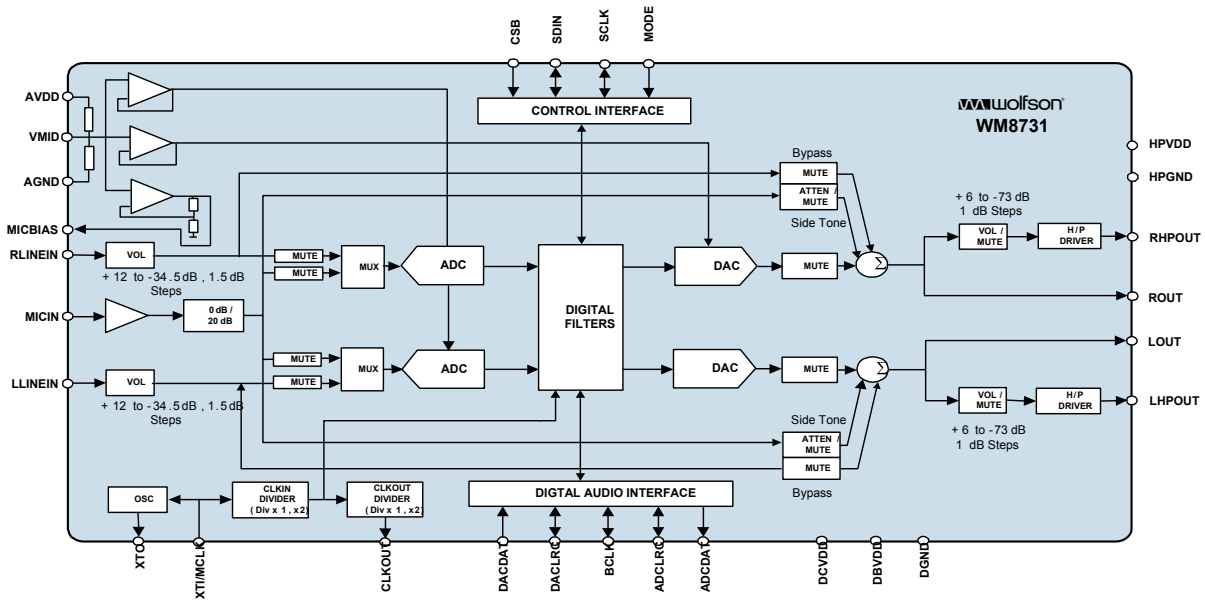
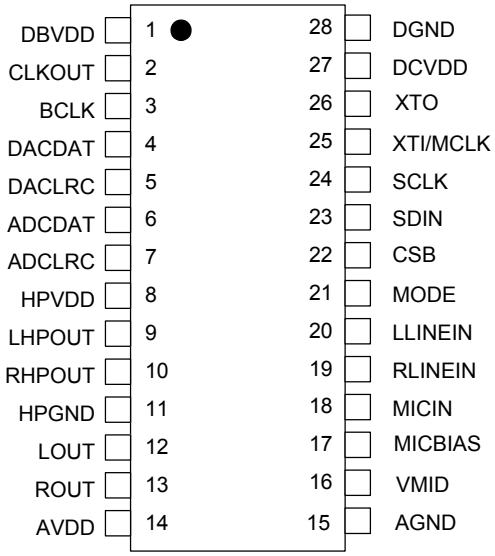


TABLE OF CONTENTS

PIN CONFIGURATION - 28 PIN SSOP

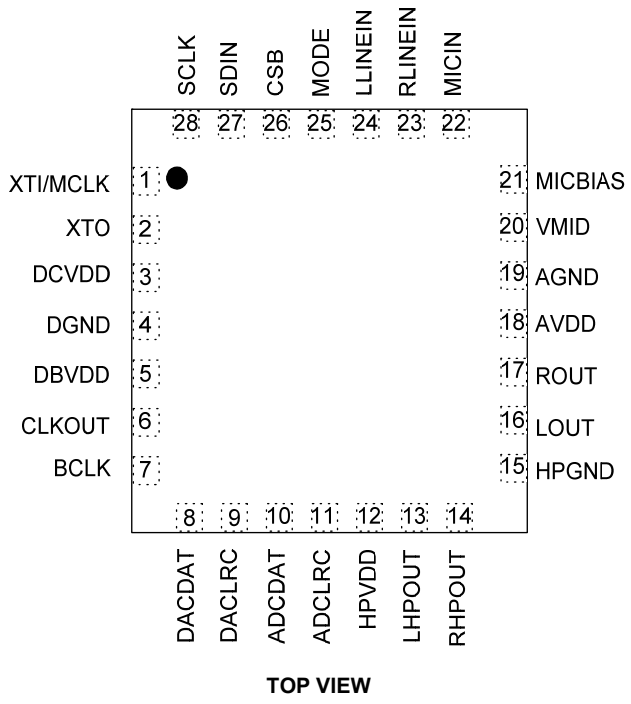


ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	AVDD RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8731SEDS/V	-40 to +85°C	2.7 to 3.6V	28-lead SSOP (Pb-free)	MSL3	260°C
WM8731SEDS/RV	-40 to +85°C	2.7 to 3.6V	28-lead SSOP (Pb-free, tape and reel)	MSL3	260°C

Note:
Reel quantity = 2,000

PIN CONFIGURATION – 28 PIN QFN



TOP VIEW

ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	AVDD RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8731CLSEFL	-40 to +85°C	1.8 to 3.6V	28-lead QFN (Pb-free)	MSL1	260°C
WM8731CLSEFL/R	-40 to +85°C	1.8 to 3.6V	28-lead QFN (Pb-free, tape and reel)	MSL1	260°C
WM8731CSEFL	-40 to +85°C	2.7 to 3.6V	28-lead QFN (Pb-free)	MSL1	260°C
WM8731CSEFL/R	-40 to +85°C	2.7 to 3.6V	28-lead QFN (Pb-free, tape and reel)	MSL1	260°C

Note:
Reel quantity = 3,500

PIN DESCRIPTION

28 PIN SSOP	28 PIN QFN	NAME	TYPE	DESCRIPTION
1	5	DBVDD	Supply	Digital Buffers VDD
2	6	CLKOUT	Digital Output	Buffered Clock Output
3	7	BCLK	Digital Input/Output	Digital Audio Bit Clock, Pull Down, (see Note 1)
4	8	DACDAT	Digital Input	DAC Digital Audio Data Input
5	9	DACLRC	Digital Input/Output	DAC Sample Rate Left/Right Clock, Pull Down (see Note 1)
6	10	ADCDAT	Digital Output	ADC Digital Audio Data Output
7	11	ADCLRC	Digital Input/Output	ADC Sample Rate Left/Right Clock, Pull Down (see Note 1)
8	12	HPVDD	Supply	Headphone VDD
9	13	LHPOUT	Analogue Output	Left Channel Headphone Output
10	14	RHPOUT	Analogue Output	Right Channel Headphone Output
11	15	HPGND	Ground	Headphone GND
12	16	LOUT	Analogue Output	Left Channel Line Output
13	17	ROUT	Analogue Output	Right Channel Line Output
14	18	AVDD	Supply	Analogue VDD
15	19	AGND	Ground	Analogue GND
16	20	VMID	Analogue Output	Mid-rail reference decoupling point
17	21	MICBIAS	Analogue Output	Electret Microphone Bias
18	22	MICIN	Analogue Input	Microphone Input (AC coupled)
19	23	RLINEIN	Analogue Input	Right Channel Line Input (AC coupled)
20	24	LLINEIN	Analogue Input	Left Channel Line Input (AC coupled)
21	25	MODE	Digital Input	Control Interface Selection, Pull Up (see Note 1)
22	26	CSB	Digital Input	3-Wire MPU Chip Select/ 2-Wire MPU interface address selection, active low, Pull up (see Note 1)
23	27	SDIN	Digital Input/Output	3-Wire MPU Data Input / 2-Wire MPU Data Input
24	28	SCLK	Digital Input	3-Wire MPU Clock Input / 2-Wire MPU Clock Input
25	1	XTI/MCLK	Digital Input	Crystal Input or Master Clock Input (MCLK)
26	2	XTO	Digital Output	Crystal Output
27	3	DCVDD	Supply	Digital Core VDD
28	4	DGND	Ground	Digital GND

Note:

1. Pull Up/Down only present when Control Register Interface ACTIVE=0 to conserve power.
2. It is recommended that the QFN ground paddle is connected to analogue ground on the application PCB.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+3.63V
Analogue supply voltage	-0.3V	+3.63V
Voltage range digital inputs	DGND -0.3V	DVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Operating temperature range, T_A	-40°C	+85°C
Storage temperature after soldering	-65°C	+150°C

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.
2. The digital supply core voltage (DCVDD) must always be less than or equal to the analogue supply voltage (AVDD)

RECOMMENDED OPERATING CONDITIONS – WM8731

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD		1.42		3.6	V
Digital supply range (Buffer)	DBVDD		2.7		3.6	V
Analogue supply range	AVDD, HPVDD		2.7		3.6	V
Ground	DGND,AGND,HPGND			0		V

Notes:

1. DCVDD must be lower than or equal to DBVDD.
2. USB Mode should not be used with DCVDD lower than 2V

RECOMMENDED OPERATING CONDITIONS – WM8731L

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD		1.42		3.6	V
Digital supply range (Buffer)	DBVDD		1.8		3.6	V
Analogue supply range	AVDD, HPVDD		1.8		3.6	V
Ground	DGND,AGND,HPGND			0		V

Notes:

1. If DBVDD is lower than 2.5V, DCVDD must be at least 0.225V lower than DBVDD.
2. If DBVDD is higher than or equal to 2.5V, DCVDD must be lower than or equal to DBVDD.
3. USB Mode should not be used with DCVDD lower than 2V

ELECTRICAL CHARACTERISTICS – WM8731

Test Conditions

AVDD, HPVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (CMOS Levels)						
Input LOW level	V_{IL}				0.3 x DBVDD	V
Input HIGH level	V_{IH}		0.7 x DBVDD			V
Output LOW	V_{OL}				0.10 x DBVDD	V
Output HIGH	V_{OH}		0.9 x DBVDD			V
Power On Reset Threshold (DCVDD)						
DCVDD Threshold On -> Off	V_{th}			0.9		V
Hysteresis	V_{IH}			0.3		V
DCVDD Threshold Off -> On	V_{OL}			0.6		V
Analogue Reference Levels						
Reference voltage (VMID)	V_{VMID}			AVDD/2		V
Potential divider resistance	R_{VMID}			50k		Ω
Line Input to ADC						
Input Signal Level (0dB)	V_{INLINE}			1.0 AVDD/3.3		Vrms
Signal to Noise Ratio (Note 1,3)	SNR	A-weighted, 0dB gain @ fs = 48kHz	85	90		dB
		A-weighted, 0dB gain @ fs = 96kHz		90		
		A-weighted, 0dB gain @ fs = 48kHz, AVDD = 2.7V		88		
Dynamic Range (Note 3)	DR	A-weighted, -60dB full scale input	85	90		dB
Total Harmonic Distortion	THD	-1dB input, 0dB gain		-84 0.006	-74 0.02	dB %
Power Supply Rejection Ratio	PSRR	1kHz, 100mVpp		50		dB
		20Hz to 20kHz, 100mVpp		45		
ADC channel separation		1kHz input		90		dB
Programmable Gain		1kHz input Rsource < 50Ω	-34.5	0	+12	dB
Programmable Gain Step Size		Guaranteed Monotonic		1.5		dB
Mute attenuation		0dB, 1kHz input		80		dB
Input Resistance	R_{INLINE}	0dB gain	20k	30k		Ω
		12dB gain	10k	15k		
Input Capacitance	C_{INLINE}			10		pF

Test Conditions

AVDD, HPVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

Microphone Input to ADC @ 0dB Gain, fs = 48kHz (40kΩ Source Impedance. See Figure 12)						
Input Signal Level (0dB)	V_{INMIC}			1.0 AVDD/3.3		Vrms
Signal to Noise Ratio (Note 1,3)	SNR	A-weighted, 0dB gain		85		dB
Dynamic Range (Note 3)	DR	A-weighted, -60dB full scale input		85		dB
Total Harmonic Distortion	THD	0dB input, 0dB gain		-60	-55	dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Programmable Gain Boost	MICBOOST bit set	1kHz input Rsource < 50Ω		34		dB
Mic Path gain (MICBOOST gain is additional to this nominal gain)		MICBOOST = 0 Rsource < 50Ω		14		dB
Mute attenuation		0dB, 1kHz input		80		dB
Input Resistance	R_{INMIC}			10k		Ω
Input Capacitance	C_{INMIC}			10		pF
Microphone Bias						
Bias Voltage	$V_{MICBIAS}$		0.75*AVDD – 100mV	0.75*AVDD	0.75*AVDD + 100mV	V
Bias Current Source	$I_{MICBIAS}$				3	mA
Output Noise Voltage	Vn	1K to 20kHz		25		nV/√Hz
Line Output for DAC Playback Only (Load = 10kΩ. 50pF)						
0dBfs Full scale output voltage		At LINE outputs		1.0 x AVDD/3.3		Vrms
Signal to Noise Ratio (Note 1,3)	SNR	A-weighted, @ fs = 48kHz	95	100		dB
		A-weighted @ fs = 96kHz		98		
		A-weighted, fs = 48kHz, AVDD = 2.7V		98		
Dynamic Range (Note 3)	DR	A-weighted, -60dB full scale input	85	95		dB
Total Harmonic Distortion	THD	1kHz, 0dBfs		-88	-80	dB
		1kHz, -3dBfs		-92		
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		
DAC channel separation	1kHz, 0dB			100		dB
Analogue Line Input to Line Output (Load = 10kΩ. 50pF, No Gain on Input) Bypass Mode						
0dB Full scale output voltage				1.0 x AVDD/3.3		Vrms
Signal to Noise Ratio (Note 1,3)	SNR		90	95		dB
Total Harmonic Distortion	THD	1kHz, 0dB		-86	-80	dB
		1kHz, -3dB		-92		
Power Supply Rejection Ratio	PSSR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		

Test Conditions

AVDD, HPVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

Mute attenuation		1kHz, 0dB		80		dB
Stereo Headphone Output						
0dB Full scale output voltage				1.0 x AVDD/3.3		Vrms
Max Output Power	P_O	RL = 32Ω		30		mW
		RL = 16Ω		50		
Signal to Noise Ratio (Note 1, 3)	SNR	A-weighted	90	97		dB
Total Harmonic Distortion	THD	1kHz, R_L = 32Ω		0.056	0.1	%
		P_O = 10mW rms (-5dB)		-65	60	dB
		1kHz, R_L = 32Ω		0.56	1.0	%
		P_O = 20mW rms (-2dB)		-45	40	dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz - 20kHz, 100mVpp		45		
Programmable Gain		1kHz	-73	0	6	dB
Programmable Gain Step Size		1kHz		1		dB
Mute attenuation		1kHz, 0dB		80		dB
Microphone Input to Headphone Output Side Tone Mode						
0dB Full scale output voltage				1.0 x AVDD/3.3		Vrms
Signal to Noise Ratio (Note 1,3)	SNR		90	95		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		
Programmable Attenuation		1kHz	6		15	dB
Programmable Attenuation Step Size		1kHz		3		dB
Mute attenuation		1kHz, 0dB		80		dB

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with the input short circuited, measured 'A' weighted over a 20Hz to 20kHz bandwidth using an Audio analyser.
2. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted over a 20Hz to 20kHz bandwidth.
3. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
4. VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.

POWER CONSUMPTION – WM8731

MODE DESCRIPTION	POWEROFF	CLKOUTPD	OSCPD	OUTPD	DACPD	ADCPD	MICPD	LINEINPD	CURRENT CONSUMPTION TYPICAL				
									AVDD (3.3V)	HP VDD (3.3V)	DC VDD (1.5V)	DB VDD (3.3V)	UNIT
Record and Playback													
Oscillator enabled	0	0	0	0	0	0	0	0	13.1	1.7	3.0	1.5	mA
External MCLK	0	0	1	0	0	0	0	0	13.1	1.7	3.2	0.8	mA
Oscillator and CLKOUT disabled, No microphone	0	1	1	0	0	0	1	0	12.2	1.7	3.2	0.07	mA
Playback Only													
Oscillator enabled	0	0	0	0	0	1	1	1	3.4	1.7	2.1	1.5	mA
External MCLK	0	1	1	0	0	1	1	1	3.3	1.7	2.3	0.07	mA
Record Only													
Line Record, oscillator enabled	0	0	0	1	1	0	1	0	9.2	-	2.6	1.3	mA
Line Record, using external MCLK	0	0	1	1	1	0	1	0	9.2	-	2.6	0.7	mA
Mic Record, oscillator enabled	0	0	0	1	1	0	0	1	8.6	-	2.7	1.5	mA
Mic Record, using external MCLK	0	0	1	1	1	0	0	1	8.6	-	2.6	0.7	mA
Side Tone (Microphone Input to Headphone Output)													
External clock still running	0	0	1	0	1	1	0	1	1.6	1.7	0.08	0.7	mA
Clock stopped	0	0	1	0	1	1	0	1	1.5	1.7	-	-	mA
Analogue Bypass (Line-in to Line-out)													
External clock still running	0	0	1	0	1	1	1	0	2.1	1.7	0.08	0.7	mA
Clock stopped	0	0	1	0	1	1	1	0	2.2	1.7	-	-	mA
Standby													
External clock still running	0	1	1	1	1	1	1	1	16	0.3	77	65	µA
Clock stopped	0	1	1	1	1	1	1	1	16	0.3	0.3	0.2	µA
Power Down													
External clock still running	1	1	1	1	1	1	1	1	0.2	0.3	77	65	µA
Clock stopped	1	1	1	1	1	1	1	1	0.3	0.3	0.3	0.3	µA

Table 1 Powerdown Mode Current Consumption Examples

Notes:

1. T_A = +25°C. fs = 48kHz, XTI/MCLK = 256fs (12.288MHz).
2. The data presented here was measured with the audio interface in master mode whenever the internal clock oscillator was used, and in slave mode whenever an external clock was used (i.e. MS = 1 when OSCPD = 0 and vice versa). However, it is also possible to use the WM8731 with MS = OSCPD = 0 or MS = OSCPD = 1.
3. All figures are quiescent, with no signal.
4. The power dissipation in the headphone itself not included in the above table.

ELECTRICAL CHARACTERISTICS – WM8731L

Test Conditions

AVDD, HPVDD, DBVDD = 1.8V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (CMOS Levels)						
Input LOW level	V_{IL}				0.3 x DBVDD	V
Input HIGH level	V_{IH}		0.7 x DBVDD			V
Output LOW	V_{OL}				0.10 x DBVDD	V
Output HIGH	V_{OH}		0.9 x DBVDD			V
Power On Reset Threshold (DCVDD)						
DCVDD Threshold On -> Off	V_{th}			0.9		V
Hysteresis	V_{IH}			0.3		V
DCVDD Threshold Off -> On	V_{OL}			0.6		V
Analogue Reference Levels						
Reference voltage (VMID)	V_{VMID}			AVDD/2		V
Potential divider resistance	R_{VMID}			50k		Ω
Line Input to ADC						
Input Signal Level (0dB)	V_{INLINE}			1.0 AVDD/3.3		Vrms
Signal to Noise Ratio (Note 1,3)	SNR	A-weighted, 0dB gain @ fs = 48kHz	75	85		dB
		A-weighted, 0dB gain @ fs = 96kHz		85		
Dynamic Range (Note 3)	DR	A-weighted, -60dB full scale input	80	88		dB
Total Harmonic Distortion	THD	-1dB input, 0dB gain		-76	-60	dB
Power Supply Rejection Ratio	PSRR	1kHz, 100mVpp		50		dB
		20Hz to 20kHz, 100mVpp		45		
ADC channel separation		1kHz input		90		dB
Programmable Gain		1kHz input Rsource < 50Ω	-34.5	0	+12	dB
Programmable Gain Step Size		Guaranteed Monotonic		1.5		dB
Mute attenuation		0dB, 1kHz input		80		dB
Input Resistance	R_{INLINE}	0dB gain	20k	30k		Ω
		12dB gain	10k	15k		
Input Capacitance	C_{INLINE}			10		pF

Test Conditions

AVDD, HPVDD, DBVDD = 1.8V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

Microphone Input to ADC @ 0dB Gain, fs = 48kHz (40kΩ Source Impedance. See Figure 12)						
Input Signal Level (0dB)	V_{INMIC}			1.0 AVDD/3.3		Vrms
Signal to Noise Ratio (Note 1,3)	SNR	A-weighted, 0dB gain		80		dB
Dynamic Range (Note 3)	DR	A-weighted, -60dB full scale input		70		dB
Total Harmonic Distortion	THD	0dB input, 0dB gain		-55		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Programmable Gain Boost	MICBOOST bit set	1kHz input Rsource < 50Ω		34		dB
Mic Path gain (MICBOOST gain is additional to this nominal gain)		MICBOOST = 0 Rsource < 50Ω		14		dB
Mute attenuation		0dB, 1kHz input		80		dB
Input Resistance	R_{INMIC}			10k		Ω
Input Capacitance	C_{INMIC}			10		pF
Microphone Bias						
Bias Voltage	$V_{MICBIAS}$		0.75*AVDD – 100mV	0.75*AVDD	0.75*AVDD + 100mV	V
Bias Current Source	$I_{MICBIAS}$				3	mA
Output Noise Voltage	Vn	1K to 20kHz		25		nV/√Hz
Line Output for DAC Playback Only (Load = 10k Ω. 50pF)						
0dBfs Full scale output voltage		At LINE outputs		1.0 x AVDD/3.3		Vrms
Signal to Noise Ratio (Note 1,3)	SNR	A-weighted, @ fs = 48kHz	85	95		dB
		A-weighted @ fs = 96kHz		93		
Dynamic Range (Note 3)	DR	A-weighted, -60dB full scale input	85	90		dB
Total Harmonic Distortion	THD	1kHz, 0dBfs		-80	-75	dB
		1kHz, -3dBfs		-90		
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		
DAC channel separation	1kHz, 0dB			100		dB
Analogue Line Input to Line Output (Load = 10k Ω. 50pF, No Gain on Input) Bypass Mode						
0dB Full scale output voltage				1.0 x AVDD/3.3		Vrms
Signal to Noise Ratio (Note 1,3)	SNR		85	90		dB
Total Harmonic Distortion	THD	1kHz, 0dB		-83	-76	dB
		1kHz, -3dB		-92		
Power Supply Rejection Ratio	PSSR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		
Mute attenuation		1kHz, 0dB		80		dB

Test Conditions

AVDD, HPVDD, DBVDD = 1.8V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

Stereo Headphone Output						
0dB Full scale output voltage				1.0 x AVDD/3.3		Vrms
Max Output Power	P_O	RL = 32 Ω		9		mW
		RL = 16 Ω		18		
Signal to Noise Ratio (Note 1,3)	SNR	A-weighted	86	95		dB
Total Harmonic Distortion	THD	1kHz, -5dB FS signal		0.08	0.1	%
		R_L = 32Ω		-62	-60	dB
		1kHz, -2dB FS signal			1	
		R_L = 32Ω			-40	
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz - 20kHz, 100mVpp		45		
Programmable Gain		1kHz	-73	0	6	dB
Programmable Gain Step Size		1kHz		1		dB
Mute attenuation		1kHz, 0dB		80		dB
Microphone Input to Headphone Output Side Tone Mode						
0dB Full scale output voltage				1.0 x AVDD/3.3		Vrms
Signal to Noise Ratio (Note 1,3)	SNR		85	90		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		
Programmable Attenuation		1kHz	6		15	dB
Programmable Attenuation Step Size		1kHz		3		dB
Mute attenuation		1kHz, 0dB		80		dB

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with the input short circuited, measured 'A' weighted over a 20Hz to 20kHz bandwidth using an Audio analyser.
2. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted over a 20Hz to 20kHz bandwidth.
3. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
4. VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.

POWER CONSUMPTION – WM8731L

MODE DESCRIPTION	POWEROFF	CLKOUTPD	OSCPD	OUTPD	DACPD	ADCPD	MICPD	LINEINPD	CURRENT CONSUMPTION TYPICAL				
									AVDD (1.8V)	HP VDD (1.8V)	DC VDD (1.5V)	DB VDD (1.8V)	UNIT
Record and Playback													
All active, oscillator enabled	0	0	0	0	0	0	0	0	6	0.6	2.7	0.9	mA
Playback Only													
Oscillator enabled	0	0	0	0	0	1	1	1	1.7	0.6	1.8	0.9	mA
Record Only													
Line Record, oscillator enabled	0	0	0	1	1	0	1	0	3.9	-	2.4	0.9	mA
Mic Record, oscillator enabled	0	0	0	1	1	0	0	1	3.6	-	2.4	0.9	mA
Side Tone (Microphone Input to Headphone Output)													
Clock stopped	0	0	1	0	1	1	0	1	0.8	0.6	-	-	mA
Analogue Bypass (Line-in to Line-out)													
Clock stopped	0	0	1	0	1	1	1	0	1.1	0.6	-	-	mA
Standby													
Clock stopped	0	1	1	1	1	1	1	1	8	-	-	-	μA
Power Down													
Clock stopped	1	1	1	1	1	1	1	1	0.2	0.2	0.3	0.2	μA

Table 2 Powerdown Mode Current Consumption Examples

Notes:

1. AVDD, HPVDD, DBVDD = 1.8V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C. Slave Mode, fs = 48kHz, XTI/MCLK = 256fs (12.288MHz).
2. All figures are quiescent, with no signal.
3. All figures are measured with the audio interface in master mode (MS = 1).
4. The power dissipation in the headphone itself is not included in the above table.

MASTER CLOCK TIMING

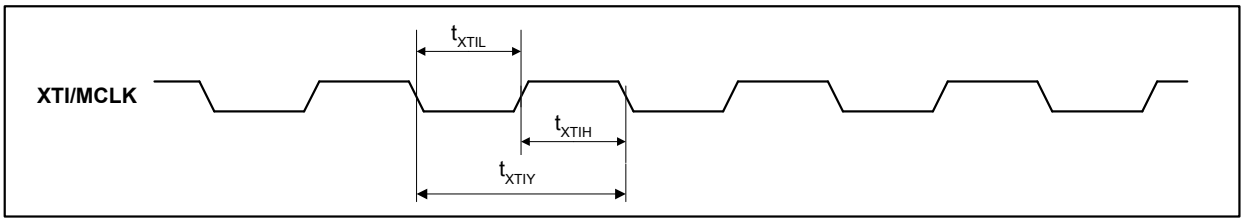


Figure 1 System Clock Timing Requirements

Test Conditions

AVDD, HPVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
XTI/MCLK System clock pulse width high	t_{XTIH}		18			ns
XTI/MCLK System clock pulse width low	t_{XTIL}		18			ns
XTI/MCLK System clock cycle time	t_{XTIY}		54			ns
XTI/MCLK Duty cycle			40:60		60:40	

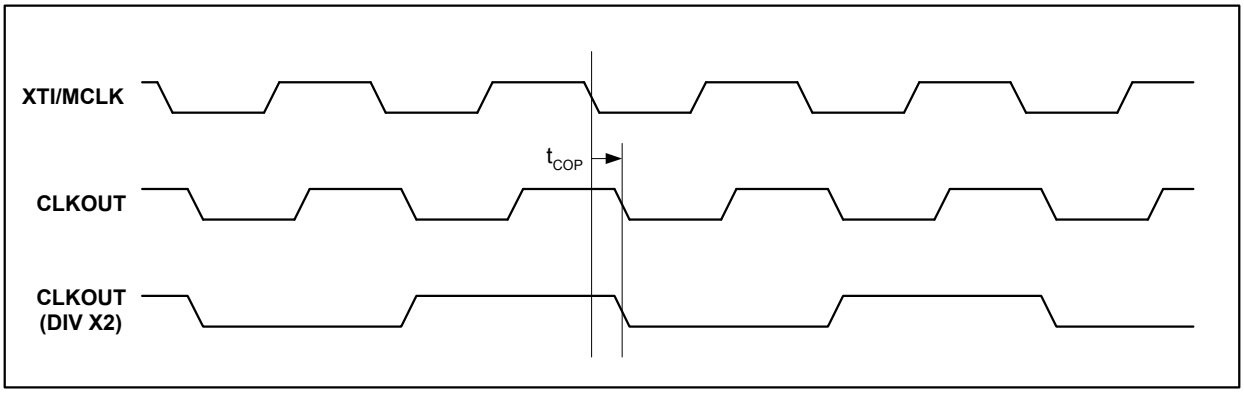


Figure 2 Clock Out Timing Requirements

Test Conditions

AVDD, HPVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
CLKOUT propagation delay from XTI/MCLK falling edge	t_{COP}		0		10	ns

DIGITAL AUDIO INTERFACE – MASTER MODE

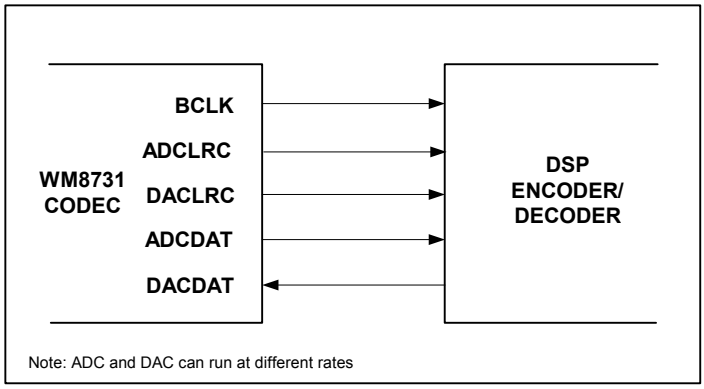


Figure 3 Master Mode Connection

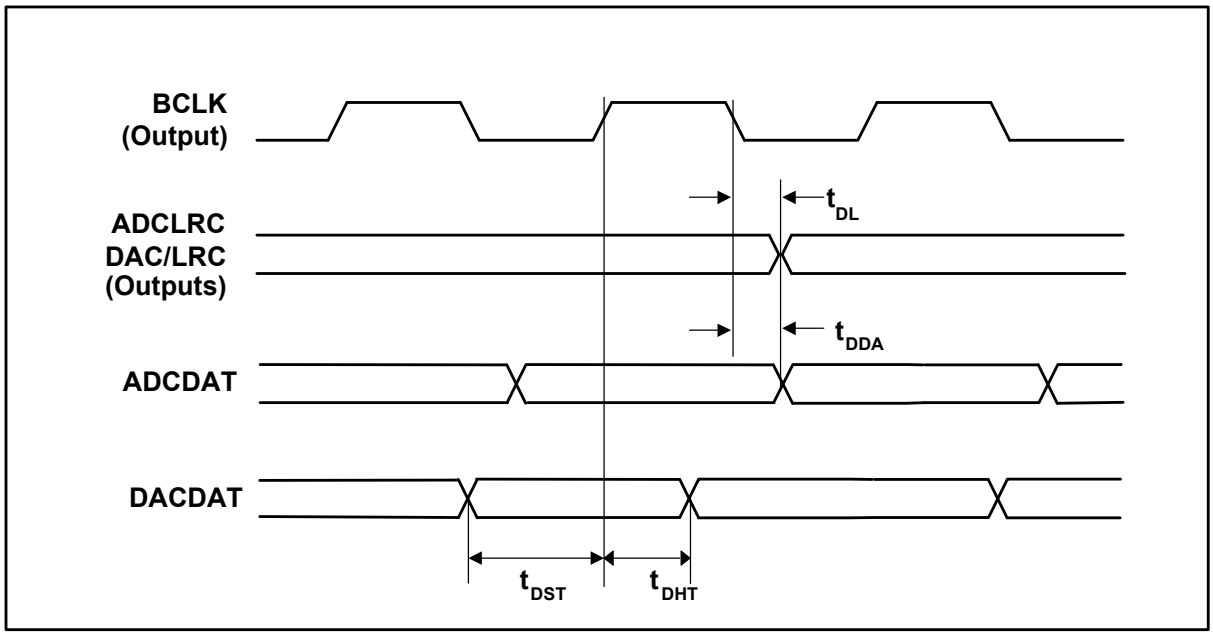


Figure 4 Digital Audio Data Timing – Master Mode

Test Conditions

AVDD, HPVDD, DBDD = 3.3V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
ADCLRC/DACLRC propagation delay from BCLK falling edge	t_{DL}		0		10	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}		0		35	ns
DACDAT setup time to BCLCK rising edge	t_{DST}		10			ns
DACDAT hold time from BCLK rising edge	t_{DHT}		10			ns

DIGITAL AUDIO INTERFACE – SLAVE MODE

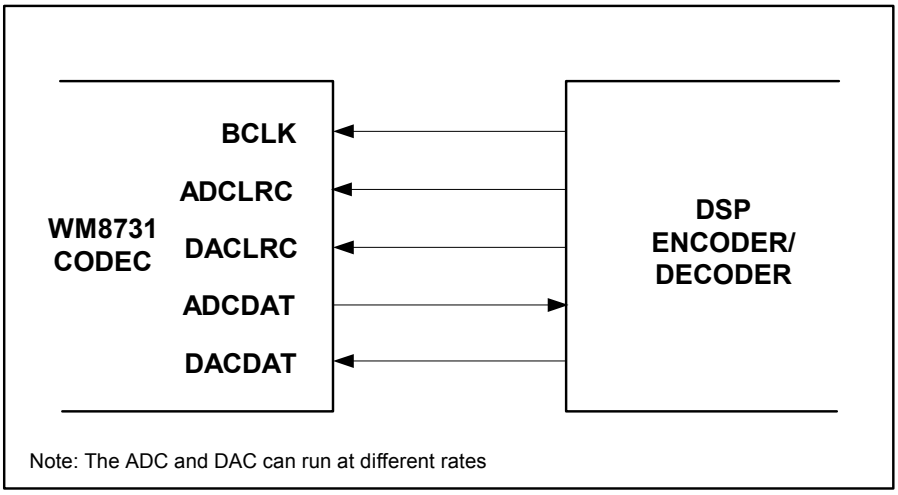


Figure 5 Slave Mode Connection

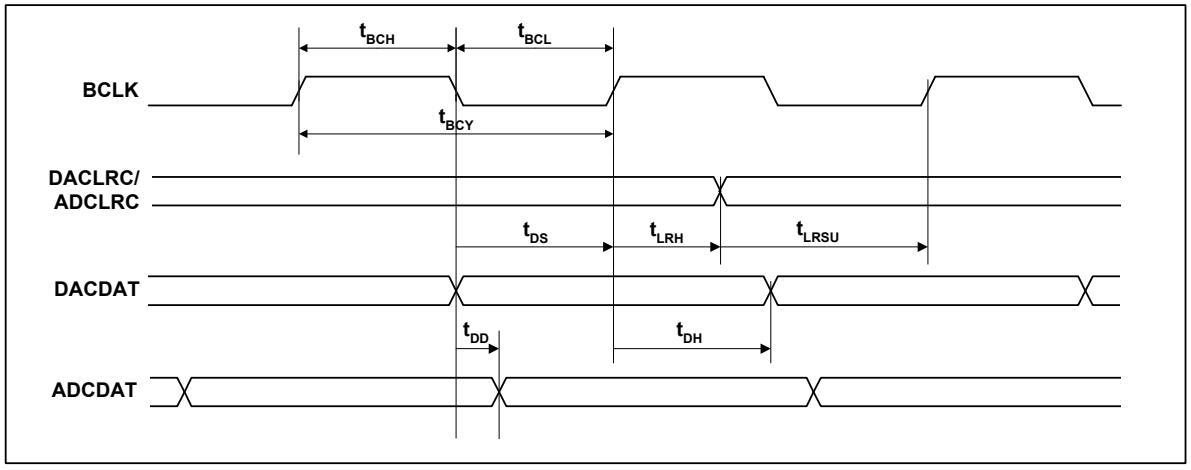


Figure 6 Digital Audio Data Timing – Slave Mode

Test Conditions

AVDD, HPVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCLK cycle time	t_{BCY}		50			ns
BCLK pulse width high	t_{BCH}		20			ns
BCLK pulse width low	t_{BCL}		20			ns
DACLRC/ADCLRC set-up time to BCLK rising edge	t_{LRSU}		10			ns
DACLRC/ADCLRC hold time from BCLK rising edge	t_{LRH}		10			ns
DACDAT set-up time to BCLK rising edge	t_{DS}		10			ns
DACDAT hold time from BCLK rising edge	t_{DH}		10			ns

Test Conditions

AVDD, HPVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADCDAT propagation delay from BCLK falling edge	t_{DD}		0		35	ns

MPU INTERFACE TIMING

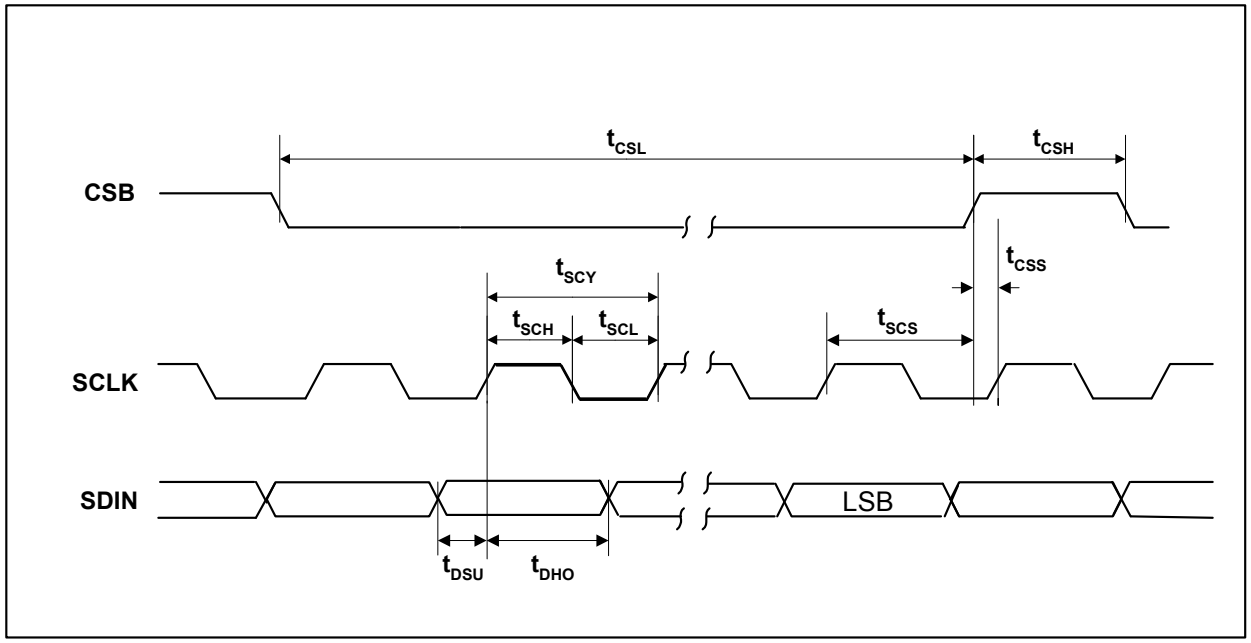


Figure 7 Program Register Input Timing - 3-Wire MPU Serial Control Mode

Test Conditions

AVDD, HPVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Register Input Information						
SCLK rising edge to CSB rising edge	t_{SCS}		60			ns
SCLK pulse cycle time	t_{SCY}		80			ns
SCLK pulse width low	t_{SCL}		20			ns
SCLK pulse width high	t_{SCH}		20			ns
SDIN to SCLK set-up time	t_{DSU}		20			ns
SCLK to SDIN hold time	t_{DHO}		20			ns
CSB pulse width low	t_{CSL}		20			ns
CSB pulse width high	t_{CSH}		20			ns
CSB rising to SCLK rising	t_{CSS}		20			ns

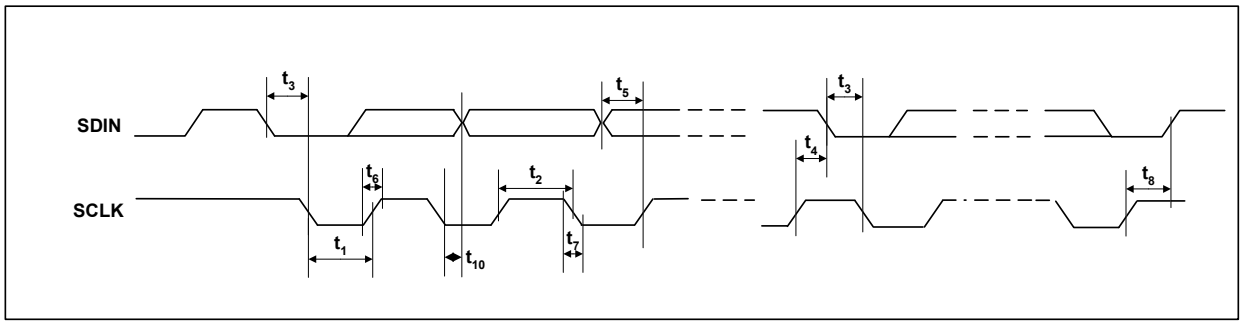


Figure 8 Program Register Input Timing – 2-Wire MPU Serial Control Mode

Test Conditions

AVDD, HPVDD, DBVDD = 3.3V, AGND = 0V, DCVDD = 1.5V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, XTI/MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Register Input Information						
SCLK Frequency			0		526	kHz
SCLK Low Pulsewidth	t_1		1.3			us
SCLK High Pulsewidth	t_2		600			ns
Hold Time (Start Condition)	t_3		600			ns
Setup Time (Start Condition)	t_4		600			ns
Data Setup Time	t_5		100			ns
SDIN, SCLK Rise Time	t_6				300	ns
SDIN, SCLK Fall Time	t_7				300	ns
Setup Time (Stop Condition)	t_8		600			ns
Data Hold Time	t_{10}				900	ns

DEVICE DESCRIPTION

INTRODUCTION

The WM8731/L is a low power audio CODEC designed specifically for portable audio products. It's features, performance and low power consumption make it ideal for portable MP3 players and portable mini-disc players.

The CODEC includes line and microphone inputs to the on-board ADC, line and headphone outputs from the on-board DAC, a crystal oscillator, configurable digital audio interface and a choice of 2 or 3 wire MPU control interface. It is fully compatible and an ideal partner for a range of industry standard microprocessors, controllers and DSPs.

The CODEC includes three low noise inputs - mono microphone and stereo line. Line inputs have +12dB to -34dB logarithmic volume level adjustments and mute. The Microphone input has -6dB to 34dB volume level adjustment. An electret microphone bias level is also available. All the required input filtering is contained within the device with no external components required.

The on-board stereo analogue to digital converter (ADC) is of a high quality using a multi-bit high-order oversampling architecture delivering optimum performance with low power consumption. The output from the ADC is available on the digital audio interface. The ADC includes an optional digital high pass filter to remove unwanted dc components from the audio signal.

The on-board digital to analogue converter (DAC) accepts digital audio from the digital audio interface. Digital filter de-emphasis at 32kHz, 44.1kHz and 48kHz can be applied to the digital data under software control. The DAC employs a high quality multi-bit high-order oversampling architecture to again deliver optimum performance with low power consumption.

The DAC outputs, Microphone (SIDETONE) and Line Inputs (BYPASS) are available both at line level and through a headphone amplifier capable of efficiently driving low impedance headphones. The headphone output volume is adjustable in the analogue domain over a range of +6dB to –73dB and can be muted.

The design of the WM8731/L has given much attention to power consumption without compromising performance. It includes the ability to power off selective parts of the circuitry under software control, thus conserving power. Nine separate power save modes be configured under software control including a standby and power off mode.

Special techniques allow the audio to be muted and the device safely placed into standby, sections of the device powered off and volume levels adjusted without any audible clicks, pops or zipper noises. Therefore standby and power off modes maybe used dynamically under software control, whenever recording or playing is not required.

The device caters for a number of different sampling rates including industry standard 8kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz and 96kHz. Additionally, the device has an ADC and DAC that can operate at different sample rates.

There are two unique schemes featured within the programmable sample rates of the WM8731/L: Normal industry standard 256/384fs sampling mode may be used, with the added ability to mix different sampling rates. Also a special USB mode is included, whereby all audio sampling rates can be generated from a 12.00MHZ USB clock. Thus, for example, the ADC can record to the DSP at 44.1kHz and be played back from the CODEC at 8kHz with no external digital signal processing required. The digital filters used at for both record and playback are optimised for each sampling rate used.

The digitised output is available in a number of audio data formats I^2S, DSP Mode (a burst mode in which frame sync plus 2 data packed words are transmitted), MSB-First, left justified and MSB-First, right justified. The digital audio interface can operate in both master or slave modes.

The software control uses either 2 or 3-wire MPU interface.

A crystal oscillator is included on board the device. The device can generate the system master clock or alternatively it can accept an external master clock from the audio system.

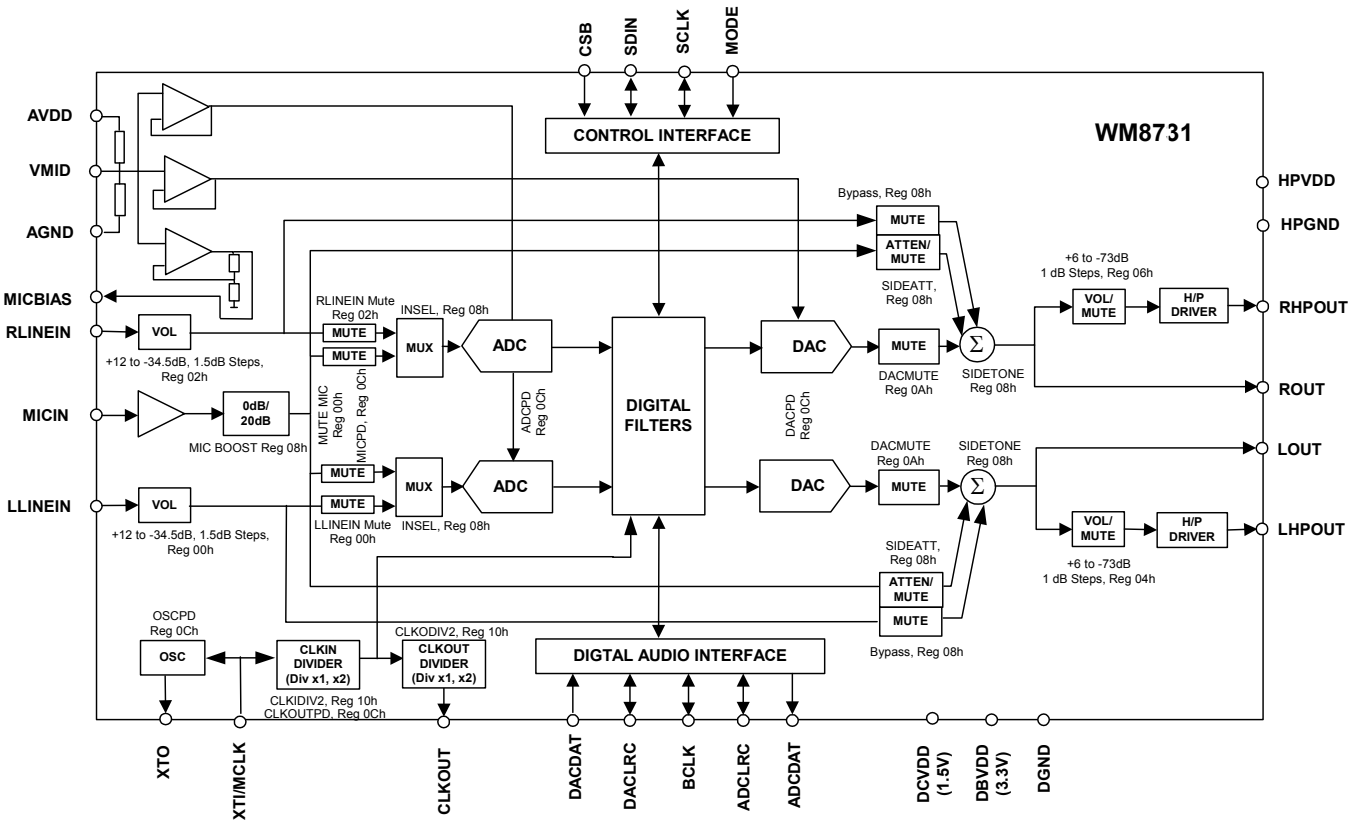


Figure 9 Functional Block Diagram

AUDIO SIGNAL PATH

LINE INPUTS

The WM8731/L provides Left and Right channel line inputs (RLINEIN and LLINEIN). The inputs are high impedance and low capacitance, thus ideally suited to receiving line level signals from external hi-fi or audio equipment.

Both line inputs include independent programmable volume level adjustments and ADC input mute. The scheme is illustrated in Figure 10. Passive RF and active Anti-Alias filters are also incorporated within the line inputs. These prevent high frequencies aliasing into the audio band or otherwise degrading performance.

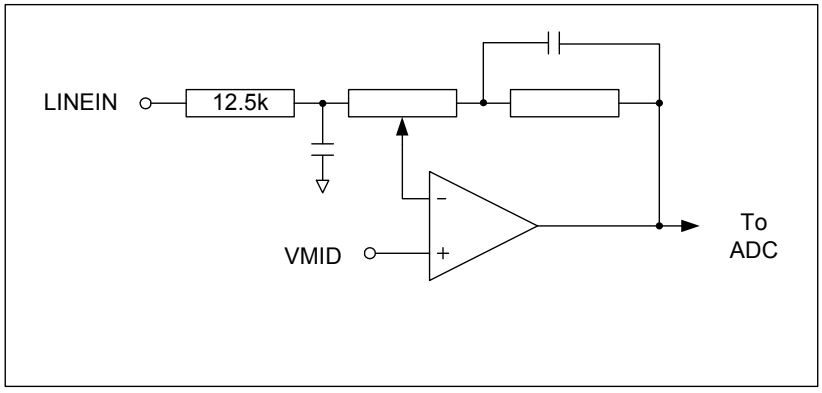


Figure 10 Line Input Schematic

The gain between the line inputs and the ADC is logarithmically adjustable from +12dB to –34.5dB in 1.5dB steps under software control. The ADC Full Scale input is 1.0V rms at AVDD = 3.3 volts. Any voltage greater than full scale will possibly overload the ADC and cause distortion. Note that the full scale input tracks directly with AVDD. The gain is independently adjustable on both Right and Left Line Inputs. However, by setting the INBOTH bit whilst programming the volume control, both channels are simultaneously updated with the same value. Use of INBOTH reduces the required number of software writes required. The line inputs to the ADC can be muted in the analogue domain under software control. The software control registers are shown Table 3. Note that the Line Input Mute only mutes the input to the ADC, this will still allow the Line Input signal to pass to the line output in Bypass Mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000000 Left Line In	4:0	LINVOL[4:0]	10111 (0dB)	Left Channel Line Input Volume Control 11111 = +12dB . . 1.5dB steps down to 00000 = -34.5dB
	7	LINMUTE	1	Left Channel Line Input Mute to ADC 1 = Enable Mute 0 = Disable Mute
	8	LRINBOTH	0	Left to Right Channel Line Input Volume and Mute Data Load Control 1 = Enable Simultaneous Load of LINVOL[4:0] and LINMUTE to RINVOL[4:0] and RINMUTE 0 = Disable Simultaneous Load
0000001 Right Line In	4:0	RINVOL[4:0]	10111 (0dB)	Right Channel Line Input Volume Control 11111 = +12dB . .1.5dB steps down to 00000 = -34.5dB
	7	RINMUTE	1	Right Channel Line Input Mute to ADC 1 = Enable Mute 0 = Disable Mute
	8	RLINBOTH	0	Right to Left Channel Line Input Volume and Mute Data Load Control 1 = Enable Simultaneous Load of RINVOL[4:0] and RINMUTE to LINVOL[4:0] and LINMUTE 0 = Disable Simultaneous Load

Table 3 Line Input Software Control

The line inputs are biased internally through the operational amplifier to VMID. Whenever the line inputs are muted or the device placed into standby mode, the line inputs are kept biased to VMID using special anti-thump circuitry. This reduces any audible clicks that may otherwise be heard when re-activating the inputs.

The external components required to complete the line input application is shown in the Figure 11.

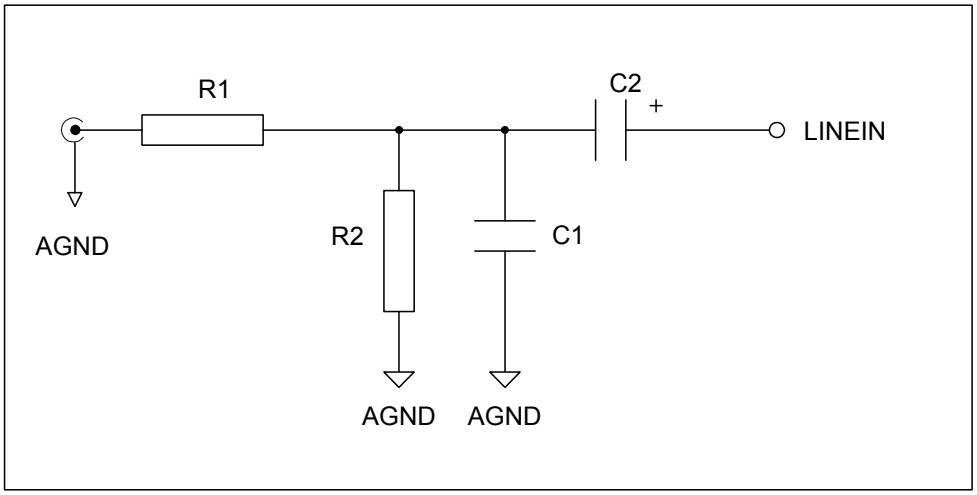


Figure 11 Line Input Application Drawing

For interfacing to a typical CD system, it is recommended that the input is scaled to ensure that there is no clipping of the signal. R1 = 5.6k, R2 = 5.6k, C1 = 220pF, C2 = 1μF.

R1 and R2 form a resistive divider to attenuate the 2 Vrms output from a CD player to a 1 Vrms level, so avoiding overloading the inputs. R2 also provides a discharge path for C2, thus preventing the input to C2 charging to an excessive voltage which may otherwise damage any equipment connected that is not suitably protected against high voltages. C1 forms an RF low pass filter for increasing the rejection of RF interference picked up on any cables. C2 forms a DC blocking capacitor to remove the DC path between the WM8731/L and the driving audio equipment. C2 together with the input impedance of the WM8731/L form a high pass filter.

MICROPHONE INPUT

MICIN is a high impedance, low capacitance input suitable for connection to a wide range of monophonic microphones of different dynamics and sensitivities.

The MICIN includes programmable volume adjustments and a mute function. The scheme is shown in Figure 12. Passive RF and active Anti-Alias filters are also incorporated within the microphone inputs. These allow a matched interface to the multi-bit oversampling ADC and preventing high frequencies aliasing into the audio band or otherwise degrading performance.

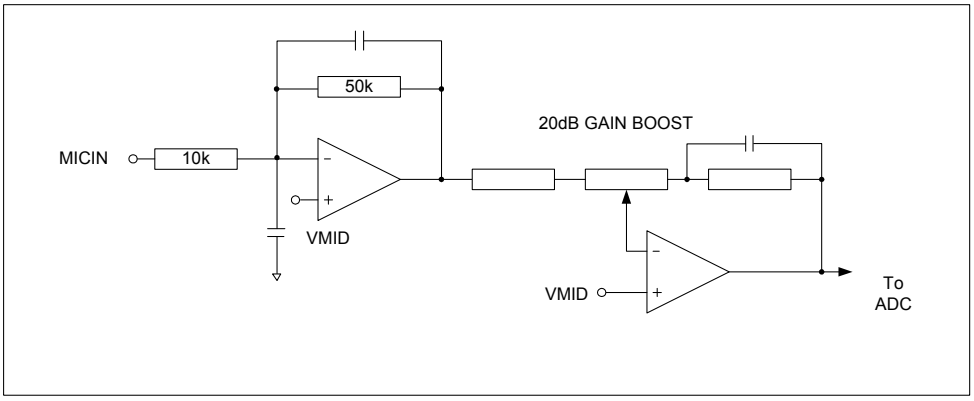


Figure 12 Microphone Input Schematic

There are 2 stages of gain made up of two low noise inverting operational amplifiers.

The 1st stage comprises a nominal gain of G1 = 50k/10k = 5. By adding an external resistor (Rmic) in series with MICIN the gain of stage can be adjusted. For example adding Rmic = 40K sets the gain of stage 1 to x1 (0dB). The equation below can be used to calculate the gain versus Rmic.

G1 = 50k/ (Rmic + 10k)

Or alternatively to calculate the value of Rmic to achieve a given gain, G1.

Rmic = (50k/G1) – 10k

The internal 50k and 10k resistors have a tolerance of 15%. For Rmicext = 90k G = 0.5 (-6dB) and for Rmicext = 0 G = x10 (14dB).

The 2nd stage comprises a 0dB gain stage that can be software configured to provide a fixed 20dB of gain for low sensitivity microphones.

The microphone input can therefore be configured with a variable gain of between -6dB and 14dB on the 1st stage, and an additional fixed 0dB or 20dB on the 2nd stage. This allows for all gains to the input signal in the range –6dB to 34dB to be catered for.

The ADC Full Scale input is 1.0V rms at AVDD = 3.3 volts. Any voltage greater than full scale will possibly overload the ADC and cause distortion. Note that the full scale input tracks directly with AVDD. Stage 1 and Stage 2 gains should be configured so that the ADC receives a maximum signal equal to its full scale for maximising the signal to noise.

The software control for the MICIN is shown in Table 4. Note that the Microphone Mute only mutes the input to the ADC, this will still allow the Microphone Input signal to pass to the line output in Sidetone Mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000100 Analogue Audio Path Control	0	MICBOOST	0	Microphone Input Level Boost 1 = Enable Boost 0 = Disable Boost
	1	MUTEMIC	1	Line Input Mute to ADC 1 = Enable Mute 0 = Disable Mute

Table 4 Microphone Input Software Control

The microphone input is biased internally through the operational amplifier to VMID. Whenever the line inputs are muted the MICIN input is kept biased to VMID using special anti-thump circuitry. This reduces any audible clicks that may otherwise be heard when re-activating the input.

The application drawing for the microphone is shown in Figure 13.

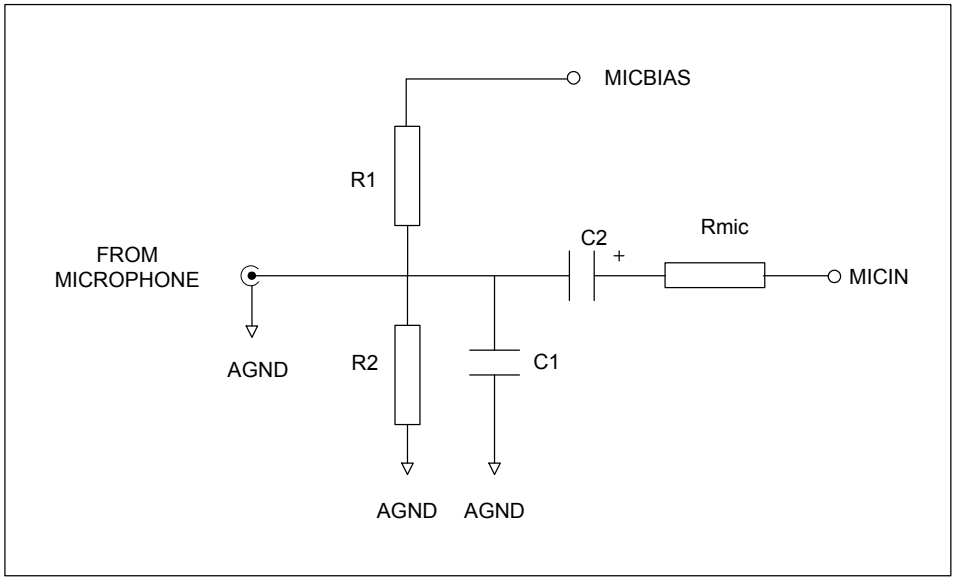


Figure 13 Microphone Input and Bias Application Drawing

Recommended component values are C1 = 220pF (npo ceramic), C2 = 1μF, R1 = 680 Ω, R2 = 47k. Rmic values depends on gain setting (see above).

R1 and R2 form part of the biasing network (refer to Microphone Bias section below). R1 connected to MICBIAS is necessary only for electret type microphones that require a voltage bias. R2 should always be present to prevent the microphone input from charging to a high voltage which may damage the microphone on connection. R1 and R2 should be large so as not to attenuate the signal from the microphone, which can have source impedance greater than 2k. C1 together with the source impedance of the microphone and the input impedance of MICIN forms an RF filter. C2 is a DC blocking capacitor to allow the microphone to be biased at a different DC voltage to the MICIN signal.

MICROPHONE BIAS

The MICBIAS output provides a low noise reference voltage suitable for biasing electret type microphones and the associated external resistor biasing network. Refer to the Microphone Input section for an application drawing and further description.

The scheme for MICBIAS is shown in Figure 14. Note that there is a maximum source current capability of 3mA available for the MICBIAS. This limits the smallest value of external biasing resistors that can safely be used.

Note that the MICBIAS output is not active in standby mode.

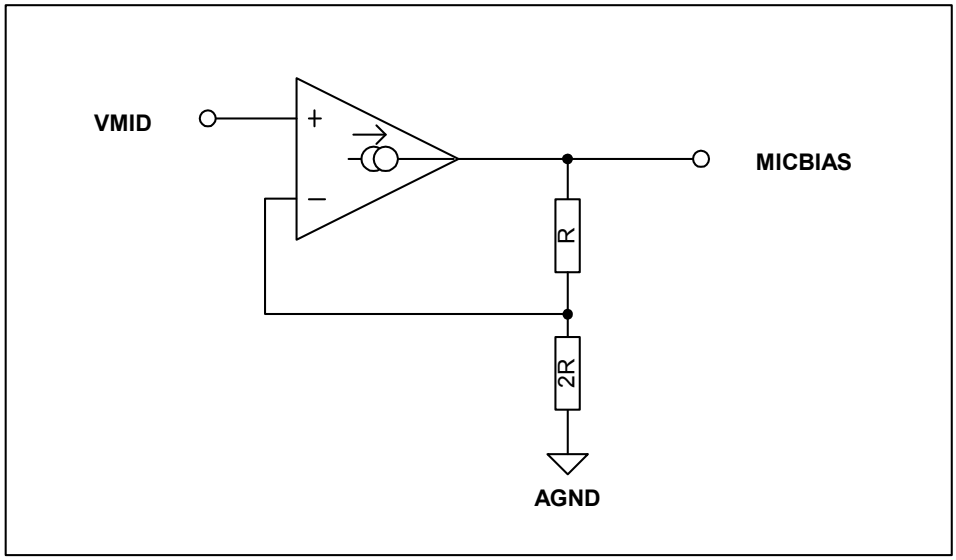


Figure 14 Microphone Bias Schematic

ADC

The WM8731/L uses a multi-bit oversampled sigma-delta ADC. A single channel of the ADC is illustrated in the Figure 15.

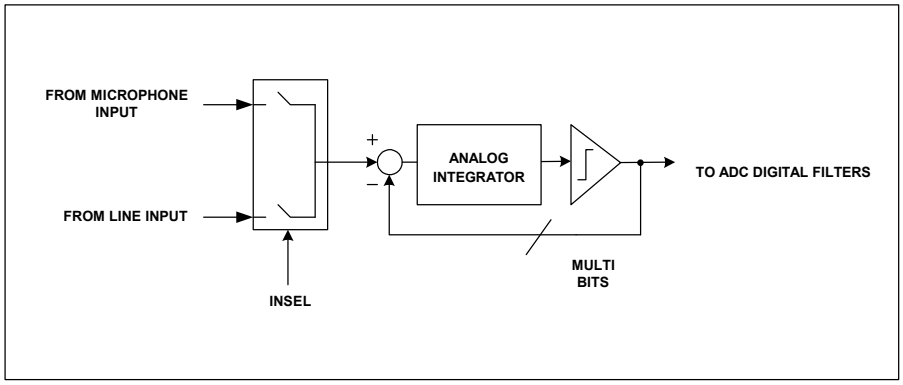


Figure 15 Multi-Bit Oversampling Sigma Delta ADC Schematic