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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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WM8741

24-bit 192kHz DAC with Advanced Digital Filtering

DESCRIPTION

The WM8741 is a very high performance stereo DAC designed for audio applications such as professional recording systems, A/V receivers and high specification CD, DVD and home theatre systems. The device supports PCM data input word lengths from 16 to 32-bits and sampling rates up to 192kHz. The WM8741 also supports DSD bit-stream data format, in both direct DSD and PCM-converted DSD modes.

The WM8741 includes fine resolution volume and soft mute control, digital de-emphasis and a range of advanced digital filter responses, followed by a digital interpolation filter, multi-bit sigma delta modulator and stereo DAC. Wolfson's patented architecture optimises the linearity of the DAC and provides maximum insensitivity to clock jitter.

The digital filters include several selectable roll-off and performance characteristics. The user can select between standard sharp or slow roll-off responses. In addition, the WM8741 includes a selection of advanced digital filter characteristics including non-half band filters and minimum phase filters.

This flexibility provides a range of benefits, such as significantly reduced pre-ringing and minimal group delay. The internal digital filters can also be by-passed and the WM8741 used with an external digital filter.

The WM8741 supports two connection schemes for audio DAC control. The 2/3 wire serial control interface provides access to all features. A range of features can also be accessed by hardware control interface.

The WM8741 is available in a convenient 28-SSOP package, and is pin compatible with the WM8740.

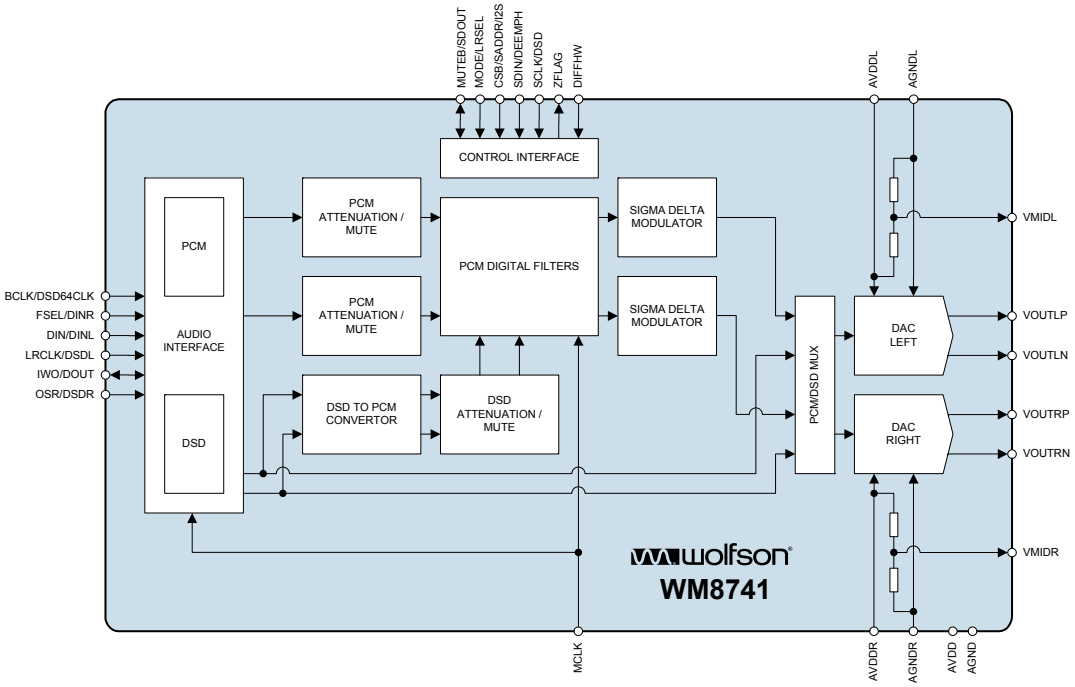
FEATURES

- Advanced Ultra High Performance Multi-bit Sigma-Delta Architecture
  - 128dB SNR ('A'-weighted mono @ 48kHz)
  - 125dB SNR ('A'-weighted stereo @ 48kHz)
  - 123dB SNR (non-weighted stereo @ 48kHz)
  - -100dB THD @ 48kHz
  - Differential analogue voltage outputs
  - High tolerance to clock jitter
- PCM Mode
  - Sampling frequency: 32kHz to 192kHz
  - Input data word length support: 16 to 32-bit
  - Supports all standard audio interface formats
  - Selectable advanced digital filter responses
    - Includes linear/minimum phase and range of tailored characteristics
    - Enables low pre-ringing, minimal latency
  - Optional interface to industry standard external filters
  - Digital volume control in 0.125dB steps with soft ramp and soft mute
  - Anti-clipping mode to prevent distortion even with input signals recorded up to 0dB
  - Selectable de-emphasis support
  - Zero Flag output
- DSD Mode
  - DSD bit-stream support for SACD applications
  - Support for normal or phase modulated bit-streams
  - Direct or PCM converted DSD paths (DSD Plus)
  - DSD mute
- Hardware or software control modes:
  - 2 and 3 wire serial control interface support
- Pin compatible with WM8740
- 4.5V to 5.5V analogue, 3.15V to 3.6V digital supply operation
- 28-lead SSOP Package

APPLICATIONS

- Professional audio systems
- CD, DVD, SACD audio
- Home theatre systems
- A/V receivers

BLOCK DIAGRAM



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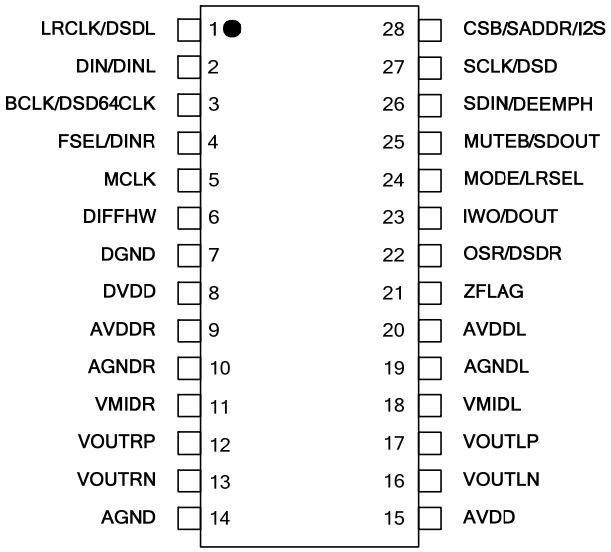
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8741GEDS/V	-0° to +70°C	28-lead SSOP (Pb-free)	MSL2	260˚C
WM8741GEDS/RV	-0° to +70°C	28-lead SSOP (Pb-free, tape and reel)	MSL2	260˚C

Note:

Reel Quantity = 2,000

PIN DESCRIPTION (SOFTWARE CONTROL MODE)

PIN	NAME	TYPE	DESCRIPTION		
			PCM MODE	8FS PCM MODE	DSD MODES
1	LRCLK / DSDL	Digital input	Audio interface left/right clock input	Audio interface left/right clock input	DSD left audio data in
2	DIN / DINL	Digital input	Audio interface data input	Audio interface left data input	Unused
3	BCLK / DSD64CLK	Digital input	Audio interface bit clock input	Audio interface bit clock input	64fs system clock input
4	FSEL / DINR	Digital input Tri-level	Unused	Audio interface right data input	Unused
5	MCLK	Digital input	Master clock input	Master clock input	Unused
6	DIFFHW	Digital input Internal pull-down	Differential mono mode selection 0 = normal operation 1 = differential mono mode	Differential mono mode selection 0 = normal operation 1 = differential mono mode	Differential mono mode selection 0 = normal operation 1 = differential mono mode
7	DGND	Supply	Digital ground	Digital ground	Digital ground
8	DVDD	Supply	Digital supply	Digital supply	Digital supply
9	AVDDR	Analogue Input	Right analogue positive reference	Right analogue positive reference	Right analogue positive reference
10	AGNDR	Analogue Input	Right analogue negative reference	Right analogue negative reference	Right analogue negative reference
11	VMIDR	Analogue Output	Right analogue midrail decoupling pin	Right analogue midrail decoupling pin	Right analogue midrail decoupling pin
12	VOUTRP	Analogue Output	Right DAC positive output	Right DAC positive output	Right DAC positive output
13	VOUTRN	Analogue Output	Right DAC negative output	Right DAC negative output	Right DAC negative output
14	AGND	Supply	Analogue ground	Analogue ground	Analogue ground
15	AVDD	Supply	Analogue supply	Analogue supply	Analogue supply
16	VOUTLN	Analogue Output	Left DAC negative output	Left DAC negative output	Left DAC negative output
17	VOUTLP	Analogue Output	Left DAC positive output	Left DAC positive output	Left DAC positive output
18	VMIDL	Analogue Output	Left analogue midrail decoupling pin	Left analogue midrail decoupling pin	Left analogue midrail decoupling pin
19	AGNDL	Analogue Input	Left analogue negative reference	Left analogue negative reference	Left analogue negative reference
20	AVDDL	Analogue Input	Left analogue positive reference	Left analogue positive reference	Left analogue positive reference
21	ZFLAG	Digital Output	Zero flag output	Zero flag output	Zero flag output
22	OSR/DSDR	Digital input Tri-level	Unused	Unused	DSD right audio data in
23	IWO / DOUT	Digital input/output	Buffered audio interface data output	Unused	Unused

PIN	NAME	TYPE	DESCRIPTION		
			PCM MODE	**8FS PCM MODE**	**DSD MODES**
24	MODE / LRSEL	Digital input, tri-level	When DIFFHW=0: 0 = hardware mode 1 = 3-wire software mode Z = 2-wire software mode When DIFFHW=1: 0 = left channel mono 1 = right channel mono	When DIFFHW=0: 0 = hardware mode 1 = 3-wire software mode Z = 2-wire software mode When DIFFHW=1: 0 = left channel mono 1 = right channel mono	When DIFFHW=0: 0 = hardware mode 1 = 3-wire software mode Z = 2-wire software mode When DIFFHW=1: 0 = left channel mono 1 = right channel mono
25	MUTEB / SDOUT	Digital input or output: Internal pull-up	Softmute Control 0 = mute active 1 = normal operation NOTE: In 3-wire mode only, this pin may be used as a buffered control interface data output	Softmute Control 0 = mute active 1 = normal operation	Softute Control 0 = mute active 1 = normal operation **Note:** In DSD Direct mode this is an analogue mute
26	SDIN / DEEMPH	Digital input Tri-level	Serial control interface data input	Serial control interface data input	Serial control interface data input
27	SCLK / DSD	Digital input	Serial control interface clock input	Serial control interface clock input	Serial control interface clock input
28	CSB / SADDR / I^2S	Digital input	3-wire mode: serial control interface latch 2-wire mode: device address select	3-wire mode: serial control interface latch 2-wire mode: device address select	3-wire mode: serial control interface latch 2-wire mode: device address select

Notes:

1. Undefined inputs should be connected to DVDD or DGND
2. Tri-level pins which require the 'Z' state to be selected should be left floating (open)

PIN DESCRIPTION (HARDWARE CONTROL MODE)

PIN	NAME	TYPE	DESCRIPTION	
			PCM MODE	DSD DIRECT MODE
1	LRCLK / DSDL	Digital input	Audio interface left/right clock input	DSD left audio data in
2	DIN / DINL	Digital input	Audio interface data input	Unused
3	BCLK / DSD64CLK	Digital input	Audio interface bit clock input	64fs system clock input
4	FSEL / DINR	Digital input Tri-level	Selects between one of three digital filters – see Table 50	Unused
5	MCLK	Digital input	Master clock input	Unused
6	DIFFHW	Digital input Internal pull-down	Differential mono mode selection 0 = normal operation 1 = differential mono mode	Differential mono mode selection 0 = normal operation 1 = differential mono mode
7	DGND	Supply	Digital ground	Digital ground
8	DVDD	Supply	Digital supply	Digital supply
9	AVDDR	Analogue Input	Right analogue positive reference	Right analogue positive reference
10	AGNDR	Analogue Input	Right analogue negative reference	Right analogue negative reference
11	VMIDR	Analogue Output	Right analogue midrail decoupling pin	Right analogue midrail decoupling pin
12	VOUTRP	Analogue Output	Right DAC positive output	Right DAC positive output
13	VOUTRN	Analogue Output	Right DAC negative output	Right DAC negative output
14	AGND	Supply	Analogue ground	Analogue ground
15	AVDD	Supply	Analogue supply	Analogue supply
16	VOUTLN	Analogue Output	Left DAC negative output	Left DAC negative output
17	VOUTLP	Analogue Output	Left DAC positive output	Left DAC positive output
18	VMIDL	Analogue Output	Left analogue midrail decoupling pin	Left analogue midrail decoupling pin
19	AGNDL	Analogue Input	Left analogue negative reference	Left analogue negative reference
20	AVDDL	Analogue Input	Left analogue positive reference	Left analogue positive reference
21	ZFLAG	Digital Output	Zero flag output	Unused
22	OSR/DSDR	Digital input Tri-level	Controls internal oversampling rate: 0 = low rate Z = medium rate 1 = high rate	DSD right audio data in
23	IWO / DOUT	Digital input/output	Controls audio interface wordlength – see Table 46	Unused

PIN	NAME	TYPE	DESCRIPTION	
			PCM MODE	DSD DIRECT MODE
24	MODE / LRSEL	Digital input, tri-level	When DIFFHW=0: 0 = hardware mode 1 = 3-wire software mode Z = 2-wire software mode When DIFFHW=1: 0 = left channel mono 1 = right channel mono	When DIFFHW=0: 0 = hardware mode 1 = 3-wire software mode Z = 2-wire software mode When DIFFHW=1: 0 = left channel mono 1 = right channel mono
25	MUTEB / SDOUT	Digital input or output: Internal pull-up	Softmute Control 0 = mute active 1 = normal operation	Analogue Mute Control 0 = mute active 1 = normal operation
26	SDIN / DEEMPH	Digital input Tri-level	De-emphasis Control 0 = normal operation 1 = de-emphasis applied Z = anti-clipping digital filter mode	Unused
27	SCLK / DSD	Digital input	HW Mode Select: 0 = PCM 1 = DSD Direct	HW Mode Select: 0 = PCM 1 = DSD Direct
28	CSB / SADDR / I^2S	Digital input	Controls audio interface format – see Table 46	Unused

Notes:

1. Undefined inputs should be connected to DVDD or DGND
2. Tri-level pins who require the 'Z' state to be selected should be left floating (open)

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson Microelectronics tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Digital supply voltage, DVDD	-0.3V	+4.5V
Analogue supply voltage, AVDD	-0.3V	+7V
Voltage range digital inputs	DGND - 0.3V	DVDD + 0.3V
Voltage range analogue inputs	AGND - 0.3V	AVDD + 0.3V
Master Clock Frequency		38.462MHz
Operating temperature range, T_A	-0°C	+70°C
Storage temperature	-65°C	+150°C
Ambient temperature (supplies applied)	-55°C	+125°C
Pb free package body temperature (soldering 10 seconds)		+260°C
Pb free package body temperature (soldering 2 minutes)		+183°C

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.

THERMAL PERFORMANCE

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal resistance – junction to case	θ_{JC}			23.9		°C/W
Thermal resistance – junction to ambient	θ_{JA}			67.1		°C/W

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		3.15	3.3	3.6	V
Analogue supply range	AVDD		4.5	5	5.5	V
Ground	AGND, DGND			0		V
Difference DGND to AGND			-0.3	0	+0.3	V
Analogue operating current	I_{AVDD}	AVDD = 5V		55		mA
Digital operating current	I_{DVDD}	DVDD = 3.3V		40		mA
Analogue standby current	$I_{AVDD\ (Standby)}$	AVDD = 5V Clocks stopped		45		mA
Digital standby current	$I_{DVDD\ (Standby)}$	DVDD = 3.3V Clocks stopped		1.5		mA

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS

AVDD = 5V, DVDD = 3.3V, AGND, DGND = 0V, T_A = +25°C, 1kHz test signal, fs = 48kHz, MCLK = 512fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels						
Input LOW level	V_{IL}				0.3 x DVDD	V
Input HIGH level	V_{IH}		0.7 x DVDD			V
Output LOW level	V_{OL}	I_{OL} = 2mA			0.1 x DVDD	V
Output HIGH level	V_{OH}	I_{OH} = 2mA	0.9 x DVDD			V
DSD Input Characteristics						
DSD reference level		DSD Direct or DSD Plus Mode		0 50		dB_{DSD} %
DAC Performance						
Signal to Noise Ratio (Note 1)	SNR	A-weighted mono @ fs = 48kHz		128		dB
		A-weighted stereo @ fs = 48kHz	120	125		dB
		A-weighted stereo @ fs = 96kHz		123		dB
		A-weighted stereo @ fs = 192kHz		120		dB
		Non-weighted stereo @ fs = 48kHz		122		dB
Dynamic Range (Note 2)	DNR	A=weighted, -60dB full scale input		125		dB
Total Harmonic Distortion (Note 2)	THD	Mono 0dB @ fs = 48kHz		-100		dB
		Stereo 0dB @ fs = 48kHz		-100		dB
		Stereo 0dB @ fs = 96kHz		-100		dB
		Stereo 0dB @ fs = 192kHz		-100		dB
Channel Separation		1kHz		130		dB
Channel Level Matching				0.1		dB
Channel Phase Deviation				0.01		Degree
Power Supply Rejection Ratio	PSRR	100mVpp at 1kHz		-80		dB
		20Hz to 20kHz 100mVpp		-67		dB

TEST CONDITIONS

AVDD = 5V, DVDD = 3.3V, AGND, DGND = 0V, T_A = +25°C, 1kHz test signal, fs = 48kHz, MCLK = 512fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal Analogue Filter						
Bandwidth		-3dB		474		kHz
Passband edge response		20kHz		-0.0077		dB
Analogue Output Levels						
PCM full scale differential output level		Into 10kΩ load, 0dBFS input		2		V_{RMS}
DSD Direct differential output level		Into 10kΩ load, $0dB_{DSD}$ input		0.948		V_{RMS}
DSD Plus differential output level		Into 10kΩ load, $0dB_{DSD}$ input		0.991		V_{RMS}
Minimum resistance load		To midrail or AC coupled		2		kΩ
Maximum capacitance load				1		nF
Output DC level				AVDD/2		V
Reference Levels						
Potential divider resistance		AVDD to VMIDL/VMIDR and VMIDL/VMIDR to AGND		10		kΩ
Voltage at VMIDL/VMIDR				AVDD/2		V

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted over a 20Hz to 20kHz bandwidth.
2. All performance measurements done with 20kHz low pass filter. Failure to use such a filter will result in higher THD and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.

MASTER CLOCK TIMING

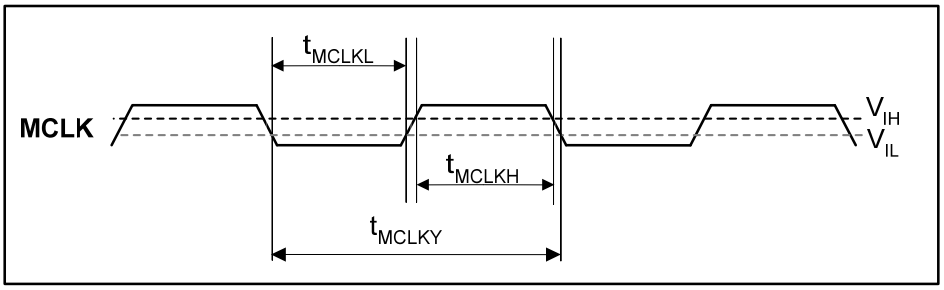


Figure 1 Master Clock Timing Requirements

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Master Clock Timing Information						
MCLK Master clock pulse width high	t_{MCLKH}		10			ns
MCLK Master clock pulse width low	t_{MCLKL}		10			ns
MCLK Master clock cycle time	t_{MCLKY}		27			ns
MCLK Duty cycle			40:60		60:40	

Table 1 MCLK Timing Requirements

PCM DIGITAL AUDIO INTERFACE TIMINGS

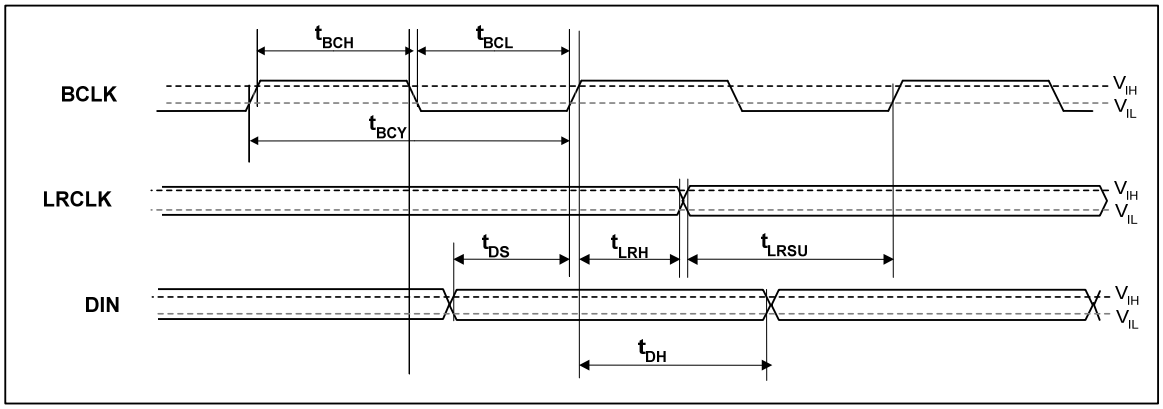


Figure 2 Digital Audio Data Timing

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCLK cycle time	t_{BCY}		40			ns
BCLK pulse width high	t_{BCH}		16			ns
BCLK pulse width low	t_{BCL}		16			ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}		8			ns
LRCLK hold time from BCLK rising edge	t_{LRH}		8			ns
DIN set-up time to BCLK rising edge	t_{DS}		8			ns
DIN hold time from BCLK rising edge	t_{DH}		8			ns

Table 2 Digital Audio Interface Timing Requirements

DSD AUDIO INTERFACE TIMINGS

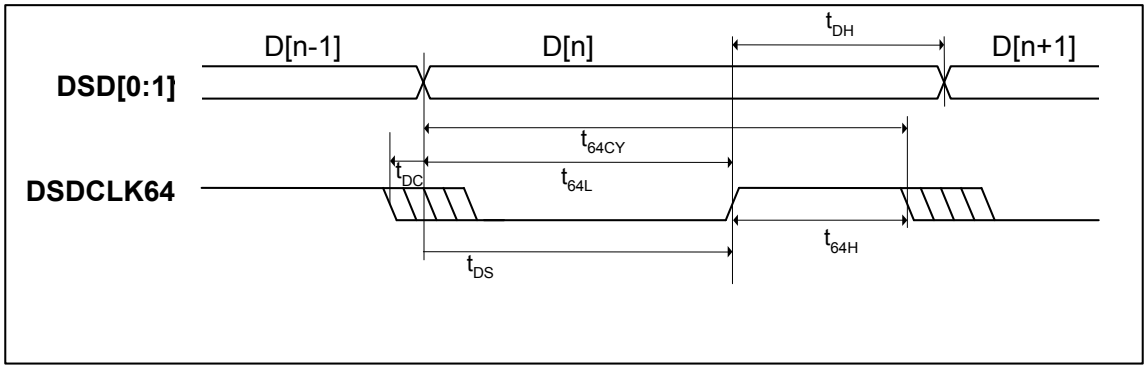


Figure 3 DSD Audio Timing - Normal Mode

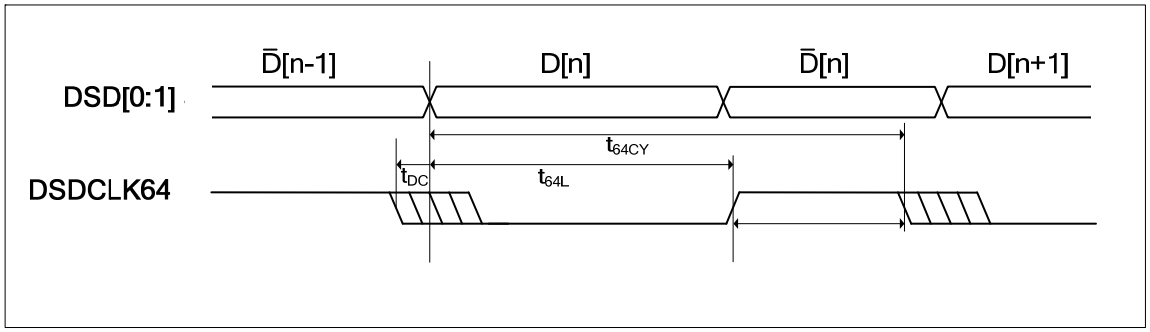


Figure 4 DSD Audio Timing - Phase Modulated Mode

Test Conditions

DVDD = 3.3V, GND = 0V, T_A = +25°C, fs = 44.1kHz, DSDCLK64 = 64fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
DSDCLK64 cycle time	t_{64CY}			354.3		ns
DSDCLK64 pulse width high	t_{64H}		140			ns
DSDCLK64 pulse width low	t_{64L}		140			ns
DSD[0:1] set-up time to DSDCLK64 rising edge	t_{DSN}		20			ns
DSD[0:1] hold time from DSDCLK64 rising edge	t_{DHN}		20			ns
Difference in edge timing of DSD[0:1] to DSDCLK64	t_{DC}		-10		10	ns

Table 3 DSD Audio Interface Timing Requirements

CONTROL INTERFACE TIMING – 3-WIRE MODE

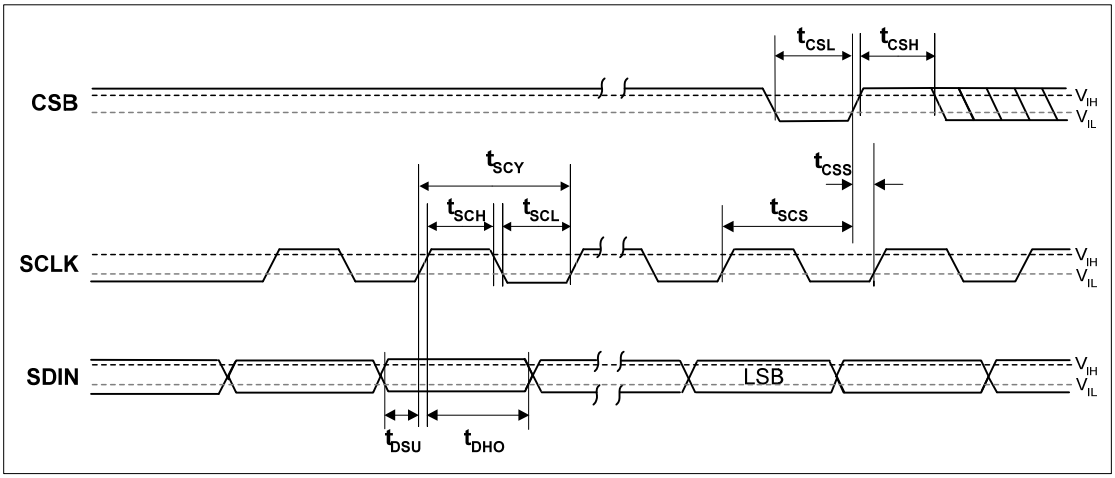


Figure 5 Control Interface Timing - 3-Wire Serial Control Mode

Test Conditions

DVDD = 3.3V, GND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCLK rising edge to LATCH rising edge	t_{SCS}		40			ns
SCLK pulse cycle time	t_{SCY}		80			ns
SCLK pulse width low	t_{SCL}		32			ns
SCLK pulse width high	t_{SCH}		32			ns
SDIN to SCLK set-up time	t_{DSU}		20			ns
SCLK to SDIN hold time	t_{DHO}		20			ns
LATCH pulse width low	t_{CSL}		20			ns
LATCH pulse width high	t_{CSH}		20			ns
LATCH rising to SCLK rising	t_{CSS}		20			ns

Table 4 Control Interface Timing – 3-Wire Serial Control Mode

CONTROL INTERFACE TIMING – 2-WIRE MODE

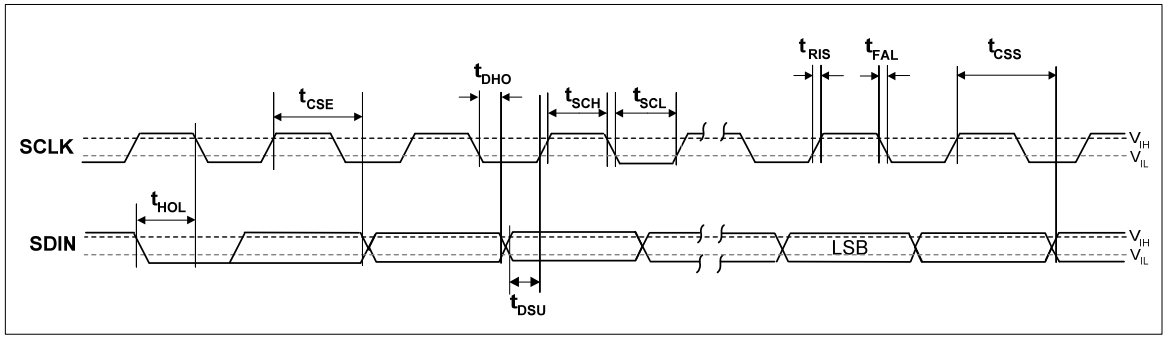


Figure 6 Control Interface Timing - 2-Wire Serial Control Mode

Test Conditions

DVDD = 3.3V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SCLK Frequency		0		5	MHz
SCLK Low Pulse-Width	t_{SCL}	80			ns
SCLK High Pulse-Width	t_{SCH}	80			us
Hold Time (Start Condition)	t_{HOL}	600			ns
Setup Time (Start Condition)	t_{CSE}	600			ns
Data Setup Time	t_{DSU}	100			ns
SDIN, SCLK Rise Time	t_{RIS}			300	ns
SDIN, SCLK Fall Time	t_{FAL}			300	ns
Setup Time (Stop Condition)	t_{CSS}	600			ns
Data Hold Time	t_{DHO}			900	ns
Max Pulse width of spikes that will be suppressed	t_{PS}	4		6	ns

Table 5 Control Interface Timing – 2-wire Serial Control Mode

INTERNAL POWER ON RESET CIRCUIT

The WM8741 includes two internal Power On Reset (POR) circuits which are used to reset the digital logic into a default state after power up and to allow the analogue circuits to power-up silently.

The digital POR circuit is powered from DVDD. This circuit monitors DVDD and asserts the internal digital reset if DVDD are below the minimum DVDD threshold which will allow the digital logic to function.

The analogue POR circuit is powered from AVDD. The circuit monitors AVDD, tri-stating the DAC outputs and isolating the internal reference resistor strings from AVDDL and AVDDR until there is sufficient AVDD voltage to allow the analogue DAC stages to function correctly.

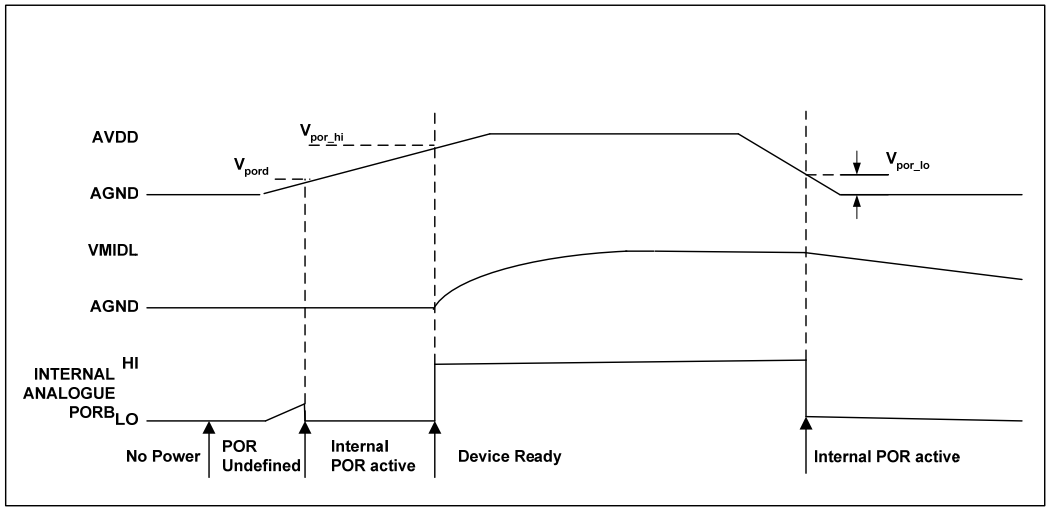


Figure 7 AVDD Power up Sequence

Test Conditions

AVDD = 5V, AGND = 0V, T_A = +25°C, T_{A_max} = +125°C, T_{A_min} = -25°C, $AVDD_{max}$ = 5.5V, $AVDD_{min}$ = 4.5V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Input Timing Information						
AVDD level to POR rising edge (AVDD rising)	V_{por_hi}	Measured from AGND		2.00		V
AVDD level to POR falling edge (AVDD falling)	V_{por_lo}	Measured from AGND		1.84		V

Table 6 Analogue POR Timing

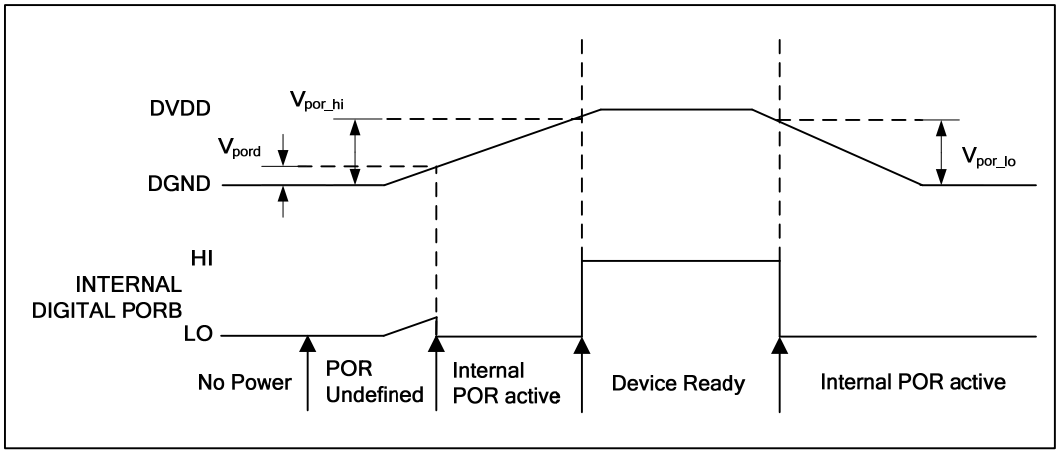


Figure 8 DVDD Power up Sequence

Test Conditions

DVDD = 3.3V, DGND = 0V, T_A = +25°C, T_{A_max} = +125°C, T_{A_min} = -25°C, $DVDD_{max}$ = 3.6V, $DVDD_{min}$ = 3.0V

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Input Timing Information						
DVDD level to POR rising edge (DVDD rising)	V_{por_hi}	Measured from DGND		1.86		V
DVDD level to POR falling edge (DVDD falling)	V_{por_lo}	Measured from DGND		1.83		V

Table 7 Digital POR Timing

In a real application the designer is unlikely to have control of the relative power up sequence of AVDD and DVDD. The POR circuit ensures a reasonable delay between applying power to the device and Device Ready.

Figure 7 and Figure 8 show typical power up scenarios in a real system. DVDD must be established before the device can be written to. Any writes to the device before device ready will be ignored.

Note: DVDD must be established before the MCLK is started. This will ensure all synchronisation circuitry within the device is fully initialised and ready.

AVDD must be established before the device will output any signal. Whilst the device will output signal as soon as the Internal Analogue PORB indicates device ready, normal operation is not possible until the VMID pin has reached the midrail voltage.

DEVICE DESCRIPTION

INTRODUCTION

The WM8741 is an ultra high performance DAC designed for digital audio applications. Its range of features makes it ideally suited for use in professional recording environments, CD/DVD players, AV receivers and other high-end consumer audio equipment.

The WM8741 is a complete differential stereo audio digital-to-analogue converter. The system includes a dithered digital interpolation filter, fine resolution volume control and digital de-emphasis, followed by a multi-bit sigma delta modulator and switched capacitor multi-bit stage with differential voltage outputs. The device supports both PCM and DSD digital audio input formats.

The WM8741 includes a configurable digital audio interface support for a 3-wire and 2-wire serial control interface, and a hardware control interface. The software control interface may be asynchronous to the audio data interface; in which case control data will be re-synchronised to the audio processing internally. It is fully compatible with, and an ideal partner for, a range of industry standard microprocessors, controllers and DSPs.

Uniquely, the WM8741 has a large range of high performance low latency advanced digital filters. The full range of filters is selectable in software mode, and a limited range of filters are available under hardware control. The filters allow users the flexibility to choose characteristics to match their group delay, phase and latency requirements.

Operation using a master clock of 128fs, 192fs, 256fs, 384fs, 512fs or 768fs is supported. Sample rates (fs) from 32kHz to 192kHz are allowed, provided the appropriate master clock is input (see Table 11 for details).

In normal PCM mode, the audio data interface supports right justified, left justified and I^2S interface formats along with a highly flexible DSP serial port interface.

There are two DSD modes. In DSD Direct mode, the datastream is subjected to the minimum possible processing steps between input and output. In DSD Plus mode, the datastream is converted to PCM and filtered to allow reduction of out of band components. This step also provides additional benefits in allowing access to other PCM features such as volume control and advanced digital filtering.

The device is packaged in a small 28-lead SSOP.

CLOCKING SCHEMES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. The external master system clock can be applied directly through the MCLK input pin with no software configuration necessary for sample rate selection.

MCLK is used to derive clocks for the DAC path in PCM mode. The DAC path consists of DAC sampling clock, DAC digital filter clock and DAC digital audio interface timing. In a system where there are a number of possible sources for the reference clock it is recommended that the clock source with the lowest jitter be used to optimise the performance of the DAC.

CONTROL INTERFACE

The WM8741 supports 2-wire and 3-wire serial control, and hardware control. Selection of control mode is made by controlling the state of the MODE pin.

PIN	NAME	DESCRIPTION
24	MODE/ LRSEL	0 = Hardware control mode 1 = 3-wire serial control mode Z = 2-wire serial control mode

Table 8 Control Mode Configuration

SOFTWARE CONTROL INTERFACE

The software control interface may be operated using a 2-wire or 3-wire (SPI-compatible) serial interface. When operating under serial control, hardware configuration pins are ignored.

Note: DIFFHW will override all other pins, forcing the device into hardware control mode and differential mono mode.

3-WIRE (SPI COMPATIBLE) SERIAL CONTROL MODE

Every rising edge of SCLK clocks in one bit of data on SDIN. A rising edge on CSB latches a complete control word consisting of 16 bits. The 3-wire interface protocol is shown in Figure 9.

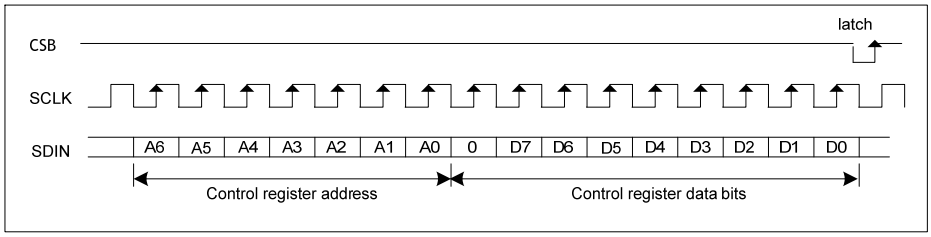


Figure 9 3-wire Serial Interface Protocol

Notes:

1. A[6:0] are Control Address Bits
2. D[7:0] are Control Data Bits
3. D[8] is always set to zero

3-WIRE CONTROL INTERFACE DAISY CHAINING

In daisy chaining mode, SDOUT (pin 25) outputs control data sampled on SDIN with a delay of 16 SCLK cycles. This data signal can be used to control another WM8741 in a daisy chain circuit as shown in Figure 10.

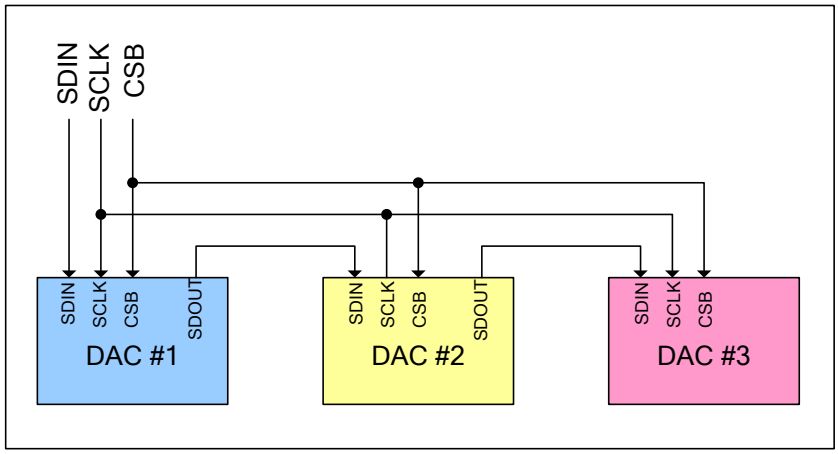


Figure 10 Control Interface Daisy Chaining Setup

To configure devices into daisy chain mode the CSB signal should be driven low while there is a register write to set register bit SDOUT=1. CSB should then be driven high, this sets the first device in daisy chain mode. CSB should then be driven low again while register bit SDOUT is set high. Setting CSB high again will cause the first register write to be output to the second device from the SDOUT pin, this sets the second device into daisy chain mode. This method must be repeated for the number of devices in the chain until they are all set into daisy chain mode. Figure 11 shows the protocol for configuring the first two devices in the daisy chain.

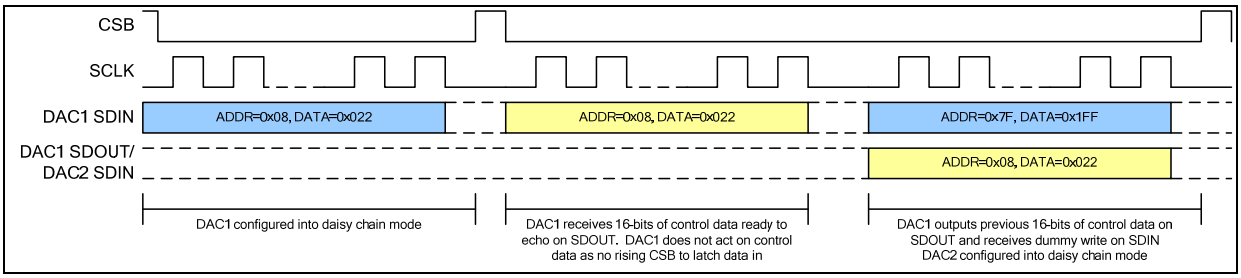


Figure 11 Initial Setup of Two WM8741 Devices into Control Interface Daisy Chain Mode

To write to a single device in the chain a complete sequence needs to be written to all the devices. Devices that do not require a register change must also be written to. The user can choose to write either the same data as the previous write, or write all 1s for the register address and data. All 1s will result in writing to a non-existent register, address 7Fh, preserving the current register settings. Figure 12 shows an example of how to access three WM8741 devices (the devices have all previously been configured in daisy chain mode):

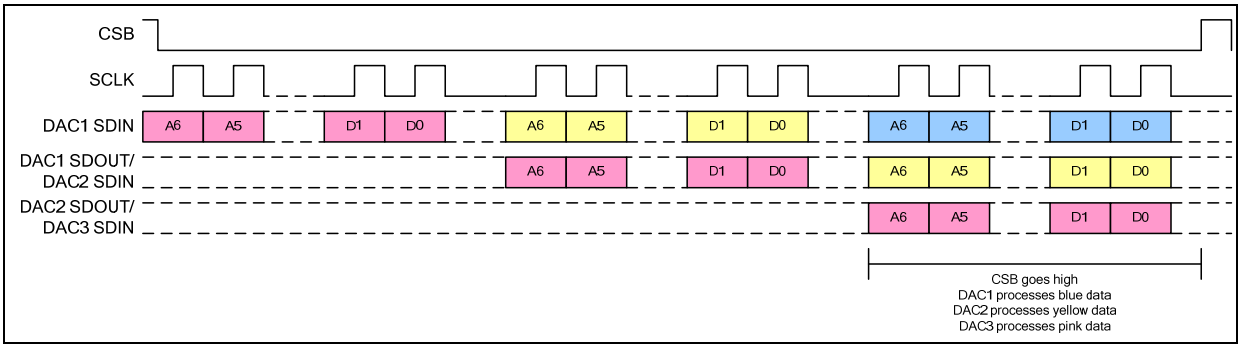


Figure 12 Daisy Chain Control Interface Example for Three WM8741 Devices

To ensure that only valid data is written to the devices in daisy chain mode, a pull up resistor is used in SDOUT. When connected to the SDIN pin of the next device in the chain, this results in all ones being written to the control interface of that device until the correct daisy chain data is written and latched.

Serial daisy chaining is available only when using 3-wire serial control mode. It is not available in 2-wire serial control mode or hardware control mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 Mode Control 2 08h	5	SDOUT	0	3 wire Serial Interface Daisy Chaining 0 = No Output 1 = Output on pin 25.

Table 9 Control Interface Daisy Chaining Selection

2-WIRE SERIAL CONTROL MODE

The WM8741 supports software control via a 2-wire serial bus. Many devices can be controlled by the same bus, and each device has a unique 7-bit address (this is not the same as the 7-bit address of each register in the WM8741).

The WM8741 operates as a slave device on the 2-wire control bus. The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the WM8741 and the R/W bit is '0', indicating a write, then the WM8741 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised or the R/W bit is '1', the WM8741 returns to the idle condition and wait for a new start condition and valid address.

Once the WM8741 has acknowledged a correct address, the controller sends the first byte of control data (B15 to B8, i.e. the WM8741 register address plus the first bit of register data). The WM8741 then acknowledges the first data byte by pulling SDIN low for one clock pulse. The controller then sends the second byte of control data (B7 to B0, i.e. the remaining 8 bits of register data), and the WM8741 acknowledges again by pulling SDIN low.

The transfer of data is complete when there is a low to high transition on SDIN while SCLK is high. After receiving a complete address and data sequence the WM8741 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the device reverts to the idle condition.

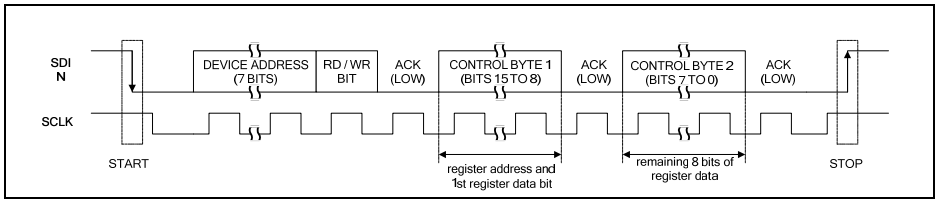


Figure 13 2-wire Serial Control Interface

The WM8741 device address can be configured between two options. This is selected by the SADDR pin.

PIN	NAME	DESCRIPTION
28	CSB/ SADDR/I^{2}S	0 = 2-wire address 0011010 1 = 2-wire address 0011011

Table 10 2-wire Serial Control Mode Address Selection

DIGITAL AUDIO INTERFACE

PCM MODE

There are a number of valid PCM data input modes. Two channel and one channel differential mono modes can be selected by serial or hardware control. It is also possible to bypass the WM8741 digital filters and apply a signal at a rate 8fs (where fs is the sampling rate) directly to the switched capacitor stage..

PCM DIGITAL AUDIO INTERFACE

Audio data is applied to the DAC system via the Digital Audio Interface. Five popular interface formats are supported:

- Left Justified mode
- Right Justified mode
- I^2S mode
- DSP mode A
- DSP mode B

All five formats require the MSB to be transmitted first, and support word lengths of 16, 20, 24 and 32 bits, with the exception that 32 bit data is not supported in right justified mode. DIN and LRCLK may be configured to be sampled on the rising or falling edge of BCLK by adjusting register bits LRP and BCP.

In left justified, right justified and I^2S audio interface modes, the digital audio interface receives data on the DIN input pin. Stereo audio data is time multiplexed on DIN, with LRCLK indicating whether the left or right channel is present. LRCLK is also used as a timing reference to indicate the beginning or end of the data words.

The minimum number of BCLK periods per LRCLK period is two times the selected word length. LRCLK must be high for a period equal to the minimum number of BCLK periods, and low for a minimum of the same period. Any mark-to-space ratio on LRCLK is acceptable provided the above requirements are met.

The WM8741 will automatically detect when data with a LRCLK period of exactly 32 BCLKs is received, and select 16-bit mode. This overrides any previously programmed word length. The operating word length will revert to a programmed value only if a LRCLK period other than 32 BCLKs is detected.

In DSP mode A or DSP mode B, the data is time multiplexed onto DIN. LRCLK is used as a frame sync signal to identify the MSB of the first word. The minimum number of BCLKs per LRCLK period is two times the selected word length. Any mark to space ratio is acceptable on LRCLK provided the rising edge is correctly positioned.

LEFT JUSTIFIED MODE

In left justified mode, the MSB is sampled on the first rising edge of BCLK following a LRCLK transition. LRCLK is high during the left data word and low during the right data word.

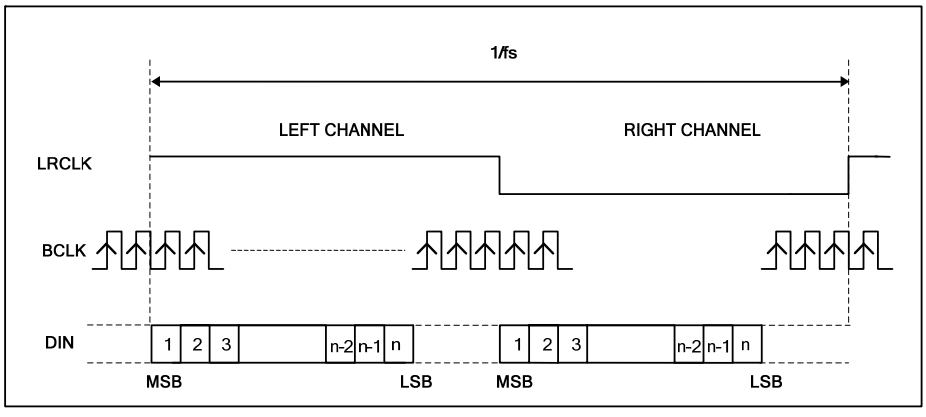


Figure 14 Left Justified Mode Timing Diagram

RIGHT JUSTIFIED MODE

In right justified mode, the LSB is sampled on the rising edge of BCLK preceding a LRCLK transition. LRCLK is high during the left data word and low during the right data word.

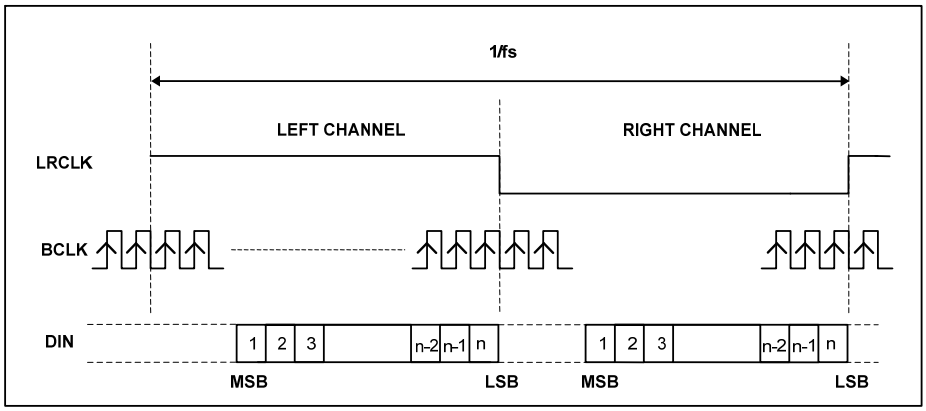


Figure 15 Right Justified Mode Timing Diagram

I²S MODE

In I²S mode, the MSB is sampled on the second rising edge of BCLK following a LRCLK transition. LRCLK is low during the left data word and high during the right data word.

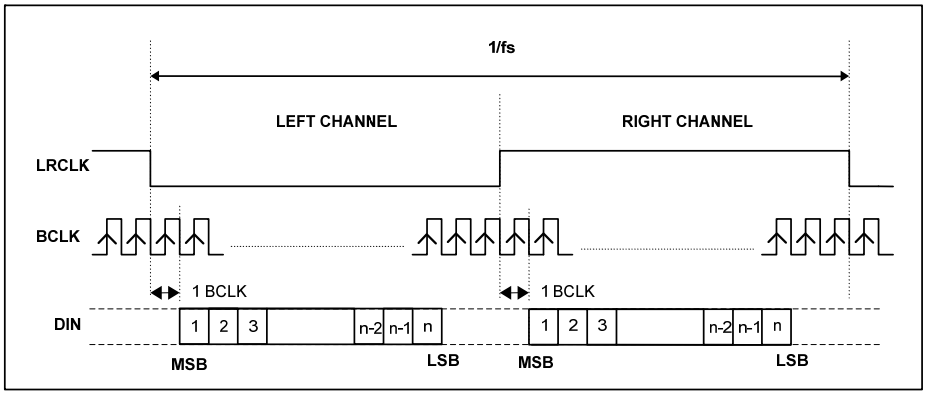


Figure 16 I²S Mode Timing Diagram

DSP MODE A

In DSP mode A, the first bit is sampled on the BCLK rising edge following the one that detects a low to high transition on LRCLK. No BCLK edges are allowed between the data words. The word order is DIN left, DIN right.

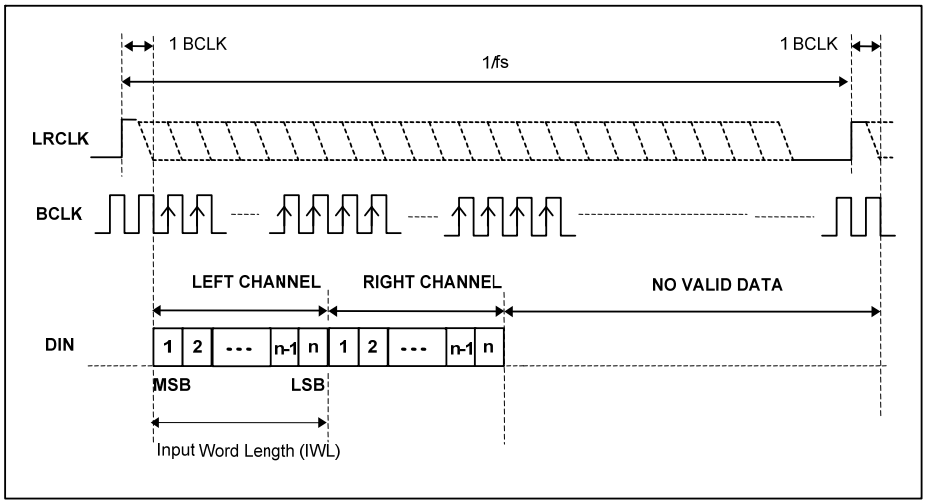


Figure 17 DSP Mode A Timing Diagram

DSP MODE B

In DSP mode B, the first bit is sampled on the BCLK rising edge, which detects a low to high transition on LRCLK. No BCLK edges are allowed between the data words. The word order is DIN left, DIN right.

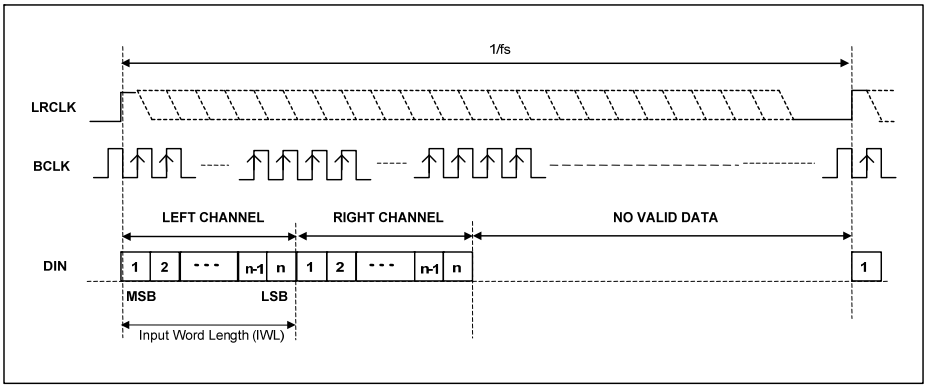


Figure 18 DSP Mode B Timing Diagram

PCM MODE SAMPLING RATES

The WM8741 supports master clock rates of 128fs to 768fs, where fs is the audio sampling frequency (LRCLK), typically 32kHz, 44.1kHz, 48kHz, 88.2kHz, 96kHz, 176.4kHz or 192kHz.

The WM8741 has a master clock detection circuit that automatically determines the relationship between the master clock frequency and the sampling rate. The master clock should be synchronised with LRCLK, although the WM8741 is tolerant of phase differences or jitter on this clock.

SAMPLING RATE (LRCLK)	MASTER CLOCK (MCLK) FREQUENCY (MHZ)					
	128fs	192fs	256fs	384fs	512fs	768fs
32kHz	Unavailable	Unavailable	8.192	12.288	16.384	24.576
44.1kHz	Unavailable	Unavailable	11.2896	16.9344	22.5792	33.8688
48kHz	Unavailable	Unavailable	12.288	18.432	24.576	36.864
88.2kHz	11.2896	16.9344	22.5792	33.8688	Unavailable	Unavailable
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable
176.4kHz	22.5792	33.8688	Unavailable	Unavailable	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable

Table 11 Typical Relationships between Master Clock Frequency and Sampling Rate in Normal PCM Mode

8FS MODE

Operation in 8FS mode requires that audio data for left and right channels is input separately on two pins. DINR (pin 4) is the input for right channel data and DINL (pin 2) is the input for left channel data. Hardware control of the device is not available.

The data can be input in two formats (left or right justified), selectable by register FMT[1:0], and two word lengths (20 or 24 bit), selectable by register IWL[1:0]. In both modes the data is clocked into the WM8741 MSB first.

For left justified data the word start is identified by the falling edge of LRCLK. The data is clocked in on the next 20/24 BCLK rising edges. This format is compatible with industry-standard DSPs and decoders such as the PMD100.

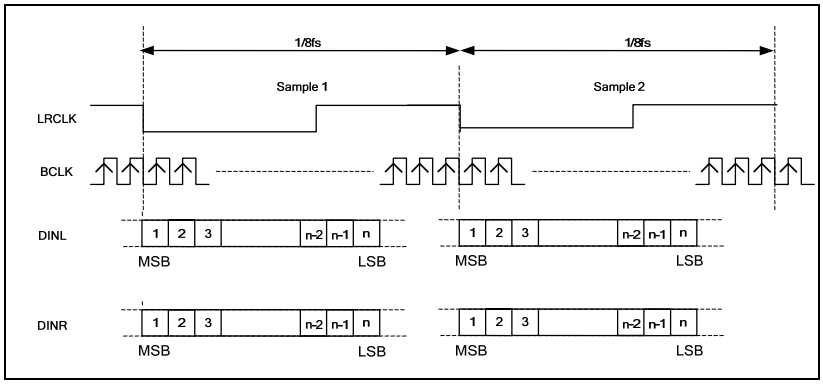


Figure 19 8FS Mode Left Justified Timing Requirements

For right justified mode, the data is justified to the rising edge of LRCLK and the data is clocked in on the preceding 20/24 BCLK rising edges before the LRCLK rising edge. This format is compatible with industry standard DSPs and decoders such as the DF1704 or SM5842.

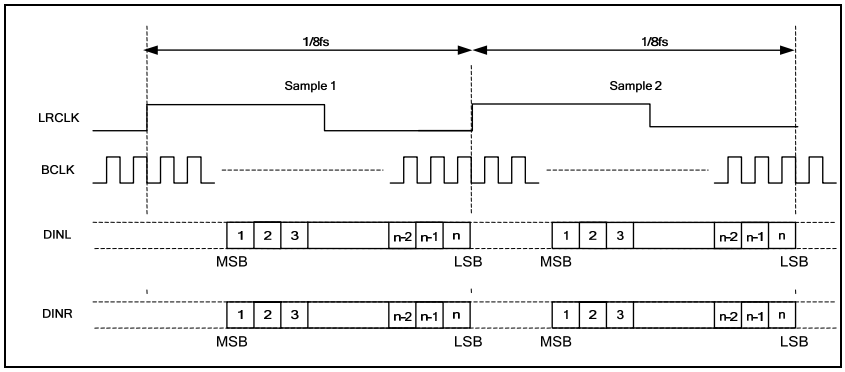


Figure 20 8FS Mode Right Justified Timing Requirements