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WM8750L

Stereo CODEC for Portable Audio Applications

DESCRIPTION

The WM8750L is a low power, high quality stereo CODEC designed for portable digital audio applications.

The device integrates complete interfaces to stereo or mono microphones and a stereo headphone. External component requirements are drastically reduced as no separate microphone or headphone amplifiers are required. Advanced on-chip digital signal processing performs graphic equaliser, 3-D sound enhancement and automatic level control for the microphone or line input.

The WM8750L can operate as a master or a slave, with various master clock frequencies including 12 or 24MHz for USB devices, or standard 256fs rates like 12.288MHz and 24.576MHz. Different audio sample rates such as 96kHz, 48kHz, 44.1kHz are generated directly from the master clock without the need for an external PLL.

The WM8750L operates at supply voltages down to 1.8V, although the digital core can operate at voltages down to 1.42V to save power, and the maximum for all supplies is 3.6 Volts. Different sections of the chip can also be powered down under software control.

The WM8750L is supplied in a very small and thin 5x5mm QFN package, ideal for use in hand-held and portable systems.

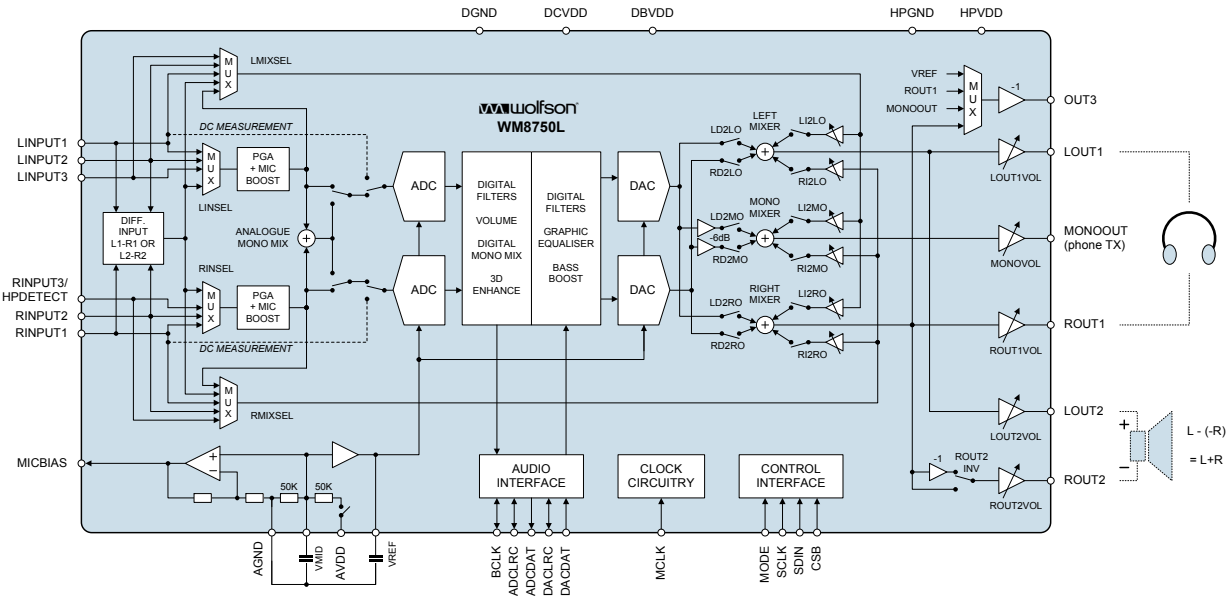
FEATURES

- DAC SNR 98dB ('A' weighted), THD -84dB at 48kHz, 3.3V
- ADC SNR 95dB ('A' weighted), THD -82dB at 48kHz, 3.3V
- Complete Stereo / Mono Microphone Interface
  - Programmable ALC / Noise Gate
- On-chip 400mW BTL Speaker Driver (mono)
- On-chip Headphone Driver
  - >40mW output power on 16Ω / 3.3V
  - THD –80dB at 20mW, SNR 90dB with 16Ω load
  - No DC blocking capacitors required (capless mode)
- Separately mixed mono output
- Digital Graphic Equaliser
- Low Power
  - 7mW stereo playback (1.8V / 1.5V supplies)
  - 14mW record & playback (1.8V / 1.5V supplies)
- Low Supply Voltages
  - Analogue 1.8V to 3.6V
  - Digital core: 1.42V to 3.6V
  - Digital I/O: 1.8V to 3.6V
- 256fs / 384fs or USB master clock rates: 12MHz, 24MHz
- Audio sample rates: 8, 11.025, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96kHz generated internally from master clock
- 5x5x0.9mm QFN package

APPLICATIONS

- MP3 Player / Recorder
- AAC/WMA/Multi-Format Player / Recorder
- Minidisc Player / Recorder
- Portable Digital Music Systems

BLOCK DIAGRAM



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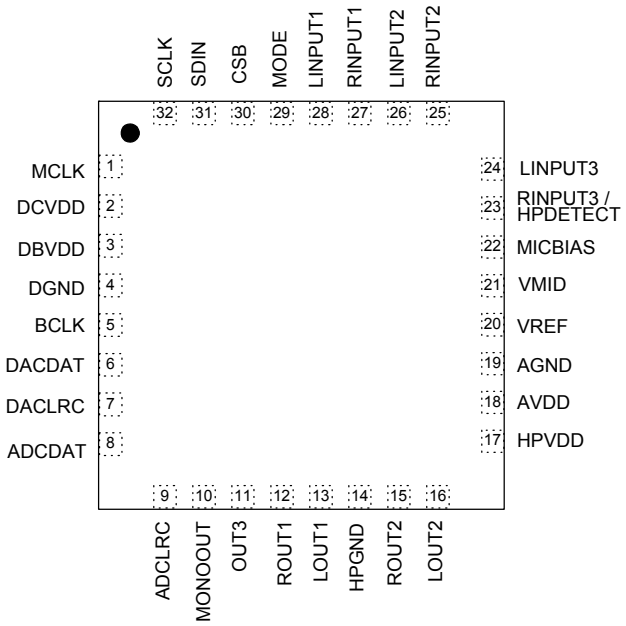
PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8750CLSEFL	-25°C to +85°C	32-lead QFN (5x5x0.9mm) (Pb-free)	MSL1	260°C
WM8750CLSEFL/R	-25°C to +85°C	32-lead QFN (5x5x0.9mm) (Pb-free, tape and reel)	MSL1	260°C

Note:
Reel quantity = 3500

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
1	MCLK	Digital Input	Master Clock
2	DCVDD	Supply	Digital Core Supply
3	DBVDD	Supply	Digital Buffer (I/O) Supply
4	DGND	Supply	Digital Ground (return path for both DCVDD and DBVDD)
5	BCLK	Digital Input / Output	Audio Interface Bit Clock
6	DACDAT	Digital Input	DAC Digital Audio Data
7	DACLRC	Digital Input / Output	Audio Interface Left / Right Clock/Clock Out
8	ADCDAT	Digital Output	ADC Digital Audio Data
9	ADCLRC	Digital Input / Output	Audio Interface Left / Right Clock
10	MONOOUT	Analogue Output	Mono Output
11	OUT3	Analogue Output	Analogue Output 3 (can be used as Headphone Pseudo Ground)
12	ROUT1	Analogue Output	Right Output 1 (Line or Headphone)
13	LOUT1	Analogue Output	Left Output 1 (Line or Headphone)
14	HPGND	Supply	Supply for Analogue Output Drivers (LOUT1/2, ROUT1/2)
15	ROUT2	Analogue Output	Right Output 1 (Line or Headphone or Speaker)
16	LOUT2	Analogue Output	Left Output 1 (Line or Headphone or Speaker)
17	HPVDD	Supply	Supply for Analogue Output Drivers (LOUT1/2, ROUT1/2, MONOUT)
18	AVDD	Supply	Analogue Supply
19	AGND	Supply	Analogue Ground (return path for AVDD)
20	VREF	Analogue Output	Reference Voltage Decoupling Capacitor
21	VMID	Analogue Output	Midrail Voltage Decoupling Capacitor
22	MICBIAS	Analogue Output	Microphone Bias
23	RINPUT3 / HPDETECT	Analogue Input	Right Channel Input 3 or Headphone Plug-in Detection
24	LINPUT3	Analogue Input	Left Channel Input 3
25	RINPUT2	Analogue Input	Right Channel Input 2
26	LINPUT2	Analogue Input	Left Channel Input 2
27	RINPUT1	Analogue Input	Right Channel Input 1
28	LINPUT1	Analogue Input	Left Channel Input 1
29	MODE	Digital Input	Control Interface Selection
30	CSB	Digital Input	Chip Select / Device Address Selection
31	SDIN	Digital Input/Output	Control Interface Data Input / 2-wire Acknowledge output
32	SCLK	Digital Input	Control Interface Clock Input

Note:

It is recommended that the QFN ground paddle should be connected to analogue ground on the application PCB.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages	-0.3V	+3.63V
Voltage range digital inputs	DGND -0.3V	DBVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Operating temperature range, T_A	-25°C	+85°C
Storage temperature after soldering	-65°C	+150°C

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other.
3. DCVDD must be less than or equal to AVDD and DBVDD.

RECOMMENDED OPERATION CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD	1.42		3.6	V
Digital supply range (Buffer)	DBVDD	1.7		3.6	V
Analogue supplies range	AVDD, HPVDD	1.8		3.6	V
Ground	DGND,AGND, HPGND		0		V

ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD = 1.5V, DBVDD = 3.3V, AVDD = HPVDD = 3.3V, T_A = +25°C,
1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

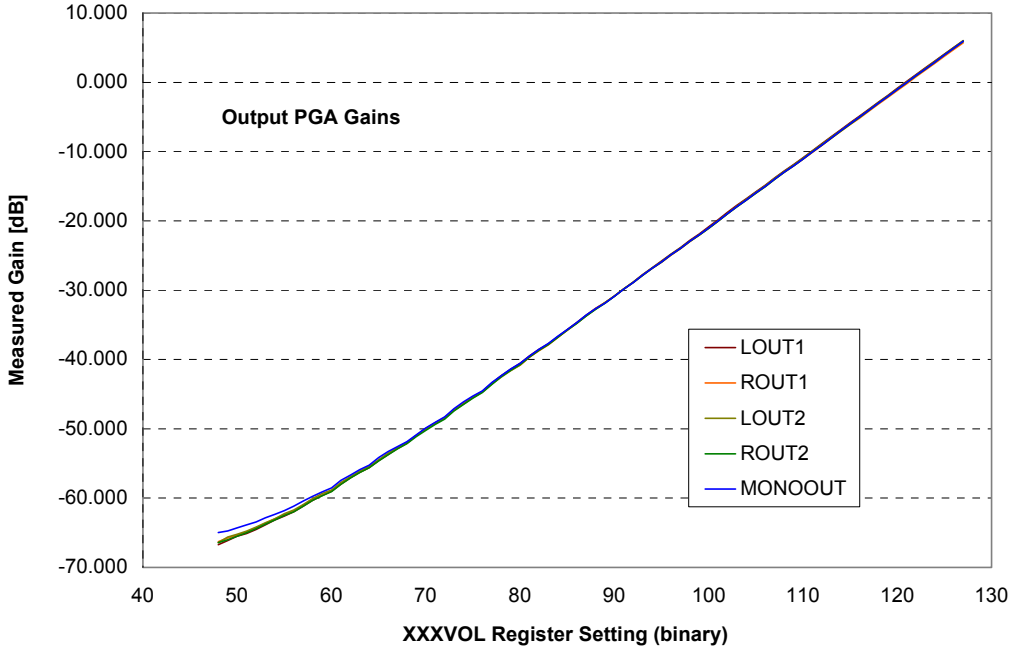
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (LINPUT1, RINPUT1, LINPUT2, RINPUT2, LINPUT3, RINPUT3) to ADC out						
Full Scale Input Signal Level (for ADC 0dB Input at 0dB Gain)	V_{INFS}	AVDD = 3.3V		1.0		V rms
		AVDD = 1.8V		0.545		
Input Resistance		L/RINPUT1 to ADC, PGA gain = 0dB		22		kΩ
		L/RINPUT1 to ADC, PGA gain = +30dB		1.5		
		L/RINPUT1 unused DC Measurement		16		
		L/RINPUT1 unused		17		
Input Capacitance				10		pF
Signal to Noise Ratio (A-weighted)	SNR	AVDD = 3.3V	80	95		dB
		AVDD = 1.8V		90		
Total Harmonic Distortion	THD	-1dBFs input, AVDD = 3.3V		-82 0.008		dB %
		-1dBFs input, AVDD = 1.8V		-74 0.02		
ADC Channel Separation		1kHz signal		85		dB
Channel Matching		1kHz signal		0.2		dB
Analogue Outputs (LOUT1/2, ROUT1/2, MONOOUT)						
0dB Full scale output voltage				AVDD/3.3		Vrms
Mute attenuation		1kHz, full scale signal		90		dB
		MONOOUT pin		81		
Channel Separation		analogue in to analogue out		85		dB
DAC to Line-Out (L/ROUT2 with 10kΩ / 50pF load)						
Signal to Noise Ratio (A-weighted)	SNR	AVDD=3.3V	90	98		dB
		AVDD=1.8V		93		
Total Harmonic Distortion	THD	AVDD=3.3V		-84		dB
		AVDD=1.8V		-80		
Channel Separation		1kHz signal		100		dB
Headphone Output (LOUT1/ROUT1, using capacitors)						
Output Power per channel	P_O	Output power is very closely correlated with THD; see below.				
Total Harmonic Distortion	THD	HPVDD=1.8V, R_L=32Ω P_O=5mW		0.016 -76		% dB
		HPVDD=1.8V, R_L=16Ω P_O=5mW		0.022 -73		
		HPVDD=3.3V, R_L=32Ω, P_O=20mW		0.013 -78		
		HPVDD=3.3V, R_L=16Ω, P_O=20mW		0.018 -75		
Signal to Noise Ratio (A-weighted)	SNR	HPVDD = 3.3V	92	96		dB
		HPVDD = 1.8V		96		

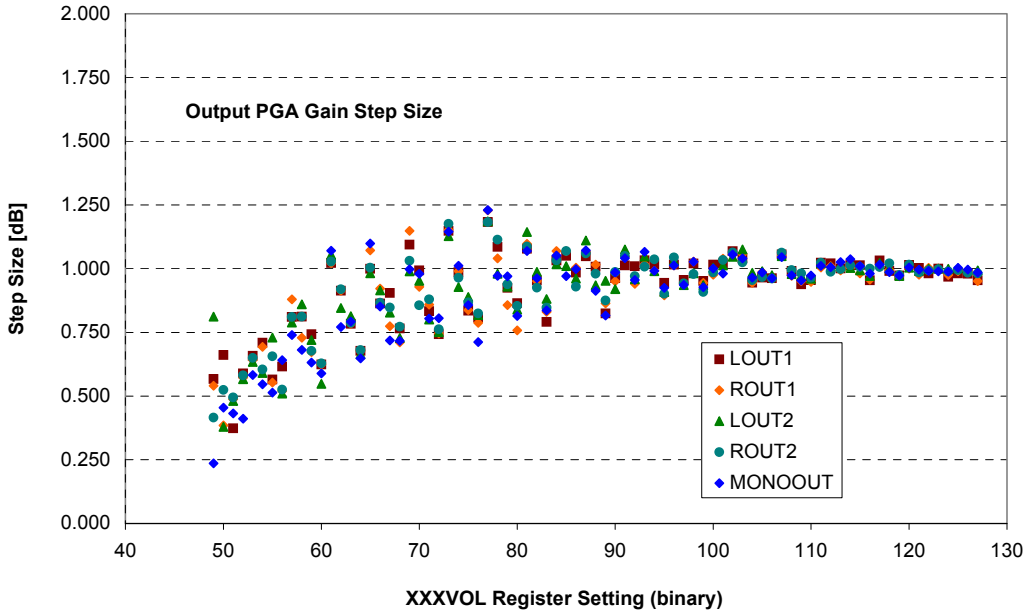
Test Conditions

DCVDD = 1.5V, DBVDD = 3.3V, AVDD = HPVDD = 3.3V, T_A = +25°C,
1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

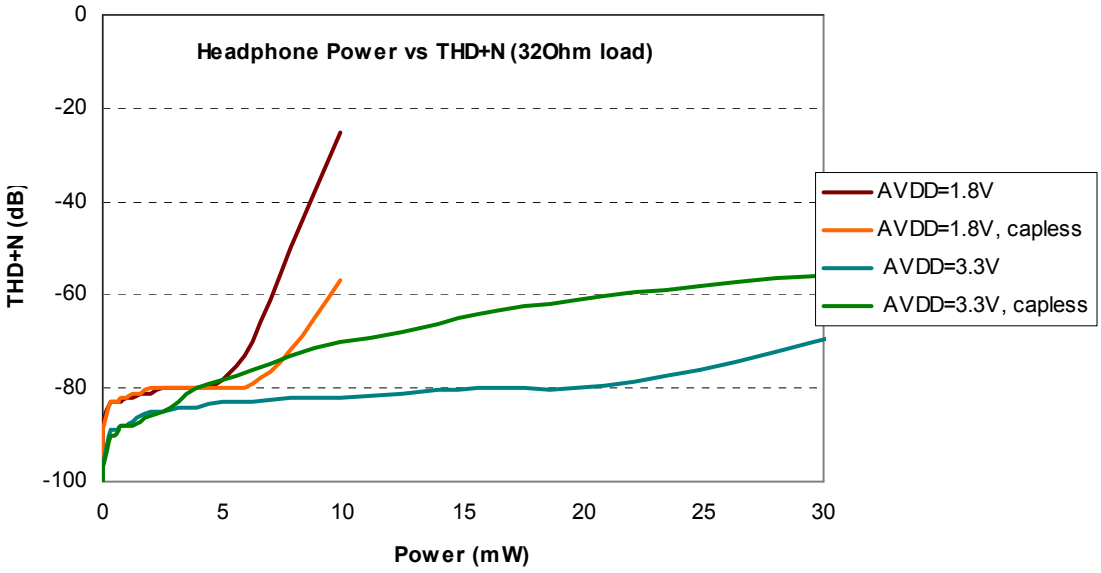
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Speaker Output (LOUT2/ROUT2 with 8Ω bridge tied load, ROUT2INV=1)						
Output Power at 1% THD	P_O	THD = 1%		330		mW (rms)
Abs. Max Power Ouptut	$P_O$max			500		mW (rms)
Total Harmonic Distortion	THD	Po=200mW, R_L=8Ω, HPVDD=3.3V		-63 0.07		dB %
Signal to Noise Ratio (A-weighted)	SNR	HPVDD=3.3V, R_L=8Ω		95		dB
Analogue Reference Levels						
Midrail Reference Voltage	VMID		–3%	AVDD/2	+3%	V
Buffered Reference Voltage	VREF		–3%	AVDD/2	+3%	V
Microphone Bias						
Bias Voltage	$V_{MICBIAS}$	3mA load current	–5%	0.9×AVDD	+ 5%	V
Bias Current Source	$I_{MICBIAS}$				3	mA
Output Noise Voltage	Vn	1K to 20kHz		15		nV/√Hz
Digital Input / Output						
Input HIGH Level	V_{IH}		0.7×DBVDD			V
Input LOW Level	V_{IL}				0.3×DBVDD	V
Output HIGH Level	V_{OH}	I_{OH} = +1mA	0.9×DBVDD			V
Output LOW Level	V_{OL}	I_{OL} = -1mA			0.1×DBVDD	V
HPDETECT (pin 23)						
Input HIGH Level	V_{IH}		0.7×AVDD			V
Input LOW Level	V_{IL}				0.3×AVDD	V

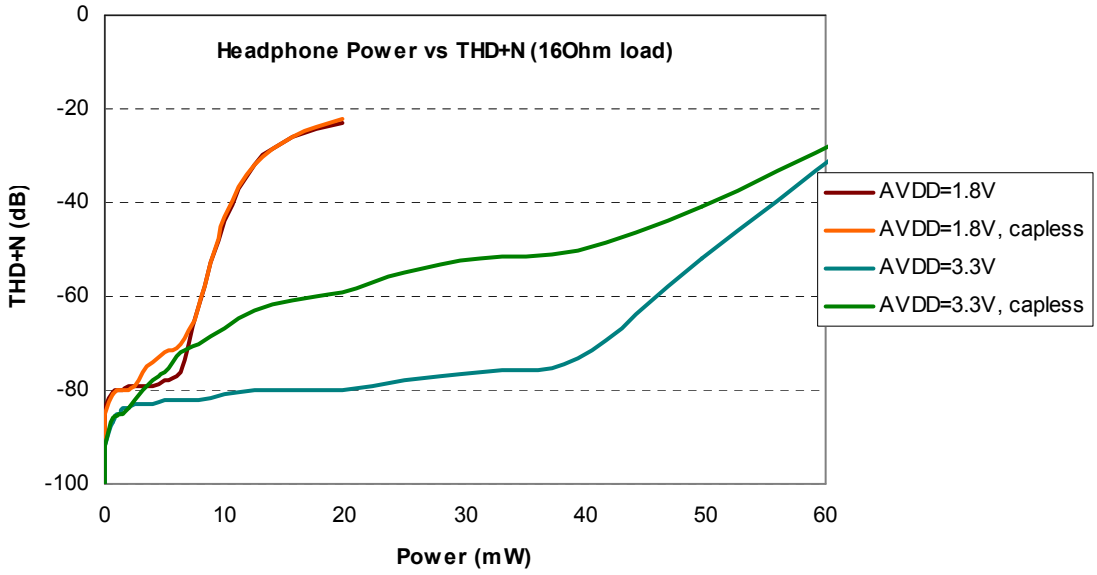
OUTPUT PGA'S LINEARITY



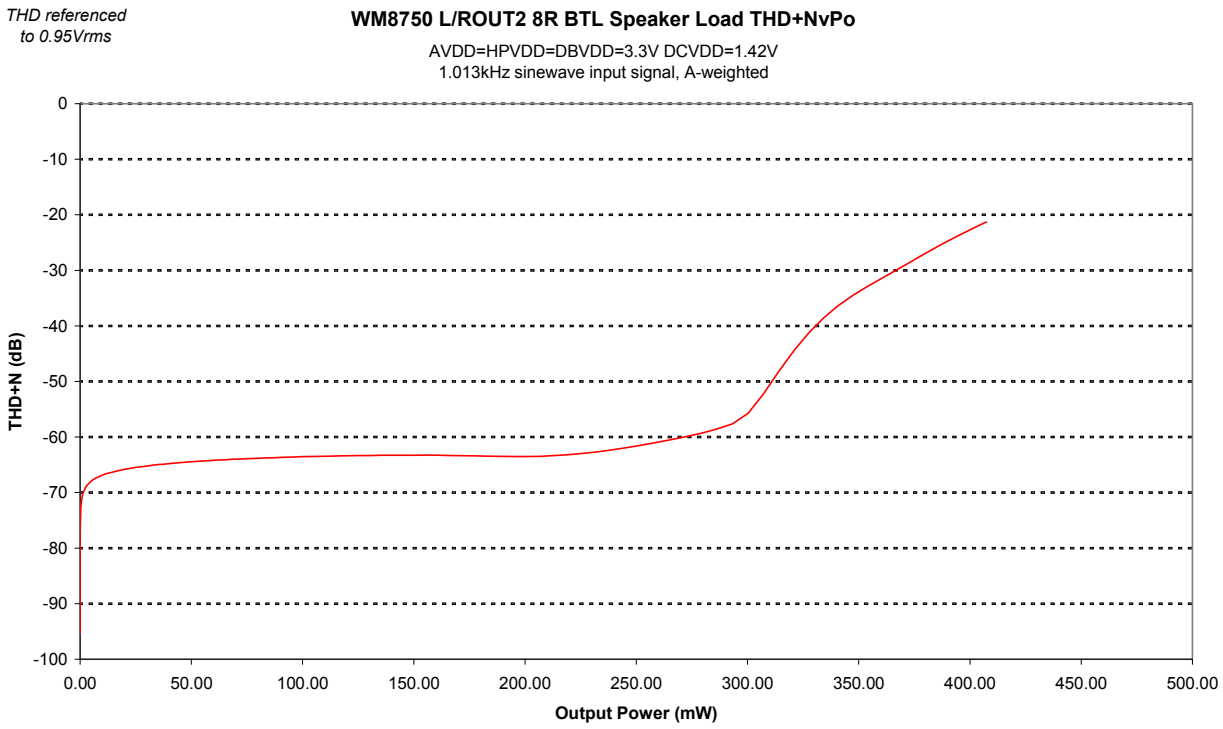


HEADPHONE OUTPUT THD VERSUS POWER





SPEAKER THD AND NOISE VERSUS POWER



POWER CONSUMPTION

The power consumption of the WM8750L depends on the following factors.

- Supply voltages: Reducing the supply voltages also reduces supply currents, and therefore results in significant power savings, especially in the digital sections of the WM8750L.
- Operating mode: Significant power savings can be achieved by always disabling parts of the WM8750L that are not used (e.g. mic pre-amps, unused outputs, DAC, ADC, etc.)

Control Register	R25 (19h)							R26 (1Ah)								R24		R23	Other settings	AVDD		DCVDD		DBVDD		HPVDD		Tot. Power
Bit	VMIDSEL	VREF	AINL	AINR	ADCL	ADCR	MICB	DACL	DACR	LOUT1	ROUT1	LOUT2	ROUT2	MONO	OUT3	ADCOSR	DACOSR	VSEL		V	I (mA)	V	I (mA)	V	I (mA)	V	I (mA)	mW
OFF	00	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	11	Clocks stopped	3.3	0.000	3.3	0.011	3.3	0.000	3.3	0.000	0.0363
																		01		2.5	0.000	2.5	0.009	2.5	0.000	2.5	0.000	0.0225
																		00		1.8	0.000	1.5	0.007	1.8	0.000	1.8	0.000	0.0105
Standby	10	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	11	Interface Stopped	3.3	0.341	3.3	0.011	3.3	0.000	3.3	0.000	1.1616
(500 KOhm VMID string)																		01		2.5	0.282	2.5	0.009	2.5	0.000	2.5	0.000	0.7275
																		00		1.8	0.194	1.5	0.007	1.8	0.000	1.8	0.000	0.3597
Playback to Line-out	01	1	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	11		3.3	4.007	3.3	5.380	3.3	0.301	3.3	0.748	34.4388
																		01		2.5	3.025	2.5	3.687	2.5	0.215	2.5	0.723	19.1250
																		00		1.8	2.449	1.5	2.029	1.8	0.147	1.8	0.427	8.4849
Playback to Line-out	01	1	0	0	0	0	0	1	1	1	1	0	0	0	0	0	1	11		3.3	3.796	3.3	4.541	3.3	0.302	3.3	0.744	30.9639
(64x oversampling mode)																		01		2.5	2.870	2.5	3.093	2.5	0.215	2.5	0.722	17.2500
																		00		1.8	2.338	1.5	1.691	1.8	0.147	1.8	0.427	7.7781
Playback to 16 Ohm Headphone	01	1	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	11		3.3	3.997	3.3	5.380	3.3	0.301	3.3	0.748	34.4058
																		01		2.5	3.026	2.5	3.687	2.5	0.215	2.5	0.723	19.1275
																		00		1.8	2.451	1.5	2.029	1.8	0.147	1.8	0.427	8.4885
Playback to 16 Ohm Headphone	01	1	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	11	-27.959 dBFS	3.3	3.998	3.3	6.430	3.3	0.301	3.3	2.142	42.4743
0.1mW / channel into load																		01	-25.547 dBFS	2.5	3.029	2.5	4.462	2.5	0.215	2.5	2.132	24.5950
(JEITA CP-2905B)																		00	-22.694 dBFS	1.8	2.454	1.5	2.475	1.8	0.147	1.8	1.977	11.9529
Playback to 16 Ohm Headphone	01	1	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0	11	-10.969 dBFS	3.3	3.980	3.3	6.481	3.3	0.301	3.3	12.558	76.9560
5mW / channel into load																		01	-8.558 dBFS	2.5	3.028	2.5	4.503	2.5	0.215	2.5	12.604	50.8750
																		00	-5.704 dBFS	1.8	2.450	1.5	2.503	1.8	0.147	1.8	12.275	30.5241
Playback to 16 Ohm Headphone	01	1	0	0	0	0	0	1	1	1	1	0	0	0	1	0	0	11	R24, OUT3SW=00	3.3	3.986	3.3	5.567	3.3	0.301	3.3	1.133	36.2571
(capless mode using OUT3)																		01		2.5	3.027	2.5	3.688	2.5	0.215	2.5	1.110	20.1000
																		00		1.8	2.452	1.5	2.029	1.8	0.147	1.8	0.726	9.0285
Playback to 8 Ohm BTL Speaker	01	1	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	11	R24, ROUT2INV=1	3.3	4.151	3.3	5.381	3.3	0.301	3.3	0.603	34.4388
																		01		2.5	3.151	2.5	3.688	2.5	0.215	2.5	0.575	19.0725
																		00		1.8	2.533	1.5	2.029	1.8	0.147	1.8	0.352	8.5011
Headphone Amp	01	1	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	11	Clocks Stopped	3.3	1.665	3.3	0.011	3.3	0.000	3.3	0.749	8.0025
(line-in to 16 Ohm headphone)																		01		2.5	1.256	2.5	0.009	2.5	0.000	2.5	0.725	4.9750
																		00		1.8	0.865	1.5	0.007	1.8	0.000	1.8	0.429	2.3397
Speaker Amp	01	1	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	11	Clocks Stopped	3.3	1.857	3.3	0.011	3.3	0.000	3.3	0.975	9.3819
(line-in to 8 Ohm speaker)																		01	R24, ROUT2INV=1	2.5	1.372	2.5	0.009	2.5	0.000	2.5	0.985	5.9150
																		00		1.8	0.928	1.5	0.007	1.8	0.000	1.8	0.732	2.9985
Record from Line-in	01	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	11		3.3	9.240	3.3	6.493	3.3	0.325	3.3	0.000	52.9914
																		01		2.5	8.407	2.5	4.243	2.5	0.232	2.5	0.000	32.2050
																		00		1.8	6.744	1.5	2.141	1.8	0.159	1.8	0.000	15.6369
Record from Line-in	01	1	1	1	1	1	0	0	0	0	0	0	0	0	0	1	0	11		3.3	5.223	3.3	5.822	3.3	0.326	3.3	0.000	37.5243
(64x oversampling mode)																		01		2.5	4.512	2.5	3.740	2.5	0.232	2.5	0.000	21.2100
																		00		1.8	3.834	1.5	1.899	1.8	0.160	1.8	0.000	10.0377
Record from mono microphone	01	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	11	R32, LMICBOOST=11;	3.3	5.207	3.3	6.337	3.3	0.325	3.3	0.000	39.1677
																		01	R23, DATSEL=01	2.5	4.630	2.5	4.139	2.5	0.231	2.5	0.000	22.5000
																		00		1.8	3.755	1.5	2.128	1.8	0.163	1.8	0.000	10.2444
Record from mono microphone	01	1	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	11	R32, LMICBOOST=11;	3.3	5.561	3.3	6.349	3.3	0.325	3.3	0.000	40.3755
(differential)																		01	R23, DATSEL=01;	2.5	4.890	2.5	4.139	2.5	0.231	2.5	0.000	23.1500
																		00	R32, LINSEL=11	1.8	3.925	1.5	2.130	1.8	0.163	1.8	0.000	10.5534
Stereo Record & Playback	01	1	1	1	1	1	1	1	1	0	0	1	1	0	0	0	0	11		3.3	12.778	3.3	10.650	3.3	0.323	3.3	0.680	80.6223
																		01		2.5	11.070	2.5	7.095	2.5	0.231	2.5	0.569	47.4125
																		00		1.8	8.585	1.5	3.846	1.8	0.159	1.8	0.351	22.1400
Stereo Record & Playback	01	1	1	1	1	1	1	1	1	0	0	1	1	0	0	1	1	11		3.3	8.570	3.3	9.237	3.3	0.325	3.3	0.698	62.1390
(64x oversampling mode)																		01		2.5	7.061	2.5	6.101	2.5	0.232	2.5	0.581	34.9375
																		00		1.8	5.601	1.5	3.258	1.8	0.160	1.8	0.348	15.8832

Table 1 Supply Current Consumption

Note: All figures are at T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 12.288 MHz (256fs), with zero signal (quiescent) unless otherwise noted.

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

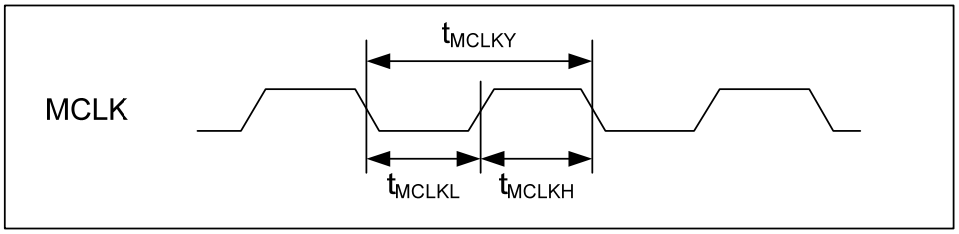


Figure 1 System Clock Timing Requirements

Test Conditions

CLKDIV2=0, DCVDD = 1.42V, DBVDD = 3.3V, DGND = 0V, T_A = +25°C,
Slave Mode fs = 48kHz, MCLK = 384fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
System Clock Timing Information					
MCLK System clock pulse width high	T_{MCLKL}	21			ns
MCLK System clock pulse width low	T_{MCLKH}	21			ns
MCLK System clock cycle time	T_{MCLKY}	54			ns
MCLK duty cycle	T_{MCLKDS}	60:40		40:60	

Test Conditions

CLKDIV2=1, DCVDD = 1.42V, DBVDD = 3.3V, DGND = 0V, T_A = +25°C,
Slave Mode fs = 48kHz, MCLK = 384fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
System Clock Timing Information					
MCLK System clock pulse width high	T_{MCLKL}	10			ns
MCLK System clock pulse width low	T_{MCLKH}	10			ns
MCLK System clock cycle time	T_{MCLKY}	27			ns

AUDIO INTERFACE TIMING – MASTER MODE

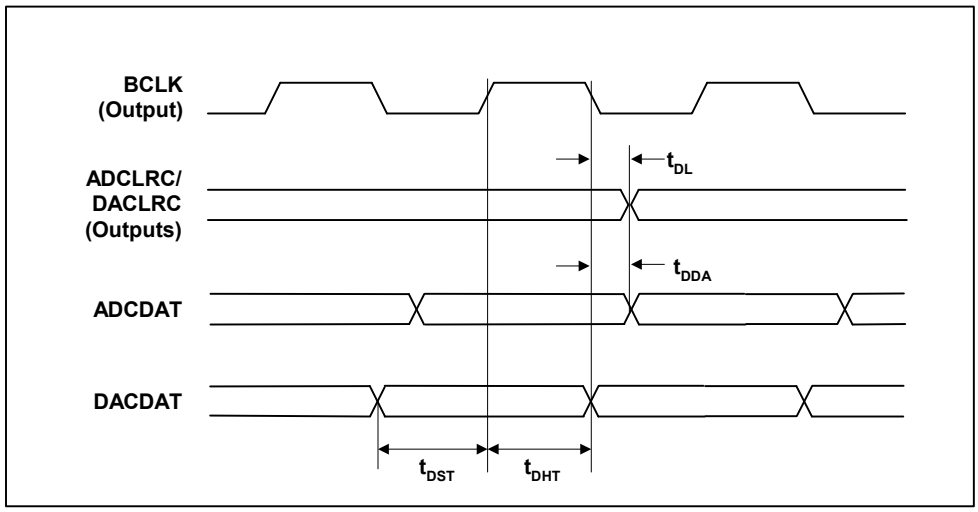


Figure 2 Digital Audio Data Timing – Master Mode (see Control Interface)

Test Conditions

DCVDD = 1.42V, DBVDD = 3.3V, DGND = 0V, T_A = +25°C,
Master Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Bit Clock Timing Information					
BCLK rise time (10pF load)	t_{BCLKR}			3	ns
BCLK fall time (10pF load)	t_{BCLKF}			3	ns
BCLK duty cycle (normal mode, BCLK = MCLK/n)	t_{BCLKDS}		50:50		
BCLK duty cycle (USB mode, BCLK = MCLK)	t_{BCLKDS}		T_{MCLKDS}		
Audio Data Input Timing Information					
ADCLRC/DACLRC propagation delay from BCLK falling edge	t_{DL}			10	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			27	ns
DACDAT setup time to BCLK rising edge	t_{DST}	10			ns
DACDAT hold time from BCLK rising edge	t_{DHT}	10			ns

AUDIO INTERFACE TIMING – SLAVE MODE

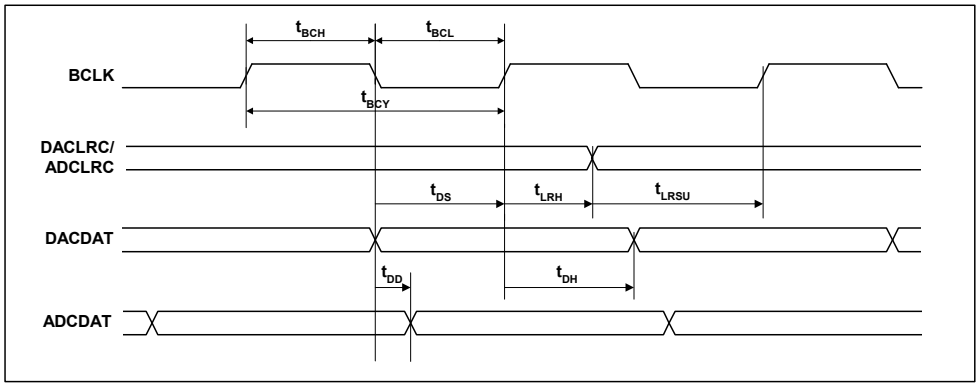


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

DCVDD = 1.42V, DBVDD = 3.3V, DGND = 0V, T_A = +25°C,
Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t_{BCY}	50			ns
BCLK pulse width high	t_{BCH}	20			ns
BCLK pulse width low	t_{BCL}	20			ns
ADCLRC/DACLRC set-up time to BCLK rising edge	t_{LRSU}	10			ns
ADCLRC/DACLRC hold time from BCLK rising edge	t_{LRH}	10			ns
DACDAT hold time from BCLK rising edge	t_{DH}	10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			10	ns

Notes:

BCLK period should always be greater than or equal to MCLK period.

For optimum ADC audio performance, the BCLK input signal edge should coincide with the falling edge of MCLK.

CONTROL INTERFACE TIMING – 3-WIRE MODE

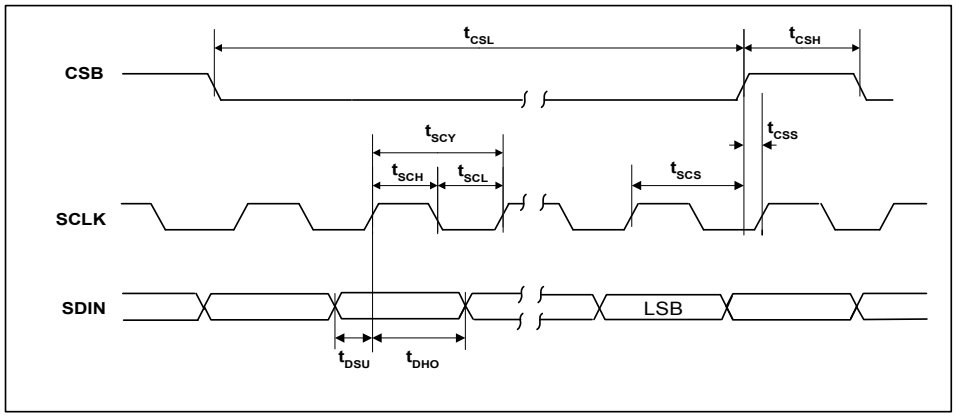


Figure 4 Control Interface Timing – 3-Wire Serial Control Mode

Test Conditions

DCVDD = 1.42V, DBVDD = 3.3V, DGND = 0V, T_A = +25°C,
Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB rising edge	t_{SCS}	80			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDIN to SCLK set-up time	t_{DSU}	40			ns
SCLK to SDIN hold time	t_{DHO}	40			ns
CSB pulse width low	t_{CSL}	40			ns
CSB pulse width high	t_{CSH}	40			ns
CSB rising to SCLK rising	t_{CSS}	40			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

CONTROL INTERFACE TIMING – 2-WIRE MODE

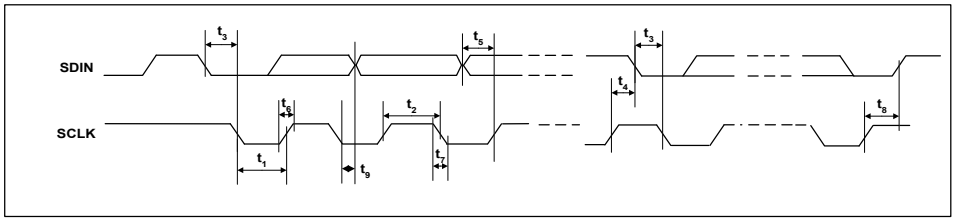


Figure 5 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DCVDD = 1.42V, DBVDD = 3.3V, DGND = 0V, T_A = +25°C,
Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency		0		526	kHz
SCLK Low Pulse-Width	t_1	1.3			us
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDIN, SCLK Rise Time	t_6			300	ns
SDIN, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

INTERNAL POWER ON RESET CIRCUIT

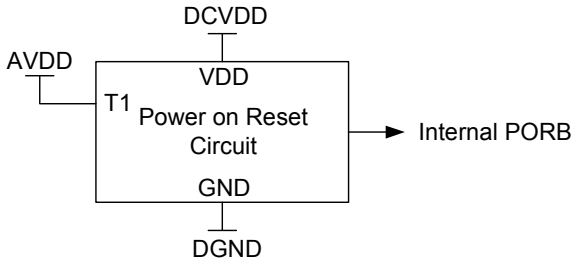


Figure 6 Internal Power on Reset Circuit Schematic

The WM8750 includes an internal Power-On-Reset Circuit, as shown in Figure 6, which is used to reset the digital logic into a default state after power up. The power on reset circuit is powered from DCVDD and monitors DCVDD and AVDD. It asserts PORB low if DCVDD or AVDD are below a minimum threshold.

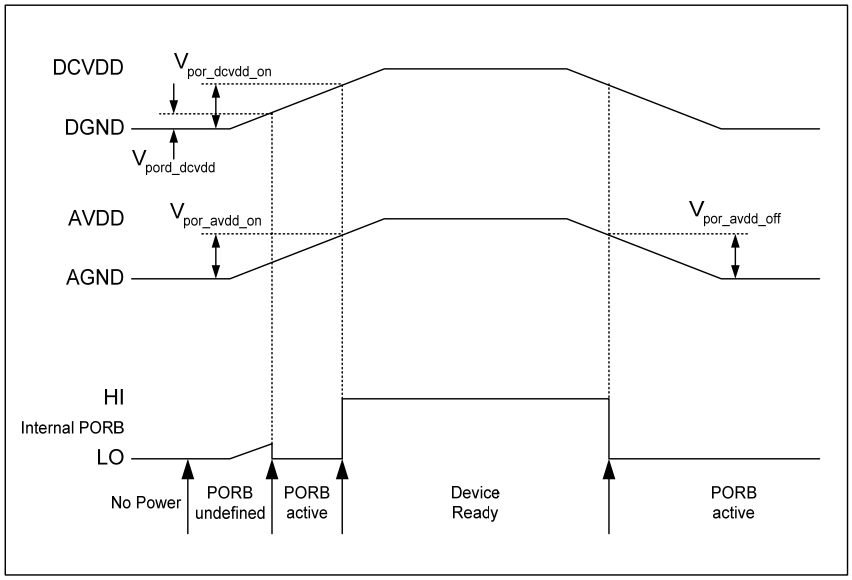


Figure 7 Typical Power-Up Sequence

Figure 7 shows a typical power-up sequence. When DCVDD and AVDD rise above the minimum thresholds, Vpord_dcvdd and Vpord_avdd, there is enough voltage for the circuit to guarantee the Power on Reset is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When DCVDD rises to Vpor_dcvdd_on and AVDD rises to Vpor_avdd_on, PORB is released high and all registers are in their default state and writes to the control interface may take place. If DCVDD and AVDD rise at different rates then PORB will only be released when DCVDD and AVDD have both exceeded the Vpor_dcvdd_on and Vpor_avdd_on thresholds.

On power down, PORB is asserted low whenever DCVDD drops below the minimum threshold Vpor_dcvdd_off or AVDD drops below the minimum threshold Vpor_avdd_off.

SYMBOL	MIN	TYP	MAX	UNIT
V_{pord_dcvdd}	0.4	0.6	0.8	V
$V_{por\_dcvdd\_on}$	0.9	1.26	1.6	V
$V_{por\_avdd\_on}$	0.5	0.7	0.9	V
$V_{por\_avdd\_off}$	0.4	0.6	0.8	V

Table 2 Typical POR Operation (typical values, not tested)

DEVICE DESCRIPTION

INTRODUCTION

The WM8750L is a low power audio codec offering a combination of high quality audio, advanced features, low power and small size. These characteristics make it ideal for portable digital audio applications such as MP3 and minidisk player / recorders. Stereo 24-bit multi-bit delta sigma ADCs and DACs are used with oversampling digital interpolation and decimation filters.

The device includes three stereo analogue inputs that can be switched internally. Each can be used as either a line level input or microphone input and LINPUT1/RINPUT1 and LINPUT2/RINPUT2 can be configured as mono differential inputs. A programmable gain amplifier with automatic level control (ALC) keeps the recording volume constant. The on-chip stereo ADC and DAC are of a high quality using a multi-bit, low-order oversampling architecture to deliver optimum performance with low power consumption.

The DAC output signal first enters an analogue mixer where an analogue input and/or the post-ALC signal can be added to it. This mix is available on line and headphone outputs.

The WM8750L has a configurable digital audio interface where ADC data can be read and digital audio playback data fed to the DAC. It supports a number of audio data formats including I^2S, DSP Mode (a burst mode in which frame sync plus 2 data packed words are transmitted), MSB-First, left justified and MSB-First, right justified, and can operate in master or slave modes.

The WM8750L uses a unique clocking scheme that can generate many commonly used audio sample rates from either a 12.00MHz USB clock or an industry standard 256/384 f_s clock. This feature eliminates the common requirement for an external phase-locked loop (PLL) in applications where the master clock is not an integer multiple of the sample rate. Sample rates of 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz and 96kHz can be generated. The digital filters used for recording and playback are optimised for each sampling rate used.

To allow full software control over all its features, the WM8750L offers a choice of 2 or 3 wire MPU control interface. It is fully compatible and an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs.

The design of the WM8750L has given much attention to power consumption without compromising performance. It operates at very low voltages, and includes the ability to power off parts of the circuitry under software control, including standby and power off modes.

INPUT SIGNAL PATH

The input signal path for each channel consists of a switch to select between three analogue inputs, followed by a PGA (programmable gain amplifier) and an optional microphone gain boost. A differential input of either (LINPUT1 – RINPUT1) or (LINPUT2 – RINPUT2) may also be selected. The gain of the PGA can be controlled either by the user or by the on-chip ALC function (see Automatic Level Control).

The signal then enters an ADC where it is digitised. Alternatively, the two channels can also be mixed in the analogue domain and digitised in one ADC while the other ADC is switched off. The mono-mix signal appears on both digital output channels.

SIGNAL INPUTS

The WM8750L has three sets of high impedance, low capacitance AC coupled analogue inputs, LINPUT1/RINPUT1, LINPUT2/RINPUT2 and LINPUT3/RINPUT3. Inputs can be configured as microphone or line level by enabling or disabling the microphone gain boost.

LINSEL and RINSEL control bits (see Table 3) are used to select independently between external inputs and internally generated differential products (LINPUT1-RINPUT1 or LINPUT2-RINPUT2). The choice of differential signal, LINPUT1-RINPUT1 or LINPUT2-RINPUT2 is made using DS (refer to Table 5).

As an example, the WM8750 can be set up to convert one differential and one single ended mono signal by applying the differential signal to LINPUT1/RINPUT1 and the single ended signal to RINPUT2. By setting LINSEL to L-R Differential (see Table 3), DS to LINPUT1 - RINPUT1 (see Table 5) and RINSEL to RINPUT2, each mono signal can then be routed to a separate ADC or Bypass path.

The signal inputs are biased internally to the reference voltage VREF. Whenever the line inputs are muted or the device placed into standby mode, the inputs are kept biased to VREF using special anti-thump circuitry. This reduces any audible clicks that may otherwise be heard when changing inputs.

DC MEASUREMENT

For DC measurements (for example, battery voltage monitoring), the input signal at the LINPUT1 and/or RINPUT1 pins can be taken directly into the respective ADC, bypassing both PGA and microphone boost. The ADC output then becomes unsigned relative to AVDD, instead of being a signed (two's complement) number relative to VREF. Setting L/RDCM will override L/RINSEL. The input range for dc measurement is AGND to AVDD.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (20h) ADC Signal Path Control (Left)	7:6	LINSEL	00	Left Channel Input Select 00 = LINPUT1 01 = LINPUT2 10 = LINPUT3 11 = L-R Differential (either LINPUT1-RINPUT1 or LINPUT2-RINPUT2, selected by DS)
	5:4	LMICBOOST	00	Left Channel Microphone Gain Boost 00 = Boost off (bypassed) 01 = 13dB boost 10 = 20dB boost 11 = 29dB boost
R33 (21h) ADC Signal Path Control (Right)	7:6	RINSEL	00	Right Channel Input Select 00 = RINPUT1 01 = RINPUT2 10 = RINPUT3 11 = L-R Differential (either LINPUT1-RINPUT1 or LINPUT2-RINPUT2, selected by DS)
	5:4	RMICBOOST	00	Right Channel Microphone Gain Boost 00 = Boost off (bypassed) 01 = 13dB boost 10 = 20dB boost 11 = 29dB boost

Table 3 Input Software Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R31 (1Fh) ADC input Mode	5	RDCM	0	Right Channel DC Measurement 0 = Normal Operation, PGA Enabled 1 = Measure DC level on RINPUT1
	4	LDCM	0	Left Channel DC Measurement 0 = Normal Operation, PGA Enabled 1 = Measure DC level on LINPUT1

Table 4 DC Measurement Select

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R31 (1Fh) ADC Input Mode	8	DS	0	Differential input select 0: LINPUT1 - RINPUT1 1: LINPUT2 – RINPUT2

Table 5 Differential Input Select

MONO MIXING

The stereo ADC can operate as a stereo or mono device, or the two channels can be mixed to mono, either in the analogue domain (i.e. before the ADC) or in the digital domain (after the ADC). MONOMIX selects the mode of operation. For analogue mono mix either the left or right channel ADC can be used, allowing the unused ADC to be powered off or used for a dc measurement conversion. The user also has the flexibility to select the data output from the audio interface using DATSEL. The default is for left and right channel ADC data to be output, but the interface may also be configured so that e.g. left channel ADC data is output as both left and right data for when an analogue mono mix is selected.

Note:

If DC measurement is selected this overrides the MONOMIX selection.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R31 (1Fh) ADC input Mode	7:6	MONOMIX [1:0]	00	00: Stereo 01: Analogue Mono Mix (using left ADC) 10: Analogue Mono Mix (using right ADC) 11: Digital Mono Mix

Table 6 Mono Mixing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) Additional Control (1)	3:2	DATSEL [1:0]	00	00: left data=left ADC; right data =right ADC 01: left data =left ADC; right data = left ADC 10: left data = right ADC; right data =right ADC 11: left data = right ADC; right data = left ADC

Table 7 ADC Data Output Configuration

The MICBIAS output provides a low noise reference voltage suitable for biasing electret type microphones and the associated external resistor biasing network. Refer to the Applications Information section for recommended external components. The output can be enabled or disables using the MICB control bit (see also the “Power Management” section).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Power Management (1)	1	MICB	0	Microphone Bias Enable 0 = OFF (high impedance output) 1 = ON

Table 8 Microphone Bias Control

The internal MICBIAS circuitry is shown below. Note that the is a maximum source current capability for MICBIAS is 3mA. The external biasing resistors therefore must be large enough to limit the MICBIAS current to 3mA.

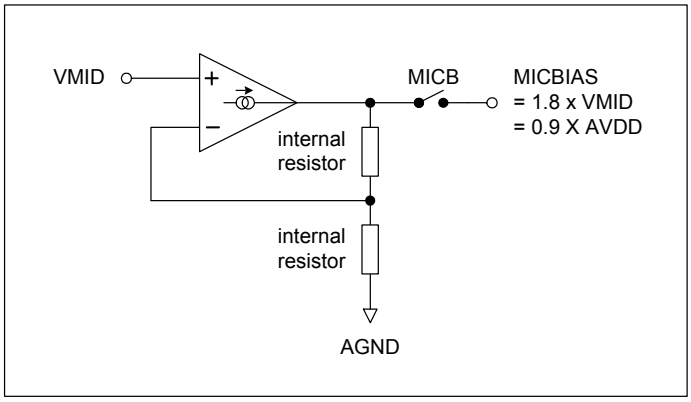


Figure 8 Microphone Bias Schematic

PGA CONTROL

The PGA matches the input signal level to the ADC input range. The PGA gain is logarithmically adjustable from +30dB to –17.25dB in 0.75dB steps. Each PGA can be controlled either by the user or by the ALC function (see Automatic Level Control). When ALC is enabled for one or both channels, then writing to the corresponding PGA control register has no effect.

The gain is independently adjustable on both Right and Left Line Inputs. Additionally, by controlling the register bits LIVU and RIVU, the left and right gain settings can be simultaneously updated. Setting the LIZC and RIZC bits enables a zero-cross detector which ensures that PGA gain changes only occur when the signal is at zero, eliminating any zipper noise. If zero cross is enabled a timeout is also available to update the gain if a zero cross does not occur. This function may be enabled by setting TOEN in register R23 (17h).

The inputs can also be muted in the analogue domain under software control. The software control registers are shown in Table 9. If zero crossing is enabled, it is necessary to enable zero cross timeout to un-mute the input PGAs. This is because their outputs will not cross zero when muted. Alternatively, zero cross can be disabled before sending the un-mute command.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (00h) Left Channel PGA	8	LIVU	0	Left Volume Update 0 = Store LINVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LINVOL, right = intermediate latch)
	7	LINMUTE	1	Left Channel Input Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: LIVU must be set to un-mute.
	6	LIZC	0	Left Channel Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately
	5:0	LINVOL [5:0]	010111 (0dB)	Left Channel Input Volume Control 111111 = +30dB 111110 = +29.25dB . . 0.75dB steps down to 000000 = -17.25dB

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 (01h) Right Channel PGA	8	RIVU	0	Right Volume Update 0 = Store RINVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (right = RINVOL, left = intermediate latch)
	7	RINMUTE	1	Right Channel Input Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: RIVU must be set to un-mute.
	6	RIZC	0	Right Channel Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately
	5:0	RINVOL [5:0]	010111 (0dB)	Right Channel Input Volume Control 111111 = +30dB 111110 = +29.25dB . . 0.75dB steps down to 000000 = -17.25dB
R23 (17h) Additional Control (1)	0	TOEN	0	Timeout Enable 0 : Timeout Disabled 1 : Timeout Enabled

Table 9 Input PGA Software Control

ANALOGUE TO DIGITAL CONVERTER (ADC)

The WM8750L uses a multi-bit, oversampled sigma-delta ADC for each channel. The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise. The ADC Full Scale input level is proportional to AVDD. With a 3.3V supply voltage, the full scale level is 1.0 Volts r.m.s. Any voltage greater than full scale may overload the ADC and cause distortion.

ADC DIGITAL FILTER

The ADC filters perform true 24 bit signal processing to convert the raw multi-bit oversampled data from the ADC to the correct sampling frequency to be output on the digital audio interface. The digital filter path is illustrated in Figure 9.

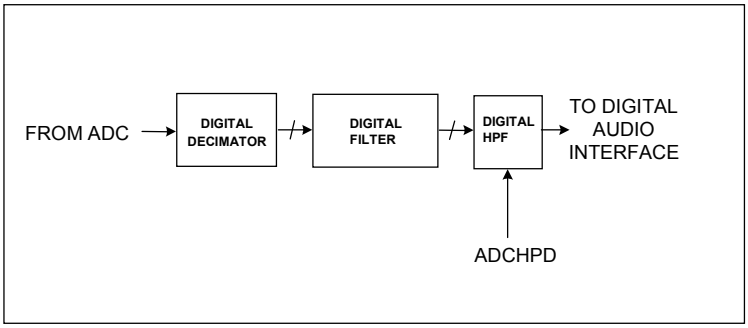


Figure 9 ADC Digital Filter

The ADC digital filters contain a digital high pass filter, selectable via software control. The high-pass filter response is detailed in the Digital Filter Characteristics section. When the high-pass filter is enabled the dc offset is continuously calculated and subtracted from the input signal. By setting HPOR, the last calculated dc offset value is stored when the high-pass filter is disabled and will continue to be subtracted from the input signal. If the DC offset is changed, the stored and subtracted value will not change unless the high-pass filter is enabled. This feature can be used for calibration purposes. In addition the highpass filter may be enabled separately on the left and right channels (see Table 11).

The output data format can be programmed by the user to accommodate stereo or monophonic recording on both inputs. The polarity of the output signal can also be changed under software control. The software control is shown in Table 10.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) ADC and DAC Control	6:5	ADCPOL [1:0]	00	00 = Polarity not inverted 01 = L polarity invert 10 = R polarity invert 11 = L and R polarity invert
	4	HPOR	0	Store dc offset when high-pass filter disabled 1 = store offset 0 = clear offset
	0	ADCHPD	0	ADC high-pass filter enable (Digital) HPFLREN = 0 1 = Disable high-pass filter on left and right channels 0 = Enable high-pass filter on left and right channels
				HPFLREN = 1 0 = High-pass enabled on left, disabled on right 1 = High-pass enabled on right, disabled on left
R27 (1Bh)	5	HPFLREN	0	ADC high-pass filter left or right enable 0 = High-pass filter enable/disable on left and right channels controlled by ADCHPD 1 = High-pass filter enabled on left or right channel, as selected by ADCHPD

Table 10 ADC Signal Path Control

HPFLREN	ADCHPD	HIGH PASS MODE
0	0	High-pass filter enabled on left and right channels
0	1	High-pass filter disabled on left and right channels
1	0	High-pass filter enabled on left channel, disabled on right channel
1	1	High-pass filter disabled on left channel, enabled on right channel

Table 11 ADC High Pass Filter Enable Modes

DIGITAL ADC VOLUME CONTROL

The output of the ADCs can be digitally amplified or attenuated over a range from –97dB to +30dB in 0.5dB steps. The volume of each channel can be controlled separately. The gain for a given eight-bit code X is given by:

$0.5 \times (X-195)$ dB for $1 \leq X \leq 255$; MUTE for X = 0

The LAVU and RAVU control bits control the loading of digital volume control data. When LAVU or RAVU are set to 0, the LADCVOL or RADCVOL control data will be loaded into the respective control register, but will not actually change the digital gain setting. Both left and right gain settings are updated when either LAVU or RAVU are set to 1. This makes it possible to update the gain of both channels simultaneously.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R21 (15h) Left ADC Digital Volume	8	LAVU	0	Left ADC Volume Update 0 = Store LADCVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LADCVOL, right = intermediate latch)
	7:0	LADCVOL [7:0]	11000011 (0dB)	Left ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -97dB 0000 0010 = -96.5dB ... 0.5dB steps up to 1111 1111 = +30dB
R22 (16h) Right ADC Digital Volume	8	RAVU	0	Right ADC Volume Update 0 = Store RADCVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = RADCVOL)
	7:0	RADCVOL [7:0]	11000011 (0dB)	Right ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -97dB 0000 0010 = -96.5dB ... 0.5dB steps up to 1111 1111 = +30dB

Table 12 ADC Digital Volume Control

AUTOMATIC LEVEL CONTROL (ALC)

The WM8750L has an automatic level control that aims to keep a constant recording volume irrespective of the input signal level. This is achieved by continuously adjusting the PGA gain so that the signal level at the ADC input remains constant. A digital peak detector monitors the ADC output and changes the PGA gain if necessary. Note that when the ALC function is enabled, the settings of registers 0 and 1 (LINVOL, LIVU, LIZC, LINMUTE, RINVOL, RIVU, RIZC and RINMUTE) are ignored.

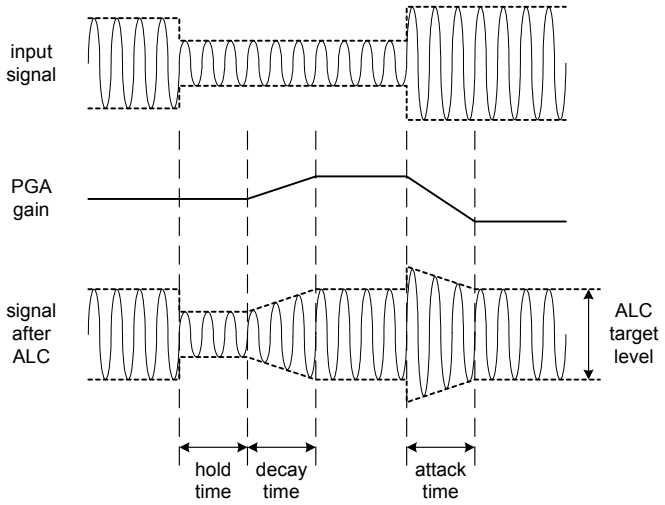


Figure 10 ALC Operation

The ALC function is enabled using the ALCSEL control bits. When enabled, the recording volume can be programmed between –6dB and –28.5dB (relative to ADC full scale) using the ALCL register bits. An upper limit for the PGA gain can be imposed by setting the MAXGAIN control bits.

HLD, DCY and ATK control the hold, decay and attack times, respectively:

Hold time is the time delay between the peak level detected being below target and the PGA gain beginning to ramp up. It can be programmed in power-of-two (2^n) steps, e.g. 2.67ms, 5.33ms, 10.67ms etc. up to 43.7s. Alternatively, the hold time can also be set to zero. The hold time only applies to gain ramp-up, there is no delay before ramping the gain down when the signal level is above target.

Decay (Gain Ramp-Up) Time is the time that it takes for the PGA gain to ramp up across 90% of its range (e.g. from –15B up to 27.75dB). The time it takes for the recording level to return to its target value therefore depends on both the decay time and on the gain adjustment required. If the gain adjustment is small, it will be shorter than the decay time. The decay time can be programmed in power-of-two (2^n) steps, from 24ms, 48ms, 96ms, etc. to 24.58s.

Attack (Gain Ramp-Down) Time is the time that it takes for the PGA gain to ramp down across 90% of its range (e.g. from 27.75dB down to -15B gain). The time it takes for the recording level to return to its target value therefore depends on both the attack time and on the gain adjustment required. If the gain adjustment is small, it will be shorter than the attack time. The attack time can be programmed in power-of-two (2^n) steps, from 6ms, 12ms, 24ms, etc. to 6.14s.

When operating in stereo, the peak detector takes the maximum of left and right channel peak values, and any new gain setting is applied to both left and right PGAs, so that the stereo image is preserved. However, the ALC function can also be enabled on one channel only. In this case, only one PGA is controlled by the ALC mechanism, while the other channel runs independently with its PGA gain set through the control register.

When one ADC channel is unused or used for DC measurement, the peak detector disregards that channel. The ALC function can also operate when the two ADC outputs are mixed to mono in the digital domain, but not if they are mixed to mono in the analogue domain, before entering the ADCs.