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WM8753L

Hi-Fi and Telephony Dual CODEC

DESCRIPTION

The WM8753L is a low power, high quality stereo CODEC with integrated Voice CODEC designed for portable digital telephony applications such as mobile phone, or headset with hi-fi playback capability.

The device integrates dual interfaces to two differentially connected microphones, and includes drivers for speakers, headphone and earpiece. External component requirements are reduced as no separate microphone or headphone amplifiers are required, and Cap-less connections can be made to all loads. Advanced on-chip digital signal processing performs tone control, Bass Boost and automatic level control for the microphone or line input through the ADC. The two ADCs may be used to support Voice noise cancellation in a partnering DSP, or for stereo recording.

The WM8753L hi-fi DAC can operate as a master or a slave, with various master clock frequencies including 12 or 24MHz for USB devices, 13MHz or 19.2MHz for cellular systems, or standard 256fs rates like 12.288MHz and 24.576MHz. Internal PLLs generate all required clocks for both Voice and hi-fi converters. If audio system clocks already exist, the PLLs may be committed to alternative uses.

The WM8753L operates at a nominal supply voltage of 2V, although the digital core can operate at voltages down to 1.42V to save power, and the maximum for all supplies is 3.6 Volts. Different sections of the chip can also be powered down under software control.

FEATURES

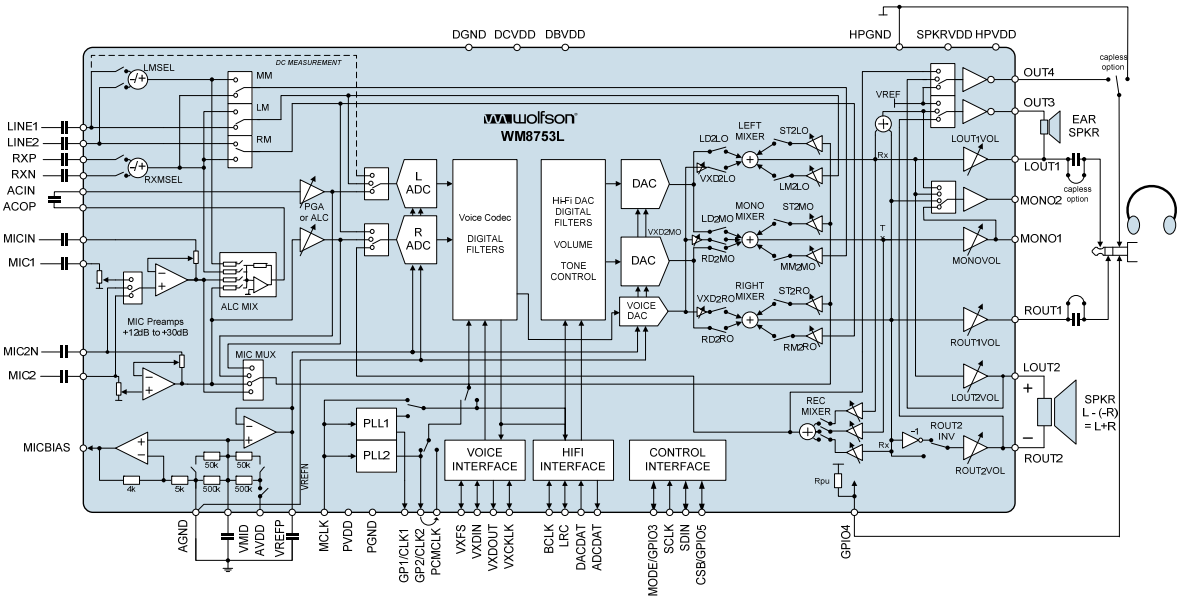
- **Hi-fi DAC:** interfaced over I^2S type link
- Audio sample rates:
  8, 11.025, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96
- DAC SNR 98dB, THD -84dB ('A' weighted @ 48kHz)
- ADC SNR 95dB, THD -82dB ('A' weighted @ 48kHz)
- On-chip Headphone Driver with cap-less output option
  - 40mW output power on 16Ω / 3.3V
  - with 16Ω load: SNR 90dB, THD –75dB
  - with 10kΩ load: SNR 94dB, THD –90dB
- On-chip speaker driver with 0.5W into 8R
- **Voice CODEC:** interfaced over Voice interface
- supports sample rates from 8ks/s to 48ks/s
- ADC and DAC SNR 82dB, THD -74dB
- Two Differential Microphone Interfaces
  - Dual ADCs support noise cancellation in external DSP
  - Programmable ALC / Noise Gate
- Low-noise bias supplied for electret microphones

Other Features

- On-chip PLLs supporting 12, 13, 19.2MHz and other clocks
- Cap-less connection options to headphones, earpiece, spkr.
- Low power, low voltage
  - 1.8V to 3.6V (digital core: 1.42V to 3.6V)
  - power consumption <20mW all-on with 2V supplies
  - <12mW for PCM CODEC operation
- 7x7x0.9mm QFN package

APPLICATIONS

- MP3 Player / Recorder mobile phone
- Bluetooth stereo headset



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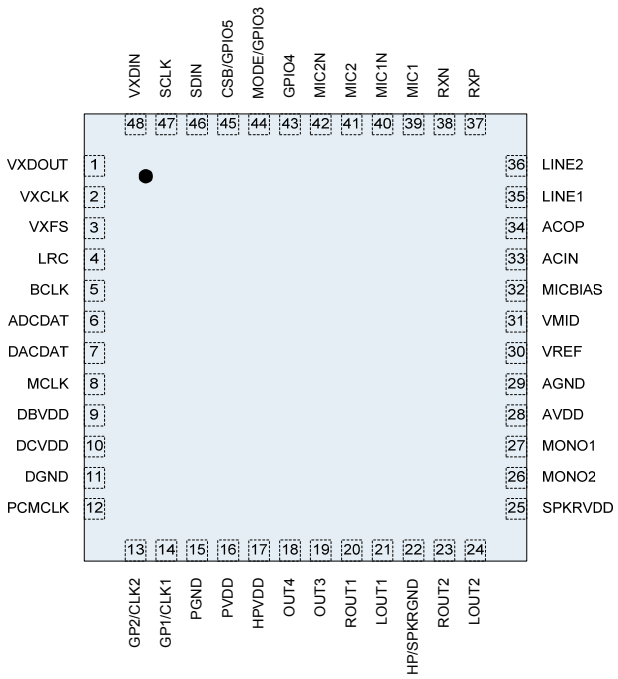
PIN CONFIGURATION



(TOP VIEW)

ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8753CLGEFL/V	-25°C to +85°C	48-lead QFN (7x7x0.9mm) (Pb-free)	MSL3	260°C
WM8753CLGEFL/RV	-25°C to +85°C	48-lead QFN (7x7x0.9mm) (Pb-free, tape and reel)	MSL3	260°C

Note:
Reel quantity = 2,200

PIN DESCRIPTION

QFN	NAME	TYPE	DESCRIPTION
1	VXDOUT	Digital Output	Voice ADC Output
2	VXCLK	Digital Input/Output	Voice CODEC data clock / ADC frame clock
3	VXFS	Digital Input/Output	Voice CODEC Frame Sync
4	LRC	Digital Input/Output	DAC Frame Sync
5	BCLK	Digital Input/Output	DAC data clock input / output
6	ADCDAT	Digital Output	ADC Digital Audio Data Alternative Output
7	DACDAT	Digital Input	DAC Digital Audio Data Input
8	MCLK	Digital Input	Master Clock Input
9	DBVDD	Supply	Digital Buffer Supply (supply for digital I/O buffers)
10	DCVDD	Supply	Digital Core Supply (supply for digital logic, except I/O buffers)
11	DGND	Supply	Digital ground (all digital logic)
12	PCMCLK	Digital Input	VOICE CODEC master clock input (may be looped from PLL output)
13	GP2/CLK2	Digital Output	General Purpose Output 2, usually PLL2 output
14	GP1/CLK1	Digital Output	General Purpose Output 1, usually PLL1 output
15	PGND	Supply	PLL ground
16	PVDD	Supply	PLL Supply
17	HPVDD	Supply	Headphone Supply
18	OUT4	Analogue Output	Analogue Output 4 (Headphone driver)
19	OUT3	Analogue Output	Analogue Output 3 (Headphone driver)
20	ROUT1	Analogue Output	Headphone Output Right
21	LOUT1	Analogue Output	Headphone Output Left
22	HP/SPKRGND	Supply	Headphone and Speaker ground
23	ROUT2	Analogue Output	Speaker Output Right
24	LOUT2	Analogue Output	Speaker Output Left
25	SPKRVDD	Supply	Speaker Supply
26	MONO2	Analogue Output	Mono analogue output 2
27	MONO1	Analogue Output	Mono analogue output 1
28	AVDD	Supply	Analogue supply (feeds ADC and DAC)
29	AGND	Supply	Analogue ground (feeds ADC and DAC)
30	VREF	Reference	Buffered ADC and DAC Reference voltage
31	VMID	Reference	Decoupling for ADC and DAC reference voltage
32	MICBIAS	Analogue Output	Microphone Bias
33	ACIN	Analogue Input	AC coupled input to ALC PGA in record path
34	ACOP	Analogue Output	ALC Mix output
35	LINE1	Analogue Input	Left Channel Input
36	LINE2	Analogue Input	Right Channel input
37	RXP	Analogue Input	RX mono differential input positive signal
38	RXN	Analogue Input	RX mono differential input negative signal
39	MIC1	Analogue Input	Mic Pre-amp input 1
40	MIC1N	Analogue Input	Mic Pre-amp 1 common mode or negative input
41	MIC2	Analogue Input	Mic Pre-amp input 2
42	MIC2N	Analogue Input	Mic Pre-amp 2 common mode or negative input
43	GPIO4	Digital input/Output	GPIO (General Purpose input/output) usually headphone jack insert autodetect with selectable pull-up/pull-down.
44	MODE/GPIO3	Digital Input / Output	Control interface Mode select on reset or GPIO3
45	CSB/GPIO5	Digital Input / Output	3-wire MPU Chip Select / 2-wire MPU interface address selection or GPIO5
46	SDIN	Digital Input / Output	3-wire MPU Data Input / 2-wire MPU Date Input / Acknowledge
47	SCLK	Digital Input	3-wire MPU Clock Input / 2-wire MPU Clock Input
48	VXDIN	Digital Input	VOICE DAC Input

Note: 1. It is recommended that the QFN ground paddle is connected to analogue ground on the application PCB

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages	-0.3V	+4.5V
Voltage range digital inputs	DGND - 0.3V	DVDD + 0.3V
Voltage range analogue inputs	AGND - 0.3V	AVDD + 0.3V
Operating temperature range, T_A	-25°C	+85°C
Storage temperature after soldering	-65°C	+150°C

Notes:

1. Analogue, PLL and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other.
3. DCVDD must be less than or equal to AVDD.
4. DCVDD must be less than or equal to DBVDD

SIMULATED THERMAL PROPERTIES

POWER INPUT (WATTS)	THETA Ja (^{O}C/W)	THETA Jc (^{O}C/W)	Tj (^{O}C)	Tc(^{O}C)
1 Watt	48.8	17.4	73.8	26.5
0.5 Watt	48.9	18.2	49.4	25.7

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD		1.42		3.6	V
Digital supply range (Buffer)	DBVDD		1.8		3.6	V
Analogue supplies range	AVDD		1.8		3.6	V
PLL supplies range	PLLVDD		1.8		3.6	V
Ground	DGND,AGND,PLLGND, HP/SPKRGND			0		V

ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD = 1.5V, AVDD = HPVDD = DBVDD = SPKRVDD = PLLVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (LINE1, LINE2, RXP, RXN)						
Full-scale Input Signal Level (0dB) – note this changes with AVDD	V_{INFS}			1.0		Vrms
Input Capacitance	$C_{LINE1/2,}$ RXP/N			10		pF
Microphone Preamp Inputs (MIC1, MIC1N, MIC2, MIC2N)						
Full-scale Input Signal Level (0dB) – note this changes with AVDD	V_{INFS}			177 -12		mVrms dBV
Mic preamp gain range			12		30	dB
Input resistance	$R_{MIC1N,}$ R_{MIC2N}	Gain set to 30dB		5		kΩ
Input resistance	$R_{MIC1N,}$ R_{MIC2N}	Gain set to 24dB		10		kΩ
Input resistance	$R_{MIC1N,}$ R_{MIC2N}	Gain set to 18dB		18		kΩ
Input resistance	$R_{MIC1N,}$ R_{MIC2N}	Gain set to 12dB		33		kΩ
Input resistance	$R_{MIC1,}$ R_{MIC2}			163		kΩ
Recommended decoupling cap	C_{DECOUP}			0.33		uF
Input Capacitance	C_{MICIN}			10		pF
Programmable Gain Amplifier (PGA)						
Programmable Gain			-17.25		30	dB
Programmable Gain Step Size		Guaranteed Monotonic		0.75		dB
Mute Attenuation				100		dB
Automatic Level Control (ALC)						
Target Record Level			-28.5		-6	dB
Gain Hold Time (Note 1)	t_{HOLD}	MCLK = 12.288MHz (Note 3)	0, 2.67, 5.33, 10.67, … , 43691 (time doubles with each step)			ms
Gain Ramp-Up (Decay) Time (Note2)	t_{DCY}		24, 48, 96, … , 2458 (time doubles with each step)			ms
Gain Ramp-Down (Attack) Time (Note 2)	t_{ATK}		6, 12, 24, … , 6140 (time doubles with each step)			ms
LINE1/2 to Analogue to Digital Converter (ADC)						
Signal to Noise Ratio (Note 4, 5)		A-weighted, 0dB gain	80	90		dB
Total Harmonic Distortion (Note 6)		full-scale, 0dB gain		-82		dB
Channel Separation (Note 7)		1kHz input signal		90		dB
LINE1/2 to Voice Analogue to Digital Converter (ADC), fs = 8kHz						
Signal to Noise Ratio (Note 4, 5)		A-weighted, 0dB gain		82		dB
Total Harmonic Distortion (Note 6)		full-scale, 0dB gain		-74		dB
Channel Separation (Note 7)		1kHz input signal		90		dB
Digital to Analogue Converter (DAC) to Lineout (LOUT1, ROUT1, MONO1, MONO2 with 10kΩ / 50pF load)						
Signal to Noise Ratio (A-weighted)	SNR	A-weighted	90	98		dB
Total Harmonic Distortion (Note 6)	THD	R_L = 10 kΩ full-scale signal		-85	-80	dB
Digital to Analogue Converter (DAC) to Lineout (LOUT2, ROUT2, OUT3, OUT4 with 10kΩ / 50pF load)						
Signal to Noise Ratio (A-weighted)	SNR	A-weighted		98		dB
Total Harmonic Distortion (Note 6)	THD	R_L = 10 kΩ full-scale signal		-85		dB

Test Conditions

DCVDD = 1.5V, AVDD = HPVDD = DBVDD = SPKRVDD = PLLVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Voice Digital to Analogue Converter (DAC) to Lineout (LOUT1/2, ROUT1/2, MONO1, MONO2,OUT3 with 10kΩ / 50pF load), fs = 8kHz						
Signal to Noise Ratio (A-weighted)	SNR	A-weighted		82		dB
Input Resistance	$R_{LINE1/2}$	LINE1/2 input to output mixer, gain = +6dB	10			kΩ
	R_{RXP}		30			kΩ
	R_{RXN}		20			kΩ
Total Harmonic Distortion (Note 6)	THD	R_L = 10 kΩ full-scale signal		-74		dB
Tone Control						
Bass Boost			-6	0	+9	dB
Bass Boost Step Size				1.5dB		dB
Bass Filter Characteristic				2nd order		
Treble Boost			-6	0	+9	dB
Treble Boost Step Size				1.5dB		dB
Treble Filter Characteristic				2nd order		
Output Mixers (Left, Right and Mono mix)						
PGA gain range into mixer			-15		+6	dB
PGA gain step into mixer				3		dB
Analogue Outputs (L/ROUT1, L/ROUT2, MONO1)						
0dB full scale output voltage				AVDD/3.3		Vrms
Programmable Gain range		1kHz signal	-73		+6	dB
Programmable Gain step size		monotonic		1		dB
Mute Attenuation		1kHz, full scale signal		85		dB
Channel Separation				90		dB
Headphone Output (LOUT1/2, OUT3)						
Total Harmonic Distortion	THD	HPVDD=1.8V, R_L=32Ω Po = 5mW		0.013 -78		% dB
		HPVDD=1.8V, R_L=16Ω Po = 5mW		0.013 - 78		% dB
		HPVDD=3.3V, R_L=32Ω Po = 20mW		0.01 -80		% dB
		HPVDD=3.3V, R_L=16Ω Po = 20mW		0.01 -80	0.03 -70	% dB
Signal to Noise Ratio (A-weighted)	SNR	HPVDD = 3.3V	90	95		dB
		HPVDD = 1.8V		90		dB
Speaker Output (L/ROUT2)						
Total Harmonic Distortion	THD	Po=180mW, RL=8Ω, SPKRVDD=3.3V		-50 0.3		dB %
		Po=400mW, RL=8Ω, SPKRVDD=3.3V		-40 1		dB %
Signal to Noise Ratio (A-weighted)	SNR	SPKRVDD=3.3V, RL=8Ω		90		dB
		SPKRVDD=2.5V, RL=8Ω		90		dB

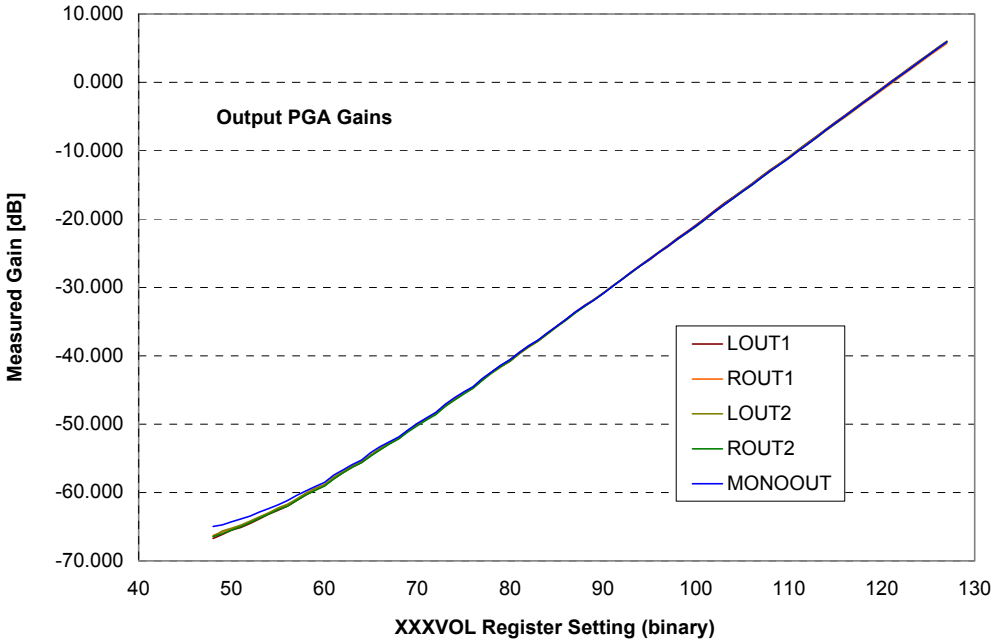
Test Conditions
DCVDD = 1.5V, AVDD = HPVDD = DBVDD = SPKRVDD = PLLVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

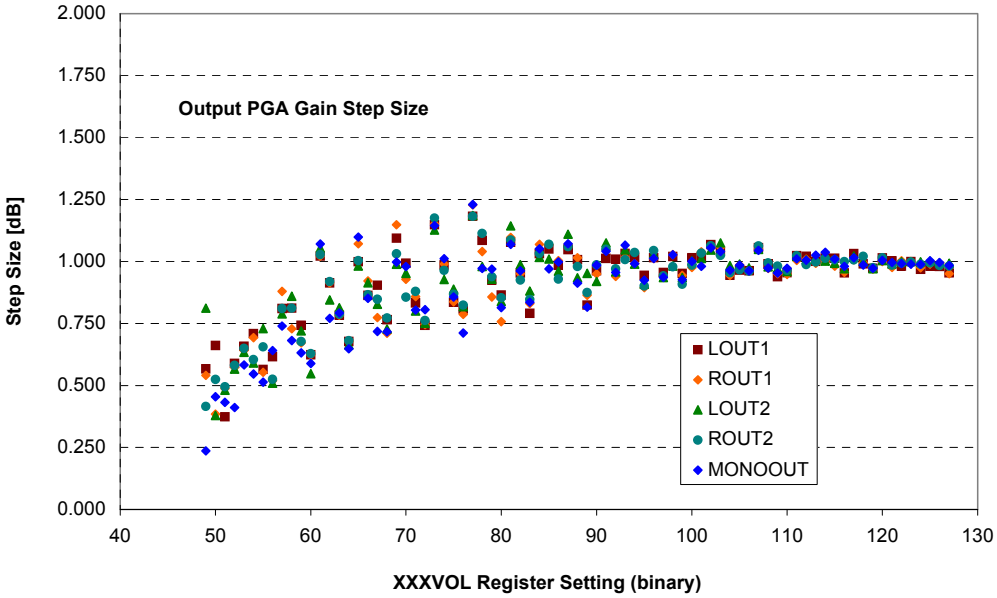
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Bias						
Bias Voltage (MBVSEL=0)	$V_{MICBIAS}$		-3%	0.9*AVDD	+3*%	V
Bias Voltage (MBVSEL=1)	$V_{MICBIAS}$		-3%	0.75*AVDD	+3*%	V
Bias Current Source	$I_{MICBIAS}$				3	mA
Output Noise Voltage	Vn	1K to 20kHz		15		nV/√Hz
Digital Input / Output (excluding GPIO4)						
Input HIGH Level	V_{IH}		0.7×DBVDD			V
Input LOW Level	V_{IL}				0.3×DBVDD	V
Output HIGH Level	V_{OH}	I_{OL}=1mA	0.9×DBVDD			V
Output LOW Level	V_{OL}	I_{OH}=-1mA			0.1×DBVDD	V
GPIO4 Input						
Input HIGH Level	V_{IH}		1.4			V
Input LOW Level	V_{IL}				0.8	V
Pullup/pulldown resistance	R_{IN}			100		kΩ

TERMINOLOGY

1. Hold Time is the length of time between a signal detected being too quiet and beginning to ramp up the gain. It does not apply to ramping down the gain when the signal is too loud, which happens without a delay.
2. Ramp-up and Ramp-Down times are defined as the time it takes for the PGA to sweep across 90% of its gain range.
3. All hold, ramp-up and ramp-down times scale proportionally with MCLK
4. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
5. Dynamic range (dB) - DR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
6. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
7. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.

OUTPUT PGA'S LINEARITY





POWER CONSUMPTION

The power consumption of the WM8753L depends on the following factors.

Supply voltages: Reducing the supply voltages also reduces supply currents, and therefore results in significant power savings.

Operating mode: Power consumption is lower in mono modes than in stereo, as one ADC / DAC / PGA is switched OFF. It is also reduced when the device is used for playback only (ADC off) or for recording only (DAC off). Unused outputs should be switched off (for example, when line out is not used, do not enable the LINE outputs).

Headphone volume: At high volume, the power dissipated in the headphone itself is greater than the power consumption of the WM8753L. High headphone volume also increases the power consumption of the on-chip headphone drivers.

	AVDD (V)	I_{AVDD} (mA)	DCVDD (V)	I_{DCVDD} (mA)	DBVDD (V)	I_{DBVDD} (mA)	HPVDD (V)	I_{HPVDD} (mA)	SPKVDD (V)	I_{SPKVDD} (mA)	PLLVDD (V)	I_{PLLVDD} (mA)	Total Power (mW)
Off	3.3	0.018	1.8	0.007	3.3	0	3.3	0	3.3	0	3.3	0	0.07
	3.3	0.018	2.7	0.009	2.7	0	3.3	0	3.3	0	2.7	0	0.08
	1.8	0.007	1.8	0.007	1.8	0	1.8	0	3.3	0	1.8	0	0.03
Off with temp sensor disabled	3.3	0	1.8	0.007	3.3	0	3.3	0	3.3	0	3.3	0	0.01
	3.3	0	2.7	0.009	2.7	0	3.3	0	3.3	0	2.7	0	0.02
	1.8	0	1.8	0.007	1.8	0	1.8	0	3.3	0	1.8	0	0.01
Standby (500k VMID, no clocks, temp sensor off)	3.3	0.004	1.8	0.007	3.3	0	3.3	0	3.3	0	3.3	0	0.03
	3.3	0.004	2.7	0.009	2.7	0	3.3	0	3.3	0	2.7	0	0.04
	1.8	0.002	1.8	0.007	1.8	0	1.8	0	3.3	0	1.8	0	0.02
Stereo 16R HP playback 44.100k, MCLK=13MHz, PLL enabled, quiescent	3.3	4.38	1.8	2.9	3.3	1.54	3.3	0	3.3	0.007	3.3	1	28.08
	3.3	4.38	1.8	2.9	1.8	0.8	3.3	0	3.3	0.007	3.3	1	24.44
	2.7	3.48	1.8	2.87	1.8	0.8	2.7	0.52	3.3	0.006	2.7	0.84	19.69
	1.8	2.22	1.5	2.35	1.8	0.8	1.8	0.31	3.3	0.004	1.8	0.64	10.68
Stereo 16R HP playback 44.100k, MCLK=13MHz, PLL enabled, 100mVrms	3.3	4.34	1.8	2.9	3.3	1.54	3.3	5.3	3.3	0.007	3.3	1	45.44
	3.3	4.33	1.8	2.9	1.8	0.8	3.3	5.44	3.3	0.007	3.3	1	42.22
	2.7	3.48	1.8	2.85	1.8	0.8	2.7	5.28	3.3	0.006	2.7	0.84	32.51
	1.8	2.22	1.5	2.36	1.8	0.8	1.8	5.33	3.3	0.004	1.8	0.64	19.74
Stereo 16R HP playback 44.100k, MCLK=256fs, quiescent	3.3	4.35	1.8	2.43	3.3	0.062	3.3	0.68	3.3	0.007	3.3	0.09	21.50
	3.3	4.33	1.8	2.42	1.8	0.004	3.3	0.68	3.3	0.007	3.3	0.09	21.22
	2.7	3.48	1.8	2.42	1.8	0.004	2.7	0.52	3.3	0.005	2.7	0.071	15.37
	1.8	2.23	1.5	1.97	1.8	0.004	1.8	0.31	3.3	0.004	1.8	0.044	7.63
Stereo 16R HP playback 44.100k, MCLK=256fs, 100mVrms	3.3	4.35	1.8	2.43	3.3	0.062	3.3	5.14	3.3	0.007	3.3	0.09	36.22
	3.3	4.33	1.8	2.42	1.8	0.004	3.3	5.45	3.3	0.007	3.3	0.09	36.96
	2.7	3.46	1.8	2.42	1.8	0.004	2.7	5.46	3.3	0.005	2.7	0.07	28.65
	1.8	2.23	1.5	1.97	1.8	0.004	1.8	5.18	3.3	0.004	1.8	0.044	16.39
Stereo 16R HP playback 44.100k, MCLK=256fs, 565mVrms = 20mW	3.3	4.35	1.8	2.43	3.3	0.062	3.3	29	3.3	0.007	3.3	0.09	114.95
Stereo 16R HP playback 44.100k, MCLK=256fs, 565mVrms = 20mW	3.3	4.34	1.8	2.46	1.8	0.004	3.3	29	3.3	0.007	3.3	0.09	114.78
Stereo 16R HP playback 44.100k, MCLK=256fs, 462mVrms = 13.3mW	2.7	3.48	1.8	2.46	1.8	0.004	2.7	19.5	3.3	0.005	2.7	0.071	66.69
Stereo 16R HP playback 44.100k, MCLK=256fs, 308mVrms = 5.9mW	1.8	2.25	1.5	2.03	1.8	0.004	1.8	8.8	3.3	0.004	1.8	0.044	23.03
PCM voice call (Right ADC, diff rec from mic2, VDAC playback to 16R, 64x OSR, 8kHz, MCLK=256fs)	3.3	5.18	1.8	0.63	3.3	0.094	3.3	5.27	3.3	0.007	3.3	0.016	36.01
	3.3	5.18	1.8	0.63	1.8	0.004	3.3	5.27	3.3	0.007	3.3	0.016	35.70
	2.7	4.4	1.8	0.63	1.8	0.004	2.7	5.26	3.3	0.006	2.7	0.013	27.28
	1.8	3.15	1.5	0.5	1.8	0.004	1.8	5	3.3	0.004	1.8	0.008	15.45

Table 1 Power Consumption Figures

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

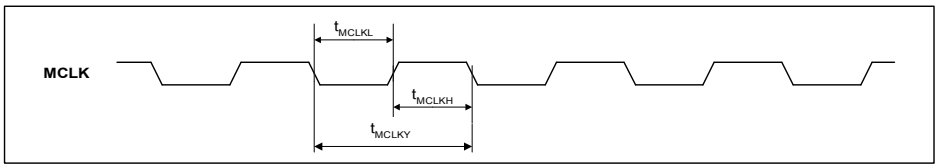


Figure 1 System Clock Timing Requirements

Test Conditions

CLKDIV2=0, DCVDD = 1.42V, DBVDD = AVDD = SPKRVDD = PLLVDD = 3.3V, DGND = AGND = PLLGND = 0V, T_A = +25°C, Slave Mode fs = 48kHz, MCLK = 384fs, 24-bit data, unless otherwise stated.

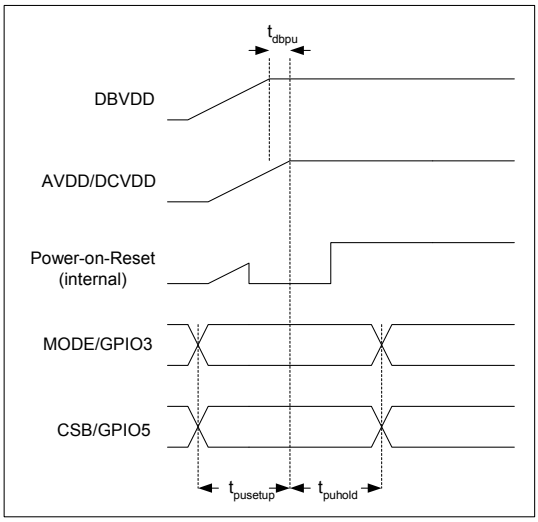
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
System Clock Timing Information					
MCLK System clock cycle time	T_{MCLKY}	54			ns
MCLK duty cycle	T_{MCLKDS}	60:40		40:60	

Test Conditions

CLKDIV2=1, DCVDD = 1.42V, DBVDD = AVDD = SPKRVDD = PLLVDD = 3.3V, DGND = AGND = PLLGND = 0V, T_A = +25°C, Slave Mode fs = 48kHz, MCLK = 384fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
System Clock Timing Information					
MCLK System clock pulse width high	T_{MCLKL}	10			ns
MCLK System clock pulse width low	T_{MCLKH}	10			ns
MCLK System clock cycle time	T_{MCLKY}	27			ns

MODE/GPIO3 AND CSB/GPIO5 LATCH ON POWERUP TIMING



Test Conditions

DCVDD = 1.42V, DBVDD = AVDD = SPKRVDD = PLLVDD = 3.3V, DGND = AGND = PLLGND = 0V, T_A = +25°C, Slave Mode fs = 48kHz, MCLK = 384fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
System Clock Timing Information					
MODE/GPIO3 and CSB/GPIO5 to AVDD and DCVDD power-up setup time	$t_{pusetup}$	100			us
AVDD and DCVDD to MODE/GPIO3 and CSB/GPIO5 hold time	t_{puhold}	1			ms
DBVDD powerup to DCVDD or AVDD powerup	t_{dbpu}	0			us

Note:

1. DBVDD must be supplied before or at same time as either DCVDD or AVDD to ensure MODE and CSB are defined internally when power on reset is released

AUDIO INTERFACE TIMING – MASTER MODE

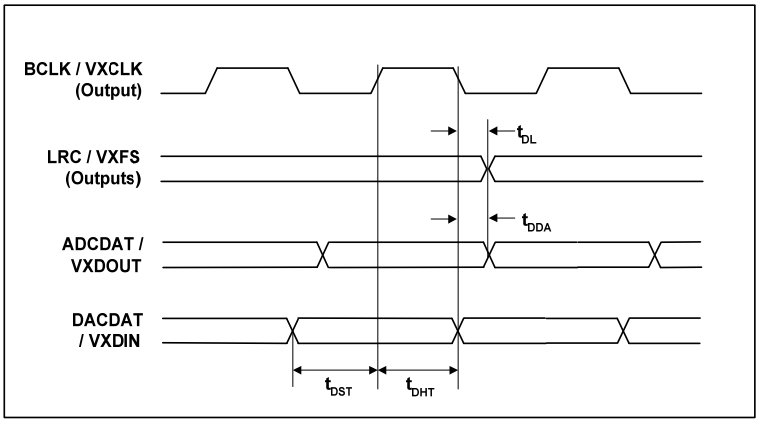


Figure 2 Digital Audio Data Timing – Master Mode (see Control Interface)

Test Conditions

DCVDD = 1.42V, DBVDD = AVDD = HPVDD = SPKRVDD = PLLVDD = 3.3V, DGND = AGND = PLLGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
LRC / VXFS propagation delay from BCLK / VXCLK falling edge	t_{DL}			10	ns
ADCDAT / VXDOUT propagation delay from BCLK / VXCLK falling edge	t_{DDA}			10	ns
DACDAT / VXDIN setup time to BCLK / VXCLK rising edge	t_{DST}	10			ns
DACDAT / VXDIN hold time from BCLK / VXCLK rising edge	t_{DHT}	10			ns

AUDIO INTERFACE TIMING – SLAVE MODE

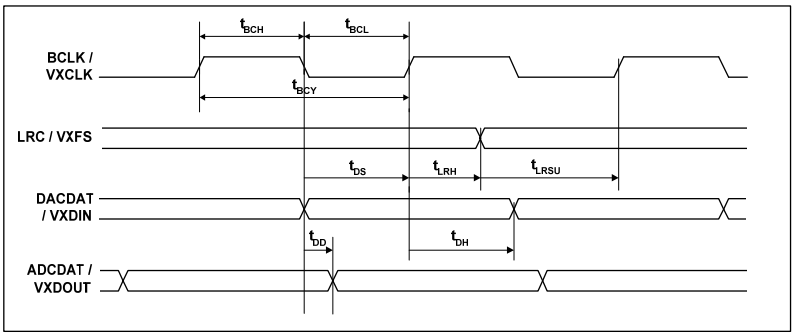


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

DCVDD = 1.42V, DBVDD = AVDD = HPVDD = SPKRVDD = PLLVDD = 3.3V, DGND = AGND = PLLGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK / VXCLK cycle time	t_{BCY}	50			ns
BCLK / VXCLK pulse width high	t_{BCH}	20			ns
BCLK / VXCLK pulse width low	t_{BCL}	20			ns
LRC / VXFS set-up time to BCLK / VXCLK rising edge	t_{LRSU}	10			ns
LRC / VXFS hold time from BCLK / VXCLK rising edge	t_{LRH}	10			ns
DACDAT / VXDIN hold time from BCLK / VXCLK rising edge	t_{DH}	10			ns
ADCDAT / VXDOUT propagation delay from BCLK / VXCLK falling edge	t_{DD}			10	ns

Note:

1. BCLK / VXCLK period should always be greater than or equal to MCLK / VXCLK period.

CONTROL INTERFACE TIMING – 3-WIRE MODE

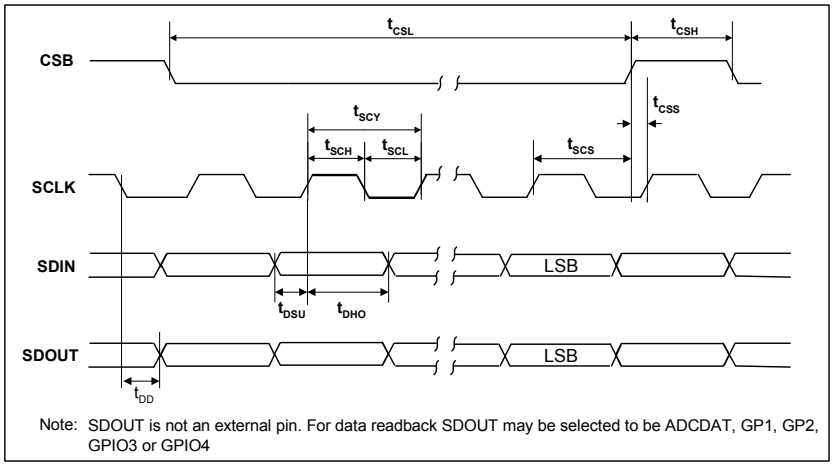


Figure 4 Control Interface Timing – 3-Wire Serial Control Mode

Test Conditions

DCVDD = 1.42V, DBVDD = AVDD = HPVDD = SPKRVDD = PLLVDD = 3.3V, DGND = AGND = PLLGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB rising edge	t_{SCS}	80			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDIN to SCLK set-up time	t_{DSU}	40			ns
SCLK to SDIN hold time	t_{DHO}	40			ns
CSB pulse width low	t_{CSL}	40			ns
CSB pulse width high	t_{CSH}	40			ns
CSB rising to SCLK rising	t_{CSS}	40			ns
SCLK falling to SDOUT propagation delay	t_{DD}			10	ns
Pulse width of spikes that will be suppressed	t_{ps}	5			ns

CONTROL INTERFACE TIMING – 2-WIRE MODE

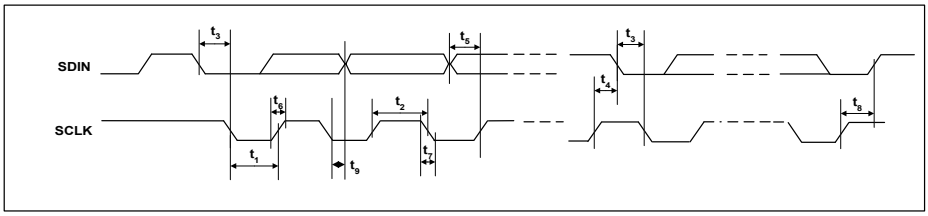


Figure 5 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DCVDD = 1.42V, DBVDD = AVDD = HPVDD = SPKRVDD = PLLVDD = 3.3V, DGND = AGND = PLLGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency		0		526	kHz
SCLK Low Pulse-Width	t_1	1.3			us
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDIN, SCLK Rise Time	t_6			300	ns
SDIN, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

INTERNAL POWER ON RESET CIRCUIT

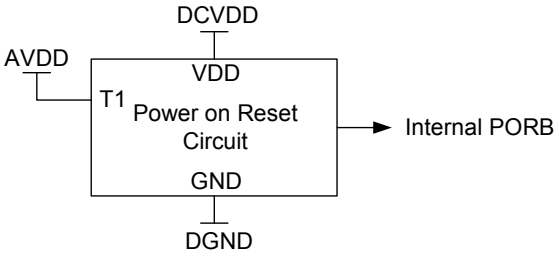


Figure 6 Internal Power on Reset Circuit Schematic

The WM8753 includes an internal Power-On-Reset Circuit, as shown in Figure 6, which is used to reset the digital logic into a default state after power up. The power on reset circuit is powered from DCVDD and monitors DCVDD and AVDD. It asserts PORB low if DCVDD or AVDD are below a minimum threshold.

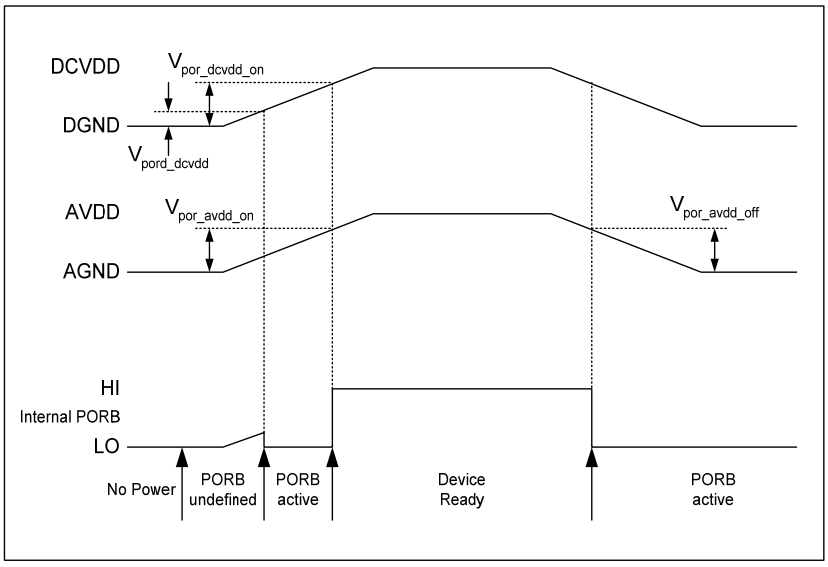


Figure 7 Typical Power-Up Sequence

Figure 7 shows a typical power-up sequence. When DCVDD and AVDD rise above the minimum thresholds, Vpord_dcvdd and Vpord_avdd, there is enough voltage for the circuit to guarantee the Power on Reset is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When DCVDD rises to Vpor_dcvdd_on and AVDD rises to Vpor_avdd_on, PORB is released high and all registers are in their default state and writes to the control interface may take place. If DCVDD and AVDD rise at different rates then PORB will only be released when DCVDD and AVDD have both exceeded the Vpor_dcvdd_on and Vpor_avdd_on thresholds.

On power down, PORB is asserted low whenever DCVDD drops below the minimum threshold Vpor_dcvdd_off or AVDD drops below the minimum threshold Vpor_avdd_off.

SYMBOL	MIN	TYP	MAX	UNIT
V_{pord_dcvdd}	0.4	0.6	0.8	V
$V_{por\_dcvdd\_on}$	0.9	1.26	1.6	V
$V_{por\_avdd\_on}$	0.5	0.7	0.9	V
$V_{por\_avdd\_off}$	0.4	0.6	0.8	V

Table 2 Typical POR Operation (typical values, not tested)

DEVICE DESCRIPTION

INTRODUCTION

The WM8753L is a low power audio CODEC combining a high quality stereo audio DAC with a high quality stereo ADC and mono DAC. The stereo ADC may be configured for operation as a mono or stereo voice ADC to operate with the mono DAC as a voice CODEC. Alternatively the ADC may be configured as a hi-fi ADC for high quality record function. In voice mode the ADC filters are optimised for voice record function. Applications for such a combined device include MP3 playing 'smart-phones' and Bluetooth connected high quality stereo headsets. The mono voice CODEC might be used either for the usual voice CODEC function, or perhaps as an additional CODEC for support of Bluetooth links from such MP3 phones. Alternatively, if not required for such functions, the ADC of the CODEC may be reconfigured so it is clocked off the I^2S audio data interface domain, and its output sent over the hi-fi audio interface as well as the voice audio interface, so it might be used as a recording ADC in an I^2S based audio system.

FEATURES

The chip offers great flexibility in use, and so can support many different modes of operation as follows:

LINE INPUTS

The device includes two pairs of stereo analogue inputs that can be switched internally. LINE1 and LINE2 can be used as either a pair of mono line level inputs, or as a single stereo pair. They may also be used as differential input or be mixed together. A further two inputs, RXP and RXN, can be used as a single differential input or mixed together. The output from these inputs can be played back in stereo form to the headphones, or mono form to the transmit mono output. The mono output supports both single ended and differential output, using a pair of output pins. If not required, the differential output buffer may be powered down.

MICROPHONE INPUTS

Two microphone preamplifiers are provided, allowing for a pair of external microphones to be differentially connected, with user defined gain using internal resistors, offering gain range from +12dB to +30dB. Alternatively, three microphones can be connected to one microphone preamplifier, with the second preamplifier disabled, and the microphone required is then selected. A microphone bias is output from the chip which can be used to bias all microphones. The signal routing can be configured to allow manual adjustment of mic levels, or indeed to allow the ALC loop to control the level of mic signal that is transmitted.

PGA AND ALC OPERATION

A programmable gain amplifier is provided in the input path to the ADC. This may be used manually or in conjunction with a mixed analog/digital automatic level control (ALC) which keeps the recording volume constant.

HI-FI DAC

The hi-fi DAC provides high quality audio playback suitable for all portable audio hi-fi type applications, including MP3 players and portable disc players of all types.

VOICE CODEC

The on-chip stereo ADC and mono DAC are of a high quality using a multi-bit high-order oversampling architecture to deliver optimum performance with low power consumption. Various sample rates are supported, from the 8ks/s rate typically used in voice CODECs, up to the 48ks/s rate used in high quality audio applications. The ADC digital filters may be switched for voice mode to filters with steeper roll-off.

OUTPUT MIXERS

Flexible mixing is provided on the outputs of the device; a stereo mixer is provided for the stereo headphone or line outputs, and an additional mono mixer for the mono output to the transmit side of the equipment. Gain adjustment capability, and signal switching is provided to allow for all possible signal combinations; eg. Sidetone, transmission of stereo music playback along with voice, whilst at the same time as listening to music, and receiving phone call if so desired. The output buffers can be configured in several ways, allowing support of up to three sets of external transducers; ie stereo headphone, BTL speaker, and BTL earpiece may be connected simultaneously. (thermal implications should be considered before simultaneous full power operation of all outputs is attempted!)

Alternatively, if a speaker output is not required, the LOUT2 and ROUT2 pins might be used as a stereo speaker or headphone driver, (disable output invert buffer on ROUT2). In that case either two sets of headphones might be driven, or the LOUT2 and ROUT2 pins used as a line output driver.

The Earpiece may be driven in BTL mode, with the ROUT1 signal inverted into the OUT3 pin, or alternatively OUT3 may be either the mono version of ROUT1 and LOUT1, or simply a buffered version of the chip midrail reference voltage. This voltage may then be used as a headphone 'pseudo ground' allowing removal of the large AC coupling capacitors often used in the output path.

AUDIO INTERFACES

The WM8753L has a pair of audio interfaces, to support the hi-fi DAC and the PCM CODEC. The hi-fi DAC is supported with a 4 wire standard audio DAC interface which supports a number of audio data formats including I^2S, DSP Mode (a burst mode in which frame sync plus 2 data packed words are transmitted), MSB-First, left justified and MSB-First, right justified, and can operate in master or slave modes.

The PCM CODEC is connected via standard PCM type interface, comprising a frame sync, FS, a bitclk VXCLK, (typically 16 clocks per frame), and a pair of data lines for DAC input and ADC output data. A master clock for the PCM CODEC (typically 256fs or 2.048MHz when running at 8ks/s) may also be supplied as an input, if the system controller can provide this, to PCMCLK input pin. In the event of the system controller not being able to provide this clock, it may be generated in the WM8753L using PLL2. Note that the MCLK input to the chip must be present for PLL2 to operate, as it is a digital PLL type of circuit and uses this high speed master clock.

In the event of the PCM CODEC not being required, (temporarily or otherwise) the ADC output data may be sent over the hi-fi audio interface using the ADCDAT line. In this case the ADC may be configured to run at the same sample rate as the hi-fi DAC and use the same clock signals (BCLK and LRC). It may also be configured to run at a different sample rate and instead use the FS and VXCLK as the ADC data frame sync and clock. Both interfaces may be configured to run in Master mode when LRC, BCLK, FS and VXCLK are outputs from the WM8753L. A mixed Master-Slave mode is also supported allowing BCLK / VXCLK to be outputs from the WM8753L and LRC / FS to be inputs.

CONTROL INTERFACES

To allow full software control over all its features, the WM8753L offers a choice of 2 or 3 wire MPU control interface. It is fully compatible and an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs.

Selection between the modes is via the MODE/GPIO3 pin. In 2 wire mode only slave operation is supported and the address of the device may be selected between two values using the CSB/GPIO5 pin. The interface mode and 2-wire address select are set on power-up by the sampling of the MODE/GPIO3 and CSB/GPIO5 pins by the power-on reset. This allows these pins to be used as GPIO pins after powerup.

CLOCKING SCHEMES

WM8753L offers the normal audio DAC clocking scheme operation, where 256 or 384fs or higher MCLK is provided to the DAC. Similarly the PCM CODEC can be operated in normal PCM type mode where a 256fs clock is sent along with the PCM frame clock and data.

However, a pair of PLLs are also included which may be used to generate these clocks in the event that they are not available from the system controller. The first PLL1 uses an input clock, typically the Rf reference clock used in most mobile systems, to generate high quality audio clocks. The second PLL2 can use this same reference clock. If these PLLs are not required for generation of these clocks, they can be reconfigured to generate alternative clocks which may then be output and used elsewhere in the system. The WM8753L can also generate standard audio clock rates from a 12 or 24MHz USB clock without the use of the PLLs.

POWER CONTROL

The design of the WM8753L has given much attention to power consumption without compromising performance. It operates at very low voltages, and includes the ability to power off any unused parts of the circuitry under software control, and includes standby and power off modes.

OPERATION SCENARIOS

Flexibility in the design of the WM8753L allows for a wide range of operational scenarios, some of which are proposed below:

Telephony with MP3 playback: The voice CODEC may be used as standard voice CODEC, and the stereo DAC used for MP3 type playback. The user may choose to transmit the mono version of the MP3 playback to the Tx side of the phone conversation as required. Recording of the phone conversation would then require to be supported in the digital domain, after the voice CODEC. (digital Tx and Rx sides of the conversation would need to be digitally summed as required).

Telephony with recording: In many smart-phone applications the voice CODEC for voice conversion will be included in the cellphone base-band chipset. In such cases the analogue (often differential) mic input and speaker outputs from this voice CODEC will be routed to the WM8753L line or mic inputs, and mono outputs. The WM8753L will then provide the buffers to connect to the system transducers (speakers, mics, headphones etc.) and also the stereo hi-fi DAC and mixers to allow MP3 type playback. The ADC may then be used for recording the phone conversation, both Tx and Rx parts, and the extra DAC might be used for generation of confirmation tones or ringtones as required.

Bluetooth hi-fi stereo headset; In Bluetooth headsets a mono PCM CODEC is required for the standard telephony quality voice channel. But for the support of compressed hi-fi quality stereo, a hi-fi quality stereo DAC is required. In this case WM8753L can supply both these needs. The BTL speaker driver could be recommitted as either stereo headphone driver, or stereo speaker driver, and perhaps the other headphone output re-used as stereo line output.

Analogue FM tuner support: An analogue stereo FM tuner might be connected to the Line inputs of WM8753, and the stereo signal listened to via headphones, or transmitted over the ‘phone.

INPUT SIGNAL PATH

The WM8753L has a combination of analogue inputs, microphone preamps, mixers and switches allowing flexibility in the configuration of the input to left and right ADCs and to analogue bypass paths into the Left, Right and Mono output Mixers. The input to the ADC may be routed through a PGA whose gain is controlled either by the user or by the on-chip ALC function (see Automatic Level Control). The ADCs may be powered off independently and a single ADC may be used for left and right ADC input mono mixing.

SIGNAL INPUTS

The WM8753L has three sets of high impedance, low capacitance AC coupled differential inputs as well as two high impedance, low capacitance AC coupled mono line inputs. Two of the differential inputs (MIC1N/MIC1N and MIC2N/MIC2N) have a microphone pre-amp and selectable gain of +12dB to +30dB in 6dB steps. RXN and RXP are a differential line input and can also be configured as a stereo to mono mix input. In addition there are two mono LINE inputs (LINE1 and LINE2) which can be used as a single stereo input.

The LINE1 and LINE2 inputs may be configured as a differential input or a stereo to mono mix using the Line input mixer under the control of register bits LMSEL. The LMSEL bits also allow either one of the inputs to be enabled and the other disabled. The Line mixer output may then be routed to the ALC mixer by setting LINEALC and/or to the output Mono mixer via the bypass path. The Line mixer has -6dB of gain so that a 0dB signal on LINE1 and LINE2 will sum to give a 0dB signal at the mixer output.

There is an analogue input to analogue output bypass path into the Left, Right and Mono output mixers. The Left bypass path may be selected to be either the output of the RX mixer or the LINE1 input under the control of LM. The Right bypass path may be selected to be either the output of the RX mixer or the LINE2 input under the control of RM. The Mono bypass path may be selected to be either the output of the Line mixer or the RX mixer under the control of MM.

RXN and RXP are inputs to a mixer controlled by the RXMSEL register bits. By default this is a differential input (RXP-RXN). The RX mixer can also be configured as a stereo to mono mix input (RXP+RXN). Alternatively RXP or RXN can be individually selected as mono inputs with the other input disabled. The RX mixer has -6dB of gain so that a 0dB signal on RXP and RXN will sum to give a 0dB signal at the mixer output.

In addition there is a Sidetone path from the Mic Mux to the left, right and mono mixers. This Sidetone path may be selected to be the output from the left or right ADC input PGA, the Mic1 preamp or the Mic2 preamp under the control of MICMUX[1:0].

The Left ADC input is selected using LADCSEL[1:0]. It can be selected to be i) a direct analogue input from LINE1 or the output of the RX mixer block; ii) through the input PGA and ALC mixer; iii) DC measurement input from LINE1. For direct analogue input the input may be selected from either LINE1 or the RX mixer using LM. The ALC mixer may be used to mix MIC1, MIC2, LINE and RX differential inputs, selected using MIC1ALC, MIC2ALC, LINEALC and RXALC.

The Right ADC input is selected using RADCSEL[1:0]. It can be selected to be i) a direct analogue input from LINE2 or the RX mixer input; ii) through the input PGA from the MIC2 preamp; iii) Record mixer output. For direct analogue input the input may be selected from either LINE2 or the RX mixer using RM. The Record mixer may be used to mix the output from the left, right and mono output mixers, e.g. for recording a phone call. The inputs to the Record mixer are selected using LSEL, RSEL and MSEL and have independent input gain control from -15dB to +6dB.

The input to the Left ADC PGA via the external dc blocking capacitor is from the output of the ALC mixer, which allows the mixing of the output from the Line mixer, the RX mixer, the Mic1 preamp and the Mic2 preamp under the control of LINEALC, RXALC, MIC1ALC and MIC2ALC.

The signal inputs are biased internally to the reference voltage VREF. Whenever the analogue inputs are muted or the device placed into standby mode, the inputs are kept biased to VREF using special anti-thump circuitry. This reduces any audible clicks that may otherwise be heard when changing inputs.

DC MEASUREMENT

For DC measurements (for example, battery voltage monitoring), the input signal at the LINE1 input can be taken directly into the left ADC, bypassing the PGA. The ADC output then becomes unsigned relative to AVDD, instead of being a signed (two's complement) number relative to VREF. The input range for dc measurement is AGND to AVDD. The ADC high pass filter should be disabled when measuring DC voltages.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R46 (2Eh) ADC input Mode	[3:2]	RADCSEL[1:0]	00	Right ADC Input Select 00 : PGA 01 : LINE2 or RXP-RXN 10 : Left + Right + Mono output Mix 11 : unused
	[1:0]	LADCSEL[1:0]	00	Left ADC Input Select 00 : PGA 01 : LINE1 or RXP-RXN 10 : LINE1 DC measurement 11 : unused

Table 3 ADC Input Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R47 (2Fh) Input Control (1)	[4:3]	LMSEL[1:0]	00	Line Mix Select: 00: LINE1 + LINE2 01: LINE1 – LINE2 10: LINE1 (LINE2 disconnected) 11: LINE2 (LINE1 disconnected)
	2	MM	0	Mono Mux Select 0 : Line Mix Output 1: Rx Mix output (RXP +/– RXN)
	1	RM	0	Right Mux Select 0 : LINE2 1 : Rx Mix output (RXP +/– RXN)
	0	LM	0	Left Mux Select 0 : LINE1 1 : Rx Mix output (RXP +/– RXN)

Table 4 Input and Bypass Mux Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R48 (30h) Input Control (2)	[7:6]	RXMSEL[1:0]	00	Differential input, Rx, mixer 00: RXP – RXN 01: RXP + RXN 10: RXP (RXN disconnected) 11: RXN (RXP disconnected)
	[5:4]	MICMUX[1:0]	00	Mic Mux Sidetone Select 00 : Sidetone = Left PGA output 01 : Sidetone = Mic 1 preamp output 10 : Sidetone = Mic 2 preamp output 11 : Sidetone = Right PGA output
	3	LINEALC	0	ALC Mix input select Line Mix 0 : Line Mix not selected into ALC Mix 1 : Line Mix selected into ALC Mix
	2	MIC2ALC	0	ALC Mix input select MIC2 0 : MIC2 not selected into ALC Mix 1 : MIC2 selected into ALC Mix
	1	MIC1ALC	0	ALC Mix input select MIC1 0 : MIC1 not selected into ALC Mix 1 : MIC1 selected into ALC Mix
	0	RXALC	0	ALC Mix input select RX 0 : RX not selected into ALC Mix 1 : RX selected into ALC Mix

Table 5 ALC Mix and Mic Mux Input Select

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (20h) Record Mix (1)	7	RSEL	0	Record Mixer Select Right Mix 0 : Right Mix not selected into Record mixer 1 : Right mix selected into Record mixer
	6:4	RRECVOL [2:0]	101 (-9dB)	Right mixer signal to Record mixer Volume 000 = +6dB … (3dB steps) 111 = -15dB
	3	LSEL	0	Record Mixer Select Left Mix 0 : Left Mix not selected into Record mixer 1 : Left mix selected into Record mixer
	2:0	LRECVOL[2:0]	101 (-9dB)	Left mixer signal to Record mixer Volume 000 = +6dB … (3dB steps) 111 = -15dB
R33 (21h) Record Mix (2)	3	MSEL	0	Record Mixer Select Mono Mix 0 : Mono Mix not selected into Record mixer 1 : Mono mix selected into Record mixer
	2:0	MRECVOL [2:0]	101 (-9dB)	Mono mixer signal to Record mixer Volume 000 = +6dB … (3dB steps) 111 = -15dB

Table 6 Record Mixer Input Select and Gain Control

MONO MIXING

The stereo ADC can operate as a stereo or mono device, or the two channels can be mixed to mono, either in the analogue domain (in the front end of the ADC) or in the digital domain (after the ADC). MONOMIX selects the mode of operation. For analogue mono mix either the left or right channel ADC can be used, allowing the unused ADC to be powered off or used for a dc measurement conversion. The user also has the flexibility to select the data output from the audio interface using DATSEL. The default is for left and right channel ADC data to be output, but the interface may also be configured so that e.g. left channel ADC data is output as both left and right data for when an analogue mono mix is selected.

Note:

If DC measurement is selected this overrides the MONOMIX selection.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R46 (2Eh) ADC input Mode	5:4	MONOMIX[1:0]	00	00: Stereo 01: Analogue Mono Mix (using left ADC) 10: Analogue Mono Mix (using right ADC) 11: Digital Mono Mix

Table 7 Mono Mixing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) Additional Control (1)	8:7	DATSEL [1:0]	00	00: left data = left ADC; right data = right ADC 01: left data = left ADC; right data = left ADC 10: left data = right ADC; right data = right ADC 11: left data = right ADC; right data = left ADC

Table 8 ADC Data Output Configuration

MICROPHONE INPUTS

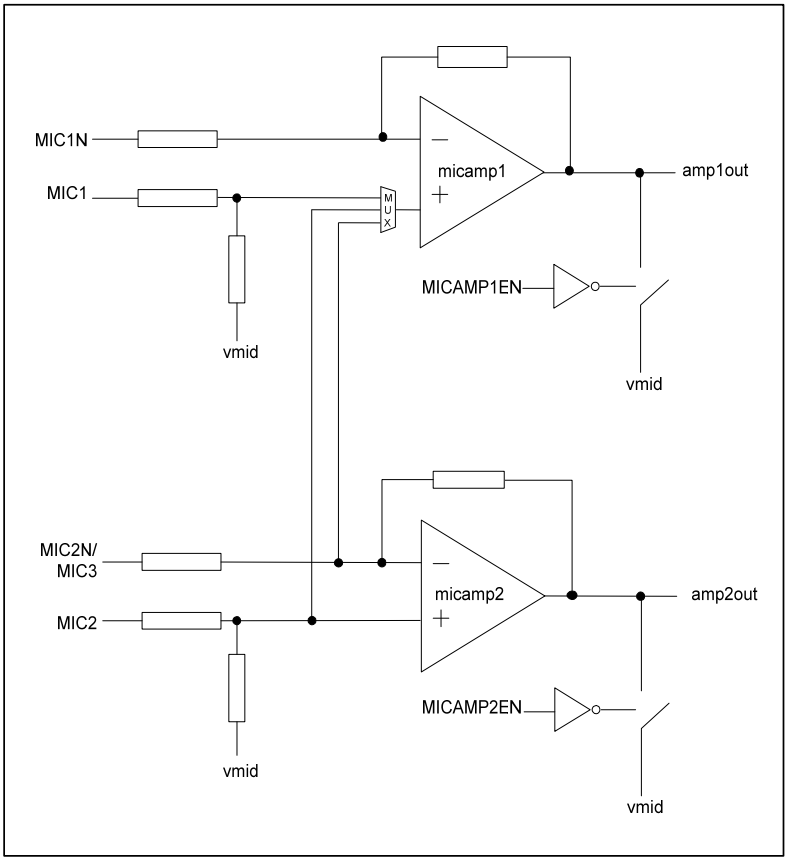


Figure 8 Internal Microphone Input Circuit

There are two microphone pre-amplifiers which can be configured in a variety of ways to accommodate up to 3 single ended or 2 differential microphone inputs. The microphone input circuit is shown in Figure 8.

Each microphone preamplifier has a separate enable bit, MICAMP1EN and MICAMP2EN. The gain for each preamp can be set independently using MIC1BOOST and MIC2BOOST.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R21 (15h)	8	MICAMP1EN	0	Microphone amplifier 1 enable 0 = Mic1 amp disabled 1 = Mic1 amp enabled
	7	MICAMP2EN	0	Microphone amplifier 2 enable 0 = Mic2 amp disabled 1 = Mic2 amp enabled

Table 9 Mic Preamp Enables

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R47 (2Fh) Mic Input Boost	[8:7]	MIC2BOOST[1:0]	00	MIC2 Preamp Gain Control 00 : +12dB 01 : +18dB 10 : +24dB 11 : +30dB
	[6:5]	MIC1BOOST[1:0]	00	MIC1 Preamp Gain Control 00 = +12dB 01 = +18dB 10 = +24dB 11 = +30dB

Table 10 MIC Preamp Gain Control

The suggested configuration for the external microphone circuit is shown in Figure 9.

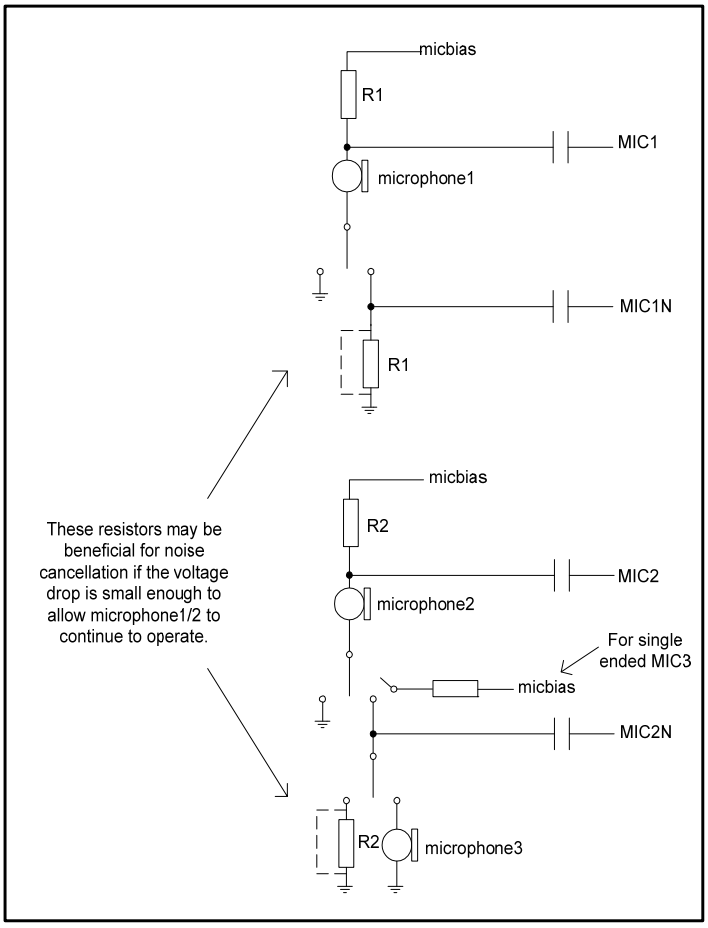


Figure 9 Suggested External Microphone Input Configuration

DIFFERENTIAL OPERATION

It is possible to connect up to two mics differentially. Microphone1 is connected between the MIC1 and MIC1N inputs and microphone2 is connected between the MIC2 and MIC2N inputs. It should be noted that in differential mode, with mic inputs routed to the ADCs, an extra invert occurs in the MIC1 (left ADC) path due to the extra mixer. This can be compensated for by inverting the left ADC signal back again using ADCPOL.