Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

WM8758B

Stereo CODEC with Headphone Driver and Line Out

DESCRIPTION

The WM8758B is a low power, high quality stereo CODEC designed for portable applications such as MP3 audio player.

The device integrates preamps for stereo differential mics, and drivers for headphone and differential or stereo line output. External component requirements are reduced as no separate microphone or headphone amplifiers are required. Headphone and line common feedback improves crosstalk and noise performance.

Advanced on-chip digital signal processing includes a 5-band equaliser, a mixed signal Automatic Level Control for the microphone or line input through the ADC as well as a purely digital limiter function for record or playback. Additional digital filtering options are available in the ADC path, to cater for application filtering such as 'wind noise reduction' and notch filter.

The WM8758B digital audio interface can operate in master or slave mode with an integrated PLL.

The WM8758B operates at analogue supply voltages from 2.5V to 3.3V, although the digital supply voltages can operate at voltages down to 1.71V to save power. Additional power management control enables individual sections of the chip to be powered down under software control.

FEATURES

Stereo CODEC:

- DAC SNR 100dB, THD -86dB ('A' weighted @ 48kHz)
- ADC SNR 92.5dB, THD -75dB ('A' weighted @ 48kHz)
- Headphone Driver
- 40mW per channel output power into 16Ω / 3.3V AVDD2
- Line output

Mic Preamps:

- Stereo Differential or mono microphone Interfaces
- Programmable preamp gain
- Psuedo differential inputs with common mode rejection
- Programmable ALC / Noise Gate in ADC path
- Low-noise bias supplied for electret microphones

Other Features:

- Enhanced 3-D function for improved stereo separation
- Digital playback limiter
- 5-band Equaliser (record or playback)
- Programmable ADC High Pass Filter (wind noise reduction)
- Programmable ADC Notch Filter
- PLL supporting various clocks between 8MHz-50MHz
- Sample rates supported (kHz): 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48
- Low power, low voltage
- 2.5V to 3.6V analogue supplies
- 1.71V to 3.6V digital supplies
- 5x5mm 32-lead QFN package

APPLICATIONS

- Portable audio player

BLOCK DIAGRAM

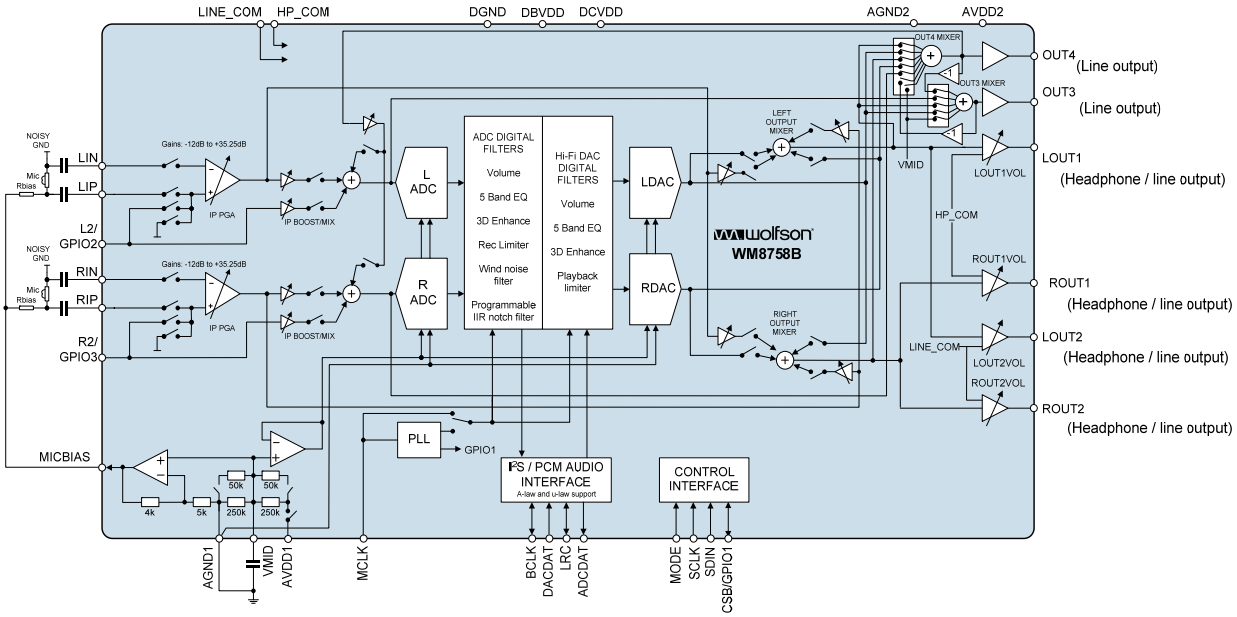
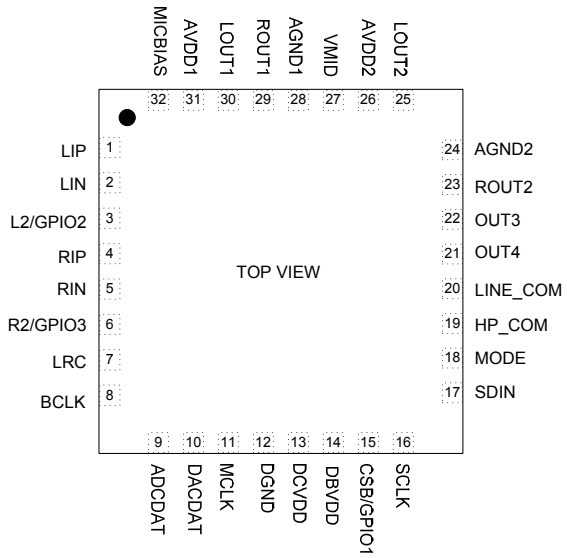


TABLE OF CONTENTS

PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8758CBGEFL/V	-40°C to +85°C	32-lead QFN (5 x 5 mm) (Pb-free)	MSL3	260°C
WM8758CBGEFL/RV	-40°C to +85°C	32-lead QFN (5 x 5 mm) (Pb-free, tape and reel)	MSL3	260°C

Note:

Reel quantity = 3,500

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	LIP	Analogue Input	Left MIC pre-amp positive input
2	LIN	Analogue Input	Left MIC pre-amp negative input
3	L2/GPIO2	Analogue Input	Left channel line input/secondary mic pre-amp positive input/GPIO2 pin
4	RIP	Analogue Input	Right MIC pre-amp positive input
5	RIN	Analogue Input	Right MIC pre-amp negative input
6	R2/GPIO3	Analogue Input	Right channel line input/secondary mic pre-amp positive input/GPIO3 pin
7	LRC	Digital Input / Output	DAC and ADC sample rate clock
8	BCLK	Digital Input / Output	Digital audio bit clock
9	ADCDAT	Digital Output	ADC digital audio data output
10	DACDAT	Digital Input	DAC digital audio data input
11	MCLK	Digital Input	Master clock input
12	DGND	Supply	Digital ground
13	DCVDD	Supply	Digital core logic supply
14	DBVDD	Supply	Digital buffer (I/O) supply
15	CSB/GPIO1	Digital Input / Output	3-Wire control interface chip select / GPIO1 pin
16	SCLK	Digital Input	3-Wire control interface clock input / 2-wire control interface clock input
17	SDIN	Digital Input / Output	3-Wire control interface data input / 2-Wire control interface data input
18	MODE	Digital Input	Control interface selection
19	HP_COM	Analogue Input	Headphone ground common feedback input
20	LINE_COM	Analogue Input	Line out ground common feedback input
21	OUT4	Analogue Output	Right line output / mono mix output
22	OUT3	Analogue Output	Left line output / mono mix output
23	ROUT2	Analogue Output	Line output right 2
24	AGND2	Supply	Analogue ground (return path for ROUT2/LOUT2)
25	LOUT2	Analogue Output	Line output left 2
26	AVDD2	Supply	Analogue supply (supply for output amplifiers ROUT2/LOUT2)
27	VMID	Reference	Decoupling for ADC and DAC reference voltage
28	AGND1	Supply	Analogue ground (return path for all input amplifiers, PLL, ADC and DAC, internal bias circuits, output amplifiers LOUT1, ROUT1 and OUT3/OUT4 on AVDD1 AGND1)
29	ROUT1	Analogue Output	Line or headphone output right 1
30	LOUT1	Analogue Output	Line or headphone output left 1
31	AVDD1	Supply	Analogue supply (feeds all input amplifiers, PLL, ADC and DAC, internal bias circuits, output amplifiers LOUT1, ROUT1))
32	MICBIAS	Analogue Output	Microphone bias

Note:

It is recommended that the QFN ground paddle should be connected to analogue ground on the application PCB.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
DBVDD, DCVDD, AVDD1, AVDD2 supply voltages	-0.3V	+3.63V
Voltage range digital inputs	DGND -0.3V	DVDD +0.3V
Voltage range analogue inputs	AGND1 -0.3V	AVDD1 +0.3V
Storage temperature prior to soldering	30°C max / 85% RH max	
Storage temperature after soldering	-65°C	+150°C

Notes

1. Analogue and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are internally independent (i.e. not connected).
3. Analogue supply voltages should not be less than digital supply voltages.
4. DBVDD must be greater than or equal to DCVDD.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD		1.71[1,2]	1.8	3.6	V
Digital supply range (Buffer)	DBVDD		1.71	3.3	3.6	V
Analogue supply range	AVDD1, AVDD2		2.5[1]	3.3	3.6	V
Ground	DGND, AGND1, AGND2			0		V

Notes

1. Analogue supply voltages must not be less than digital supply voltages.
2. DBVDD must be greater than or equal to DCVDD.

ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD=1.8V, AVDD1=AVDD2=3.0V, DBVDD=3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Preamp Inputs (LIP, LIN, RIP, RIN, L2, R2)						
Full-scale Input Signal Level – Single-ended input via LIN/RIN	V_{INFS}	PGABOOST = 0dB INPPGAVOL = 0dB		AVDD1/3.3		Vrms
Full-scale Input Signal Level – Pseudo-differential input	V_{INFS}	PGABOOST = 0dB INPPGAVOL = 0dB		AVDD1*0.7/ 3.3		Vrms
Mic PGA equivalent input noise	At 35.25dB gain	0 to 20kHz		150		uV
Input resistance (LIN, RIN)	R_{MICIN}	Gain set to 35.25dB		1.6		kΩ
Input resistance (LIN, RIN)	R_{MICIN}	Gain set to 0dB		46		kΩ
Input resistance (LIN, RIN)	R_{MICIN}	Gain set to -12dB		71		kΩ
Input resistance (LIP, RIP)	R_{MICIP}			90		kΩ
Input resistance (L2, R2)	R_{L2R2}	L/RIP2INPPGA = 1, L/R2_2BOOSTVOL = 000		90		kΩ
Input resistance (L2, R2)	R_{L2R2}	L/RIP2INPPGA = 0, Gain set to 6dB		11		kΩ
Input resistance (L2, R2)	R_{L2R2}	L/RIP2INPPGA = 0, Gain set to 0dB		22		kΩ
Input resistance (L2, R2)	R_{L2R2}	L/RIP2INPPGA = 0, Gain set to -12dB		60		kΩ
Input Capacitance	C_{MICIN}			10		pF
Maximum Programmable Gain				+35.25		dB
Minimum Programmable Gain				-12		dB
Programmable Gain Step Size		Guaranteed monotonic		0.75		dB
MIC Mute Attenuation		INPPGAMUTEL/R=1		100		dB
MIC Gain Boost		PGABOOSTL/R=0		0		dB
		PGABOOSTL/R=1		20		dB
L2, R2 Line Input Programmable Gain						
Maximum Gain from L/R2 input to boost/mixer		Gain adjusted by L2_2BOOSTVOL R2_2BOOSTVOL		+6		dB
Minimum Gain from L/R2 input to boost/mixer		Gain adjusted by L2_2BOOSTVOL R2_2BOOSTVOL		-12		dB
L2/R2 boost step size		Guaranteed monotonic		3		dB
L2/R2 Mute attenuation				100		dB
OUT4 to Left or Right Input Boost Record Path						
Maximum Gain				+6		dB
Minimum Gain				-12		dB
Gain step size		Guaranteed monotonic		3		dB
Mute attenuation				100		dB
Automatic Level Control (ALC)						
Target Record Level			-22.5		-1.5	dB
Programmable gain			-12		35.25	

Test Conditions

DCVDD=1.8V, AVDD1=AVDD2=3.0V, DBVDD=3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue to Digital Converter (ADC) - Input from LIN/P and RIN/P, PGA and boost gains=0dB						
Signal to Noise Ratio (Note 5,6)	SNR	A-weighted AVDD1=AVDD2=3.0V		92.5		dB
		A-weighted AVDD1=AVDD2=2.5V		91.5		dB
		22Hz to 20kHz AVDD1=AVDD2=3.0V		90		dB
		22Hz to 20kHz AVDD1=AVDD2=2.5V		90		dB
Total Harmonic Distortion (Note 7)	THD	-12dBFS Input AVDD1=AVDD2=3.0V		-75		dB
		-12dBFS Input AVDD1=AVDD2=2.5V		-75		dB
Total Harmonic Distortion + Noise (Note 7)	THD+N	-12dBFS Input AVDD1=AVDD2=3.0V		-72		dB
		-12dBFS Input AVDD1=AVDD2=2.5V		-72		dB
Channel Separation (Note 8)		1kHz full scale input signal		100		dB
Analogue to Digital Converter (ADC) - Input from L2, R2						
Signal to Noise Ratio (Note 5,6)	SNR	A-weighted AVDD1=AVDD2=3.0V	85	92.5		dB
		A-weighted AVDD1=AVDD2=2.5V		92.5		dB
		22Hz to 20kHz AVDD1=AVDD2=3.0V		90		dB
		22Hz to 20kHz AVDD1=AVDD2=2.5V		90		dB
Total Harmonic Distortion (Note 7)	THD	-3dBFS Input AVDD1=AVDD2=3.0V		-83	-75	dB
		-3dBFS Input AVDD1=AVDD2=2.5V		-66		dB
Total Harmonic Distortion + Noise (Note 7)	THD+N	-3dBFS Input AVDD1=AVDD2=3.0V		-81	-70	dB
		-3dBFS Input AVDD1=AVDD2=2.5V		-65		dB
Channel Separation (Note 8)		1kHz input signal		100		dB

Test Conditions

DCVDD=1.8V, AVDD1=AVDD2=3.0V, DBVDD=3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to L/R Mix to Line-Out (LOUT1/ROUT1 with 10kΩ / 50pF load, analogue volume controls set to 0dB)						
Full-scale output		PGA gains set to 0dB		AVDD1/3.3		Vrms
Signal to Noise Ratio (Note 5,6)	SNR	A-weighted AVDD1=AVDD2=3.0V		100		dB
		A-weighted AVDD1=AVDD2=2.5V		96		dB
		22Hz to 20kHz AVDD1=AVDD2=3.0V		95.5		dB
		22Hz to 20kHz AVDD1=AVDD2=2.5V		93.5		dB
Total Harmonic Distortion (Note 7)	THD	full-scale signal AVDD1=AVDD2=3.0V		-86		dB
		full-scale signal AVDD1=AVDD2=2.5V		-86		dB
Total Harmonic Distortion + Noise (Note 7)	THD+N	full-scale signal AVDD1=AVDD2=3.0V		-84		dB
		full-scale signal AVDD1=AVDD2=2.5V		-84		dB
Channel Separation (Note 8)		1kHz signal		100		dB
Ground noise rejection		10mV, 20kHz noise on HPCOM, HPCOM enabled		40		dB
DAC to L/R Mix to Line-Out (LOUT2/ROUT2 with 10kΩ / 50pF load, analogue volume controls set to 0dB)						
Full-scale output		PGA gains set to 0dB		AVDD1/3.3		Vrms
Signal to Noise Ratio (Note 5,6)	SNR	A-weighted AVDD1=AVDD2=3.0V	95	100		dB
		A-weighted AVDD1=AVDD2=2.5V		96		dB
		22Hz to 20kHz AVDD1=AVDD2=3.0V		95.5		dB
		22Hz to 20kHz AVDD1=AVDD2=2.5V		93.5		dB
Total Harmonic Distortion (Note 7)	THD	full-scale signal AVDD1=AVDD2=3.0V		-87	-80	dB
		full-scale signal AVDD1=AVDD2=2.5V		-82		dB
Total Harmonic Distortion + Noise (Note 7)	THD+N	full-scale signal AVDD1=AVDD2=3.0V		-85	-75	dB
		full-scale signal AVDD1=AVDD2=2.5V		-80		dB
Channel Separation (Note 8)		1kHz signal		100		dB
Ground noise rejection		10mV, 20kHz noise on LCOM, LCOM enabled		40		dB

Test Conditions

DCVDD=1.8V, AVDD1=AVDD2=3.0V, DBVDD=3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to L/R Mix to Headphone (LOUT1/ROUT1, analogue volume controls set to 0dB)						
Full-scale output		PGA gains set to 0dB		AVDD1/3.3		Vrms
Signal to Noise Ratio (Note 5,6)	SNR	A-weighted		100		dB
		22Hz to 20kHz		95.5		dB
Total Harmonic Distortion (Note 7)	THD	P_o = 20mW RL=16Ω		-75		dB
		P_o = 20mW RL=32Ω		-79		dB
Total Harmonic Distortion + Noise (Note 7)	THD+N	P_o = 20mW RL=16Ω		-75		dB
		P_o = 20mW RL=32Ω		-79		dB
Channel Separation (Note 8)		1kHz signal		100		dB
Ground noise rejection		10mV, 20kHz noise on HPCOM, HPCOM enabled		40		dB
DAC to L/R Mix to Headphone (LOUT2/ROUT2, analogue volume controls set to 0dB)						
Full-scale output		PGA gains set to 0dB		AVDD1/3.3		Vrms
Signal to Noise Ratio (Note 5,6)	SNR	A-weighted	90	97		dB
		22Hz to 20kHz		95.5		dB
Total Harmonic Distortion (Note 7)	THD	P_o = 20mW RL=16Ω		-79		dB
		P_o = 20mW RL=32Ω		-82		dB
Channel Separation (Note 8)		1kHz signal		100		dB
Ground noise rejection		10mV, 20kHz noise on LCOM, LCOM enabled		40		dB
Bypass Paths to Output Mixers						
Maximum PGA gain into mixer				+6		dB
Minimum PGA gain into mixer				-15		dB
PGA gain step into mixer		Guaranteed monotonic		3		dB
Mute attenuation				100		dB
Analogue Outputs (LOUT1, ROUT1, LOUT2, ROUT2)						
Maximum Programmable Gain				+6		dB
Minimum Programmable Gain				-57		dB
Programmable Gain step size		Guaranteed monotonic		1		dB
Mute attenuation		1kHz, full scale signal		85		dB

Test Conditions

DCVDD=1.8V, AVDD1=AVDD2=3.0V, DBVDD=3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MIC PGA to Input Boost to OUT3/OUT4 outputs (with 10kΩ / 50pF load)						
Full-scale output voltage, 0dB gain (Note 9)				AVDD2/3.3		Vrms
Signal to Noise Ratio (Note 5,6)	SNR	A-weighted AVDD1=AVDD2=3.0V	90	98		dB
		A-weighted AVDD1=AVDD2=2.5V		96		dB
		22Hz to 22kHz AVDD1=AVDD2=3.0V		95.5		dB
		22Hz to 22kHz AVDD1=AVDD2=2.5V		93.5		dB
Total Harmonic Distortion (Note 7)	THD	full-scale signal AVDD1=AVDD2=3.0V		-84		dB
		full-scale signal AVDD1=AVDD2=2.5V		-82		dB
Total Harmonic Distortion + Noise (Note 7)	THD+N	full-scale signal AVDD1=AVDD2=3.0V		-82		dB
		full-scale signal AVDD1=AVDD2=2.5V		-80		dB
Channel Separation				100		dB
MIC PGA Bypass to LOUT1/ROUT1 (with 16Ω load)						
Full-scale output voltage, 0dB gain (Note 9)				AVDD1/3.3		Vrms
Signal to Noise Ratio (Note 5,6)	SNR	A-weighted AVDD1=AVDD2=3.0V	90	100		dB
		A-weighted AVDD1=AVDD2=2.5V		96		dB
		22Hz to 22kHz AVDD1=AVDD2=3.0V		95.5		dB
		22Hz to 22kHz AVDD1=AVDD2=2.5V		93.5		dB
Total Harmonic Distortion (Note 7)	THD	-5dBFS signal AVDD1=AVDD2=3.0V		-87	-75	dB
		-5dBFS signal AVDD1=AVDD2=2.5V		-69		dB
Total Harmonic Distortion + Noise (Note 7)	THD+N	-5dBFS signal AVDD1=AVDD2=3.0V		-85	-73	dB
		-5dBFS signal AVDD1=AVDD2=2.5V		-68		dB
Channel separation		1kHz full scale signal		100		dB

Test Conditions

DCVDD=1.8V, AVDD1=AVDD2=3.0V, DBVDD=3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Bias						
Bias Voltage	$V_{MICBIAS}$	MBVSEL=0		0.9*AVDD1		V
		MBVSEL=1		0.65*AVDD1		V
Bias Current Source	$I_{MICBIAS}$	for $V_{MICBIAS}$ within +/-3%			3	mA
Output Noise Voltage	Vn	1kHz to 20kHz		15		nV/√Hz
Digital Input / Output						
Input HIGH Level	V_{IH}		0.7×DBVDD			V
Input LOW Level	V_{IL}				0.3× DBVDD	V
Output HIGH Level	V_{OH}	I_{OL}=1mA	0.9×DBVDD			V
Output LOW Level	V_{OL}	I_{OH}-1mA			0.1x DBVDD	V

TERMINOLOGY

1. Signal-to-noise ratio (dB) – SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. THD+N (dB) – THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
3. Channel Separation (dB) – Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
4. THD (dB) – THD is a ratio of the rms value of the first seven harmonics compared to the rms value of the fundamental.

HEADPHONE OUTPUT PERFORMANCE

SNR Graphs TBA:

SNR vs AVDD1=AVDD2 L/ROUT1 (DAC path) for 16Ω, 32Ω

SNR vs AVDD1=AVDD2 L/ROUT2 (DAC path) for 16Ω, 32Ω

THD+N Graphs TBA:

THD+N vs output power (Analogue in to L/ROUT1) 16Ω, 32Ω

Plots for AVDD1=AVDD2=2.7, 3.0, 3.3, 3.6V

THD+N vs output power (Analogue in to L/ROUT2) 16Ω, 32Ω

Plots for AVDD1=AVDD2=2.7, 3.0, 3.3, 3.6V

PSRR Graphs TBA:

AVDD1 PSRR vs Frequency (DAC to L/ROUT1), 16Ω

AVDD1 PSRR vs Frequency (DAC to L/ROUT2), 16Ω

AVDD2 PSRR vs Frequency (DAC to L/ROUT2), 16Ω

POWER CONSUMPTION

TYPICAL SCENARIOS

Estimated current consumption for typical scenarios are shown below.

All measurements are made with quiescent signal.

Power delivered to the load is not included.

Control Register / Operational Mode	Clocking Scheme (Unless otherwise specified) / Slave Mode MCLK = 12.288Mhz LRC = 48kHz BCLK = 3.048MHz	Load / Ω	register settings (Hex values)	DCVDD (V)	DCVDD (mA)	DBVDD (V)	DBVDD (mA)	AVDD1 (V)	AVDD1 (mA)	AVDD2 (V)	AVDD2 (mA)	Total Power (mW)
OFF	No clocks	None	All default	3.3	0.001	3.3	0	3.3	0.01	3.3	0	0.036
				2.5	0	2.5	0	2.5	0.008	2.5	0	0.020
				1.8	0	1.8	0	2.5	0.008	2.5	0	0.020
Standby	No clocks	None	R1= 009, R49 = 006	3.3	0.001	3.3	0	3.3	0.145	3.3	0	0.482
				2.5	0	2.5	0	2.5	0.115	2.5	0	0.288
				1.8	0	1.8	0	2.5	0.115	2.5	0	0.288
L/ROUT1	Clocks on	None	R1=009, R2=180, R3=06F, R4=050, R6=000, R32=001, R33=001	3.3	6.8	3.3	0.008	3.3	5.8	3.3	0.7	43.916
				2.5	4.8	2.5	0.005	2.5	4.3	2.5	0.5	24.013
				1.8	3.2	1.8	0.003	2.5	4.3	2.5	0.5	17.765
L/ROUT2	Clocks on	None	R1=009, R3=06F, R4=050, R11=024, R17=004, R6=000, R32=001, R33=001	3.3	6.8	3.3	0.008	3.3	5.1	3.3	0.7	41.606
				2.5	4.8	2.5	0.005	2.5	3.8	2.5	0.5	22.763
				1.8	3.2	1.8	0.003	2.5	3.8	2.5	0.5	16.515
OUT3/OUT4 Stereo line out	Clocks on	None	R1=1FF, R3=1EF, R4=050, R6=000, R38=001, R39=001	3.3	6.88	3.3	0.008	3.3	5.1	3.3	0.7	41.870
				2.5	4.82	2.5	0.005	2.5	3.8	2.5	0.5	22.813
				1.8	3.2	1.8	0.003	2.5	3.8	2.5	0.5	16.515
ADC Stereo Record (psuedo MIC)	Clocks on	N/A	R1=OCD, R2=1BF, R4=050, R6=000, R2C=033, R2D=110, R2F=000, R2E=110, R30=000	3.3	7.3	3.3	0.04	3.3	8.1	3.3	0	50.952
				2.5	5.1	2.5	0.03	2.5	6.5	2.5	0	29.075
				1.8	3.45	1.8	0.02	2.5	6.5	2.5	0	22.496
ADC Stereo Record (line in)	Clocks on	N/A	R1=0CD, R2=1BF, R4=050, R6=000, R2F=050, R30=050	3.3	7.5	3.3	0.04	3.3	7.6	3.3	0	49.962
				2.5	5.2	2.5	0.03	2.5	6.05	2.5	0	28.200
				1.8	3.55	1.8	0.02	2.5	6.05	2.5	0	21.551
L/ROUT1 Master mode	Master mode / MCLK=13MHz	None	R1=029, R2=180, R3=00F, R4=050, R6=149, R32=001, R33=001, R24=007,R25=023, R26=1EA, R27=126	3.3	3.06	3.3	7.9	3.3	7.1	3.3	0	59.598
				2.5	2.18	2.5	3.5	2.5	5.24	2.5	0	27.300
				1.8	3.7	1.8	1.6	2.5	5.24	2.5	0	22.640
BYPASS to OUT3/OUT4	No clocks	None	R1=0CD, R2=03C, R3=180, R2F=050, R38=004, R30=050, R39=004	3.3	0.001	3.3	0.001	3.3	2.15	3.3	0	7.102
				2.5	0	2.5	0	2.5	1.54	2.5	0	3.850
				1.8	0	1.8	0	2.5	1.54	2.5	0	3.850

AUDIO PATHS OVERVIEW

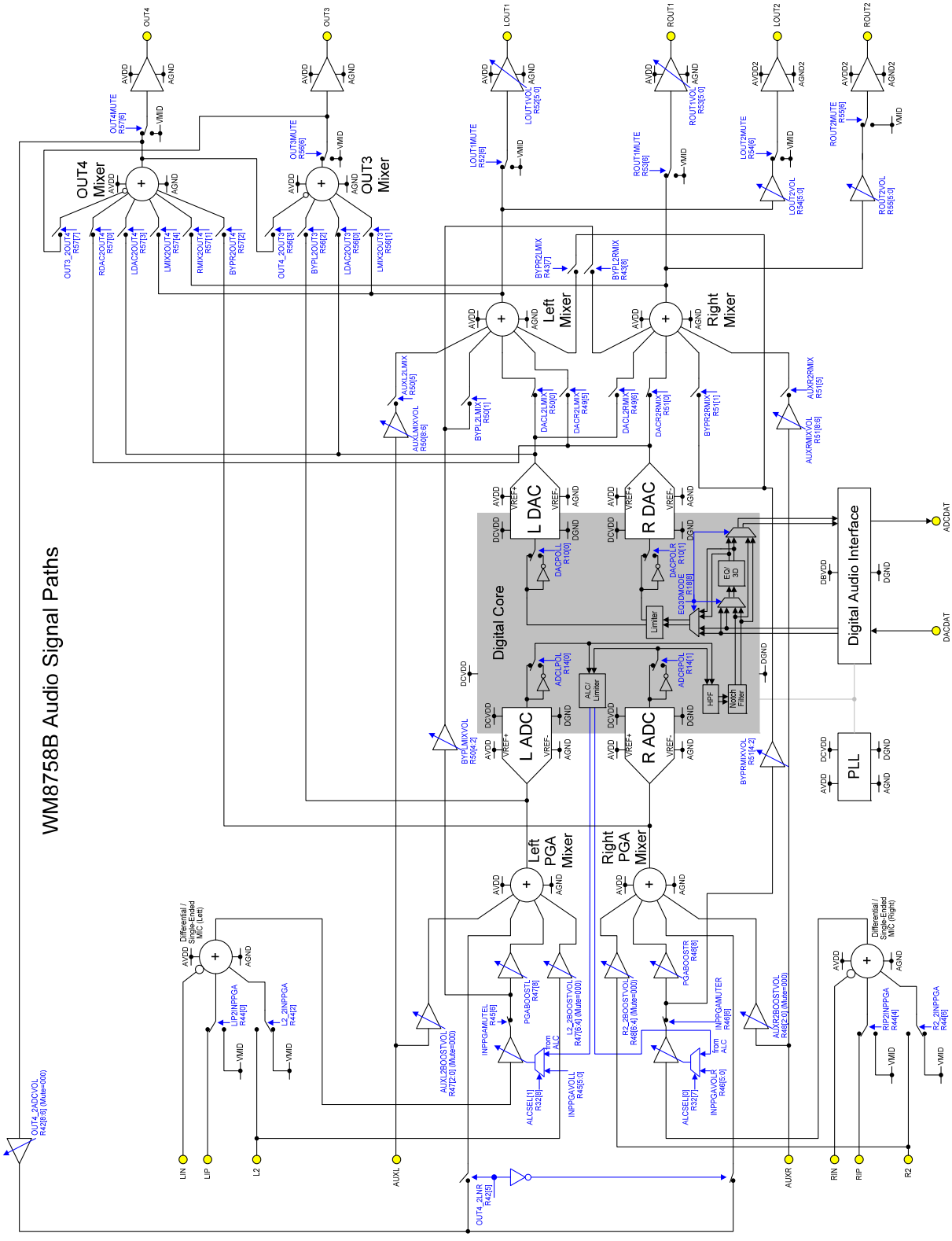


Figure 1 Audio Paths Overview

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

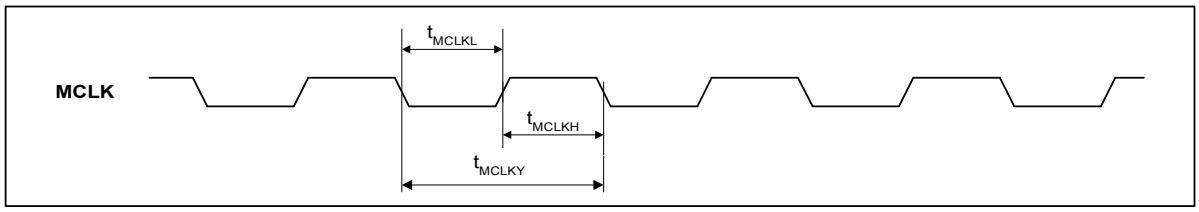


Figure 2 System Clock Timing Requirements

Test Conditions

DCVDD=1.8V, DBVDD=3.3V, AVDD1=AVDD2=3.0V, DGND=AGND1=AGND2=0V, T_A = +25°C, Slave Mode

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK cycle time	T_{MCLKY}	MCLK=SYSCLK (=256fs)	81.38			ns
		MCLK input to PLL [Note 1]	20			ns
MCLK duty cycle	T_{MCLKDS}		60:40		40:60	

Note:

1. PLL pre-scaling and PLL N and K values should be set appropriately so that SYSCLK is no greater than 12.288MHz.

AUDIO INTERFACE TIMING – MASTER MODE

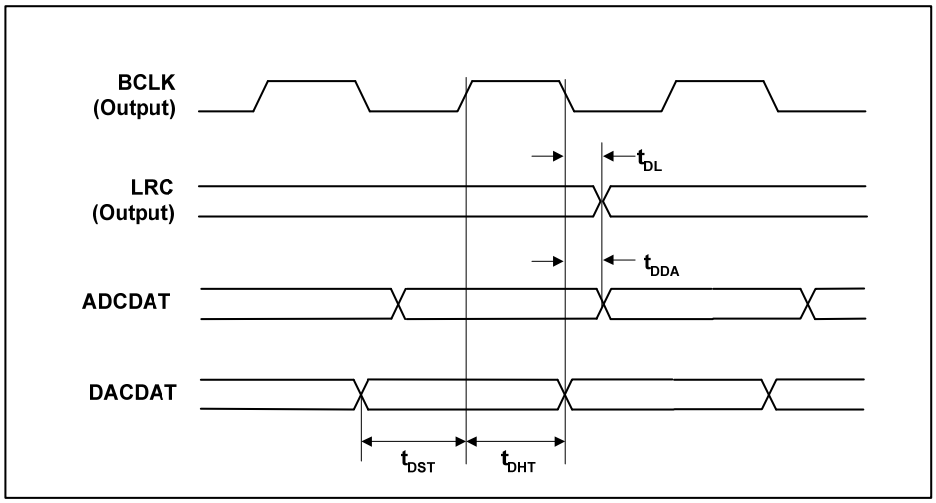


Figure 3 Digital Audio Data Timing – Master Mode (see Control Interface)

Test Conditions

DCVDD=1.8V, DBVDD=3.3V, AVDD1=AVDD2=3.0V, DGND=AGND1=AGND2=0V, T_A=+25°C, Master Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
LRC propagation delay from BCLK falling edge	t_{DL}			10	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			10	ns
DACDAT setup time to BCLK rising edge	t_{DST}	10			ns
DACDAT hold time from BCLK rising edge	t_{DHT}	10			ns

AUDIO INTERFACE TIMING – SLAVE MODE

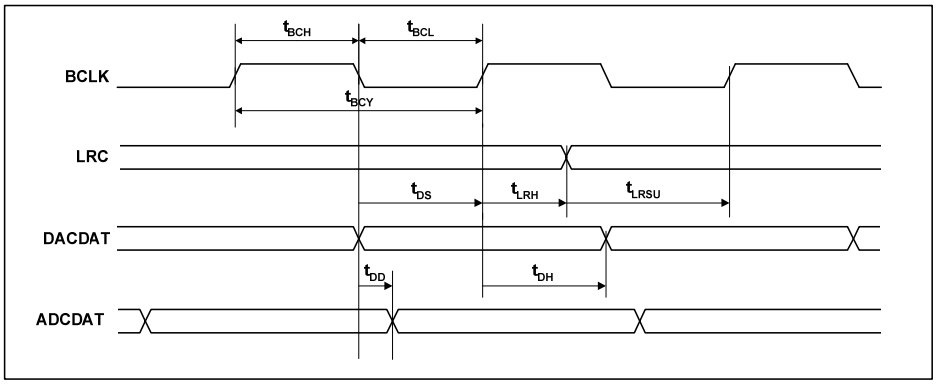


Figure 4 Digital Audio Data Timing – Slave Mode

Test Conditions

DCVDD=1.8V, DBVDD=3.3V, AVDD1=AVDD2=3.0V, DGND=AGND1=AGND2=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK= 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t_{BCY}	50			ns
BCLK pulse width high	t_{BCH}	20			ns
BCLK pulse width low	t_{BCL}	20			ns
LRC set-up time to BCLK rising edge	t_{LRSU}	10			ns
LRC hold time from BCLK rising edge	t_{LRH}	10			ns
DACDAT hold time from BCLK rising edge	t_{DH}	10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			10	ns

Note:

BCLK period should always be greater than or equal to MCLK period.

CONTROL INTERFACE TIMING – 3-WIRE MODE

3-wire mode is selected by connecting the MODE pin high.

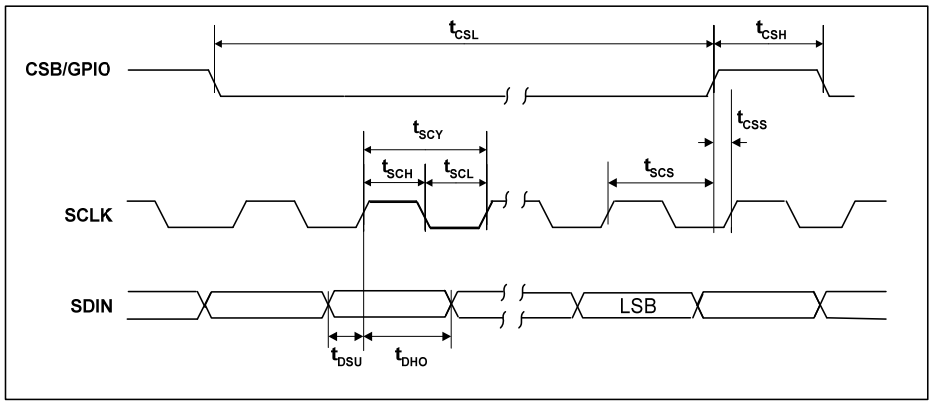


Figure 5 Control Interface Timing – 3-Wire Serial Control Mode

Test Conditions

DCVDD=1.8V, DBVDD=3.3V, AVDD1=AVDD2=3.0V, DGND = AGND1 = AGND2 = 0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB rising edge	t_{SCS}	80			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDIN to SCLK set-up time	t_{DSU}	40			ns
SCLK to SDIN hold time	t_{DHO}	40			ns
CSB pulse width low	t_{CSL}	40			ns
CSB pulse width high	t_{CSH}	40			ns
CSB rising to SCLK rising	t_{CSS}	40			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

CONTROL INTERFACE TIMING – 2-WIRE MODE

2-wire mode is selected by connecting the MODE pin low.

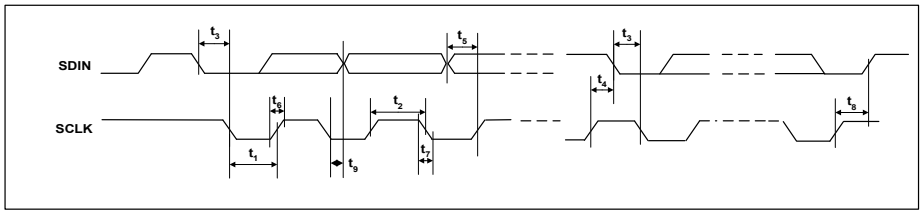


Figure 6 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DCVDD=1.8V, DBVDD=3.3V, AVDD1=AVDD2=3.0V, DGND=AGND1=AGND2=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency		0		526	kHz
SCLK Low Pulse-Width	t_1	1.3			us
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDIN, SCLK Rise Time	t_6			300	ns
SDIN, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

INTERNAL POWER ON RESET CIRCUIT

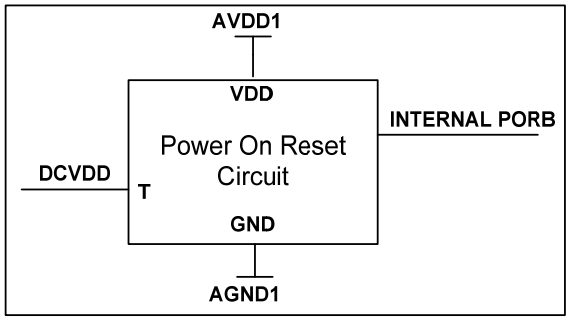


Figure 7 Internal Power on Reset Circuit Schematic

The WM8758B includes an internal Power-On-Reset Circuit, as shown in Figure 7, which is used to reset the digital logic into a default state after power up. The POR circuit is powered from AVDD1 and monitors DCVDD. It asserts PORB low if AVDD1 or DCVDD is below a minimum threshold.

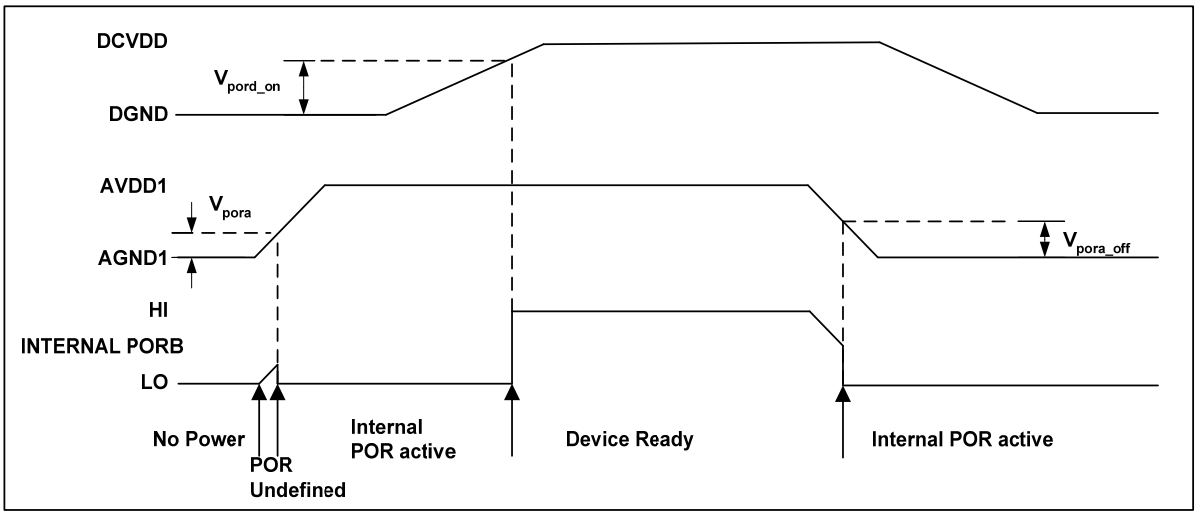


Figure 8 Typical Power up Sequence where AVDD1 is Powered before DCVDD

Figure 8 shows a typical power-up sequence where AVDD1 comes up first. When AVDD1 goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. Now AVDD1 is at full supply level. Next DCVDD rises to V_{pord_on} and PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where AVDD1 falls first, PORB is asserted low whenever AVDD1 drops below the minimum threshold V_{pora_off}.

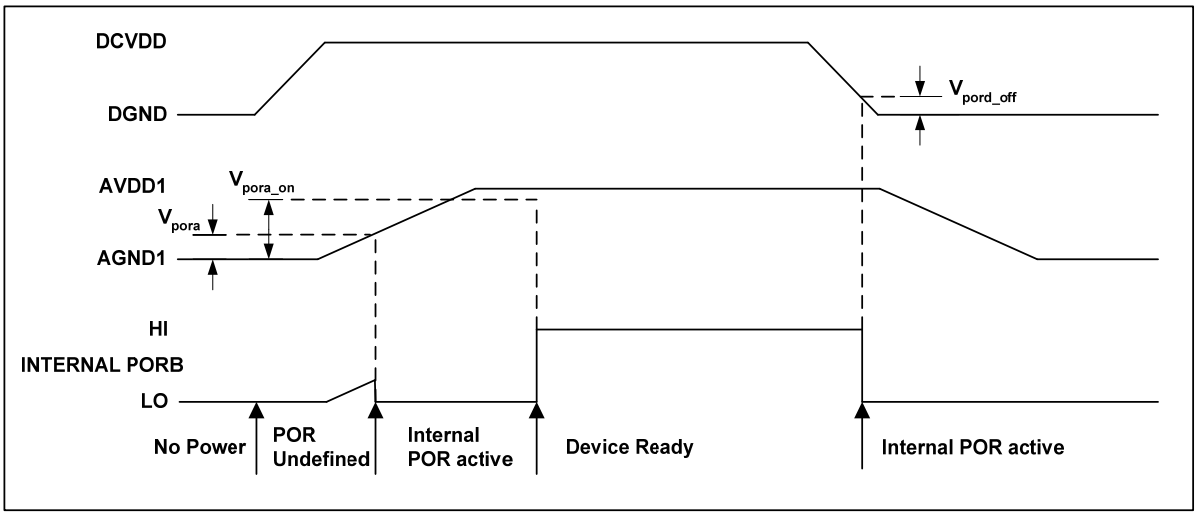


Figure 9 Typical Power up Sequence where DCVDD is Powered before AVDD1

Figure 9 shows a typical power-up sequence where DCVDD comes up first. First it is assumed that DCVDD is already up to specified operating voltage. When AVDD1 goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When AVDD1 rises to V_{pora_on}, PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where DCVDD falls first, PORB is asserted low whenever DCVDD drops below the minimum threshold V_{pord_off}.

SYMBOL	MIN	TYP	MAX	UNIT
V_{pora}	0.4	0.6	0.8	V
V_{pora_on}	0.9	1.2	1.6	V
V_{pora_off}	0.4	0.6	0.8	V
V_{pord_on}	0.5	0.7	0.9	V
V_{pord_off}	0.4	0.6	0.8	V

Table 1 Typical POR Operation (typical values, not tested)

Notes:

If AVDD1 and DCVDD suffer a brown-out (i.e. drop below the minimum recommended operating level but do not go below V_{pora_off} or V_{pord_off}) then the chip will not reset and will resume normal operation when the voltage is back to the recommended level again.

The chip will enter reset at power down when AVDD1 or DCVDD falls below V_{pora_off} or V_{pord_off}. This may be important if the supply is turned on and off frequently by a power management system.

The minimum t_{por} period is maintained even if DCVDD and AVDD1 have zero rise time. This specification is guaranteed by design rather than test.

RECOMMENDED POWER UP/DOWN SEQUENCE

In order to minimise output pop and click noise, it is recommended that the WM8758B device is powered up and down under control using the following sequences:

Power Up:

1. Turn on external power supplies. Wait for supply voltage to settle.
2. Set low bias mode, BIASCUT = 1.
3. Enable HPCOM = 1, LINECOM = 1.
4. Mute all Outputs and set PGAs to minimum gain, R52 to R57 = 0x140h.
5. Enable L/ROUT1
6. Enable L/ROUT2
7. Enable VMID independent current bias, POBCTRL = 1.
8. Enable required DACs and mixers.
9. Enable VMIDSEL=01, BIASEN = 1 and BUFIOEN = 1
10. Setup digital interface, input amplifiers, PLL, ADCs and DACs for desired operation.
11. Wait 100ms to allow VMID to rise sufficiently before unmuting outputs
12. Unmute L/ROUT1 and set desired volume, e.g. for 0dB R52 and R53 = 0x139h.
13. Unmute L/ROUT2 and set desired volume, e.g. for 0dB R54 and R55 = 0x139h.
14. Disable VMID independent current bias, POBCTRL = 0.

Power Down:

1. Disable Thermal shutdown
2. Enable VMIDTOG = 1
3. Disable VMIDSEL=00 and BUFIOEN=0
4. Wait for VMID to discharge
5. Power off registers R1, R2, R3 = 0x000h
6. Remove external power supplies

Notes:

1. Charging time constant is determined by impedance selected by VMIDSEL and the value of decoupling capacitor connected to VMID pin.
2. It is possible to interrupt the power down sequence and power up to VMID before the allocated VMID discharge time.

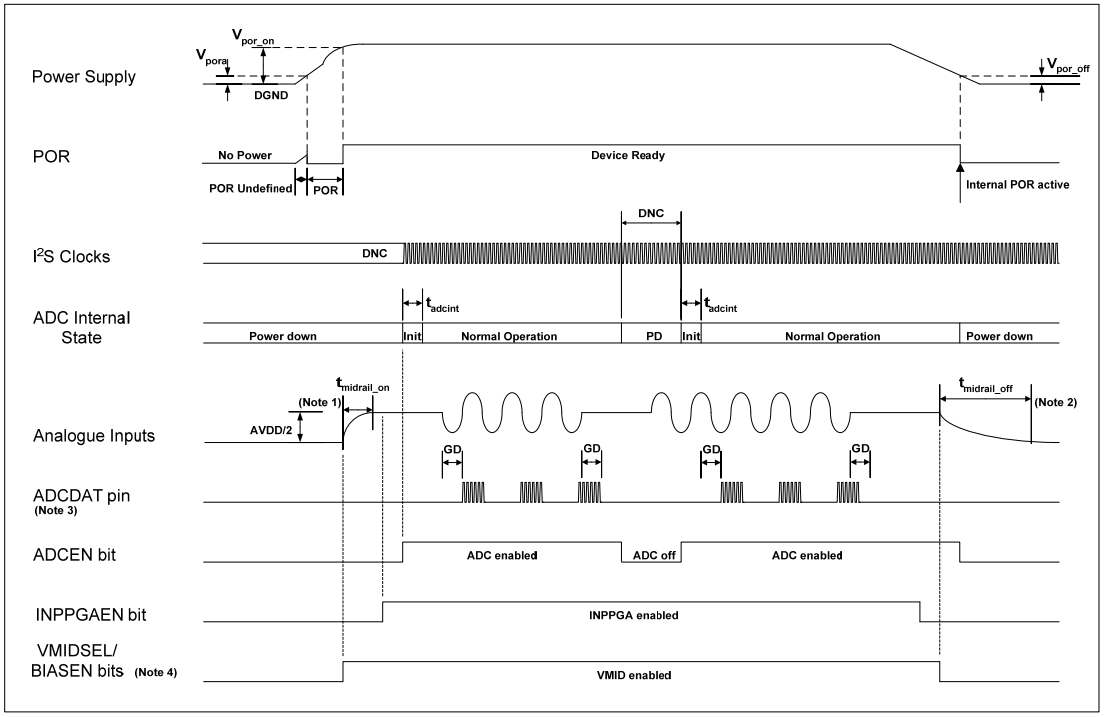


Figure 10 ADC Power Up and Down Sequence (not to scale)

SYMBOL	MIN	TYPICAL	MAX	UNIT
$t_{midrail\_on}$		300		ms
$t_{midrail\_off}$		>6		s
t_{adcint}		2/fs		*n*/fs
ADC Group Delay		29/fs		*n*/fs

Table 2 Typical POR Operation (typical values, not tested)

Notes:

1. The analogue input pin charge time, $t_{midrail\_on}$, is determined by the VMID pin charge time. This time is dependent upon the value of VMID decoupling capacitor and VMID pin input resistance and AVDD power supply rise time.
2. The analogue input pin discharge time, $t_{midrail\_off}$, is determined by the analogue input coupling capacitor discharge time. The time, $t_{midrail\_off}$, is measured using a 1µF capacitor on the analogue input but will vary dependent upon the value of input coupling capacitor.
3. While the ADC is enabled there will be LSB data bit activity on the ADCDAT pin due to system noise but no significant digital output will be present.
4. The VMIDSEL and BIASEN bits must be set to enable analogue input midrail voltage and for normal ADC operation.
5. ADCDAT data output delay from power up - with power supplies starting from 0V - is determined primarily by the VMID charge time. ADC initialisation and power management bits may be set immediately after POR is released; VMID charge time will be significantly longer and will dictate when the device is stabilised for analogue input.
6. ADCDAT data output delay at power up from device standby (power supplies already applied) is determined by ADC initialisation time, 2/fs.

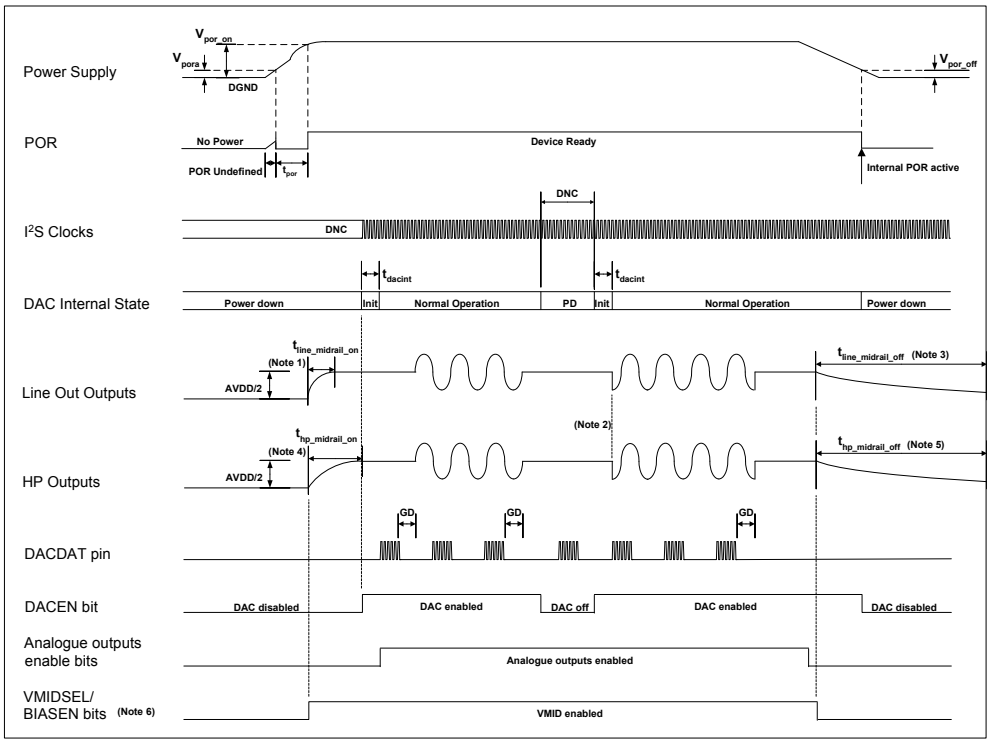


Figure 11 DAC Power Up and Down Sequence (not to scale)

SYMBOL	MIN	TYPICAL	MAX	UNIT
$t_{line\_midrail\_on}$		300		ms
$t_{line\_midrail\_off}$		>6		s
$t_{hp\_midrail\_on}$		300		ms
$t_{hp\_\_midrail\_off}$		>6		s
t_{dacint}		2/fs		*n*/fs
DAC Group Delay		29/fs		*n*/fs

Table 3 Typical POR Operation (typical values, not tested)

Notes:

1. The lineout charge time, $t_{line\_midrail\_on,}$ is determined by the VMID pin charge time. This time is dependent upon the value of VMID decoupling capacitor and VMID pin input resistance and AVDD power supply rise time. The values above were measured using a 4.7µF capacitor.

2. It is not advisable to allow DACDAT data input during initialisation of the DAC. If the DAC data value is not zero at point of initialisation, then this is likely to cause a pop noise on the analogue outputs. The same is also true if the DACDAT is removed at a non-zero value, and no mute function has been applied to the signal beforehand.

3. The lineout discharge time, $t_{line\_midrail\_off,}$ is determined by the VMID pin discharge time. This time is dependent upon the value of VMID decoupling capacitor and VMID pin input resistance. The values above were measured using a 4.7µF capacitor.

4. The headphone charge time, $t_{hp\_midrail\_on,}$ is dependent upon the value of VMID decoupling capacitor and VMID pin input resistance and AVDD power supply rise time. The values above were measured using a 4.7µF VMID decoupling capacitor.

5. The headphone discharge time, $t_{hp\_midrail\_off,}$ is dependent upon the value of VMID decoupling capacitor and VMID pin input resistance. The values above were measured using a 4.7µF VMID decoupling capacitor.

6. The VMIDSEL and BIASEN bits must be set to enable analogue output midrail voltage and for normal DAC operation.

DEVICE DESCRIPTION

INTRODUCTION

The WM8758B is a low power audio codec combining a high quality stereo audio DAC and ADC, with flexible line and microphone input and output processing.

FEATURES

The chip offers great flexibility in use, and so can support many different modes of operation as follows:

MICROPHONE INPUTS

Two pairs of stereo microphone inputs are provided, allowing a pair of stereo microphones to be pseudo-differentially connected, with user defined gain. The provision of the common mode input pin for each stereo input allows for rejection of common mode noise on the microphone inputs (level depends on gain setting chosen). A microphone bias is output from the chip which can be used to bias both microphones. The signal routing can be configured to allow manual adjustment of mic levels, or to allow the ALC loop to control the level of mic signal that is transmitted.

Total gain through the microphone paths of up to +55.25dB can be selected.

PGA AND ALC OPERATION

A programmable gain amplifier is provided in the input path to the ADC. This may be used manually or in conjunction with a mixed analogue/digital automatic level control (ALC) which keeps the recording volume constant.

ADC

The stereo ADC uses a 24-bit high-order oversampling architecture to deliver optimum performance with low power consumption.

HI-FI DAC

The hi-fi DAC provides high quality audio playback suitable for all portable audio hi-fi type applications, including MP3 players and portable disc players of all types.

OUTPUT MIXERS

Flexible mixing is provided on the outputs of the device. A stereo mixer is provided for the stereo headphone or line outputs, LOUT1/ROUT1, and additional summers on the OUT3/OUT4 outputs allow for an optional differential or stereo line output on these pins. Gain adjustment PGAs are provided for the LOUT1/ROUT1 and LOUT2/ROUT2 outputs, and signal switching is provided to allow for all possible signal combinations.

OUT3 and OUT4 can be configured to provide an additional stereo or mono differential lineout from the output of the DACs, the mixers or the input microphone boost stages. They can also provide a midrail reference for pseudo differential inputs to external amplifiers. OUT3 and OUT4 should not be used as a buffered midrail reference in capless mode.

AUDIO INTERFACES

The WM8758B has a standard audio interface, to support the transmission of stereo data to and from the chip. This interface is a 3 wire standard audio interface which supports a number of audio data formats including:

- I^2S
- DSP/PCM Mode (a burst mode in which LRC sync plus 2 data packed words are transmitted)
- MSB-First, left justified
- MSB-First, right justified

The interface can operate in master or slave modes.

CONTROL INTERFACES

To allow full software control over all features, the WM8758B offers a choice of 2 or 3 wire control interface. It is fully compatible and an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs.

Selection of the mode is via the MODE pin. In 2 wire mode, the address of the device is fixed as 0011010b.