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WM8772

24-bit, 192kHz 6-Channel Codec with Volume Control

DESCRIPTION

The WM8772 is a multi-channel audio codec ideal for DVD and surround sound processing applications for home hi-fi, automotive and other audio visual equipment.

A stereo 24-bit multi-bit sigma delta ADC is used. Digital audio output word lengths from 16-32 bits and sampling rates from 32kHz to 96kHz are supported. The 32-lead version allows separate ADC and DAC samples rates.

Three stereo 24-bit multi-bit sigma delta DACs are used with oversampling digital interpolation filters. Digital audio input word lengths from 16-32 bits and sampling rates from 8kHz to 192kHz are supported. Each DAC channel has independent digital volume and mute control.

The audio data interface supports I^2S, left justified, right justified and DSP digital audio formats.

The device is controlled via a 3 wire serial interface. The interface provides access to all features including channel selection, volume controls, mutes, de-emphasis and power management facilities. The device is available in a 28-pin SSOP or 32 pin TQFP.

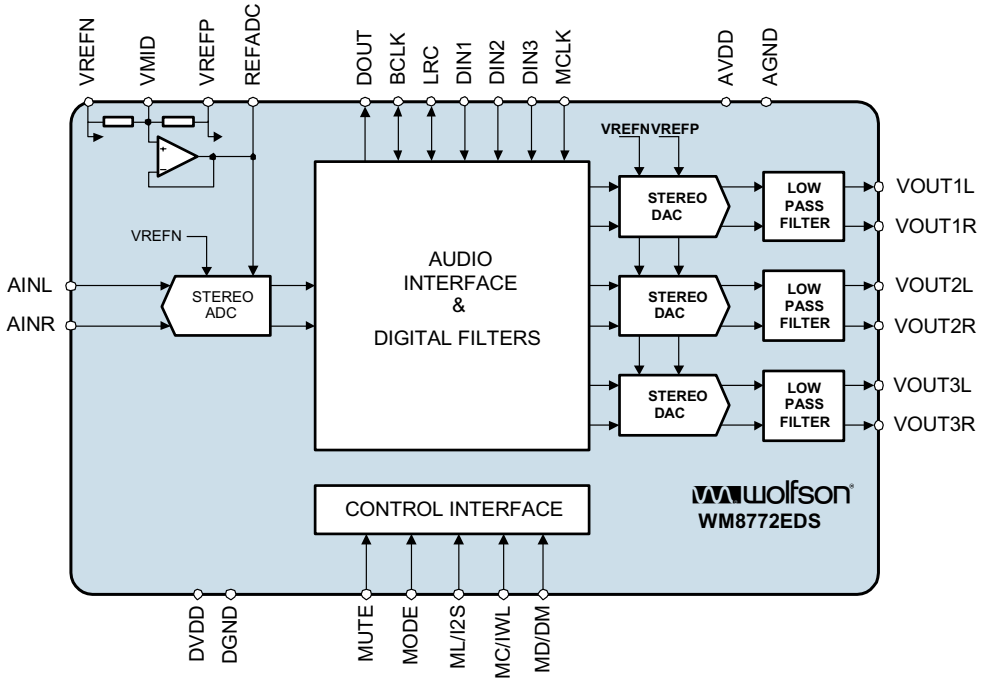
FEATURES

- Audio Performance
  - 103dB SNR ('A' weighted @ 48kHz) DAC
  - 100dB SNR ('A' weighted @ 48kHz) ADC (TQFP)
- DAC Sampling Frequency: 8kHz – 192kHz
- ADC Sampling Frequency: 32kHz – 96kHz
- ADC and DAC can run at different sample rates (32 pin TQFP version only)
- 3-Wire SPI Serial or Hardware Control Interface
- Programmable Audio Data Interface Modes
  - I^2S, Left, Right Justified or DSP
  - 16/20/24/32 bit Word Lengths
- Three Independent stereo DAC outputs with independent digital volume controls
- Master or Slave Audio Data Interface
- 2.7V to 5.5V Analogue, 2.7V to 3.6V Digital supply Operation
- 28 pin SSOP or 32 pin TQFP Package

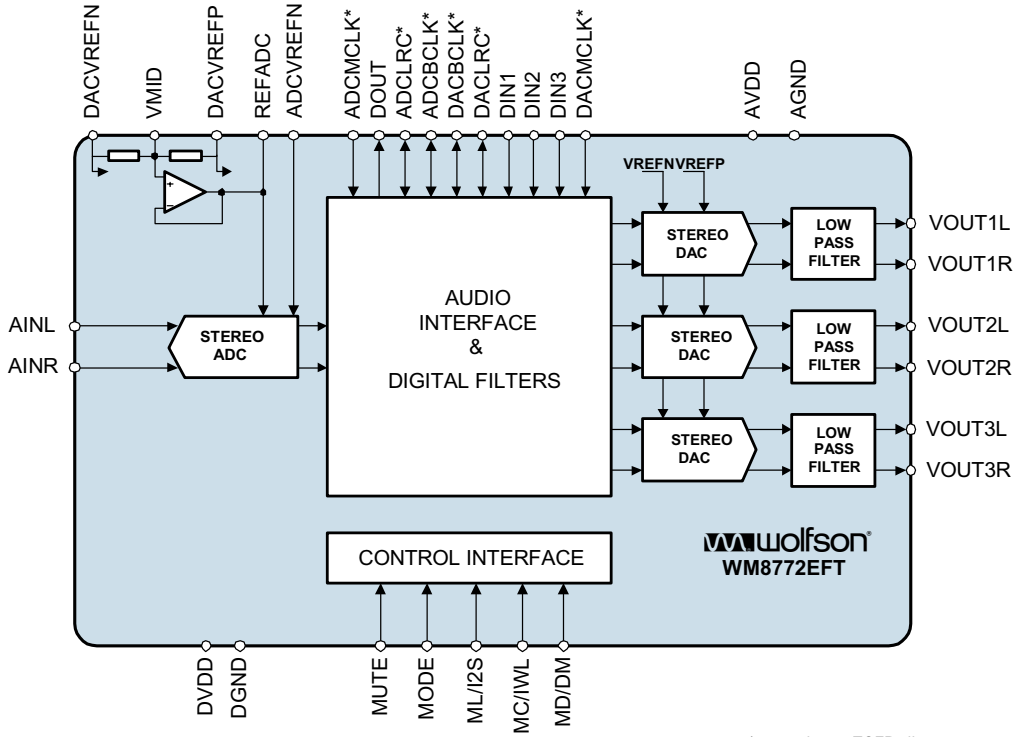
APPLICATIONS

- DVD Players
- Surround Sound AV Processors and Hi-Fi systems
- Automotive Audio

BLOCK DIAGRAM - 28 PIN SSOP



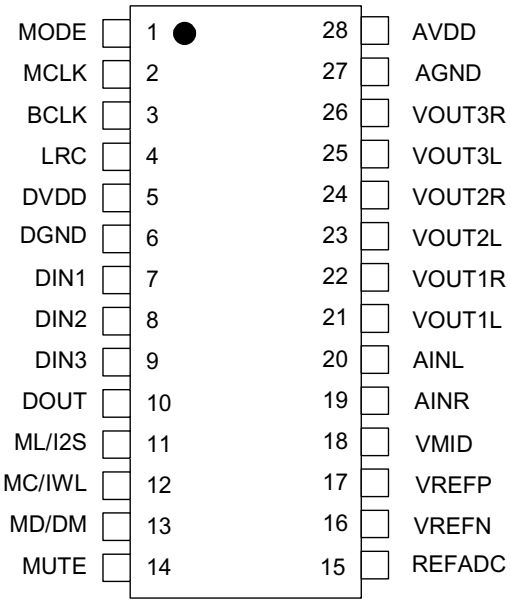
BLOCK DIAGRAM – 32 PIN TQFP



* extra pins on TQFP allow separate clocking of ADC and DAC

TABLE OF CONTENTS

PIN CONFIGURATION - 28 LEAD SSOP



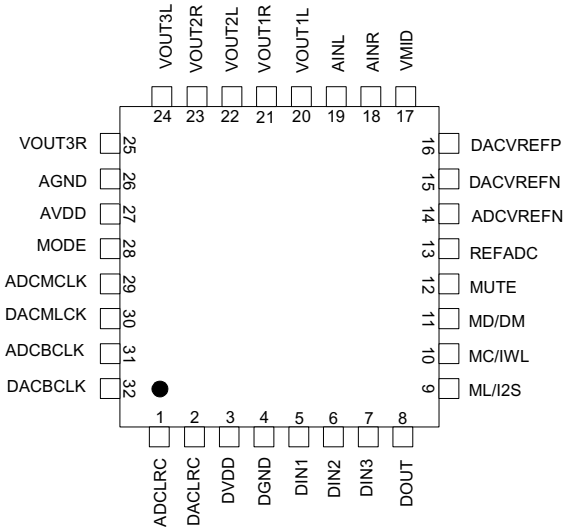
ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8772EDS	-25 to +85°C	28-pin SSOP	MSL1	260°C
WM8772EDS/R	-25 to +85°C	28-pin SSOP (tape and reel)	MSL1	260°C
WM8772SEDS/V	-25 to +85°C	28-pin SSOP (lead free)	MSL2	260°C
WM8772SEDS/RV	-25 to +85°C	28-pin SSOP (lead free, tape and reel)	MSL2	260°C

Note:

Reel quantity = 2,000

PIN CONFIGURATION
32 LEAD TQFP



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8772EFT	-25 to +85°C	32-lead TQFP	MSL1	240°C
WM8772SEFT/V	-25 to +85°C	32-lead TQFP (lead free)	MSL2	260°C
WM8772EFT/R	-25 to +85°C	32-lead TQFP (tape and reel)	MSL1	240°C
WM8772SEFT/RV	-25 to +85°C	32-lead TQFP (lead free, tape and reel)	MSL2	260°C

Note:

Reel quantity = 2,200

PIN DESCRIPTION – 28 LEAD SSOP

PIN	NAME	TYPE	DESCRIPTION
1	MODE	Digital input	Control format selection 0 = Software control 1 = Hardware control
2	MCLK	Digital input	Master clock; 256, 384, 512 or 768fs (fs = word clock frequency) (combined ADCMCLK and DACMCLK)
3	BCLK	Digital input/output	Audio interface bit clock (combined ADCBCLK and DACBCLK)
4	LRC	Digital input/output	Audio left/right word clock (combined ADCLRC and DACLRC)
5	DVDD	Supply	Digital positive supply
6	DGND	Supply	Digital negative supply
7	DIN1	Digital input	DAC channel 1 data input
8	DIN2	Digital input	DAC channel 2 data input
9	DIN3	Digital input	DAC channel 3 data input
10	DOUT	Digital output	ADC data output
11	ML/I2S	Digital input	Software Mode: Serial interface Latch signal Hardware Mode: Input Audio Data Format
12	MC/IWL	Digital input	Software Mode: Serial control interface clock Hardware Mode: Audio data input word length
13	MD/DM	Digital input	Software Mode: Serial interface data Hardware Mode: De-emphasis selection
14	MUTE	Digital input/output	DAC Zero Flag output or DAC mute input
15	REFADC	Analogue output	ADC reference buffer decoupling pin; 10uF external decoupling
16	VREFN	Supply	ADC and DAC negative supply
17	VREFP	Supply	DAC positive reference supply
18	VMID	Analogue output	Midrail divider decoupling pin; 10uF external decoupling
19	AINR	Analogue input	ADC right input
20	AINL	Analogue input	ADC left input
21	VOUT1L	Analogue output	DAC channel 1 left output
22	VOUT1R	Analogue output	DAC channel 1 right output
23	VOUT2L	Analogue output	DAC channel 2 left output
24	VOUT2R	Analogue output	DAC channel 2 right output
25	VOUT3L	Analogue output	DAC channel 3 left output
26	VOUT3R	Analogue output	DAC channel 3 right output
27	AGND	Supply	Analogue negative supply and substrate connection
28	AVDD	Supply	Analogue positive supply

Note: Digital input pins have Schmitt trigger input buffers.

PIN DESCRIPTION – 32 LEAD TQFP

PIN	NAME	TYPE	DESCRIPTION
1	ADCLRC	Digital Input/Output	ADC left/right word clock
2	DACLRC	Digital Input/Output	DAC left/right word clock
3	DVDD	Supply	Digital positive supply
4	DGND	Supply	Digital negative supply
5	DIN1	Digital Input	DAC channel 1 data input
6	DIN2	Digital Input	DAC channel 2 data input
7	DIN3	Digital Input	DAC channel 3 data input
8	DOUT	Digital Output	ADC data output
9	ML/I2S	Digital Input	Software Mode: Serial interface Latch signal Hardware Mode: Input Audio Data Format
10	MC/IWL	Digital Input	Software Mode: Serial control interface clock Hardware Mode: Audio data input word length
11	MD/DM	Digital Input	Software Mode: Serial interface data Hardware Mode: De-emphasis selection
12	MUTE	Digital Input/Output	DAC Zero Flag output or DAC Mute Input
13	REFADC	Analogue Output	ADC reference buffer decoupling pin; 10uF external decoupling
14	ADCVREFN	Supply	ADC negative supply
15	DACVREFN	Supply	DAC negative supply
16	DACVREFP	Supply	DAC positive reference supply
17	VMID	Analogue Output	Midrail divider decoupling pin; 10uF external decoupling
18	AINR	Analogue Input	ADC right input
19	AINL	Analogue Input	ADC left input
20	VOUT1L	Analogue Output	DAC channel 1 left output
21	VOUT1R	Analogue Output	DAC channel 1 right output
22	VOUT2L	Analogue Output	DAC channel 2 left output
23	VOUT2R	Analogue Output	DAC channel 2 right output
24	VOUT3L	Analogue Output	DAC channel 3 left output
25	VOUT3R	Analogue Output	DAC channel 3 right output
26	AGND	Supply	Analogue negative supply and substrate connection
27	AVDD	Supply	Analogue positive supply
28	MODE	Digital Input	Control format selection 0 = Software control 1 = Hardware control
29	ADCMCLK	Digital Input	Master ADC clock; 256, 384, 512 or 768fs (fs = word clock frequency)
30	DACMCLK	Digital Input	Master DAC clock; 256, 384, 512 or 768fs (fs = word clock frequency)
31	ADCBCLK	Digital Input/Output	ADC audio interface bit clock
32	DACBCLK	Digital Input/Output	DAC audio interface bit clock

Note: Digital input pins have Schmitt trigger input buffers.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+5V
Analogue supply voltage	-0.3V	+7V
Voltage range digital inputs [1]	DGND -0.3V	DVDD +0.3V
Voltage range analogue inputs [1]	AGND -0.3V	AVDD +0.3V
Master Clock Frequency		37MHz
Operating temperature range, T_A	-25°C	+85°C
Storage temperature after soldering	-65°C	+150°C
Package body temperature (soldering 10 seconds)		Refer to Ordering Information, p5 and p6
Package body temperature (soldering 2 minutes)		+183°C

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		2.7		3.6	V
Analogue supply range	AVDD, VREFP		2.7		5.5	V
Ground	AGND, VREFN, DGND			0		V
Difference DGND to AGND			-0.3	0	+0.3	V

Note: Digital supply DVDD must never be more than 0.3V greater than AVDD.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD, VREFP = 5V, DVDD = 3.3V, AGND, VREFN = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs, 32-pin TQFP version unless otherwise stated. ADC/DAC in Slave Mode unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC Performance (Load = 10kΩ, 50pF)						
0dBFs Full scale output voltage				1.0 x VREFP/5		V_{rms}
SNR (Note 1,2,4)		A-weighted, @ fs = 48kHz	95	103		dB
SNR (Note 1,2,4)		A-weighted @ fs = 96kHz		102		dB
SNR (Note 1,2,4)		A-weighted @ fs = 192kHz		101		dB
SNR (Note 1,2,4)		A-weighted @ fs = 48kHz, AVDD = 3.3V		99		dB
SNR (Note 1,2,4)		A-weighted @ fs = 96kHz, AVDD = 3.3V		99		dB
Dynamic Range (Note 2,4)	DNR	A-weighted, -60dB full scale input	90	103		dB
Total Harmonic Distortion (THD)		1kHz, 0dB.Fs		-90	-80	dB
Mute Attenuation		1kHz Input, 0dB gain		100		dB
DAC channel separation				100		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mV_{p-p}		50		dB
		20Hz to 20kHz 100mV_{p-p}		45		dB

Test Conditions

AVDD, VREFP = 5V, DVDD = 3.3V, AGND, VREFN = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs, 32-pin TQFP version unless otherwise stated. ADC/DAC in Slave Mode unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Performance						
Input Signal Level (0dB)				2.0 x REFADC/5		V_{rms}
Input resistance				20		kΩ
Input capacitance				10		pF
SNR (Note 1,2,4)		A-weighted, 0dB gain @ fs = 48kHz	80	100		dB
SNR (Note 1,2,4)		A-weighted, 0dB gain @ fs = 96kHz 64 x OSR		100		dB
SNR (Note 1,2,4)		A-weighted, 0dB gain @ fs = 48kHz, AVDD = 3.3V		93		dB
SNR (Note 1,2,4)		A-weighted, 0dB gain @ fs = 96kHz, AVDD = 3.3V 64 x OSR		93		dB
Total Harmonic Distortion (THD)		kHz, 0dBFs		-80		dB
		1kHz, -1dBFs		-82		dB
ADC Channel Separation		1kHz Input		90		dB
Mute Attenuation		1kHz Input, 0dB gain		90		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Digital Logic Levels (CMOS Levels)						
Input LOW level	V_{IL}				0.3 x DVDD	V
Input HIGH level	V_{IH}		0.7 x DVDD			V
Input leakage current				±0.2	±1	µA
Input capacitance				5		pF
Output LOW	V_{OL}	I_{OL}=1mA			0.1 x DVDD	V
Output HIGH	V_{OH}	I_{OH}= -1mA	0.9 x DVDD			V
Analogue Reference Levels						
Reference voltage	V_{VMID}		VREFP/2 – 50mV	VREFP/2	VREFP/2 + 50mV	V
Potential divider resistance	R_{VMID}	VREFP to VMID and VMID to VREFN		50		kΩ
Supply Current						
Analogue supply current		AVDD, VREFP = 5V		45		mA
Digital supply current		DVDD = 3.3V		16		mA

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted.
2. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
3. VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
5. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
6. Pass-Band Ripple - Any variation of the frequency response in the pass-band region.

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter					
Passband	±0.01 dB	0		0.4535fs	
	-6dB		0.5fs		
Passband ripple				±0.01	dB
Stopband		0.5465fs			
Stopband Attenuation	f > 0.5465fs	-65			dB
DAC Filter					
Passband	±0.05 dB			0.444fs	
	-3dB		0.487fs		
Passband ripple				±0.05	dB
Stopband		0.555fs			
Stopband Attenuation	f > 0.555fs	-60			dB

Table 1 Digital Filter Characteristics

DAC FILTER RESPONSES

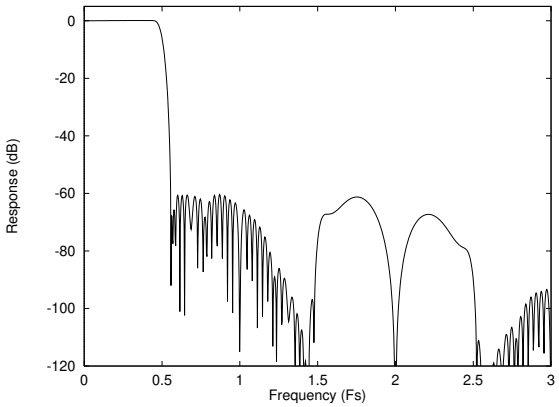


Figure 1 DAC Digital Filter Frequency Response – 44.1, 48 and 96KHz

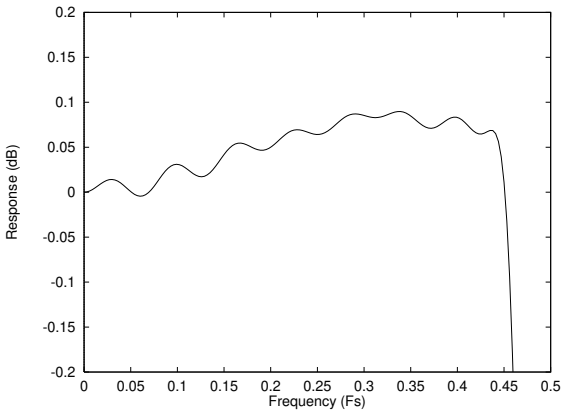


Figure 2 DAC Digital Filter Ripple –44.1, 48 and 96kHz

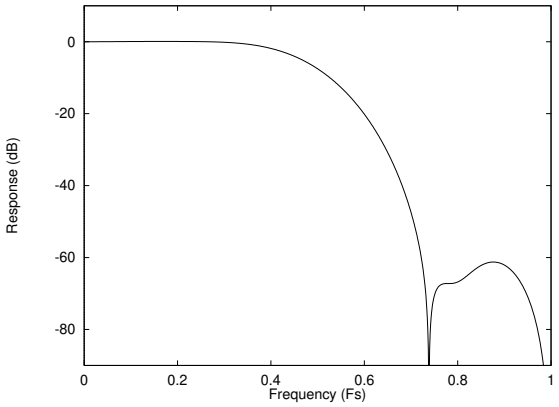


Figure 3 DAC Digital Filter Frequency Response – 192KHz

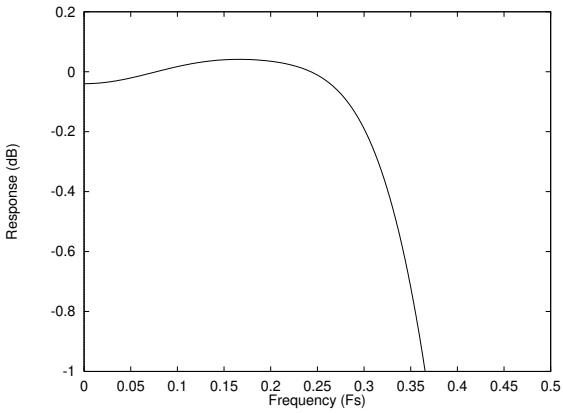


Figure 4 DAC Digital Filter Ripple – 192kHz

ADC FILTER RESPONSES

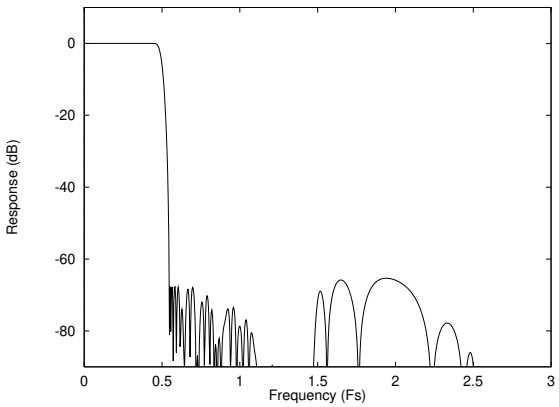


Figure 5 ADC Digital Filter Frequency Response

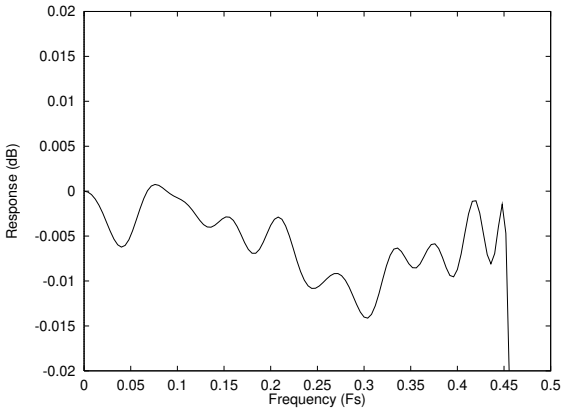


Figure 6 ADC Digital Filter Ripple

ADC HIGH PASS FILTER

The WM8772EDS has a selectable digital high pass filter to remove DC offsets. The filter response is characterised by the following polynomial.

$$H(z) = \frac{1 - z^{-1}}{1 - 0.9995z^{-1}}$$

DIGITAL DE-EMPHASIS CHARACTERISTICS

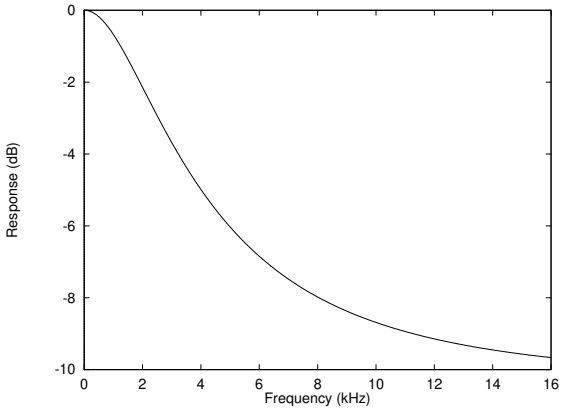


Figure 7 De-Emphasis Frequency Response (32kHz)

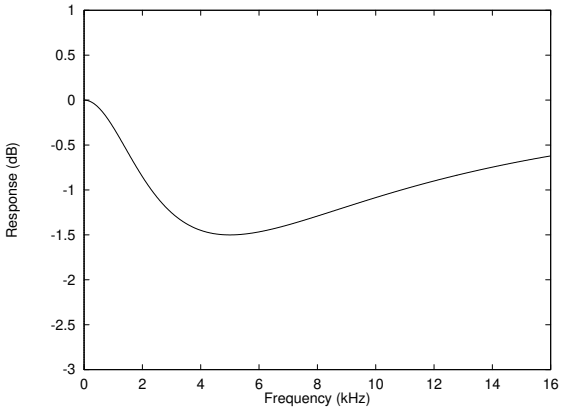


Figure 8 De-Emphasis Error (32KHz)

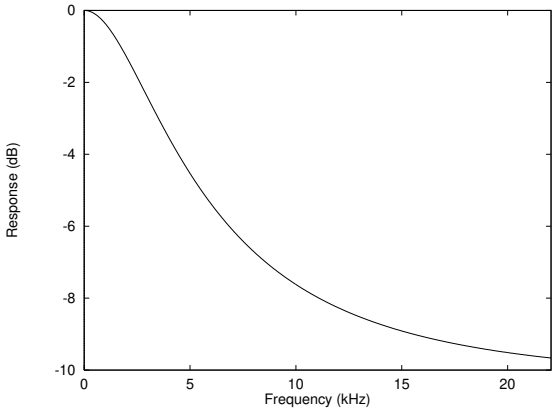


Figure 9 De-Emphasis Frequency Response (44.1KHz)

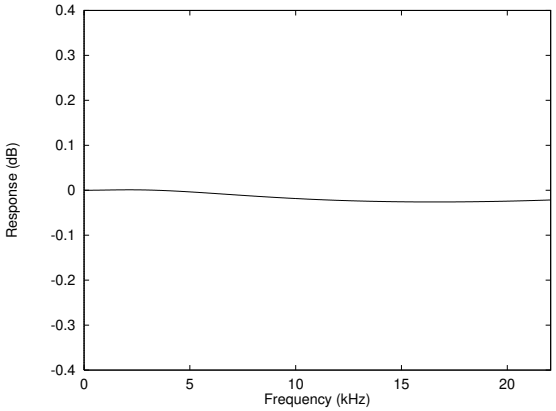


Figure 10 De-Emphasis Error (44.1KHz)

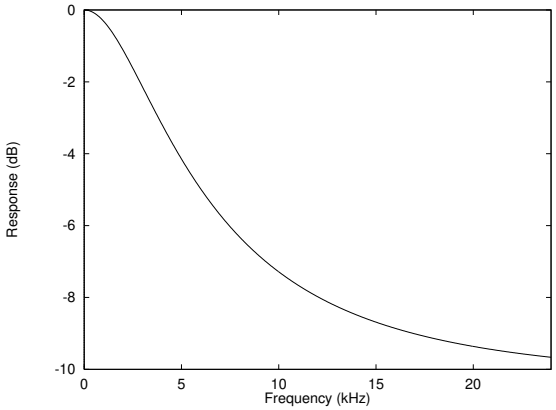


Figure 11 De-Emphasis Frequency Response (48kHz)

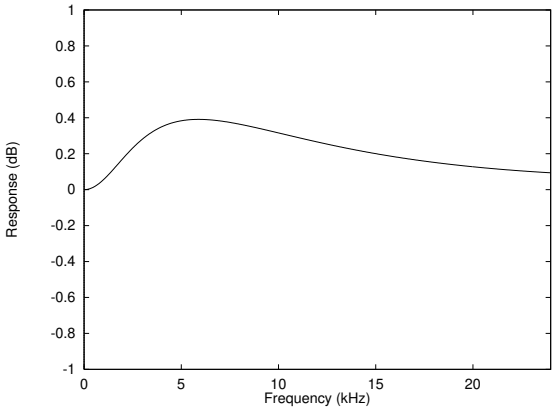


Figure 12 De-Emphasis Error (48kHz)

PAGES 12 TO 36 DESCRIBE THE OPERATION OF THE WM8772EDS 28 PIN SSOP PRODUCT VARIANT.

PAGES 37 TO 66 DESCRIBE THE OPERATION OF THE WM8772EFT 32 PIN TQFP PRODUCT VARIANT.

WM8772EDS – 28 PIN SSOP

MASTER CLOCK TIMING

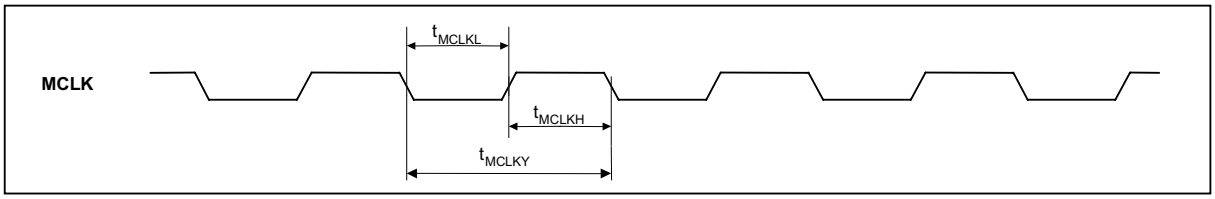


Figure 13 ADC and DAC Master Clock Timing Requirements

Test Conditions

AVDD, VREFP = 5V, DVDD = 3.3V, AGND, VREFN = 0V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, DACMCLK and ADCMCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK System clock pulse width high	t_{MCLKH}		11			ns
MCLK System clock pulse width low	t_{MCLKL}		11			ns
MCLK System clock cycle time	t_{MCLKY}		28			ns
MCLK Duty cycle			40:60		60:40	

Table 2 Master Clock Timing Requirements

DIGITAL AUDIO INTERFACE – MASTER MODE

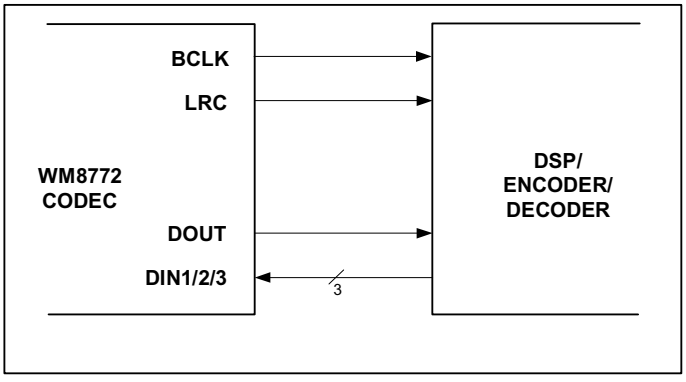


Figure 14 Audio Interface - Master Mode

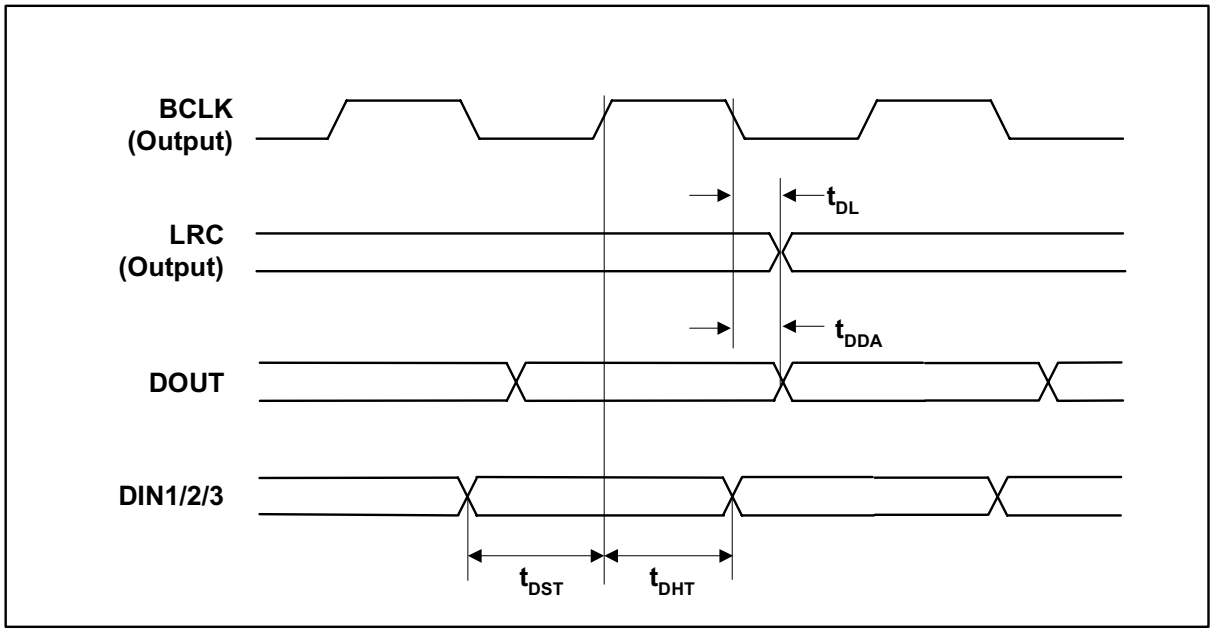


Figure 15 Digital Audio Data Timing – Master Mode

Test Conditions

AVDD, VREFP = 5V, DVDD = 3.3V, AGND, VREFN, DGND = 0V, T_A = +25°C, Master Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
LRC propagation delay from BCLK falling edge	t_{DL}		0		10	ns
DOUT propagation delay from BCLK falling edge	t_{DDA}		0		10	ns
DIN1/2/3 setup time to BCLK rising edge	t_{DST}		10			ns
DIN1/2/3 hold time from BCLK rising edge	t_{DHT}		10			ns

Table 3 Digital Audio Data Timing – Master Mode

DIGITAL AUDIO INTERFACE – SLAVE MODE

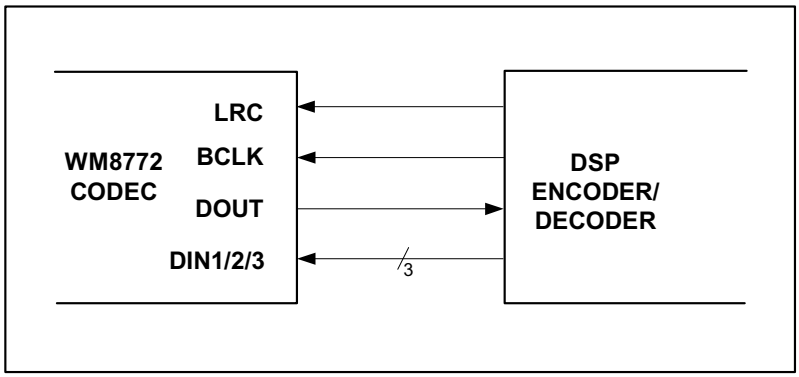


Figure 16 Audio Interface – Slave Mode

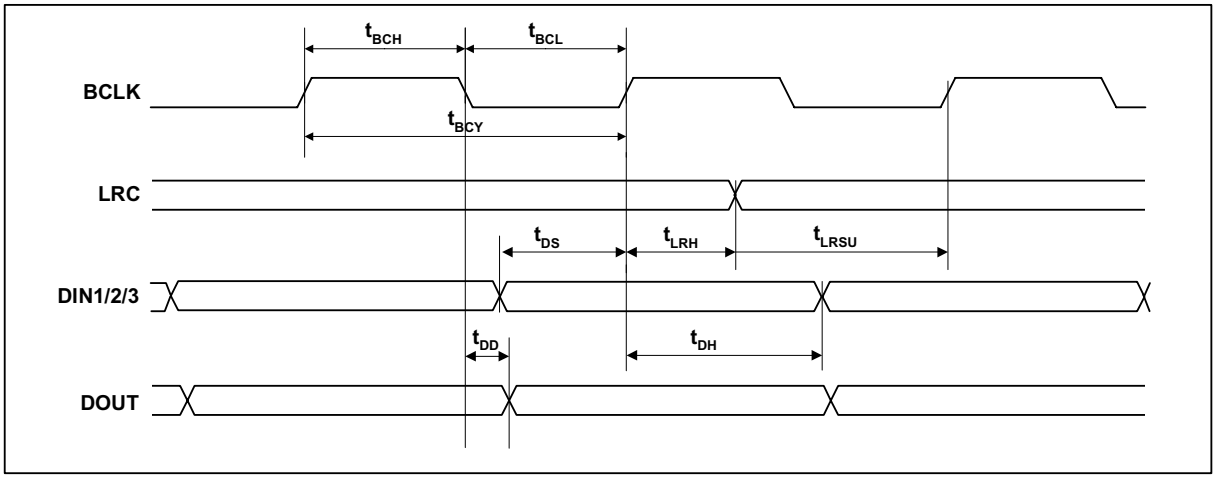


Figure 17 Digital Audio Data Timing – Slave Mode

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCLK cycle time	t_{BCY}		50			ns
BCLK pulse width high	t_{BCH}		20			ns
BCLK pulse width low	t_{BCL}		20			ns
LRC set-up time to BCLK rising edge	t_{LRSU}		10			ns
LRC hold time from BCLK rising edge	t_{LRH}		10			ns
DIN1/2/3 set-up time to BCLK rising edge	t_{DS}		10			ns
DIN1/2/3 hold time from BCLK rising edge	t_{DH}		10			ns

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DOUT propagation delay from BCLK falling edge	t_{DD}		0		10	ns

Table 4 Digital Audio Data Timing – Slave Mode

MPU INTERFACE TIMING

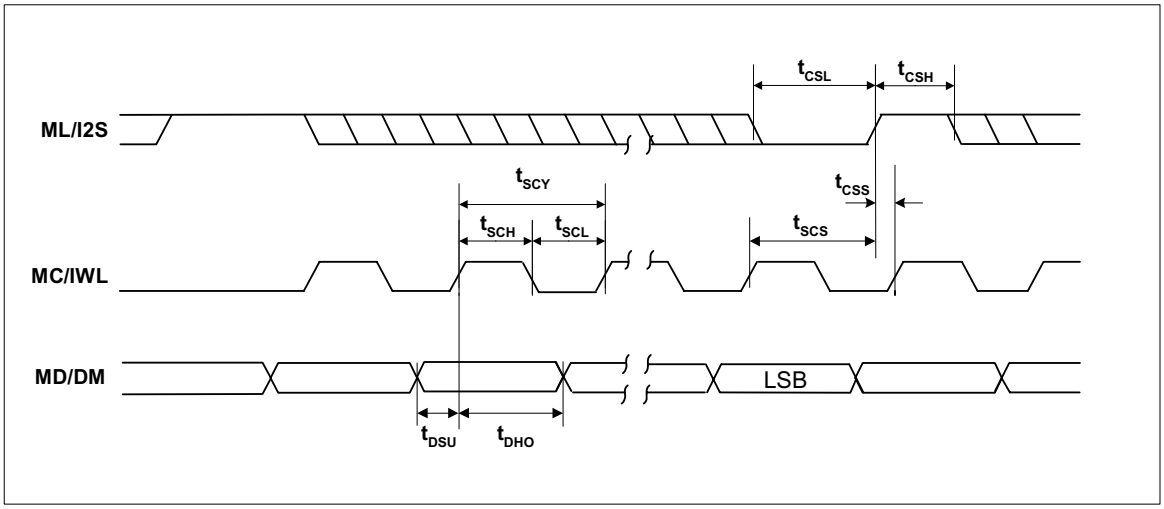


Figure 18 SPI Compatible Control Interface Input Timing

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND, DGND = 0V, T_A = +25°C, fs = 48kHz, DACMCLK and ADCMCLK = 256fs unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
MC/IWL rising edge to ML/I2S rising edge	t_{SCS}	60			ns
MC/IWL pulse cycle time	t_{SCY}	80			ns
MC/IWL pulse width low	t_{SCL}	30			ns
MC/IWL pulse width high	t_{SCH}	30			ns
MD/DM to MC/IWL set-up time	t_{DSU}	20			ns
MC/IWL to MD/DM hold time	t_{DHO}	20			ns
ML/I2S pulse width low	t_{CSL}	20			ns
ML/I2S pulse width high	t_{CSH}	20			ns
ML/I2S rising to MC/IWL rising	t_{CSS}	20			ns

Table 5 3-Wire SPI Compatible Control Interface Input Timing Information

DEVICE DESCRIPTION

INTRODUCTION

WM8772EDS is a complete 6-channel DAC, 2-channel ADC audio codec, including digital interpolation and decimation filters, multi-bit sigma delta stereo ADC, and switched capacitor multi-bit sigma delta DACs with digital volume controls on each channel and output smoothing filters.

The device is implemented as three separate stereo DACs and a stereo ADC in a single package and controlled by a single interface.

Each stereo DAC has its own data input DIN1/2/3, the stereo ADC has it's own data output DOUT. The word clock LRC, bit clock BCLK and master clock MCLK are shared between them.

The Audio Interface may be configured to operate in either master or slave mode. In Slave mode LRC and BCLK are all inputs. In Master mode LRC and BCLK are all outputs.

Each DAC has its own digital volume control that is adjustable in 0.5dB steps. The digital volume controls may be operated independently. In addition, a zero cross detect circuit is provided for each DAC for the digital volume controls. The digital volume control detects a transition through the zero point before updating the volume. This minimises audible clicks and 'zipper' noise as the gain values change.

Control of internal functionality of the device is by 3-wire serial or pin programmable control interface. The software control interface may be asynchronous to the audio data interface as control data will be re-synchronised to the audio processing internally.

Operation using master clocks of 128fs, 192fs, 256fs, 384fs, 512fs or 768fs is provided for the DAC, for operation of both the ADC and DAC master clocks of 256fs, 384fs, 512fs and 768fs is provided. In Slave mode selection between clock rates is automatically controlled. In master mode, the sample rate is set by control bits RATE. Audio sample rates (fs) from less than 8ks/s up to 192ks/s are allowed for the DAC and from less than 32ks/s up to 96ks/s for the ADC, provided the appropriate master clock is input.

The audio data interface supports right, left and I^2S interface formats along with a highly flexible DSP serial port interface.

AUDIO DATA SAMPLING RATES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. The external master system clock can be applied directly through the MCLK input pin with no software configuration necessary. In a system where there are a number of possible sources for the reference clock it is recommended that the clock source with the lowest jitter be used to optimise the performance of the ADC and DAC.

The master clock for WM8772EDS supports audio sampling rates from 128fs to 768fs, where fs is the audio sampling frequency (LRC) typically 32kHz, 44.1kHz, 48kHz, 96kHz or 192kHz (for DAC operation only). For ADC operation sample rates from 256fs to 768fs are supported. The master clock is used to operate the digital filters and the noise shaping circuits.

In Slave mode the WM8772EDS has a master clock detection circuit that automatically determines the relationship between the system clock frequency and the sampling rate (to within +/- 32 master clocks). If there is a greater than 32 clocks error the interface defaults to 768fs mode. The master clocks must be synchronised with LRC, although the WM8772EDS is tolerant of phase variations or jitter on this clock. Table 6 shows the typical master clock frequency inputs for the WM8772EDS.

The signal processing for the WM8772EDS typically operates at an oversampling rate of 128fs for both ADC and DAC. The exception to this for the DAC is for operation with a 128/192fs system clock, e.g. for 192kHz operation, when the oversampling rate is 64fs. For ADC operation at 96kHz it is recommended that the user set the ADCOSR bit. This changes the ADC signal processing oversample rate to 64fs.

SAMPLING RATE (LRC)	System Clock Frequency (MHz)					
	128fs	192fs	256fs	384fs	512fs	768fs
32kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1kHz	5.6448	8.467	11.2896	16.9340	22.5792	33.8688
48kHz	6.144	9.216	12.288	18.432	24.576	36.864
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable

Table 6 System Clock Frequencies Versus Sampling Rate (ADC does not support 128fs and 192fs)

HARDWARE CONTROL MODES

When the MODE pin is held high, the following hardware modes of operation are available.

Note: When in hardware mode the ADC and DAC will only run in slave mode.

MUTE AND AUTOMUTE OPERATION

In both hardware and software modes, MUTE controls the selection of MUTE directly, and can be used to enable and disable the automute function. This pin becomes an output when left floating and indicates infinite ZERO detect (IZD) has been detected.

	DESCRIPTION
0	Normal Operation
1	Mute DAC channels
Floating	Enable IZD, MUTE becomes an output to indicate when IZD occurs. L=IZD detected, H=IZD not detected.

Table 7 Mute and Automute Control

Figure 19 shows the application and release of MUTE whilst a full amplitude sinusoid is being played at 48kHz sampling rate. When MUTE (lower trace) is asserted, the output (upper trace) begins to decay exponentially from the DC level of the last input sample. The output will decay towards V_{MID} with a time constant of approximately 64 input samples. If MUTE is applied to all channels for 1024 or more input samples the outputs will be connected directly to V_{MID} if IZD is set. When MUTE is de-asserted, the output will restart immediately from the current input sample.

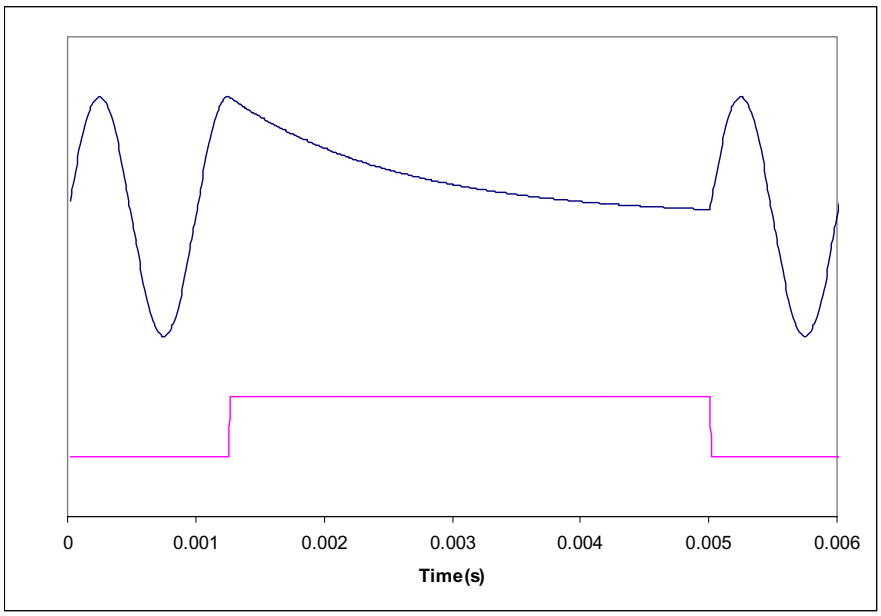


Figure 19 Application and Release of Soft Mute

The MUTE pin is an input to select mute or not mute. MUTE is active high; taking the pin high causes the filters to soft mute, ramping down the audio signal over a few milliseconds. Taking MUTE low again allows data into the filter.

The automute function detects a series of ZERO value audio samples of 1024 samples long being applied to both channels. After such an event, a latch is set whose output (AUTOMUTED) is wire OR'ed through a 10kΩ resistor to the MUTE pin. Thus if the MUTE pin is not being driven, the automute function will assert mute.

If MUTE is tied low, AUTOMUTED is overridden and will not mute unless the IZD register bit is set. If MUTE is driven from a bi-directional source, then both MUTE and automute functions are available. If MUTE is not driven, AUTOMUTED appears as a weak output (10kΩ source impedance) and can be used to drive external mute circuits. AUTOMUTED will be removed as soon as any channel receives a non-ZERO input.

A diagram showing how the various Mute modes interact is shown below Figure 20.

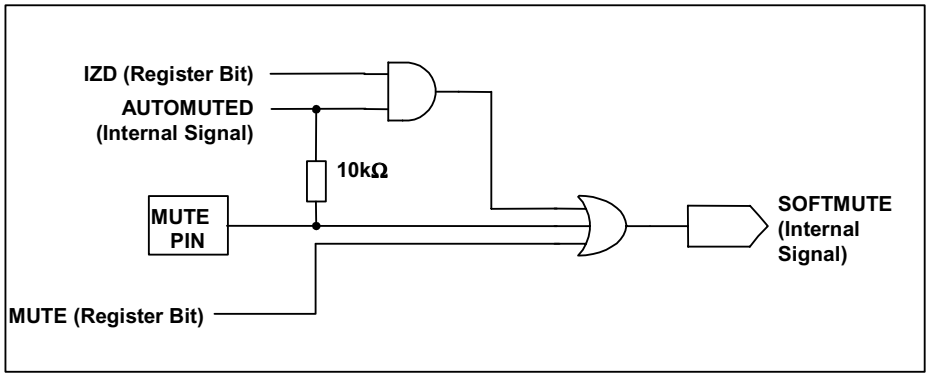


Figure 20 Selection Logic for MUTE Modes

INPUT FORMAT SELECTION

In hardware mode, ML/I2S and MC/IWL become input controls for selection of input data format type and input data word length for both the ADC and DAC.

ML/I2S	MC/IWL	INPUT DATA MODE
0	0	24-bit right justified
0	1	20-bit right justified
1	0	16-bit I^2S
1	1	24-bit I^2S

Table 8 Input Format Selection

Note:

In 24 bit I^2S mode, any width of 24 bits or less is supported provided that the left/right clocks (LRC) are high for a minimum of 24 bit clocks (BCLK) and low for a minimum of 24 bit clocks.

DE-EMPHASIS CONTROL

In hardware mode, the MD/DM pin becomes an input control for selection of de-emphasis filtering to be applied.

MD/DM	DE-EMPHASIS
0	Off
1	On

Table 9 De-emphasis Control

DIGITAL AUDIO INTERFACE

MASTER AND SLAVE MODES

The audio interface operates in either Slave or Master mode, selectable using the MS control bit. In both Master and Slave modes DIN1/2/3 are always inputs to the WM8772EDS and DOUT is always an output. The default is Slave mode.

In Slave mode, LRC and BCLK are inputs to the WM8772EDS (Figure 21). DIN1/2/3 and LRC are sampled by the WM8772EDS on the rising edge of BCLK. ADC data is output on DOUT and changes on the falling edge of BCLK.

By setting the control bit BCP the polarity of BCLK may be reversed so that DIN1/2/3 and LRC are sampled on the falling edge of BCLK and DOUT changes on the rising edge of BCLK.

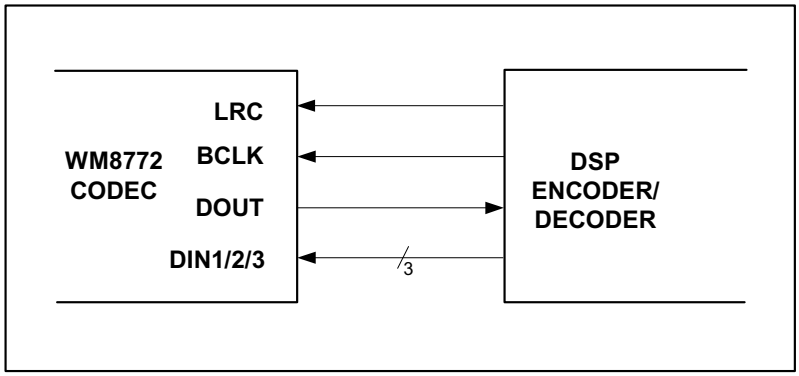


Figure 21 Slave Mode

In Master mode, LRC and BCLK are outputs from the WM8772EDS (Figure 22). LRC and BCLK are generated by the WM8772EDS. DIN1/2/3 are sampled by the WM8772EDS on the rising edge of BCLK so the controller must output DAC data that changes on the falling edge of BCLK. ADC data is output on DOUT and changes on the falling edge of BCLK.

By setting control bit BCP the polarity of BCLK may be reversed so that DIN1/2/3 are sampled on the falling edge of BCLK, and DOUT changes on the rising edge of BCLK.

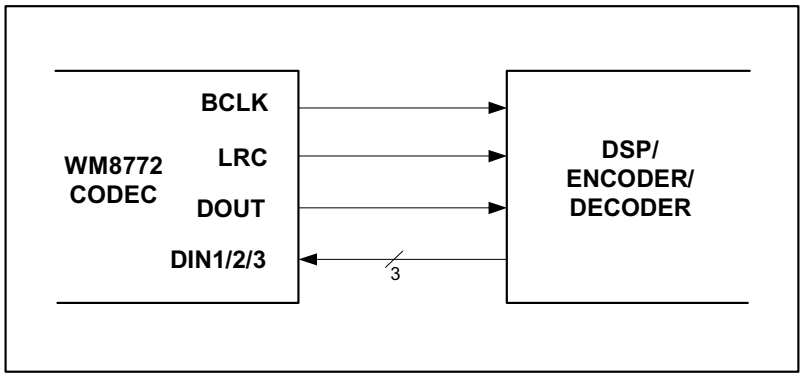


Figure 22 Master Mode

AUDIO INTERFACE FORMATS

Audio data is applied to the internal DAC filters, or output from the ADC filters, via the Digital Audio Interface. 5 popular interface formats are supported:

- Left Justified mode
- Right Justified mode
- I^2S mode
- DSP Early mode
- DSP Late mode

All 5 formats send the MSB first and support word lengths of 16, 20, 24 and 32 bits, with the exception of 32 bit right justified mode, which is not supported.

In left justified, right justified and I^2S modes, the digital audio interface receives DAC data on the DIN1/2/3 inputs and outputs ADC data on DOUT. Audio Data for each stereo channel is time multiplexed with LRC indicating whether the left or right channel is present. LRC is also used as a timing reference to indicate the beginning or end of the data words.

In left justified, right justified and I^2S modes, the minimum number of BCLKs per LRC period is 2 times the selected word length. LRC must be high for a minimum of word length BCLKs and low for a minimum of word length BCLKs. Any mark to space ratio on LRC is acceptable provided the above requirements are met.

In DSP early or DSP late mode, all 6 DAC channels are time multiplexed onto DIN1. LRC is used as a frame sync signal to identify the MSB of the first word. The minimum number of BCLKs per LRC period is 6 times the selected word length. Any mark to space ratio is acceptable on LRC provided the rising edge is correctly positioned. The ADC data may also be output in DSP early or late modes, with LRC used as a frame sync to identify the MSB of the first word. The minimum number of BCLKs per LRC period is 2 times the selected word length if only the ADC is being operated.

LEFT JUSTIFIED MODE

In left justified mode, the MSB of DIN1/2/3 is sampled by the WM8772EDS on the first rising edge of BCLK following a LRC transition. The MSB of the ADC data is output on DOUT and changes on the same falling edge of BCLK as LRC and may be sampled on the rising edge of BCLK. LRC is high during the left samples and low during the right samples (Figure 23).

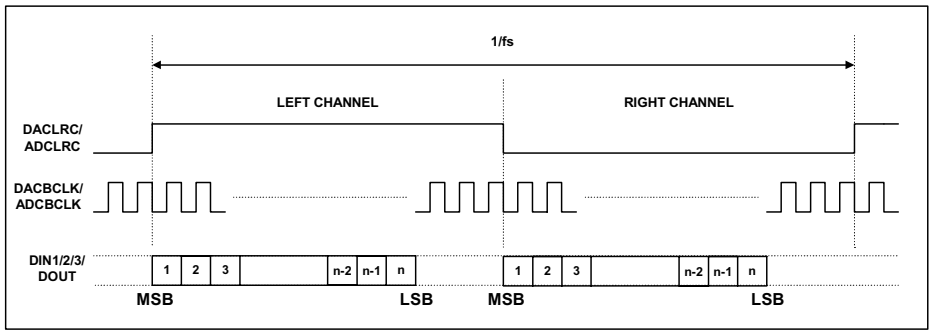


Figure 23 Left Justified Mode Timing Diagram

RIGHT JUSTIFIED MODE

In right justified mode, the LSB of DIN1/2/3 is sampled by the WM8772EDS on the rising edge of BCLK preceding a LRC transition. The LSB of the ADC data is output on DOUT and changes on the falling edge of BCLK preceding a LRC transition and may be sampled on the rising edge of BCLK. LRC are high during the left samples and low during the right samples (Figure 24).

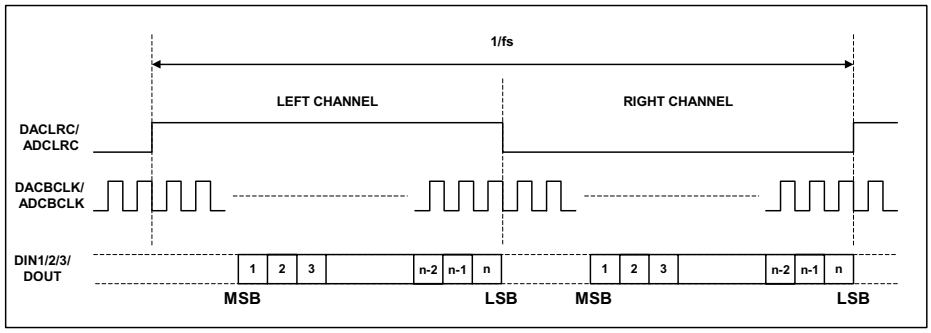


Figure 24 Right Justified Mode Timing Diagram

I²S MODE

In I²S mode, the MSB of DIN1/2/3 is sampled by the WM8772EDS on the second rising edge of BCLK following a LRC transition. The MSB of the ADC data is output on DOUT and changes on the first falling edge of BCLK following an LRC transition and may be sampled on the rising edge of BCLK. LRC are low during the left samples and high during the right samples.

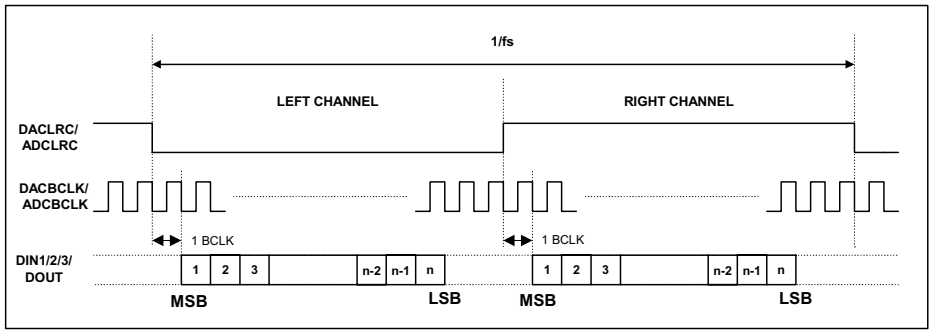


Figure 25 I²S Mode Timing Diagram

DSP EARLY MODE

In DSP early mode, the MSB of DAC channel 1 left data is sampled by the WM8772EDS on the second rising edge on BCLK following a LRC rising edge. DAC channel 1 right and DAC channels 2 and 3 data follow DAC channel 1 left data (Figure 26).

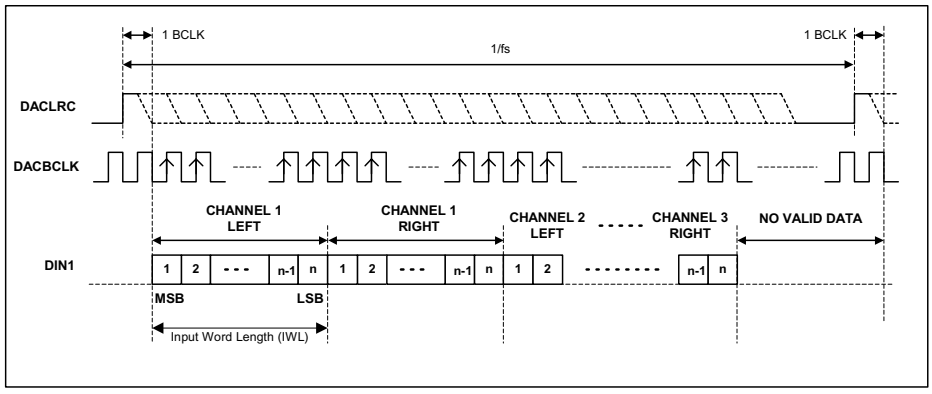


Figure 26 DSP Early Mode Timing Diagram – DAC Data Input