



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



24-bit, 192kHz Stereo CODEC

DESCRIPTION

The WM8778 is a high performance, stereo audio CODEC. It is ideal for surround sound processing applications for home hi-fi, DVD-RW and other audio visual equipment.

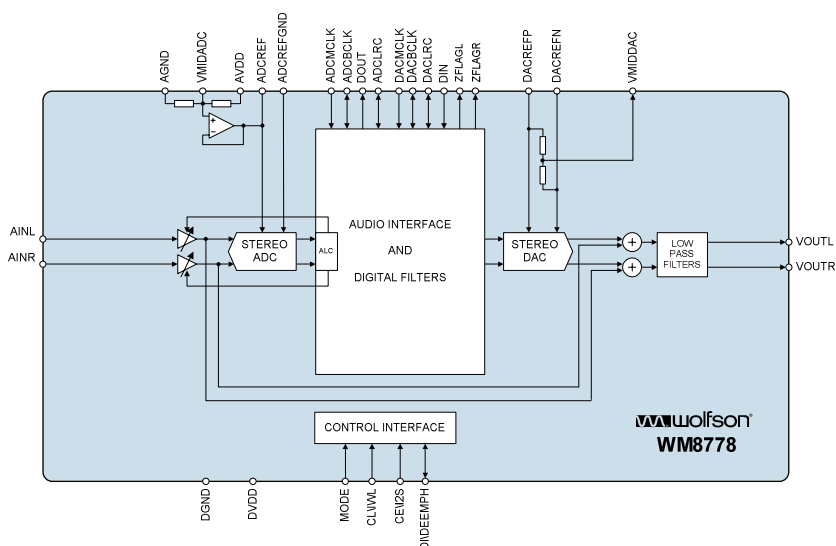
The stereo 24-bit multi-bit sigma delta ADC has programmable gain with automatic level control. Digital audio output word lengths from 16-32 bits and sampling rates from 32kHz to 96kHz are supported.

A stereo multi-bit sigma delta DAC is used with digital audio input word lengths from 16-32 bits and sampling rates from 32kHz to 192kHz. A multiplexor after the DAC allows the selection of either an external analogue input or DAC playback into the line outputs.

The WM8778 supports fully independent sample rates for the ADC and DAC. The audio data interface supports I²S, left justified, right justified and DSP formats.

The device is controlled in software via a 2 or 3 wire serial interface which provides access to all features including volume controls, mutes, and de-emphasis facilities. It can also be controlled in hardware which gives access to the most commonly used features. Control interface selection is done via the MODE pin (tri-level). The device is available in a 28-lead SSOP package.

BLOCK DIAGRAM



FEATURES

- Audio Performance
 - 108dB SNR ('A' weighted @ 48kHz) DAC
 - 102dB SNR ('A' weighted @ 48kHz) ADC
- DAC Sampling Frequency: 32kHz – 192kHz
- ADC Sampling Frequency: 32kHz – 96kHz
- Stereo ADC input analogue gain adjust from +24dB to -21dB in 0.5dB steps
- ADC digital gain from -21.5dB to -103dB in 0.5dB steps
- Programmable Automatic Level Control (ALC) or Limiter on ADC input.
- Stereo DAC with analogue line outputs.
- 3-Wire SPI Compatible or 2-wire Serial Control Interface
- Hardware Control Mode
- Master or Slave Clocking Mode
- Programmable Audio Data Interface Modes
 - I²S, Left, Right Justified or DSP
 - 16/20/24/32 bit Word Lengths
- Analogue Bypass Path Feature
- 2.7V to 5.5V Analogue, 2.7V to 3.6V Digital supply Operation

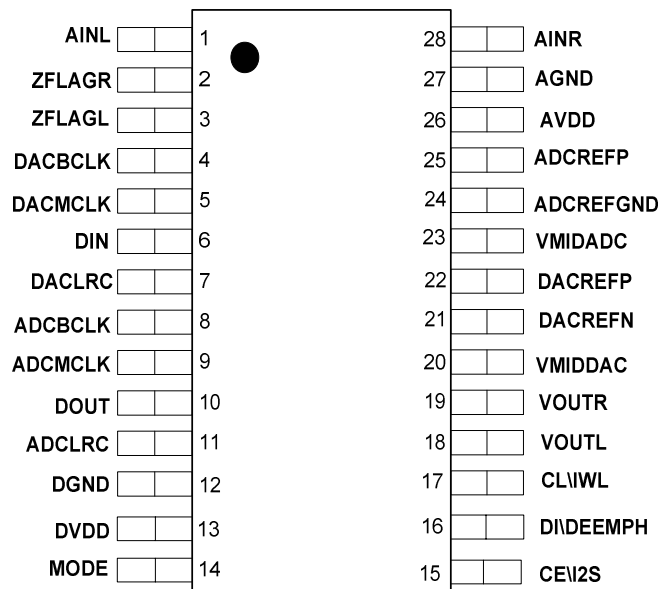
APPLICATIONS

- Surround Sound AV Processors and Hi-Fi systems
- DVD-RW

TABLE OF CONTENTS

DESCRIPTION	1
FEATURES.....	1
APPLICATIONS	1
BLOCK DIAGRAM	1
TABLE OF CONTENTS	2
PIN CONFIGURATION.....	3
ORDERING INFORMATION	3
ABSOLUTE MAXIMUM RATINGS.....	5
ELECTRICAL CHARACTERISTICS	6
TERMINOLOGY	7
MASTER CLOCK TIMING.....	8
DIGITAL AUDIO INTERFACE – MASTER MODE	8
DIGITAL AUDIO INTERFACE – SLAVE MODE	9
3-WIRE MPU INTERFACE TIMING	11
CONTROL INTERFACE TIMING – 2-WIRE MODE	12
INTERNAL POWER ON RESET CIRCUIT	13
DEVICE DESCRIPTION	15
INTRODUCTION	15
AUDIO DATA SAMPLING RATES.....	15
ZERO DETECT	17
POWERDOWN MODES	17
DIGITAL AUDIO INTERFACE	17
CONTROL INTERFACE OPERATION	22
CONTROL INTERFACE REGISTERS	24
LIMITER / AUTOMATIC LEVEL CONTROL (ALC).....	32
REGISTER MAP	38
DIGITAL FILTER CHARACTERISTICS	45
DAC FILTER RESPONSES.....	45
ADC FILTER RESPONSES.....	46
ADC HIGH PASS FILTER	46
DIGITAL DE-EMPHASIS CHARACTERISTICS.....	47
APPLICATIONS INFORMATION	48
RECOMMENDED EXTERNAL COMPONENTS.....	48
PACKAGE DIMENSIONS	50
IMPORTANT NOTICE	51
ADDRESS:	51

PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMP
WM8778SEDS/V	-25 to +85°C	28-lead SSOP (Pb-free)	MSL3	260°C
WM8778SEDS/RV	-25 to +85°C	28-lead SSOP (Pb-free, tape and reel)	MSL3	260°C

Note:

Reel quantity = 2,000

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	AINL	Analogue Input	Left channel input
2	ZFLAGR	Digital Output	Right channel zero flag output (external pull-up required)
3	ZFLAGL	Digital Output	Left channel zero flag output (external pull-up required)
4	DACBCLK	Digital Input/Output	DAC audio interface bit clock
5	DACMCLK	Digital Input	Master DAC clock; 256, 384, 512 or 768fs (fs = word clock frequency)
6	DIN	Digital Input	DAC data input
7	DACLRC	Digital Input/Output	DAC left/right word clock
8	ADCBCLK	Digital Input/Output	ADC audio interface bit clock
9	ADCMCLK	Digital Input	Master ADC clock; 256, 384, 512 or 768fs (fs = word clock frequency)
10	DOUT	Digital Output	ADC data output
11	ADCLRC	Digital Input/Output	ADC left/right word clock
12	DGND	Supply	Digital negative supply
13	DVDD	Supply	Digital positive supply
14	MODE	Digital Input	Control interface mode select, tri-level
15	CE 2S	Digital Input	Serial interface Latch signal
16	DI DEMPH	Digital Input/Output	Serial interface data
17	CL WL	Digital Input	Serial interface clock
18	VOU TL	Analogue Output	DAC channel left output
19	VOU TR	Analogue Output	DAC channel right output
20	VMIDDAC	Analogue Output	DAC midrail decoupling pin ; 10uF external decoupling
21	DACREFN	Analogue Input	DAC negative reference input
22	DACREFP	Analogue Input	DAC positive reference input
23	VMIDADC	Analogue Output	ADC midrail divider decoupling pin; 10uF external decoupling
24	ADCREFGND	Analogue Output	ADC reference buffer decoupling pin; 10uF external decoupling
25	ADCREFP	Analogue Output	ADC positive reference decoupling pin; 10uF external decoupling
26	AVDD	Supply	Analogue positive supply
27	AGND	Supply	Analogue negative supply and substrate connection
28	AINR	Analogue Input	Right channel input

Note : Digital input pins have Schmitt trigger input buffers.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+3.63V
Analogue supply voltage	-0.3V	+7V
Voltage range digital inputs (MCLK, DIN, ADCLRC, DACLRC, ADCBCLK, DACBCLK, DI, CL, CE and MODE)	DGND -0.3V	DVDD + 0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Master Clock Frequency		37MHz
Operating temperature range, T _A	-25°C	+85°C
Storage temperature	-65°C	+150°C

Notes:

- Analogue and digital grounds must always be within 0.3V of each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		2.7		3.6	V
Analogue supply range	AVDD, DACREFP		2.7		5.5	V
Ground	AGND, DGND, DACREFN, ADCREFGND			0		V
Difference DGND to AGND			-0.3	0	+0.3	V

Note: Digital supply DVDD must never be more than 0.3V greater than AVDD.

ELECTRICAL CHARACTERISTICS**Test Conditions**

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (TTL Levels)						
Input LOW level	V _{IL}				0.8	V
Input HIGH level	V _{IH}		2.0			V
Output LOW	V _{OL}	I _{OL} =1mA			0.1 x DVDD	V
Output HIGH	V _{OH}	I _{OH} =1mA	0.9 x DVDD			V
Analogue Reference Levels						
Reference voltage	V _{VMID}			AVDD/2		V
Potential divider resistance	R _{VMID}			50k		Ω
DAC Performance (Load = 10k Ω, 50pF)						
0dBfs Full scale output voltage				1.0 x AVDD/5		V _{rms}
SNR (Note 1,2)		A-weighted, @ fs = 48kHz	102	108		dB
SNR (Note 1,2)		A-weighted @ fs = 96kHz		108		dB
Dynamic Range (Note 2)	DNR	A-weighted, -60dB full scale input	102	108		dB
Total Harmonic Distortion (THD)		1kHz, 0dBfs		-97	-90	dB
DAC channel separation				100		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
ADC Performance						
Input Signal Level (0dB)				1.0 x AVDD/5		V _{rms}
SNR (Note 1,2)		A-weighted, 0dB gain @ fs = 48kHz	97	102		dB
SNR (Note 1,2)		A-weighted, 0dB gain @ fs = 96kHz 64 x OSR		99		dB
Dynamic Range (note 2)		A-weighted, -60dB full scale input		102		dB
Total Harmonic Distortion (THD)		1kHz, 0dBfs		-92		dB
		1kHz, -1dBfs		-95	-85	dB
ADC Channel Separation		1kHz Input		90		dB

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated.

Programmable Gain Step Size			0.25	0.5	0.75	dB
Programmable Gain Range (Analogue)		1kHz Input	-21		+24	dB
Programmable Gain Range (Digital)		1kHz Input	-103		-21.5	dB
Analogue Mute Attenuation (Note 6)		1kHz Input, 0dB gain		76		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Analogue input (AIN) to Analogue output (VOUT) (Load=10k Ω, 50pF, gain = 0dB) Bypass Mode						
0dB Full scale output voltage				1.0 x AVDD/5		Vrms
SNR (Note 1)			99	103		dB
THD		1kHz, 0dB		-93		dB
		1kHz, -3dB		-95		dB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Mute Attenuation		1kHz, 0dB		100		dB
Supply Current						
Analogue supply current		AVDD = 5V		48		mA
Digital supply current		DVDD = 3.3V		8		mA

Notes:

- Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted.
- All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
- VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).
- Harmonic distortion on the headphone output decreases with output power.
- All performance measurement done using certain timings conditions (Please refer to section 'Digital Audio Interface').
- A full digital MUTE can be achieved if the ADC gain (LAG/RAG) is set to minimum.

TERMINOLOGY

- Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
- Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
- THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
- Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
- Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
- Pass-Band Ripple - Any variation of the frequency response in the pass-band region.

MASTER CLOCK TIMING

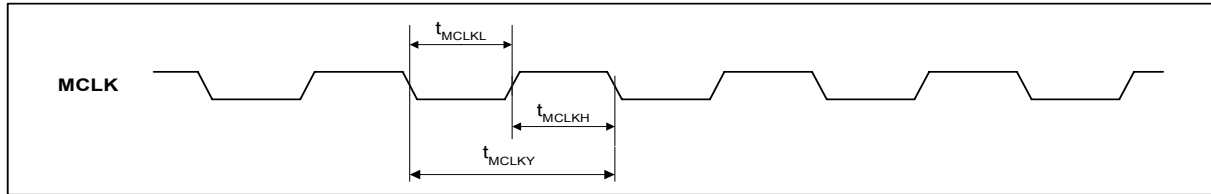


Figure 1 Master Clock Timing Requirements

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, ADC/DACMCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
ADC/DACMCLK System clock pulse width high	t_{MCLKH}		11			ns
ADC/DACMCLK System clock pulse width low	t_{MCLKL}		11			ns
ADC/DACMCLK System clock cycle time	t_{MCLKY}		28		1000	ns
ADC/DACMCLK Duty cycle			40:60		60:40	
Power-saving mode activated		After MCLK stopped	2		10	µs
Normal mode resumed		After MCLK re-started	0.5		1	MCLK cycle

Table 1 Master Clock Timing Requirements

Note:

If MCLK period is longer than maximum specified above, power-saving mode is entered and DACs are powered down with internal digital audio filters being reset. In this power-saving mode, all registers will retain their values and can be accessed in the normal manner through the control interface. Once MCLK is restored, the DACs are automatically powered up, but a write to the volume update register bit is required to restore the correct volume settings.

DIGITAL AUDIO INTERFACE – MASTER MODE

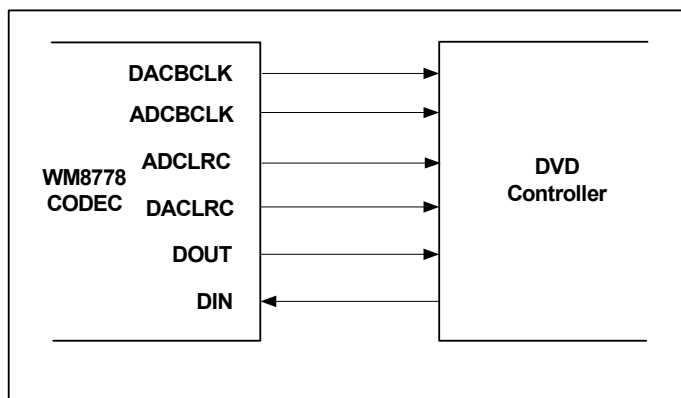


Figure 2 Audio Interface - Master Mode

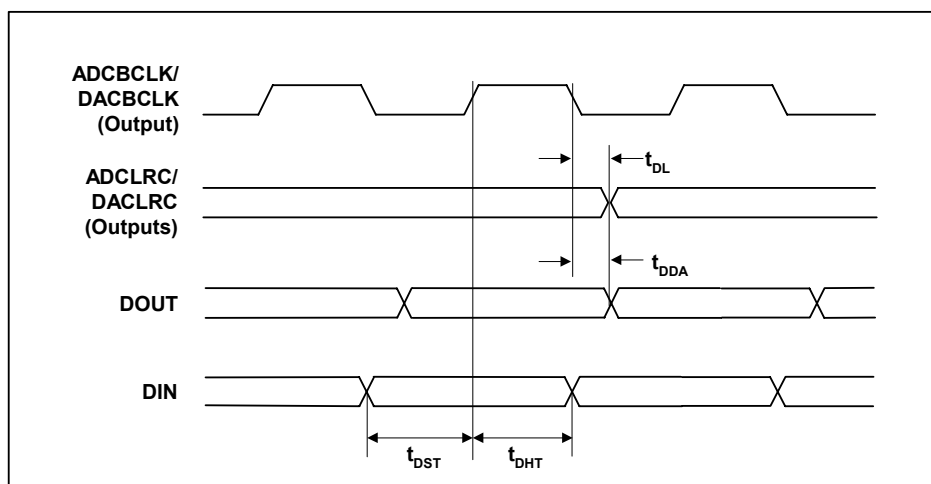


Figure 3 Digital Audio Data Timing – Master Mode

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, T_A = +25°C, Master Mode, fs = 48kHz, ADC/DACMCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
ADC/DACLRC propagation delay from ADC/DACBCLK falling edge	t _{DL}		0		10	ns
DOUT propagation delay from ADCBCLK falling edge	t _{DDA}		0		10	ns
DIN setup time to DACBCLK rising edge	t _{DST}		10			ns
DIN hold time from DACBCLK rising edge	t _{DHT}		10			ns

Table 2 Digital Audio Data Timing – Master Mode

DIGITAL AUDIO INTERFACE – SLAVE MODE

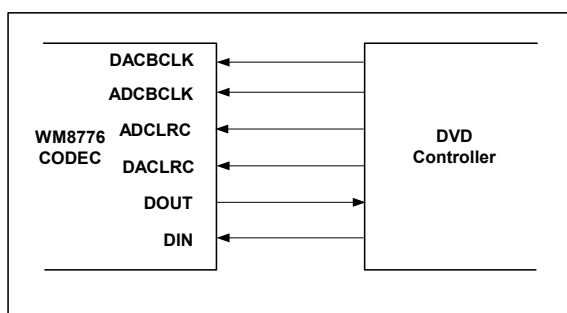


Figure 4 Audio Interface – Slave Mode

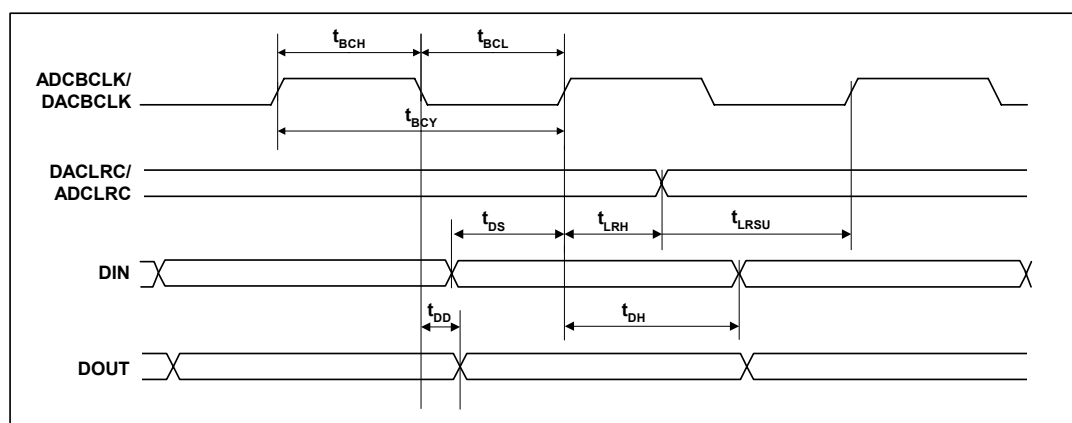


Figure 5 Digital Audio Data Timing – Slave Mode

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND = 0V, DGND = 0V, $T_A = +25^\circ\text{C}$, Slave Mode, $f_s = 48\text{kHz}$, ADC/DACMCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
ADC/DACBCLK cycle time	t_{BCY}		50			ns
ADC/DACBCLK pulse width high	t_{BCH}		20			ns
ADC/DACBCLK pulse width low	t_{BCL}		20			ns
DACLRC/ADCLRC set-up time to ADC/DACBCLK rising edge	t_{LRSU}		10			ns
DACLRC/ADCLRC hold time from ADC/DACBCLK rising edge	t_{LRH}		10			ns
DIN set-up time to DACBCLK rising edge	t_{DS}		10			ns
DIN hold time from DACBCLK rising edge	t_{DH}		10			ns
DOUT propagation delay from ADCBCLK falling edge	t_{DD}		0		10	ns

Table 3 Digital Audio Data Timing – Slave Mode

Note:

ADCLRC and DACLRC should be synchronous with MCLK, although the WM8778 interface is tolerant of phase variations or jitter on these signals.

3-WIRE MPU INTERFACE TIMING

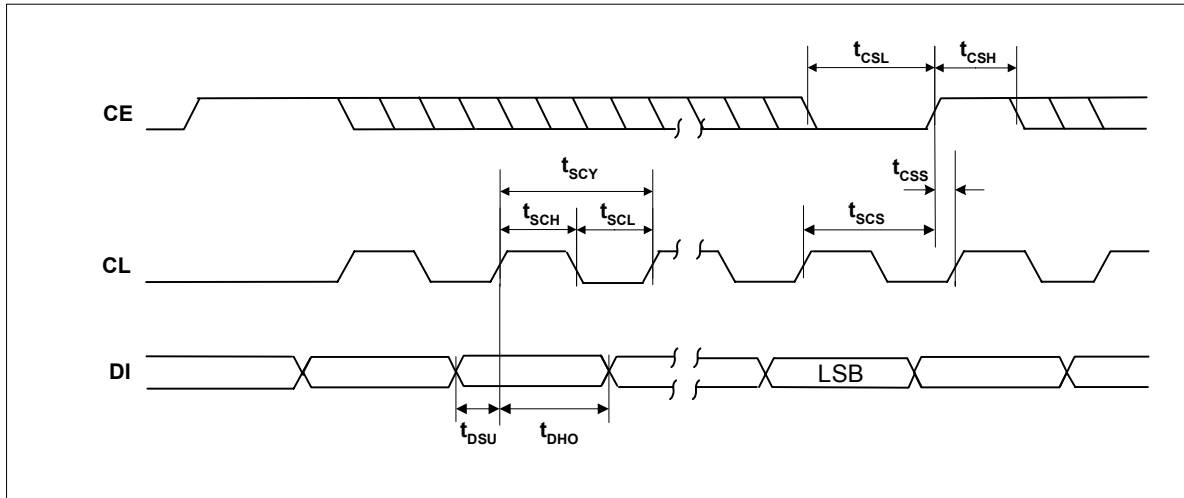


Figure 6 SPI Compatible (3-wire) Control Interface Input Timing (MODE=1)

Test Conditions					
AVDD = 5V, DVDD = 3.3V, AGND, DGND = 0V, T _A = +25°C, fs = 48kHz, MCLK = 256fs unless otherwise stated					
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CL rising edge to CE rising edge	t _{SCS}	60			ns
CL pulse cycle time	t _{SCY}	80			ns
CL pulse width low	t _{SCL}	30			ns
CL pulse width high	t _{SCH}	30			ns
DI to CL set-up time	t _{DSU}	20			ns
CL to DI hold time	t _{DHO}	20			ns
CE pulse width low	t _{CSL}	20			ns
CE pulse width high	t _{CSH}	20			ns
CE rising to CL rising	t _{CSS}	20			ns

Table 4 3-wire SPI Compatible Control Interface Input Timing Information

CONTROL INTERFACE TIMING – 2-WIRE MODE

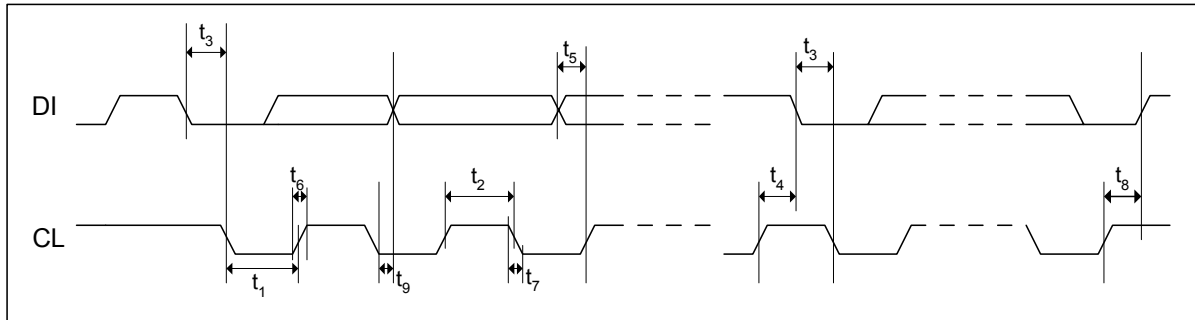


Figure 7 Control Interface Timing – 2-Wire Serial Control Mode (MODE=0)

Test Conditions

AVDD = 5V, DVDD = 3.3V, AGND, DGND = 0V, $T_A = +25^\circ\text{C}$, $f_s = 48\text{kHz}$, MCLK = 256fs unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
CL Frequency		0		526	kHz
CL Low Pulse-Width	t_1	1.3			us
CL High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
DI, CL Rise Time	t_6			300	ns
DI, CL Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

Table 5 2-wire Control Interface Timing Information

INTERNAL POWER ON RESET CIRCUIT

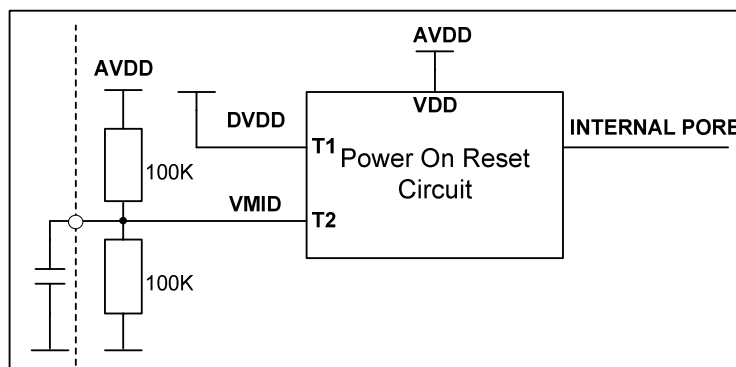


Figure 8 Internal Power on Reset Circuit Schematic

The WM8778 includes an internal Power on Reset Circuit which is used reset the digital logic into a default state after power up.

Figure 8 shows a schematic of the internal POR circuit. The POR circuit is powered from AVDD. The circuit monitors DVDD and VMID and asserts PORB low if DVDD or VMID are below the minimum threshold V_{por_off} .

On power up, the POR circuit requires AVDD to be present to operate. PORB is asserted low until AVDD and DVDD and VMID are established. When AVDD, DVDD, and VMID have been established, PORB is released high, all registers are in their default state and writes to the digital interface may take place.

On power down, PORB is asserted low whenever DVDD or VMID drop below the minimum threshold V_{por_off} .

If AVDD is removed at any time, the internal Power on Reset circuit is powered down and PORB will follow AVDD.

In most applications the time required for the device to release PORB high will be determined by the charge time of the VMID node.

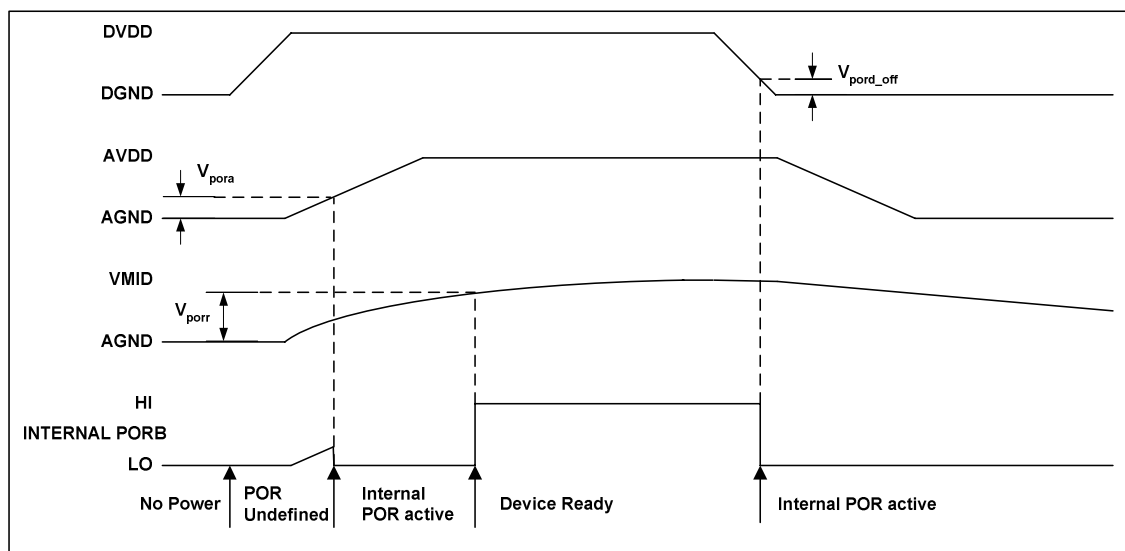


Figure 9 Typical Power up Sequence where DVDD is Powered before AVDD

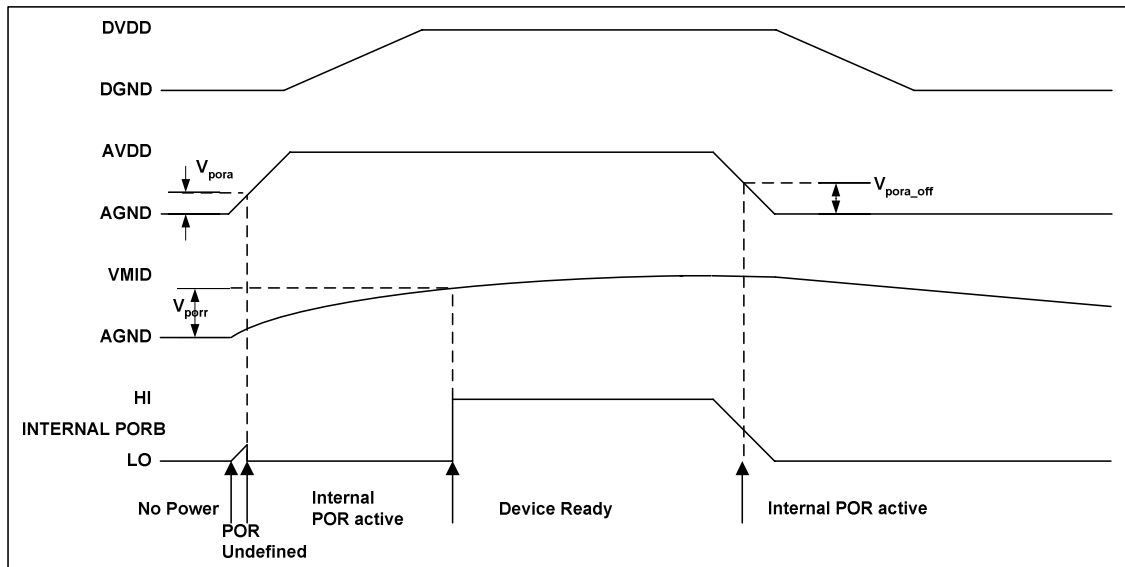


Figure 10 Typical Power up Sequence where AVDD is Powered before DVDD

Typical POR Operation (typical values, not tested)

SYMBOL	MIN	TYP	MAX	UNIT
V_{pora}	0.5	0.7	1.0	V
V_{porr}	0.5	0.7	1.1	V
V_{pora_off}	1.0	1.4	2.0	V
V_{pord_off}	0.6	0.8	1.0	V

In a real application the designer is unlikely to have control of the relative power up sequence of AVDD and DVDD. Using the POR circuit to monitor VMID ensures a reasonable delay between applying power to the device and Device Ready.

Figure 9 and Figure 10 show typical power up scenarios in a real system. Both AVDD and DVDD must be established and VMID must have reached the threshold V_{porr} before the device is ready and can be written to. Any writes to the device before Device Ready will be ignored.

Figure 9 shows DVDD powering up before AVDD. Figure 10 shows AVDD powering up before DVDD. In both cases, the time from applying power to Device Ready is dominated by the charge time of VMID.

A 10uF cap is recommended for decoupling on VMID. The charge time for VMID will dominate the time required for the device to become ready after power is applied. The time required for VMID to reach the threshold is a function of the VMID resistor string and the decoupling capacitor. The Resistor string has an typical equivalent resistance of 50kΩ (+/-20%). Assuming a 10uF capacitor, the time required for VMID to reach threshold of 1V is approx 110ms.

DEVICE DESCRIPTION

INTRODUCTION

WM8778 is a complete 2-channel DAC, 2-channel ADC audio CODEC, including digital interpolation and decimation filters, multi-bit sigma delta stereo ADC, and switched capacitor multi-bit sigma delta DACs with output smoothing filters. It is available in a single package and controlled by a 3 or 2-wire serial interface or in a hardware mode.

An analogue bypass path option is available, to allow stereo analogue signals from the stereo inputs to be sent to the stereo outputs. This allows a purely analogue input to analogue output high quality signal path to be implemented if required.

The DAC and ADC have separate left/right clocks, bit clocks, master clocks and data I/Os. The Audio Interface may be configured to operate in either master or slave mode. In Slave mode ADCLRC, DACLRC, ADCBCLK and DACBCLK are all inputs. In Master mode ADCLRC, DACLRC, ADCBCLK and DACBCLK are outputs.

The ADC has an analogue input PGA and a digital gain control, accessed by one register write. The input PGA allows input signals to be gained up to +24dB and attenuated down to -21dB in 0.5dB steps. The digital gain control allows attenuation from -21.5dB to -103dB in 0.5dB steps. This allows the user maximum flexibility in the use of the ADC.

The DAC has its own digital volume control, which is adjustable between 0dB and -127.5dB in 0.5dB steps. In addition a zero cross detect circuit is provided for digital volume controls. The digital volume control detects a transition through the zero point before updating the volume. This minimises audible clicks and 'zipper' noise as the gain values change.

The DAC output incorporates an input selector and mixer allowing a signal to be either switched into the signal path in place of the DAC signal or mixed with the DAC signal before the analogue outputs.

Control of internal functionality of the device can be by 3-wire SPI compatible or 2-wire serial control interface, or hardware mode, selected by the MODE pin. Both interfaces may be asynchronous to the audio data interface as control data will be re-synchronised to the audio processing internally.

Operation using system clock of 128fs, 192fs, 256fs, 384fs, 512fs or 768fs is provided. In Slave mode selection between clock rates is automatically controlled. In master mode the master clock to sample rate ratio is set by control bits ADCRATE and DACRATE. ADC and DAC may run at different rates. Master clock sample rates (fs) from less than 32kHz up to 192kHz are allowed, provided the appropriate system clock is input.

The audio data interface supports right, left and I²S interface formats along with a highly flexible DSP serial port interface.

AUDIO DATA SAMPLING RATES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. The WM8778 uses separate master clocks for the ADC and DAC. The external master system clocks can be applied directly through the ADCMCLK and DACMCLK input pins with no software configuration necessary. In a system where there are a number of possible sources for the reference clock it is recommended that the clock source with the lowest jitter be used to optimise the performance of the ADC and DAC.

The master clock for WM8778 supports DAC audio sampling rates from 128fs to 768fs and ADC sampling rates from 256fs to 512fs, where fs is the audio sampling frequency (DACLRC or ADCLRC) typically 32kHz, 44.1kHz, 48kHz or 96kHz. The master clock is used to operate the digital filters and the noise shaping circuits.

In Slave mode the WM8778 has a master detection circuit that automatically determines the relationship between the master clock frequency and the sampling rate (to within +/- 32 system clocks). If there is a greater than 32 clocks error the interface is disabled and maintains the output level at the last sample. The master clock must be synchronised with ADCLRC/DACLRC, although the WM8778 is tolerant of phase variations or jitter on this clock. Table 6 shows the typical master clock frequency inputs for the WM8778.

The signal processing for the WM8778 typically operates at an oversampling rate of 128fs for both ADC and DAC. The exception to this for the DAC is for operation with a 128/192fs system clock, e.g. for 192kHz operation where the oversampling rate is 64fs. For ADC operation at 96kHz it is recommended that the user set the ADCOSR bit. This changes the ADC signal processing oversample rate to 64fs.

SAMPLING RATE (DACLRC/ ADCLRC)	System Clock Frequency (MHz)					
	128fs	192fs	256fs	384fs	512fs	768fs
	DAC ONLY					
32kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1kHz	5.6448	8.467	11.2896	16.9340	22.5792	33.8688
48kHz	6.144	9.216	12.288	18.432	24.576	36.864
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable

Table 6 System Clock Frequencies Versus Sampling Rate

In Master mode DACBCLK, ADCBCLK, DACLRC and ADCLRC are generated by the WM8778. The frequencies of ADCLRC and DACLRC are set by setting the required ratio of DACMCLK to DACLRC and ADCMCLK to ADCLRC using the DACRATE and ADCRATE control bits (Table 7).

ADCRATE[2:0]/ DACRATE[2:0]	ADCMCLK/DACMCLK: ADCLRC/DACLRC RATIO
000	128fs (DAC Only)
001	192fs (DAC Only)
010	256fs
011	384fs
100	512fs
101	768fs

Table 7 Master Mode MCLK:ADCLRC/DACLRC Ratio Select

Table 8 shows the settings for ADCRATE and DACRATE for common sample rates and ADCMCLK/DACMCLK frequencies.

SAMPLING RATE (DACLRC/ ADCLRC)	System Clock Frequency (MHz)					
	128fs	192fs	256fs	384fs	512fs	768fs
	DACRATE =000	DACRATE =001	ADCRATE/ DACRATE =010	ADCRATE/ DACRATE =011	ADCRATE/ DACRATE =100	ADCRATE/ DACRATE =101
32kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1kHz	5.6448	8.467	11.2896	16.9340	22.5792	33.8688
48kHz	6.144	9.216	12.288	18.432	24.576	36.864
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable

Table 8 Master Mode ADC/DACLRC Frequency Selection

ADCBCLK and DACBCLK are also generated by the WM8778. The frequency of ADCBCLK and DACBCLK depends on the mode of operation.

In 128/192fs modes (DACRATE=000 or 001) BCLK = MCLK/2. In 256/384/512fs modes (ADCRATE/DACRATE=010 or 011 or 100) BCLK = MCLK/4. However if DSP mode is selected as the audio interface mode then BCLK=MCLK. Note that DSP mode cannot be used in 128fs mode for word lengths greater than 16 bits or in 192fs mode for word lengths greater than 24 bits.

ZERO DETECT

The WM8778 has a zero detect circuit for each DAC channel, which detects when 1024 consecutive zero samples have been input. The two zero flag outputs (ZFLAGL and ZFLAGR) may be programmed to output the zero detect signals (see Table 9) that may then be used to control external muting circuits. A '1' on ZFLAGL or ZFLAGR indicates a zero detect. The zero detect may also be used to automatically enable the mute by setting IZD. The zero flag output may be disabled by setting DZFM to 00.

DZFM[1:0]	ZFLAGL	ZFLAGR
00	Zero flag disabled	Zero flag disabled
01	Left channel zero	Right channel zero
10	Both channel zero	Both channel zero
11	Either channels zero	Either channel zero

Table 9 Zero Flag Output Select

POWERDOWN MODES

The WM8778 has powerdown control bits allowing specific parts of the WM8778 to be powered off when not being used. Control bit ADCPD powers off the ADC. The ADC input PGAs will be powered down only if ADCPD and AINPD are set. When AINPD is set the bypass path is automatically disabled. The stereo DAC has a separate powerdown control bit, DACPD allowing the DAC to be powered off when not in use. This also switches the analogue outputs VOUTL/R to VMIDDAC to maintain a dc level on the output. The output mixer will be disabled when PDWN is set.

Setting AINPD, ADCPD and DACPD will powerdown everything except the references VMIDADC, ADCREF and VMIDDAC. ADCREF and VMIDDAC can be powered down by setting PDWN, VMIDADC is always active. Setting PDWN will override all other powerdown control bits. It is recommended that AINPD, ADCPD and DACPD are set before setting PDWN. The default is for all blocks to be enabled.

DIGITAL AUDIO INTERFACE

MASTER AND SLAVE MODES

The audio interface operates in either Slave or Master mode, selectable using the MS control bit. In both Master and Slave modes DIN is always an input to the WM8778 and DOUT is always an output. The default is Slave mode.

In Slave mode (MS=0) ADCLRC, DACLRC, ADCBCLK and DACBCLK are inputs to the WM8778 (Figure 11). DIN and DACLRC are sampled by the WM8778 on the rising edge of DACBCLK, ADCLRC is sampled on the rising edge of ADCBCLK. ADC data is output on DOUT and changes on the falling edge of ADCBCLK. By setting control bit BCLKINV the polarity of ADCBCLK and DACBCLK may be reversed so that DIN and DACLRC are sampled on the falling edge of DACBCLK, ADCLRC is sampled on the falling edge of ADCBCLK and DOUT changes on the rising edge of ADCBCLK.

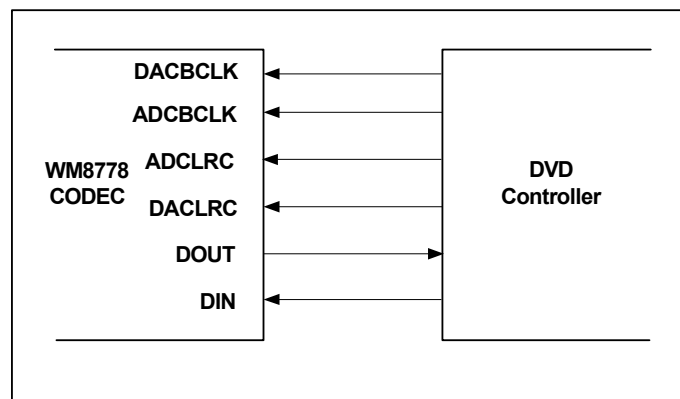


Figure 11 Slave Mode

In Master mode (MS=1) ADCLRC, DACLRC, ADCBCLK and DACBCLK are outputs from the WM8778 (Figure 12). ADCLRC, DACLRC, ADCBCLK and DACBCLK are generated by the WM8778. DIN is sampled by the WM8778 on the rising edge of DACBCLK so the controller must output DAC data that changes on the falling edge of DACBCLK. ADC data is output on DOUT and changes on the falling edge of ADCBCLK. By setting control bit BCLKINV, the polarity of ADCBCLK and DACBCLK may be reversed so that DIN is sampled on the falling edge of DACBCLK and DOUT changes on the rising edge of ADCBCLK.

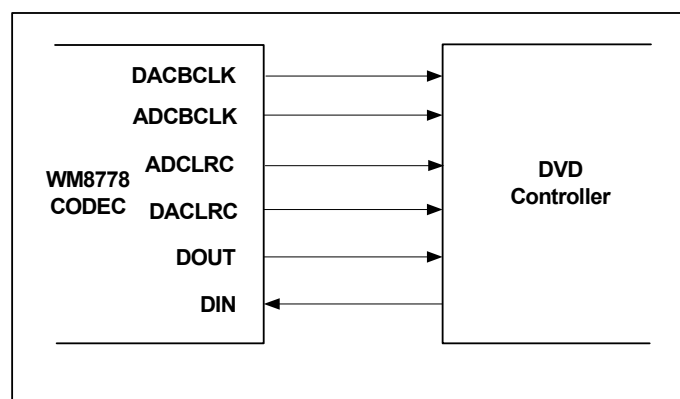


Figure 12 Master Mode

AUDIO INTERFACE FORMATS

Audio data is applied to the internal DAC filters or output from the ADC filters, via the Digital Audio Interface. 5 popular interface formats are supported:

- Left Justified mode
- Right Justified mode
- I²S mode
- DSP mode A
- DSP mode B

All 5 formats send the MSB first and support word lengths of 16, 20, 24 and 32 bits, with the exception of 32 bit right justified mode, which is not supported.

In left justified, right justified and I²S modes, the digital audio interface receives DAC data on the DIN input and outputs ADC data on DOUT. Audio Data for each stereo channel is time multiplexed with ADCLRC/DACLRC indicating whether the left or right channel is present. ADCLRC/DACLRC is also used as a timing reference to indicate the beginning or end of the data words.

In left justified, right justified and I²S modes; the minimum number of BCLKs per DACLRC/ADCLRC period is 2 times the selected word length. ADCLRC/DACLRC must be high for a minimum of word length BCLKs and low for a minimum of word length BCLKs. Any mark to space ratio on ADCLRC/DACLRC is acceptable provided the above requirements are met.

In DSP mode A or B, DACLRC is used as a frame sync signal to identify the MSB of the first word. The minimum number of DACBCLKs per DACLRC period is 2 times the selected word length. Any mark to space ratio is acceptable on DACLRC provided the rising edge is correctly positioned. The ADC data may also be output in DSP mode A or B, with ADCLRC used as a frame sync to identify the MSB of the first word. The minimum number of ADCBCLKs per ADCLRC period is 2 times the selected word length.

LEFT JUSTIFIED MODE

In left justified mode, the MSB of DIN is sampled by the WM8778 on the first rising edge of DACBCLK following a DACLRC transition. The MSB of the ADC data is output on DOUT and changes on the same falling edge of ADCBCLK as ADCLRC and may be sampled on the rising edge of ADCBCLK. ADCLRC and DACLRC are high during the left samples and low during the right samples (Figure 13).

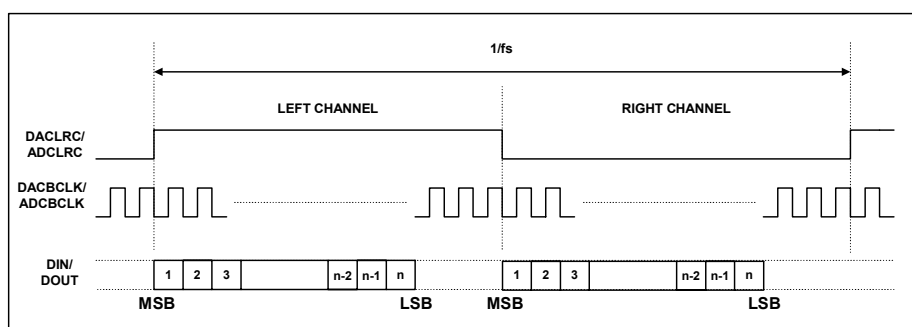


Figure 13 Left Justified Mode Timing Diagram

RIGHT JUSTIFIED MODE

In right justified mode, the LSB of DIN is sampled by the WM8778 on the rising edge of DACBCLK preceding a DACLRC transition. The LSB of the ADC data is output on DOUT and changes on the falling edge of ADCBCLK preceding a ADCLRC transition and may be sampled on the rising edge of ADCBCLK. ADCLRC and DACLRC are high during the left samples and low during the right samples (Figure 14).

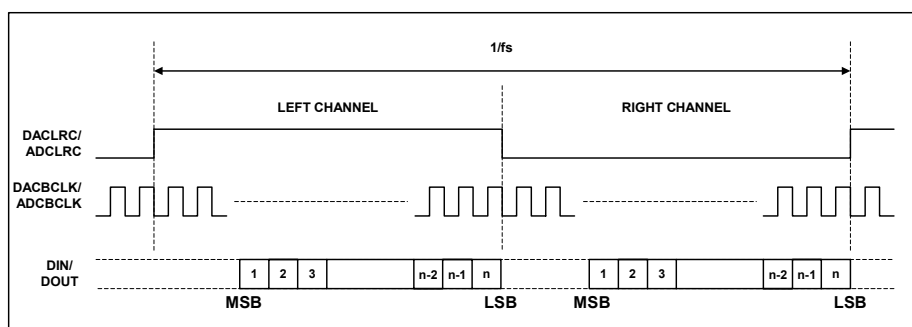


Figure 14 Right Justified Mode Timing Diagram

I²S MODE

In I²S mode, the MSB of DIN is sampled by the WM8778 on the second rising edge of DACBCLK following a DACLRC transition. The MSB of the ADC data is output on DOUT and changes on the first falling edge of ADCBCLK following an ADCLRC transition and may be sampled on the rising edge of ADCBCLK. ADCLRC and DACLRC are low during the left samples and high during the right samples.

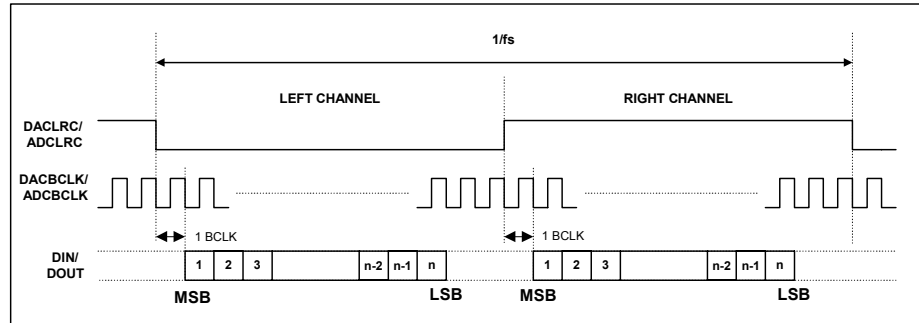


Figure 15 I²S Mode Timing Diagram

DSP MODES

In DSP/PCM mode, the left channel MSB is available on either the 1st (mode B) or 2nd (mode A) rising edge of BCLK (selectable by LRP) following a rising edge of LRC. Right channel data immediately follows left channel data. Depending on word length, BCLK frequency and sample rate, there may be unused BCLK cycles between the LSB of the right channel data and the next sample.

In device master mode, the LRC output will resemble the frame pulse shown in Figure 16 and Figure 17. In device slave mode, Figure 18 and Figure 19, it is possible to use any length of frame pulse less than 1/fs, providing the falling edge of the frame pulse occurs greater than one BCLK period before the rising edge of the next frame pulse.

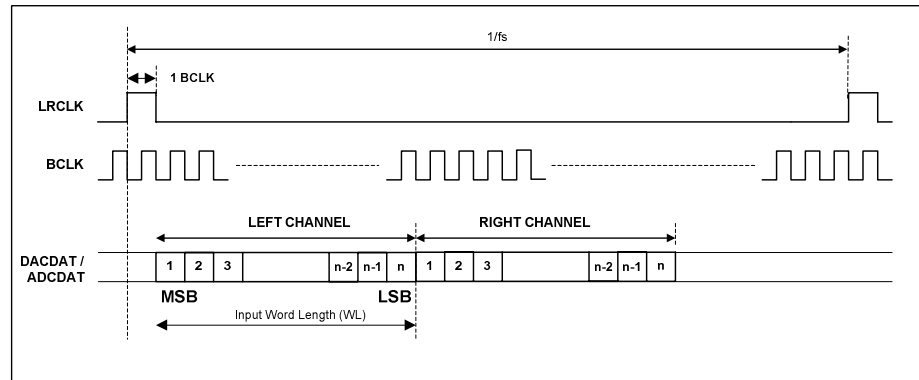


Figure 16 DSP/PCM Mode Audio Interface (mode A, LRP=0, Master)

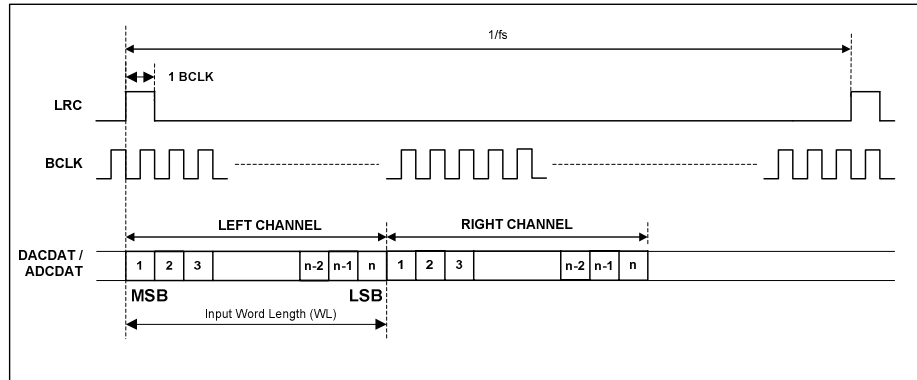


Figure 17 DSP/PCM Mode Audio Interface (mode B, LRP=1, Master)

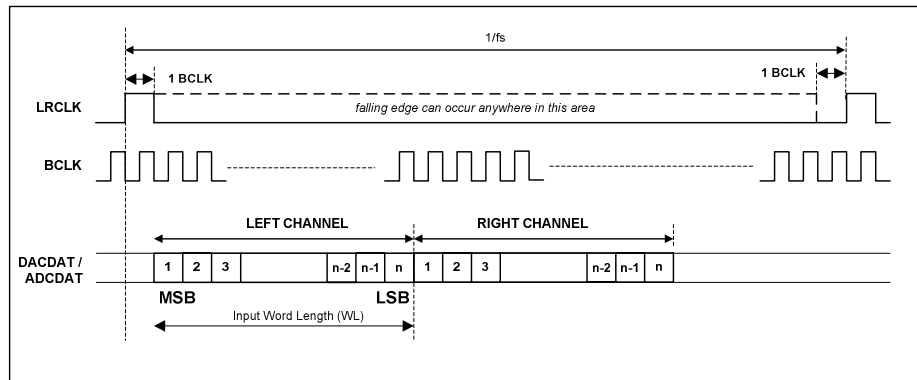


Figure 18 DSP/PCM Mode Audio Interface (mode A, LRP=0, Slave)

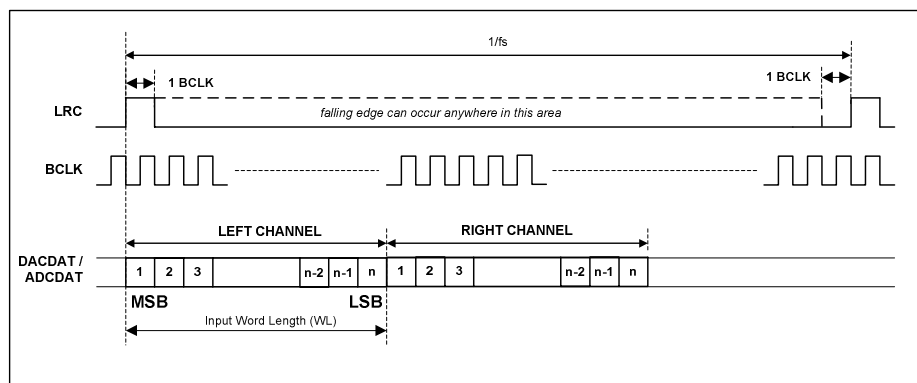


Figure 19 DSP/PCM Mode Audio Interface (mode B, LRP=0, Slave)

CONTROL INTERFACE OPERATION

The WM8778 is controlled by writing to registers through a serial control interface. A control word consists of 16 bits. The first 7 bits (B15 to B9) are address bits that select which control register is accessed. The remaining 9 bits (B8 to B0) are data bits, corresponding to the 9 bits in each control register. The control interface can operate as either a 3-wire or 2-wire MPU interface. The MODE pin selects the interface format, as shown in Table 10.

MODE	CONTROL MODE
0	2 wire software
Z / midrail	Hardware
1	3 wire software

Table 10 Control Interface Selection via MODE Pin

3-WIRE (SPI COMPATIBLE) SERIAL CONTROL MODE

In 3-wire mode, every rising edge of CL clocks in one data bit from the DI pin. A rising edge on CE latches in a complete control word consisting of the last 16 bits. The 3-wire interface protocol is shown in Figure 20.

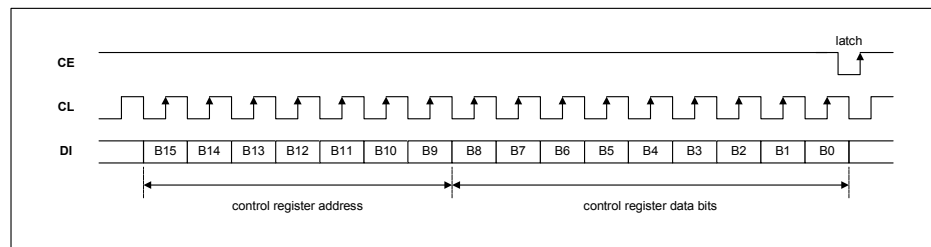


Figure 20 3-wire SPI Compatible Interface

1. B[15:9] are Control Address Bits
2. B[8:0] are Control Data Bits
3. CE is edge sensitive – the data is latched on the rising edge of CE.

2-WIRE SERIAL CONTROL MODE

The WM8778 supports software control via a 2-wire serial bus. Many devices can be controlled by the same bus, and each device has a unique 7-bit address (this is not the same as the 7-bit address of each register in the WM8778).

The WM8778 operates as a slave device only. The controller indicates the start of data transfer with a high to low transition on DI while CL remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on DI (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the WM8778 and the R/W bit is '0', indicating a write, then the WM8778 responds by pulling DI low on the next clock pulse (ACK). If the address is not recognised or the R/W bit is '1', the WM8778 returns to the idle condition and wait for a new start condition and valid address.

Once the WM8778 has acknowledged a correct address, the controller sends the first byte of control data (B15 to B8, i.e. the WM8778 register address plus the first bit of register data). The WM8778 then acknowledges the first data byte by pulling DI low for one clock pulse. The controller then sends the second byte of control data (B7 to B0, i.e. the remaining 8 bits of register data), and the WM8778 acknowledges again by pulling DI low.

The transfer of data is complete when there is a low to high transition on DI while CL is high. After receiving a complete address and data sequence the WM8778 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. DI changes while CL is high), the device jumps to the idle condition.

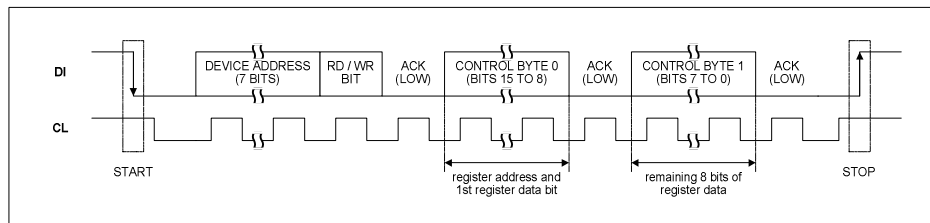


Figure 21 2-wire Serial Interface

1. B[15:9] are Control Address Bits
2. B[8:0] are Control Data Bits

The WM8778 has two possible device addresses, which can be selected using the CE pin.

CE STATE	DEVICE ADDRESS
Low	0011010 (0 x 34h)
High	0011011 (0 x 36h)

Table 11 2-Wire MPU Interface Address Selection

HARDWARE MODE

Hardware mode is selected by applying a midrail voltage to the MODE pin, or by leaving it floating. The circuit detects this condition and enables hardware mode. This allows limited control of the internal functions using the three inputs CE, CL and DI. The table below gives a summary of the use of each pin in hardware mode.

PIN NAME	FUNCTION	DESCRIPTION
CE\I2S	Interface Mode select	0 : Right Justified 1 : I ² S
CL\IWL	Interface Wordlength select	0 : 20 bit (RJ), 16 bit (I ² S) 1 : 24 bit
DI\DEEMPH	De-emphasis on/off	0 : De-emphasis disabled 1 : De-emphasis enabled

Table 12 Hardware Mode Functions

CONTROL INTERFACE REGISTERS

DIGITAL AUDIO INTERFACE CONTROL REGISTER

Interface format is selected via the FMT[1:0] register bits:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) 0001010 DAC Interface Control	1:0	DACFMT [1:0]	10	Interface format Select 00 : right justified mode 01: left justified mode
R11 (0Bh) 0001011 ADC Interface Control	1:0	ADCFMT [1:0]	10	10: I ² S mode 11: DSP mode A or B

In left justified, right justified or I²S modes, the LRP register bit controls the polarity of ADCLRC/DACLRC. If this bit is set high, the expected polarity of ADCLRC/DACLRC will be the opposite of that shown Figure 13, Figure 14, etc. Note that if this feature is used as a means of swapping the left and right channels, a 1 sample phase difference will be introduced. In DSP modes, the LRP register bit is used to select between modes A and B.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) 0001010 DAC Interface Control	2	DACLRC	0	In left/right I ² S modes: ADCLRC/DACLRC Polarity (normal) 0 : normal ADCLRC/DACLRC polarity 1: inverted ADCLRC/DACLRC polarity
R11 (0Bh) 0001011 ADC Interface Control	2	ADCLRC	0	In DSP mode: 0 : DSP mode A 1: DSP mode B

By default, ADCLRC, DACLRC and DIN are sampled on the rising edge of ADCBCLK and DACBCLK and should ideally change on the falling edge. Data sources that change ADCLRC/DACLRC and DIN on the rising edge of ADCBCLK/DACBCLK can be supported by setting the BCP register bit. Setting BCP to 1 inverts the polarity of BCLK to the inverse of that shown in Figure 13, Figure 14, etc.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) 0001010 DAC Interface Control	3	DACBCP	0	BCLK Polarity (DSP modes) 0 : normal BCLK polarity 1: inverted BCLK polarity
R11 (0Bh) 0001011 ADC Interface Control	3	ADCBCLK	0	

The WL[1:0] bits are used to control the input word length.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R10 (0Ah) 0001010 DAC Interface Control	5:4	DACWL [1:0]	10	Word Length 00 : 16 bit data 01: 20 bit data
R11 (0Bh) 0001011 ADC Interface Control	5:4	ADCWL [1:0]	10	10: 24 bit data 11: 32 bit data

Note: If 32-bit mode is selected in right justified mode, the WM8778 defaults to 24 bits.

In all modes, the data is signed 2's complement. The digital filters always input 24-bit data. If the DAC is programmed to receive 16 or 20 bit data, the WM8778 pads the unused LSBs with zeros. If the DAC is programmed into 32 bit mode, the 8 LSBs are ignored.

Note: In 24 bit I²S mode, any width of 24 bits or less is supported provided that ADCLRC/DACLRC is high for a minimum of 24 BCLKs and low for a minimum of 24 BCLKs.

When operating the ADC digital interface in slave mode, to optimise the performance of the ADC it is recommended that the ADCMCLK and ADCBCLK input signals do not have coinciding rising edges. The ADCMCLK bit provides the option to internally invert the ADCMCLK input signal when the input signals have coinciding rising edges.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11(0Bh) 0001011 Interface Control	6	ADCMCLK	0	ADCMCLK Polarity 0 : non-inverted 1: inverted

A number of options are available to control how data from the Digital Audio Interface is applied to the DAC.

MASTER MODES

Control bit ADCMS selects between audio interface Master and Slave Modes for ADC. In ADC Master mode ADCLRC and ADCBCLK are outputs and are generated by the WM8778. In Slave mode ADCLRC and ADCBCLK are inputs to WM8778.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 (0Ch) 0001100 Interface Control	8	ADCMS	0	Audio Interface Master/Slave Mode select for ADC: 0 : Slave Mode 1: Master Mode

Control bit DACMS selects between audio interface Master and Slave Modes for the DAC. In DAC Master mode DACLRC and DACBCLK are outputs and are generated by the WM8778. In Slave mode DACLRC and DACBCLK are inputs to WM8778.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 (0Ch) 0001100 Interface Control	7	DACMS	0	Audio Interface Master/Slave Mode select for DAC: 0 : Slave Mode 1: Master Mode

MASTER MODE ADCLRC/DACLRC FREQUENCY SELECT

In ADC Master mode the WM8778 generates ADCLRC and ADCBCLK, in DAC master mode the WM8778 generates DACLRC and DACBCLK. These clocks are derived from the master clock (ADCMCLK or DACMCLK). The ratios of ADCMCLK to ADCLRC and DACMCLK to DACLRC are set by ADCRATE and DACRATE respectively.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 (0Ch) 0001100 ADCLRC and DACLRC Frequency Select	2:0	ADCRATE[2:0]	010	Master Mode MCLK:ADCLRC Ratio Select: 010: 256fs 011: 384fs 100: 512fs 101: 768fs
	6:4	DACRATE[2:0]	010	Master Mode MCLK:DACLRC Ratio Select: 000: 128fs 001: 192fs 010: 256fs 011: 384fs 100: 512fs 101: 768fs