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WM8805

8:1 Digital Interface Transceiver with PLL

DESCRIPTION

The WM8805 is a high performance consumer mode S/PDIF transceiver with support for 8 received Channels and 1 transmitted Channel.

A crystal derived, or externally provided high quality master clock is used to allow low jitter recovery of S/PDIF supplied master clocks.

Generation of all typically used audio clocks is possible using the high performance internal PLL. A dedicated CLKOUT pin provides a high drive clock output.

A pass through option is provided which allows the device simply to be used to clean up (de-jitter) the received digital audio signals.

The device may be used under software control or stand alone hardware control modes. In software control mode, both 2-wire with read back and 3-wire interface modes are supported.

Status and error monitoring is built-in and results can be read back over the control interface, on the GPO pins or streamed over the audio data interface in 'With Flags' mode (audio data with status flags appended).

The audio data interface supports I^2S, left justified, right justified and DSP audio formats of 16-24 bit word length, with sample rates from 32 to 192ks/s.

The device is supplied in a 28-lead Pb-free SSOP package.

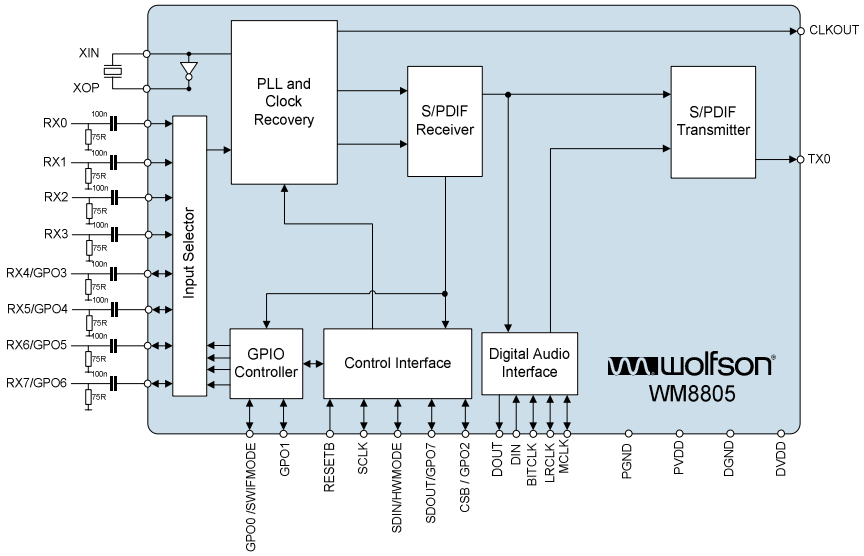
FEATURES

- S/PDIF (IEC60958-3) compliant.
- Advanced jitter attenuating PLL with low intrinsic period jitter of 50 ps RMS.
- S/PDIF recovered clock using PLL, or stand alone crystal derived clock generation.
- Supports 10 – 27MHz crystal clock frequencies.
- 2-wire / 3-Wire serial or hardware control interface.
- Programmable Audio data interface modes:
  - I^2S, Left, Right Justified or DSP
  - 16/20/24 bit word lengths
- 8 channel receiver input and 1 channel transmit output.
- Auto frequency detection / synchronisation.
- Selectable output status data bits.
- Up to 8 configurable GPO pins.
- De-emphasis flag output.
- Non-audio detection including DOLBY™ and DTS™.
- Channel status changed flag.
- Configurable clock distribution with selectable output MCLK rate of 512fs, 256fs, 128fs and 64fs.
- 2.7 to 3.6V digital and PLL supply voltages.
- 28-lead SSOP package.

APPLICATIONS

- Surround Sound AV processors and Hi-Fi systems
- Music industry applications
- DVD-P/DVD-RW
- Digital TV

BLOCK DIAGRAM



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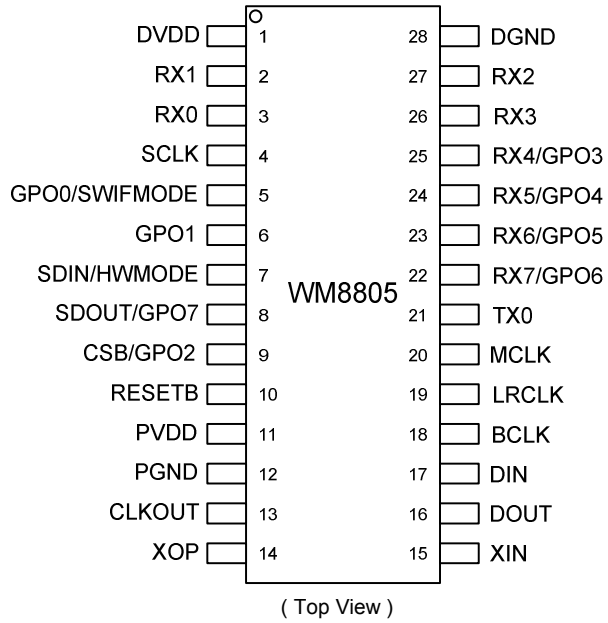
PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8805GEDS/V	-40 to +85°C	28-lead SSOP (Pb-free)	MSL3	260°C
WM8805GEDS/RV	-40 to +85°C	28-lead SSOP (Pb-free, tape and reel)	MSL3	260°C

Note:
Reel quantity = 2,000

PIN DESCRIPTION

PIN	NAME	Type	DESCRIPTION
1	DVDD	Supply	Digital core supply
2	RX1	Digital In	S/PDIF receive channel 1
3	RX0	Digital In	S/PDIF receive channel 0
4	SCLK	Digital In/Out	Control interface clock / TRANS_ERR flag in hardware control mode. See note 2.
5	GPO0 / SWIFMODE	Digital In/Out	General purpose digital output or selected functionality at hardware reset. See note 2.
6	GPO1	Digital Out	General purpose digital output
7	SDIN / HWMODE	Digital Input	Control interface data input and hardware/software mode select at hardware reset. See note 2.
8	SDOUT / GPO7	Digital In/Out	Control interface data output / NON_AUDIO flag in hardware control mode / GPO in 2-wire software control mode. See note 2.
9	CSB / GPO2	Digital In/Out	Chip select / UNLOCK flag in hardware control mode / GPO in 2-wire software control mode. See note 2.
10	RESETB	Digital Input	System reset (active low)
11	PVDD	Supply	PLL core supply
12	PGND	Supply	PLL ground
13	CLKOUT	Digital Out	High drive clock output at 64fs, 128fs, 256fs and 512fs
14	XOP	Digital Output	Crystal output
15	XIN	Digital Input	Crystal input
16	DOUT	Digital Out	Audio interface data output
17	DIN	Digital In	Audio interface data input
18	BCLK	Digital In/Out	Audio interface bit clock
19	LRCLK	Digital In/Out	Audio interface left/right word clock
20	MCLK	Digital In/Out	Master clock input or output
21	TX0	Digital Out	S/PDIF transmit
22	RX7 / GPO6	Digital In/Out	S/PDIF receive channel 7 or general purpose digital output
23	RX6 / GPO5	Digital In/Out	S/PDIF receive channel 6 or general purpose digital output
24	RX5 / GPO4	Digital In/Out	S/PDIF receive channel 5 or general purpose digital output
25	RX4 / GPO3	Digital In/Out	S/PDIF receive channel 4 or general purpose digital output
26	RX3	Digital In	S/PDIF receive channel 3
27	RX2	Digital In	S/PDIF receive channel 2
28	DGND	Supply	Digital ground

Notes:

1. Digital input pins have Schmitt trigger input buffers.
2. Refer to Table 6 Device Configuration at Power up or Hardware Reset

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Digital core and I/O buffer supply voltage	-0.3V	+5V
PLL supply voltage	-0.3V	+5V
Voltage range digital inputs	DGND -0.3V	DVDD +0.3V
Master Clock Frequency		37MHz
Operating temperature range, T_A	-40°C	+85°C
Storage temperature	-65°C	+150°C

Note:

1. PLL and digital supplies must always be within 0.3V of each other.
2. PLL and digital grounds must always be within 0.3V of each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		2.7		3.6	V
Ground	DGND			0		V
PLL supply range	PVDD		2.7		3.6	V
Ground	PGND			0		V

Note:

1. PLL and digital supplies must always be within 0.3V of each other.
2. PLL and digital grounds must always be within 0.3V of each other.

SUPPLY CURRENT

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply current	I_{DVDD}	DVDD = 3.3V		14.9		mA
PLL supply current	I_{PVDD}	PVDD = 3.3V		1.7		mA
Power consumption		DVDD/PVDD = 3.3V		54.8		mW
Standby Power consumption		DVDD/PVDD = 3.3V Device powered down		0.11		mW

ELECTRICAL CHARACTERISTICS

Test Conditions

PVDD = 3.3V, DVDD = 3.3V, PGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Jitter Characteristics						
Intrinsic Period Jitter	J_i			50		ps
Digital Logic Levels (CMOS Levels)						
Input LOW level	V_{IL}				0.3 x DVDD	V
Input HIGH level	V_{IH}		0.7 x DVDD			V
Output LOW	V_{OL}				0.1 x DVDD	V
Output HIGH	V_{OH}		0.9 x DVDD			V
CLOCKOUT buffer drive capability	I_{source}	CMOS 20pF load	25			mA
	I_{sink}		25			mA
S/PDIF Receiver Characteristics						
Input Resistance				23		kΩ

MASTER CLOCK TIMING

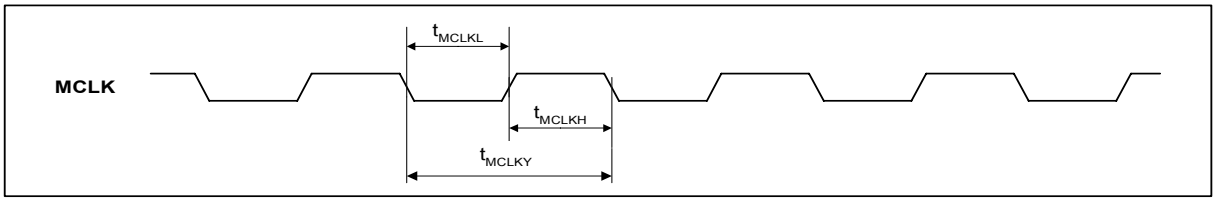


Figure 1 Master Clock Timing Requirements

Test Conditions

PVDD = 3.3V, DVDD = 3.3V, PGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information – Slave Mode						
MCLK System clock cycle time	t_{MCLKY}		27			ns
MCLK System clock pulse width high	t_{MCLKH}		11			ns
MCLK System clock pulse width low	t_{MLCKL}		11			ns
MCLK Duty cycle			40:60		60:40	%

Table 1 Slave Mode MCLK Timing Requirements

DIGITAL AUDIO INTERFACE – MASTER MODE

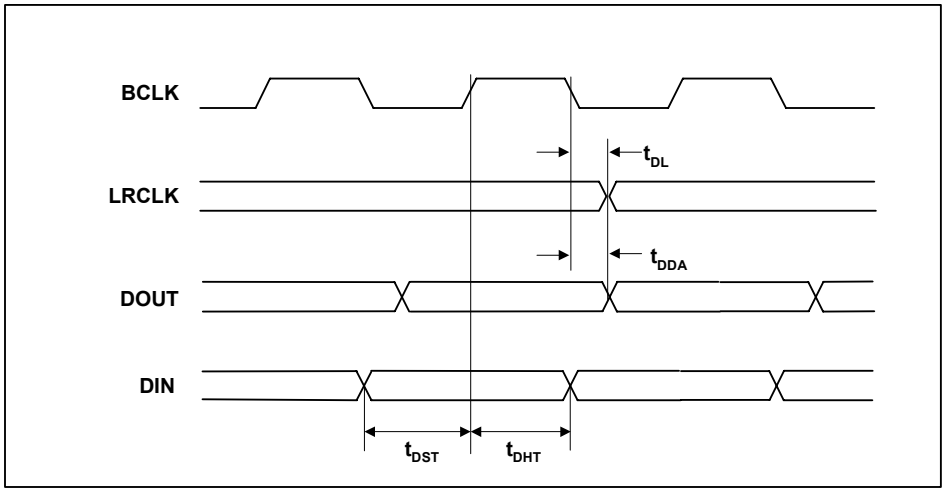


Figure 2 Digital Audio Data Timing – Master Mode

Test Conditions

PVDD = 3.3V, DVDD = 3.3V, PGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
LRCLK propagation delay from BCLK falling edge	t_{DL}		0		10	ns
DOUT propagation delay from BCLK falling edge	t_{DDA}		0		10	ns
DIN setup time to BCLK rising edge	t_{DST}		10			ns
DIN hold time from BCLK rising edge	t_{DHT}		10			ns

Table 2 Digital Audio Data Timing – Master Mode

DIGITAL AUDIO INTERFACE – SLAVE MODE

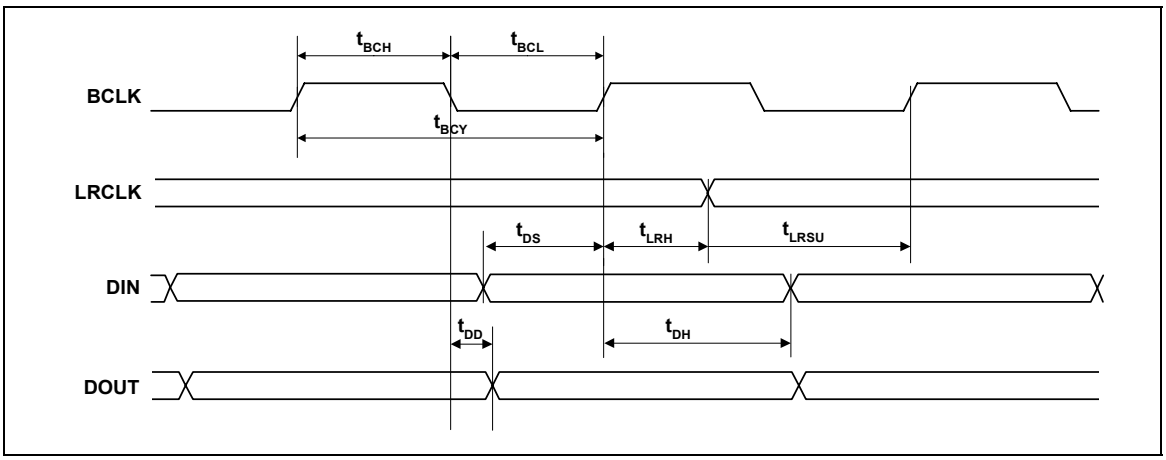


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

PVDD = 3.3V, DVDD = 3.3V, PGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCLK cycle time	t_{BCY}		50			ns
BCLK pulse width high	t_{BCH}		20			ns
BCLK pulse width low	t_{BCL}		20			ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}		10			ns
LRCLK hold time from BCLK rising edge	t_{LRH}		10			ns
DIN set-up time to BCLK rising edge	t_{DS}		10			ns
DIN hold time from BCLK rising edge	t_{DH}		10			ns
DOUT propagation delay from BCLK falling edge	t_{DD}		0		10	ns

Table 3 Digital Audio Data Timing – Slave Mode

CONTROL INTERFACE – 3-WIRE MODE

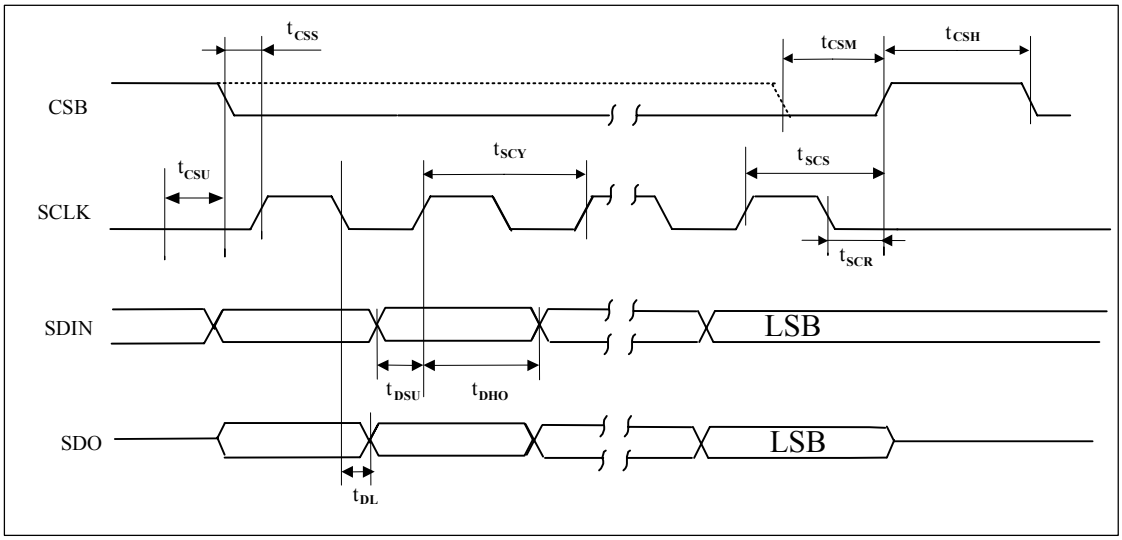


Figure 4 Control Interface Timing – 3-Wire Serial Control Mode

Test Conditions

PVDD = 3.3V, DVDD = 3.3V, PGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB rising edge	t_{SCS}	60			ns
SCLK cycle time	t_{SCY}	80			ns
SCLK duty cycle		40/60		60/40	%
SDIN to SCLK set-up time	t_{DSU}	20			ns
SDIN hold time from SCLK rising edge	t_{DHO}	20			ns
SDOUT propagation delay from SCLK rising edge	t_{DL}			5	ns
CSB pulse width high	t_{CSH}	20			ns
SCLK to CSB low (required for read cycle) set-up time	t_{CSU}	20			ns
CSB min (write cycle only)	t_{CSM}	0.5* t_{SCY}			ns
SCLK fall to CSB high	t_{CSR}	20			ns
CSB rising/falling to SCLK rising	t_{CSS}	20			ns
SCLK glitch suppression	t_{ps}	2		8	ns

Table 4 Control Interface Timing – 3-Wire Serial Control Mode

CONTROL INTERFACE – 2-WIRE MODE

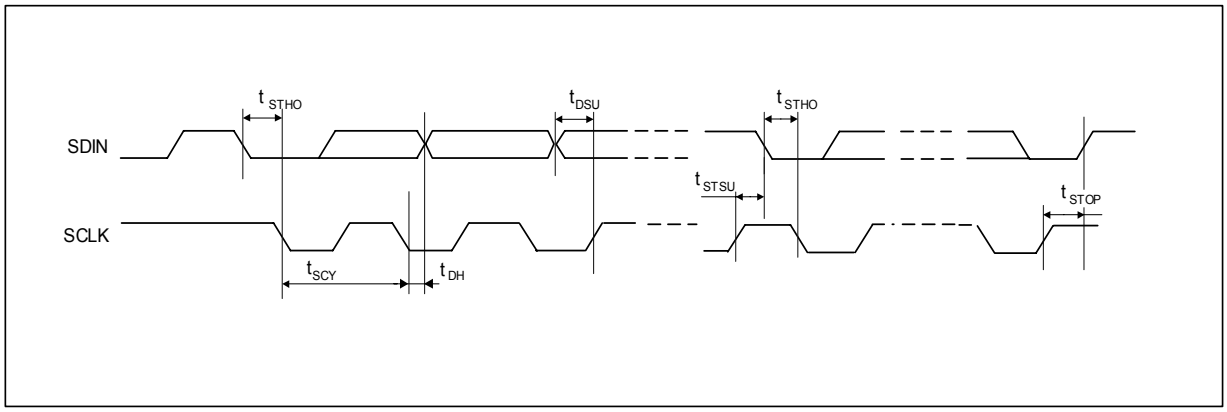


Figure 5 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

PVDD = 3.3V, DVDD = 3.3V, PGND = 0V, DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK = 256fs unless stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK cycle time	t_{SCY}	2500			ns
SCLK duty cycle		40/60		60/40	%
SCLK frequency				400	kHz
Hold Time (Start Condition)	t_{STHO}	600			ns
Setup Time (Start Condition)	t_{STSU}	600			ns
Data Setup Time	t_{DSU}	100			ns
SDIN, SCLK Rise Time				300	ns
SDIN, SCLK Fall Time				300	ns
Setup Time (Stop Condition)	t_{STOP}	600			ns
Data Hold Time	t_{DHO}			900	ns
SCLK glitch suppression	t_{ps}	2		8	ns

Table 5 Control Interface Timing – 2-Wire Serial Control Mode

DEVICE DESCRIPTION

INTRODUCTION

FEATURES

- IEC-60958-3 compatible with 32 to 192k frames/s support.
- Supports AES-3 data frames.
- Support for reception and transmission of S/PDIF data.
- Clock synthesis PLL with reference clock input and low jitter output.
- Supports input reference clock frequencies from 10MHz to 27MHz.
- Dedicated high drive clock output pin.
- Register controlled channel status bit configuration.
- Register read-back of recovered channel status bits and error flags.
- Detection of non-audio data, sample rate and de-emphasis.
- Programmable GPOs for error flags and frame status flags.

The WM8805 is an IEC-60958 compatible S/PDIF transceiver with support for up to eight received S/PDIF data streams and one transmitted S/PDIF data stream.

The receiver performs data and clock recovery, and transmits recovered data from the chip either through the digital audio interface or, alternatively, the device can loop the received S/PDIF data back out through the S/PDIF transmitter producing a de-jittered S/PDIF transmit data stream. The recovered clock may be routed to a high drive output pin for external use. If there is no S/PDIF input data stream the PLL can be configured to output all standard MCLK frequencies or it can be configured to maintain the frequency of the last received S/PDIF data stream.

The transmitter generates S/PDIF frames where audio data may be sourced from the S/PDIF receiver or the digital audio interface. Timing for the S/PDIF transmitter interface can be sourced from the internally derived MCLK in loop through mode or it can be taken from an external source.

S/PDIF FORMAT

S/PDIF is a serial, bi-phase-mark encoded data stream. An S/PDIF frame consists of two sub-frames. Each sub-frame is made up of:

- Preamble – a synchronization pattern used to identify the start of a 192-frame block or sub-frame
- 4-bit Auxiliary Data (AUX) – ordered LSB to MSB
- 20-bit Audio Data (24-bit when combined with AUX) – ordered LSB to MSB
- Validity Bit – a 1 indicates invalid data in the associated sub-frame
- User Bit – over 192-frames, this forms a User Data Block
- Channel Bit – over 192-frames, this forms a Channel Status Block
- Parity Bit – used to maintain even parity over the sub-frame (not including the preamble)

An S/PDIF Block consists of 192 frames. Channel and user blocks are incorporated within the 192-frame S/PDIF Block. For Consumer mode only the first 40-frames are used to make up the Channel and User blocks. Figure 6 illustrates the S/PDIF format. The WM8805 does not support transmission of user channel data. Received user channel data may be accessed via GPO pins.

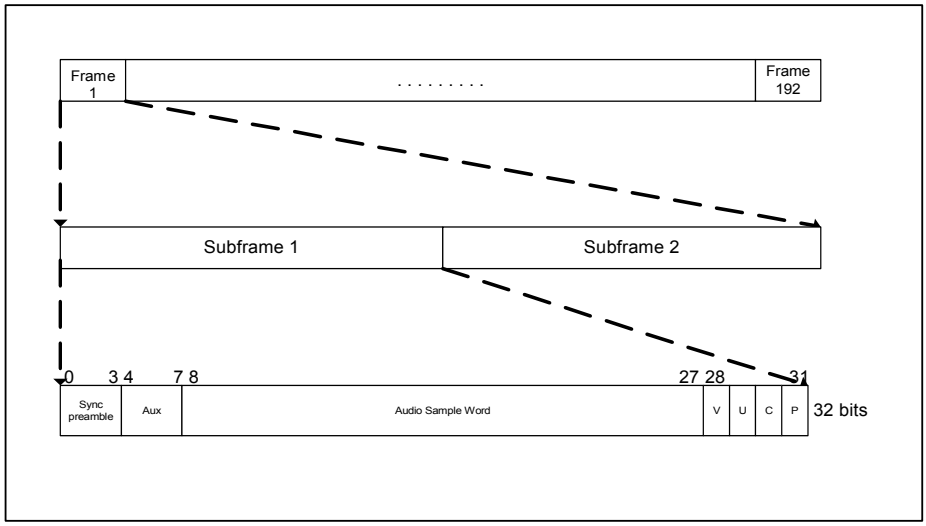


Figure 6 S/PDIF Format

POWER UP CONFIGURATION

The operating mode of the WM8805 is dependent upon the state of SDIN, SCLK, SDOUT, CSB and GPO0 when the device is powered up or a hardware reset occurs. Table 6 summarises the configuration options.

		HW RESET = 0			HW RESET = 1		
		SWMODE		**HWMODE**	**SWMODE**		**HWMODE**
PIN	**SDIN**	HWMODE / SWMODE Select			SDIN		N/A
	SCLK	N/A		AIF_MS	SCLK		GPO (TRANS_ERR)
	SDOUT	N/A		AIF_CONF[0]	2-wire	3-wire	GPO (NON_AUDIO)
					GPO	SDOUT	
	CSB	2-wire	3-wire	TXSRC	2-wire	3-wire	GPO (UNLOCK)
		Device Address	N/A		GPO	CSB	
	GPO0	2-wire/3-wire Mode Select		AIF_CONF[1]	GPO		GPO (GEN_FLAG)

Table 6 Device Configuration at Power up or Hardware Reset

Note: AIF_CONF[1:0] configures the audio interface when the device operates in hardware mode. Refer to Table 16 for description of modes.

When the device powers up, all power up configuration pins are configured as inputs for a minimum of 9.4us and a maximum of 25.6us following the release of the external reset. The times are based on 27MHz and 10MHz crystal clock frequencies respectively. This enables the pins to be sampled and the device to be configured before the pins are released to their selected operating conditions. Figure 7 illustrates how SDIN is sampled.

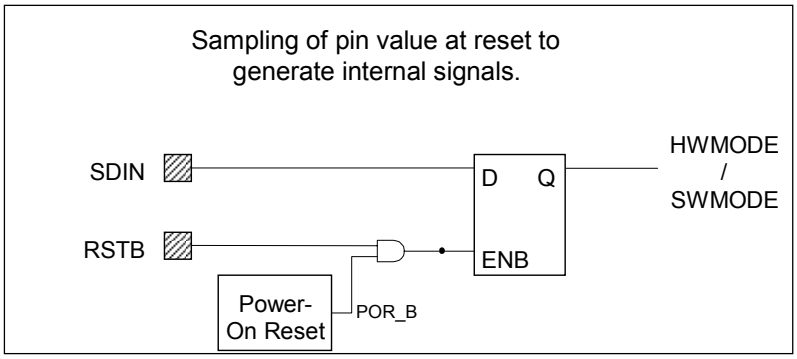


Figure 7 Pin Sampling On Power Up or Hardware Reset

If the device is powered up in Software control mode, all functions of the device are powered down by default and must be powered up individually by writing to the relevant bits of the PWRDN register (Table 7). In Hardware Control Mode, all functions of the device are powered up by default.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30 PWRDN 1Eh	0	PLLPD	1	**PLL Powerdown** 0 = PLL enabled 1 = PLL disabled
	1	SPDIFRXPD	1	**S/PDIF Receiver Powerdown** 0 = S/PDIF receiver enabled 1 = S/PDIF receiver disabled
	2	SPDIFTXPD	1	**S/PDIF Transmitter Powerdown** 0 = S/PDIF transmitter enabled 1 = S/PDIF transmitter disabled
	3	OSCPD	0	**Oscillator Power Down** 0 = Power Up 1 = Power Down
	4	AIFPD	0	**Digital Audio Interface Power Down** 0 = Power Up 1= Power Down
	5	TRIOP	0	**Tri-state all Outputs** 0 = Outputs not tri-stated 1 = Outputs tri-stated

Table 7 Power Down Register

CONTROL INTERFACE OPERATION

Control of the WM8805 is implemented in either hardware control mode or software control mode. The method of control is determined by sampling the state of the SDIN/HWMODE pin at power up or at a hardware reset. If SDIN/HWMODE is low during power up the device is configured in hardware control mode, otherwise the device is configured in software control mode.

SDIN/HWMODE	
0	Hardware mode
1	Software mode

Table 8 Hardware or Software Mode Select

Software control is achieved using a 3-wire (3-wire write, 4-wire read) or a 2-wire serial interface.

The serial interface format is configured by sampling the state of the GPO0/SWIFMODE pin on power up or at a hardware reset. If the GPO0/SWIFMODE pin is low the interface is configured in 2-wire mode, otherwise the interface is configured in 3-wire SPI compatible mode.

GPO0/SWIFMODE	
0	2-wire interface
1	3-wire interface

Table 9 Software Mode Control Interface Select

3-WIRE (SPI COMPATIBLE) SERIAL CONTROL MODE – REGISTER WRITE

SDIN is used for the program data, SCLK is used to clock in the program data and CSB is used to latch in the program data. SDIN is sampled on the rising edge of SCLK. The 3-wire interface write protocol is shown in Figure 8. The CSB can be low for the duration of the write cycle or it can be a short CSB pulse at the end of the write cycle.

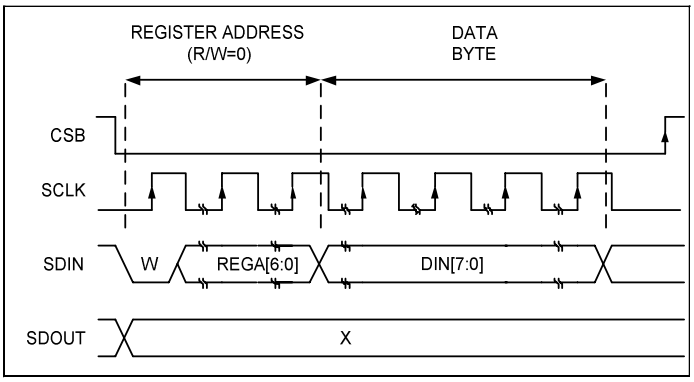


Figure 8 3-Wire Serial Interface Register Write Protocol

- W is a control bit indicating a read or write operation. 0 =write operation, 1 = read operation
- REGA[6:0] is the register Address.
- DIN[7:0] is the data to be written to the register being addressed.
- CSB is edge sensitive – the data is latched on the rising edge of CSB.

3-WIRE SERIAL CONTROL MODE REGISTER READ-BACK

Not all registers can be read. Only the device ID (registers R0, R1 and R2) and the status registers can be read. These status registers are labelled as “read only” in the Register Map section.

The read-only status registers can be read back via the SDOUT pin. The registers can be read by one of two methods, selected by the CONT register bit and the ‘W’ control bit. The oscillator must be powered up before 3-wire control interface read-back is possible.

When CONT =1 and ‘W’=0, a single read-only register can be read back by writing to any other register or to a dummy register. The register to be read is determined by the READMUX[2:0] bits. When a write to the device is performed, the device will respond by returning the status byte of the register selected by the READMUX register bits. The data is returned on the SDOUT pin. This 3-wire interface read-back method using a write access is shown in Figure 9.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R29 SPDRX1 1Dh	2:0	READMUX [2:0]	000	**Status Register Select** Determines which status register is to be read back: 000 = Interrupt Status Register 001 = Channel Status Register 1 010 = Channel Status Register 2 011 = Channel Status Register 3 100 = Channel Status Register 4 101 = Channel Status Register 5 110 = S/PDIF Status Register
	3	CONT	0	**Continuous Read Enable** 0 = Continuous read-back mode disabled 1 = Continuous read-back mode enabled

Table 10 Read-back Control Register

The SDOUT pin is tri-state unless CSB is held low; therefore CSB must be held low for the duration of the read.

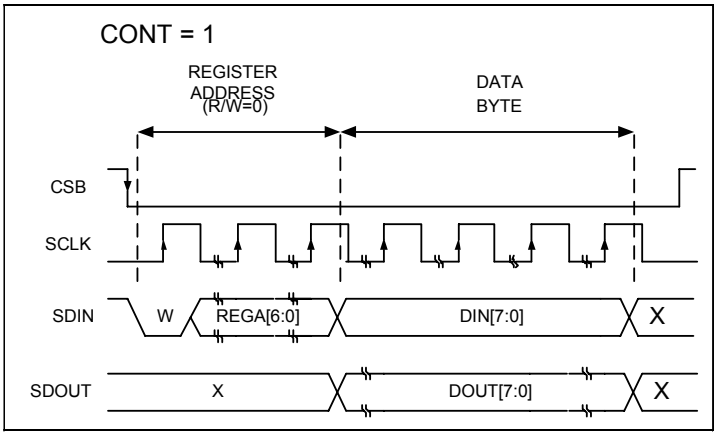


Figure 9 3-Wire Control Interface Read-Back Method 1

The second method of reading the read only status registers is If CONT=0 and ‘W’=1. Using this method the user can read back directly from a register by reading the register address. The device will respond with the contents of the register. The protocol for this read-back method is shown in Figure 10.

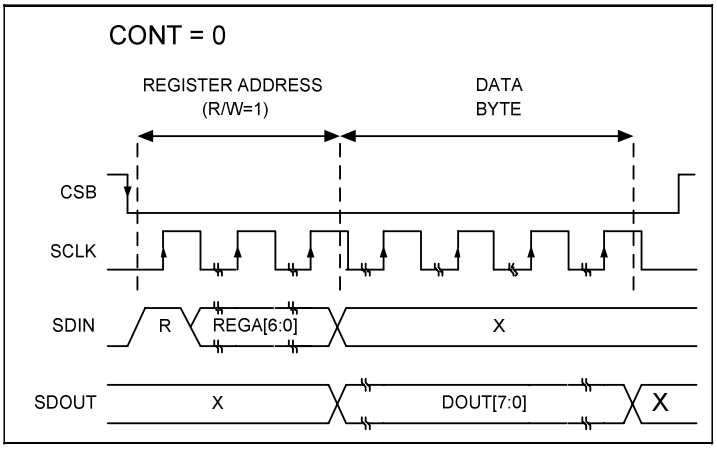


Figure 10 3-Wire Control Interface Read-Back Method 2

2-WIRE SERIAL CONTROL WITH READ-BACK MODE

The WM8805 supports software control via a 2-wire serial bus. Many devices can be controlled by the same bus and each device has a unique 7-bit address (see Table 11).

The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address, DEVA(7:1), and data, REG(6:0), will follow. All devices on the 2-wire bus will shift in the next eight bits on SDIN (7-bit address DEVA(7:1), + read/write 'W' bit, MSB first). If the device address received matches the address of the WM8805, the WM8805 responds by driving SDIN low on the next clock pulse (ACK). This is a device acknowledgement of an address match. If the address does not match that of the WM8805, the device returns to the idle condition and waits for a new start condition and valid address.

Once the WM8805 has acknowledged a matching address, the controller sends the first byte of control data, which is the WM8805 register address (REGA[6:0]). The WM8805 then acknowledges reception of the control data byte by pulling SDIN low for one clock pulse (another ACK). The controller then sends the second byte of control data (DIN[7:0], i.e. the eight bits of register data to be written), and the WM8805 acknowledges again by pulling SDIN low (another ACK).

The transfer of data is complete when there is a low to high transition on SDIN while SCLK is high. After receiving a complete address and data sequence the WM8805 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the device returns to the idle condition.

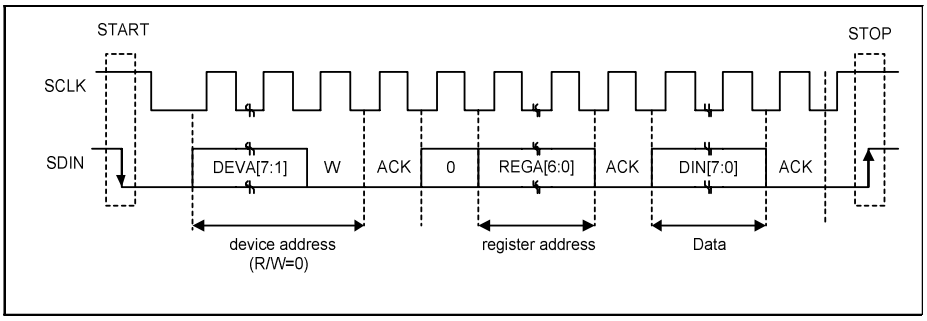


Figure 11 2-Wire Serial Control Interface Write

Multiple consecutive register writes can be performed in 2-wire control mode by setting the CONT bit high. This method allows the entire register map to be defined in a one continuous write operation.

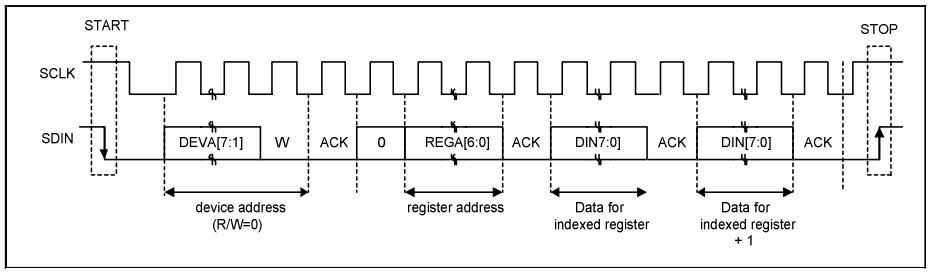


Figure 12 2-Wire Serial Control Interface Multi-Write

The WM8805 has two possible device addresses, which can be selected using the CSB pin during hardware reset.

CSB STATE	DEVICE ADDRESS IN 2-WIRE MODE	ADDRESS (X=R/W BIT)	
		X=0	X= 1
Low	0111010x	0x74	0x75
High	0111011x	0x76	0x77

Table 11 2-Wire Interface Address Selection

2-WIRE SERIAL CONTROL MODE -REGISTER READ-BACK

The WM8805 allows read-back of certain registers in 2-wire mode. The protocol is similar to that used to write to the device. The controller will issue the device address followed by a write bit, the register index will then be passed to the WM8805. At this point the controller will issue a repeated start condition and resend the device address along with a read bit. The WM8805 will acknowledge this and the WM8805 will become a slave transmitter. The WM8805 will transmit the data from the indexed register on SDIN MSB first. When the controller receives the data it will not acknowledge receipt of the data indicating that it will resume master transmitter control of SDIN. The controller will then issue a stop command completing the read cycle. Figure 13 illustrates the read protocol.

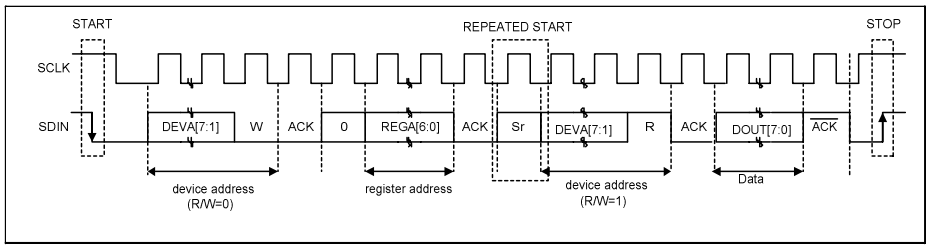


Figure 13 2-Wire Serial Control Interface Read (CONT=0)

2-WIRE SERIAL CONTROL MODE – CONTINUOUS READ-BACK

As in 3-wire mode, there are two methods of reading back data: continuous and non-continuous read-back. Continuous read-back is selected by setting CONT to 1. In continuous read-back mode, the device will return the indexed register first followed by consecutive registers in increasing index order until the controller does not acknowledge the data then issues a stop sequence. This is shown in Figure 14

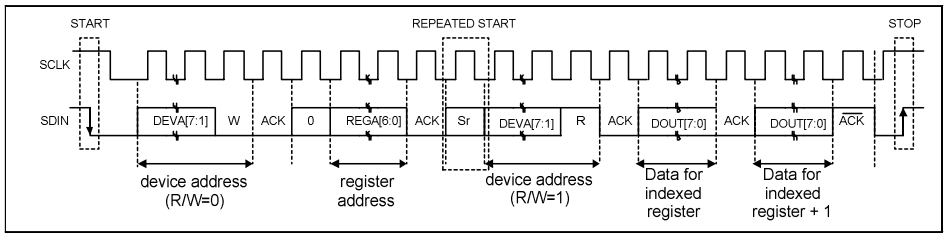


Figure 14 2-Wire Serial Interface Continuous Read-Back (CONT=1)

SOFTWARE REGISTER RESET

Writing to register 0000000 will reset the WM8805. This will reset all register bits to their default values. Note that the WM8805 is powered down by default so writing to this register will power down the device.

DEVICE ID AND REVISION IDENTIFICATION

Registers 0,1 and 2 can be read to identify the device ID and IC revision number. Refer to Table 12 for details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R00 RST/DEVID1 00h	7:0	RESET	N/A	Writing to this register will apply a reset to the device.
		DEVID1[7:0]	00000101	Reading from this register will return the second part of the device ID 00000101 = 0x05
R01 DEVID2 01h (read only)	7:0	DEVID2[7:0]	10001000	Reading from this register will return the first part of the device ID 10001000 = 0x88
R02 DEVREV 02h	3:0	DEVREV [3:0]	N/A	Reading from this register will return the device revision. 0x1 = revision 1

Table 12 Software Reset Register and Device ID

HARDWARE CONTROL MODE

The WM8805 can be operated in either software or hardware control modes. The method of control is determined by sampling the state of the SDIN pin during power up or hard reset. If SDIN is LOW during power up or hardware reset, the WM8805 will be switched into hardware control mode.

PIN	0	1
SDIN	Hardware Control Mode	Software Control Mode

Table 13 Hardware / Software Mode Configuration

In hardware control mode the user has limited control over the configuration of the device. Most of the features will assume default values but some can be configured using external pins. When the device is configured in hardware control mode, all functions of the device are powered up.

The clock and data recovery module with the WM8805 will require a 12 MHz crystal derived master clock as the default values for this module cannot be altered in Hardware Control mode.

MASTER / SLAVE MODE SELECTION

The WM8805 can be configured in either master or slave mode In software control mode this is set by writing to AIF_MS in the AIFRX register. In hardware control mode this is controlled by sampling the SCLK pin on power up or hardware reset.

PIN (HARDWARE MODE)	REGISTER (SOFTWARE MODE)	0	1
SCLK	AIF_MS	Slave Mode	Master Mode

Table 14 Master / Slave Mode Configuration in Hardware Mode

DIGITAL ROUTING CONTROL

See page 20 for a full description of the signal routing options available in the WM8805. In Software control mode the values set in registers TXSRC and RXINSEL determine the S/PDIF Rx data source and destination. In hardware control mode the device can receive data only from RX0 but can set the value of TXSRC directly using the CSB pin. This determines the S/PDIF transmitter data source

PIN (HARDWARE MODE)	REGISTER (SOFTWARE MODE)	0	1
CSB	TXSRC	S/PDIF Rx	AIF Rx

Table 15 S/PDIF Transmitter Digital Routing Control Configuration

AUDIO INTERFACE CONTROL

In software control mode the audio data word length and audio data format can be set independently for the receiver and transmitter sides of the interface. However, in hardware control mode both sides of the interface are combined and the configuration is set using SDOUT and GPO0 pins as described in Table 6 and Table 16. Note that AIF_CONF[1:0] configures the audio interface when the device operates in hardware mode.

GPO0 / AIFCONF[1]	SDOUT / AIFCONF[0]	DESCRIPTION
0	0	16-bit I^2S
0	1	24-bit I^2S
1	0	24-bit Left Justified With Flags
1	1	16-bit Right Justified

Table 16 Digital Audio Interface Control in Hardware Control Mode

STATUS INFORMATION

In hardware control mode the WM8805 outputs a selection of status flags for the user. Table 17 describes the flags which are available and the output pins on which they are available.

PIN	STATUS FLAG
SCLK	TRANS_ERR
SDOUT	NON_AUDIO
CSB	UNLOCK
GPO0	GEN_FLAG

Table 17 Hardware Control Mode Status Flag Configuration

A full description of the status flags is given in Table 45.

DIGITAL ROUTING CONTROL

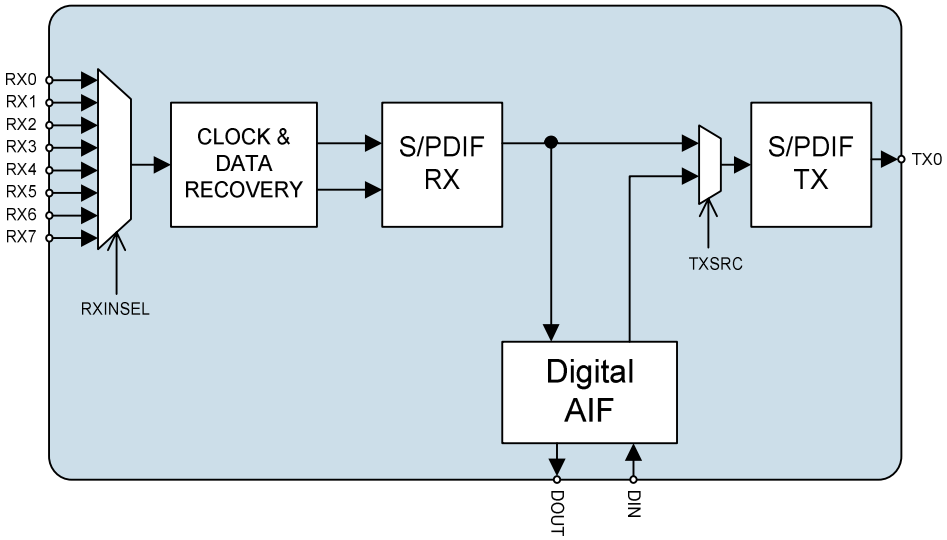


Figure 15 Digital Routing Paths within the WM8805

Digital signal routing within the WM8805 is controlled by two registers, RXINSEL and TXSRC. RXINSEL selects the S/PDIF input which is passed through the clock and data recovery circuit to the S/PDIF receiver and TXSRC selects the data source that is passed to the S/PDIF transmitter.

In order to ensure proper operation when changing TXSRC, the S/PDIF transmitter module should be powered down prior to changing the TXSRC control register and powered up again once the routing path has been changed.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8 PLL6 08h	2:0	RXINSEL[2:0]	000	**S/PDIF Rx Input Select** Select the S/PDIF input to pass to the receiver circuit. 000 – RX0 001 – RX1 010 – RX2 011 – RX3 100 – RX4 101 – RX5 110 – RX6 111 – RX7
R30 PWRDN 1Eh	2	SPDIFTXPD	1	**S/PDIF Transmitter Powerdown** 0 = S/PDIF transmitter enabled 1 = S/PDIF transmitter disabled
R21 SPDTX4 15h	6	TXSRC	1	**S/PDIF Transmitter Data Source** 0 = S/PDIF Received Data – SPDIFTXCLK Source = CLK2 1 = Digital Audio Interface Received Data – SPDIFTXCLK Source = MCLK Input/Output Signal at MCLK Pin

Table 18 Digital Signal Routing Control Registers

MASTER CLOCK AND PHASE LOCKED LOOP

SOFTWARE MODE INTERNAL CLOCKING

The WM8805 is equipped with a comprehensive clocking scheme that provides maximum flexibility and function and many configurable routing possibilities for the user in software mode. An overview of the software mode clocking scheme is shown in Figure 16.

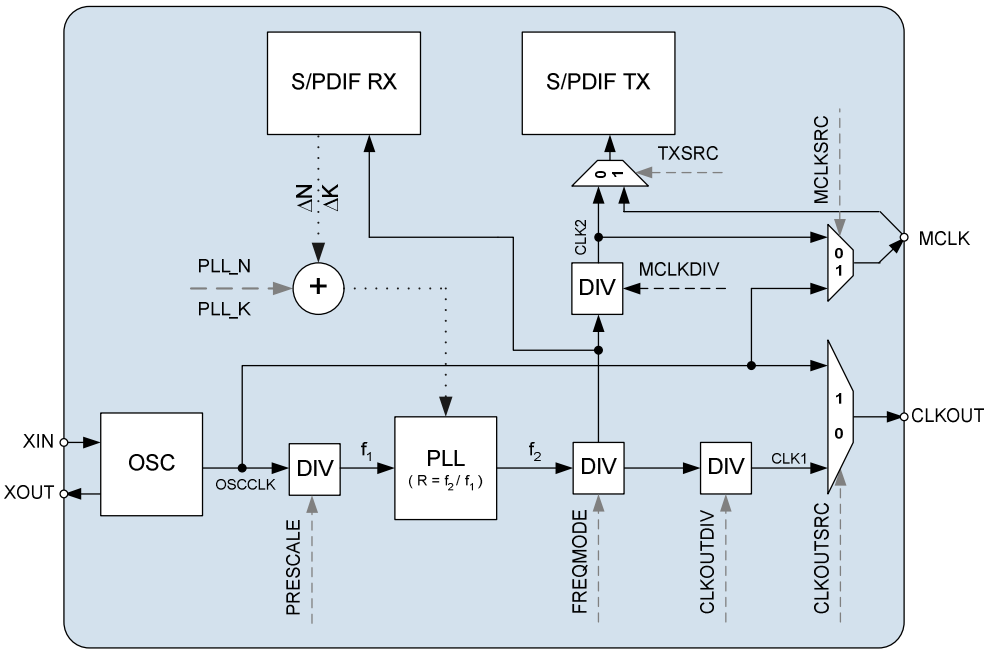


Figure 16 Software Mode Clocking Scheme Overview

The clocking scheme can be divided into four sections. These are detailed as follows:

OSCILLATOR

The primary function of the oscillator is to generate the oscillator clock (OSCCLK) for the PLL input. Whenever the PLL or the S/PDIF receiver is enabled, the oscillator must be used to generate the OSCCLK signal for the PLL.

The secondary function of the oscillator is to generate the OSCCLK so that it can be selected internally as the clock source for:

- The MCLK output pin, when the pin is configured as an output.
- The CLKOUT output pin, when enabled.

The oscillator has one control bit as shown in Table 19. The oscillator must be powered up to generate the OSCCLK signal.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30 PWRDN 1Eh	3	OSCPD	1	**Oscillator Power Down Control** 0 = Power up 1 = Power down

Table 19 Oscillator Control

The oscillator uses a Pierce type oscillator drive circuit. This circuit requires an external crystal and appropriate external loading capacitors. The oscillator circuit contains a bias generator within the WM8805 and hence an external bias resistor is not required. Crystal frequencies between 10 and 14.4MHz or 16.28 and 27MHz can be used in software mode. The recommended circuit is shown in the recommended components diagram, please refer to Figure 29.

Alternatively, an external CMOS compatible clock signal can be applied to the XIN pin in the absence of a crystal, although this is not recommended when using the PLL as the PLL requires a jitter-free OSCCLK signal for optimum performance.

PHASE-LOCKED LOOP (PLL)

The WM8805 has an on-chip phase-locked loop (PLL) circuit that can be used to synthesise clock signals from the external oscillator clock. The PLL can be used to:

- Generate clocks necessary for the S/PDIF receiver to lock on to and recover S/PDIF data from an incoming S/PDIF data stream.
- Generate clocks which may be used to drive the MCLK and/or CLKOUT pins.
- Generate clocks which may be used by the S/PDIF transmitter to encode and transmit a S/PDIF data stream.

The PLL can be enabled or disabled using the PLLPD register bit as shown in Table 1.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30 PWRDN 1Eh	0	PLLPD	1	**PLL Power Down Control** 0 = Power up PLL 1 = Power down PLL

Table 20 PLL Power Down Control

The PLL has two modes of operation:

- **S/PDIF Receive Mode (Automatic PLL Mode – Selected if S/PDIF Receiver Enabled)**

In S/PDIF receive mode, the PLL is automatically controlled by the S/PDIF receiver to allow the receiver to use the PLL to lock on to and track the incoming S/PDIF data stream.

Please refer to the S/PDIF Receiver section within the Internal Clocking description for full details.

If the CLKOUT or MCLK clocks are sourced from either CLK1 or CLK2 in this mode, the frequency of these signals will be modified based on the clock rate of the incoming S/PDIF data stream. If the sample rate of the incoming stream is changed, the MCLK and CLKOUT signals will continue to be output, but will not be valid until the S/PDIF receiver has locked to the incoming stream at the new sample rate. If the incoming S/PDIF stream stops, the PLL N and K values will be frozen and the output clocks will continue at the frequency set by the last recovered S/PDIF stream. If the S/PDIF input stream is removed then it is possible for the PLL to detect small pulse as the data is being removed. This may result in the output clocks changing to an invalid frequency. Note also that if the device is power-on and configured with no S/PDIF input data stream, then the PLL will default to approximately 24MHz.

- **User Mode (Manual PLL Mode – Selected if S/PDIF Receiver Disabled)**

In user mode, the user has full control over the PLL function and operation. In this mode, the user can accurately specify the PLL N and K multiplier values (using the PLL_N and PLL_K registers), divider values (PRESCALE and FREQMODE) and can hence control the generated CLK1 and CLK2 frequencies. Refer to Table 21 for details of the registers available for configuration in this mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 PLL1 03h	7:0	PLL_K[7:0]	00100001	Fractional (K) part of PLL frequency ratio (R). Value K is one 22-digit binary number spread over registers R3, R4 and R5 as shown. **Note: PLL_K must be set to specific values when the S/PDIF receiver is used. Refer to S/PDIF Receiver clocking section for details.**
R4 PLL2 04h	7:0	PLL_K[15:8]	11111101	
R5 PLL3 05h	5:0	PLL_K[21:16]	00110110	
R6 PLL4 06h	3:0	PLL_N[3:0]	0111	Integer (N) part of PLL frequency ratio (R). Use values in the range 5 ≤ PLL_N ≤ 13 as close as possible to 8 **Note: PLL_N must be set to specific values when the S/PDIF receiver is used. Refer to S/PDIF Receiver clocking section for details.**

Table 21 User Mode PLL_K and PLL_N Multiplier Control

PLL CONFIGURATION

The PLL performs a configurable frequency multiplication of the input clock signal (f_1). The multiplication factor of the PLL (denoted by 'R') is variable and is defined by the relationship: $R = (f_2 \div f_1)$.

The multiplication factor is set using register bits PLL_N and PLL_K (refer to Table 21). The multiplication effect of both the N and K multipliers are additive (i.e. if N is configured to provide a multiplication factor of 8 and K is configured to provide a multiplication factor of 0.192, the overall multiplication factor is 8 + 0.192 = 8.192).

In order to choose and configure the correct values for PLL_N and PLL_K, multiplication factor R must first be calculated. Once value R is calculated, the value of PLL_N is the integer (whole number) value of R, ignoring all digits to the right of the decimal point. For example, if R is calculated to be 8.196523, PLL_N is simply 8.

Once PLL_N is calculated, the PLL_K value is simply the integer value of (2^{22} (R-PLL_N)). For example, if R is 8.196523 and PLL_N is 8, PLL_K is therefore (2^{22} (8.196523-8)), which is 824277 (ignoring all digits to the right of the decimal point).

Note: the PLL is designed to operate with best performance (shortest lock time and optimum stability) when f_2 is between 90 and 100MHz and PLL_N is 8. However, acceptable PLL_N values lie in the range 5 ≤ PLL_N ≤ 13. Do not use values outwith this range and it is recommended that the chosen value of PLL_N is as close to 8 as possible for optimum performance.

An output divider is provided to allow the f_2 clock signal to be divided to a frequency suitable for use as the source for the MCLK, CLKOUT or S/PDIF transmitter. The divider output is configurable and is set by the FREQMODE bits. The PLL is also equipped with a pre-scale divider which offers frequency divide by one or two before the OSCCLK signal is fed to the PLL. Please refer to Table 22 for details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 PLL4 06h	4	PRESCALE	0	**PLL Pre-scale Divider Select** 0 = Divide by 1 (PLL input clock = oscillator clock) 1 = Divide by 2 (PLL input clock = oscillator clock ÷ 2)
R7 PLL5 07h	1:0	FREQMODE[1:0]	10	**PLL Post-scale Divider Select** Selects the PLL output divider value in conjunction with MCLKDIV and CLKOUTDIV. Refer to Table 23 for details of FREQMODE operation. **Note: FREQMODE[1:0] bits are automatically set in S/PDIF Receive Mode.**

Table 22 Pre and Post PLL Clock Divider Control

PLL CONFIGURATION EXAMPLE

Consider the situation where the oscillator clock (OSCCLK) input frequency is fixed at 12MHz and the required MCLK frequency is 12.288MHz.

1. Calculate the f_2, FREQMODE and MCLKDIV Values

The PLL is designed to operate with best performance when the f_2 clock is between 90 and 100MHz. The necessary MCLK frequency is 12.288MHz. Choose MCLKDIV and FREQMODE values to set the f_2 frequency in the range of 90 to 100MHz. In this case, the default values (MCLKDIV = 0 and FREQMODE[1:0] = 10) will set the f_2 frequency at 98.304MHz; this value is within the 90 to 100MHz range and is hence acceptable.

- MCLKDIV = 0
- FREQMODE[1:0] = 10
- f_2 = 98.304MHz

2. Calculate R Value

Using the relationship: R = ($f_2 \div f_1$), the value of R can be calculated.

- R = ($f_2 \div f_1$)
- R = (98.304 ÷ 12)
- R = 8.192

3. Calculate PLL_N Value

The value of PLL_N is the integer (whole number) value of R, ignoring all digits to the right of the decimal point. In this case, R is 8.192, hence PLL_N is 8.

4. Calculate PLL_K Value

The PLL_K value is simply the integer value of (2^{22} (R-PLL_N)).

- PLL_K = integer part of (2^{22} x (8.192 – 8))
- PLL_K = integer part of 805306.368
- PLL_K = 805306 (decimal) / C49BA (hex)

A number of example configurations are shown in Table 23. Many other configurations are possible; Table 23 shows only a small number of valid possibilities.

OSC CLK (MHz)	PRE-SCALE	F_1 (MHz)	F_2 (MHz)	R	PLL_N (Hex)	PLL_K (Hex)	FREQ MODE [1:0]	MCLK DIV	MCLK (MHz)	CLKOUT DIV [1:0]	CLK OUT (MHz)
12	0	12	98.304	8.192	8	C49BA	00	1	24.576	01	49.152
12	0	12	98.304	8.192	8	C49BA	10	0	12.288	00	24.576
12	0	12	98.304	8.192	8	C49BA	10	1	6.144	01	12.288
12	0	12	98.304	8.192	8	C49BA	10	0	12.288	10	6.144
12	0	12	98.304	8.192	8	C49BA	10	1	6.144	11	3.072
24	1	12	90.3168	7.5264	7	21B089	01	0	22.5792	00	45.1584
24	1	12	90.3168	7.5264	7	21B089	10	0	11.2896	00	22.5792
24	1	12	90.3168	7.5264	7	21B089	10	1	5.6448	01	11.2896
24	1	12	90.3168	7.5264	7	21B089	10	0	11.2896	10	5.6448
24	1	12	90.3168	7.5264	7	21B089	10	1	5.6448	11	2.8224
27	1	13.5	98.304	7.2818	7	1208A5	10	0	12.288	01	12.288
27	1	13.5	98.304	7.2818	7	1208A5	10	1	6.144	10	6.144
27	1	13.5	90.3168	6.6901	6	2C2B24	10	0	11.2896	01	11.2896
27	1	13.5	90.3168	6.6901	6	2C2B24	10	1	5.6448	10	5.6448

Table 23 User Mode PLL Configuration Examples

When considering settings not shown in this table, the key configuration parameters which must be selected for optimum operation are:

- $90MHz \leq f_2 \leq 100MHz$
- $5 \leq PLL\_N \leq 13$
- OSCCLOCK = 10 to 14.4MHz or 16.28 to 27MHz

PLL INTEGER AND FRACTIONAL CONTROL MODES

The PLL can be operated in either fractional or integer control modes. In PLL User Mode, it is recommended that the PLL should be operated in fractional control mode at all times. When the S/PDIF receiver is enabled, the PLL **must** be operated in fractional control mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 PLL5 07h	2	FRACEN	1	**Integer/Fractional PLL Mode Select** 0 = Integer PLL (PLL_N value used, PLL_K value ignored) 1 = Fractional PLL (both PLL_N and PLL_K values used) **Note: FRACEN must be set to enable the fractional PLL when using S/PDIF Receive Mode.**

Table 24 PLL Fractional/Integer Mode Select

MASTER CLOCK (MCLK)

The master clock (MCLK) signal is used to supply reference clock signals to the following circuit blocks:

- The Digital Audio Interface
- The S/PDIF Transmitter

The master clock (MCLK) pin can be configured as either a clock input or output depending on the digital audio interface mode as shown in Table 25.