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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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WM8904

Ultra Low-Power Codec for Portable Audio Applications

DESCRIPTION

The WM8904 is a high performance ultra-low power stereo CODEC optimised for portable audio applications.

The device features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques - incorporating an innovative dual-mode charge pump architecture - to optimise efficiency and power consumption during playback. The ground-referenced headphone and line outputs eliminate AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise.

Control sequences for audio path setup can be pre-loaded and executed by an integrated control write sequencer to reduce software driver development and minimise pops and clicks via SilentSwitch™ technology.

The analogue input stage can be configured for single ended or differential inputs. Up to 3 stereo microphone or line inputs may be connected. The input impedance is constant with PGA gain setting.

A stereo digital microphone interface is provided, with a choice of two inputs.

A dynamic range controller provides compression and level control to support a wide range of portable recording applications. Anti-clip and quick release features offer good performance in the presence of loud impulsive noises.

ReTune™ Mobile 5-band parametric equaliser with fully programmable coefficients is integrated for optimization of speaker characteristics. Programmable dynamic range control is also available for maximizing loudness, protecting speakers from clipping and preventing premature shutdown due to battery droop.

Common audio sampling frequencies are supported from a wide range of external clocks, either directly or generated via the FLL.

The WM8904 can operate directly from a single 1.8V switched supply. For optimal power consumption, the digital core can be operated from a 1.0V supply.

FEATURES

- 3.0mW quiescent power consumption for DAC to headphone playback
- DAC SNR 96dB typical, THD -86dB typical
- ADC SNR 91dB typical, THD -80dB typical

- 2.4mW quiescent power consumption for analogue bypass playback

- Control write sequencer for pop minimised start-up and shutdown
- Single register write for default start-up sequence

- Integrated FLL provides all necessary clocks
  - Self-clocking modes allow processor to sleep
  - All standard sample rates from 8kHz to 96kHz

- Stereo digital microphone input
- 3 single ended inputs per stereo channel
- 1 fully differential mic / line input per stereo channel

- Digital Dynamic Range Controller (compressor / limiter)
- Digital sidetone mixing

- Ground-referenced headphone driver
- Ground-referenced line outputs

- 32-pin QFN package (4 x 4mm, 0.4mm pitch)
- 36-ball WLCSP package (2.6 x 2.5mm, 6 x 6 ball grid, 0.4mm pitch)

APPLICATIONS

- Portable multimedia players
- Multimedia handsets
- Handheld gaming
- Wireless headsets
- Mobile internet devices
- Netbooks

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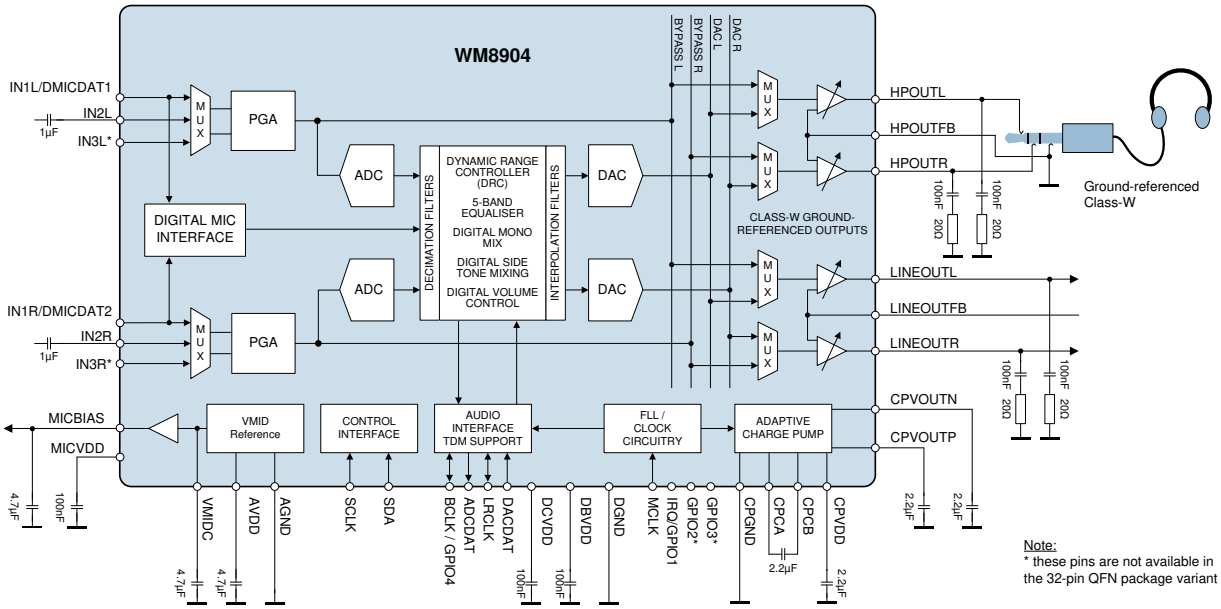
BLOCK DIAGRAM



Note:
* these pins are not available in the 32-pin QFN package variant

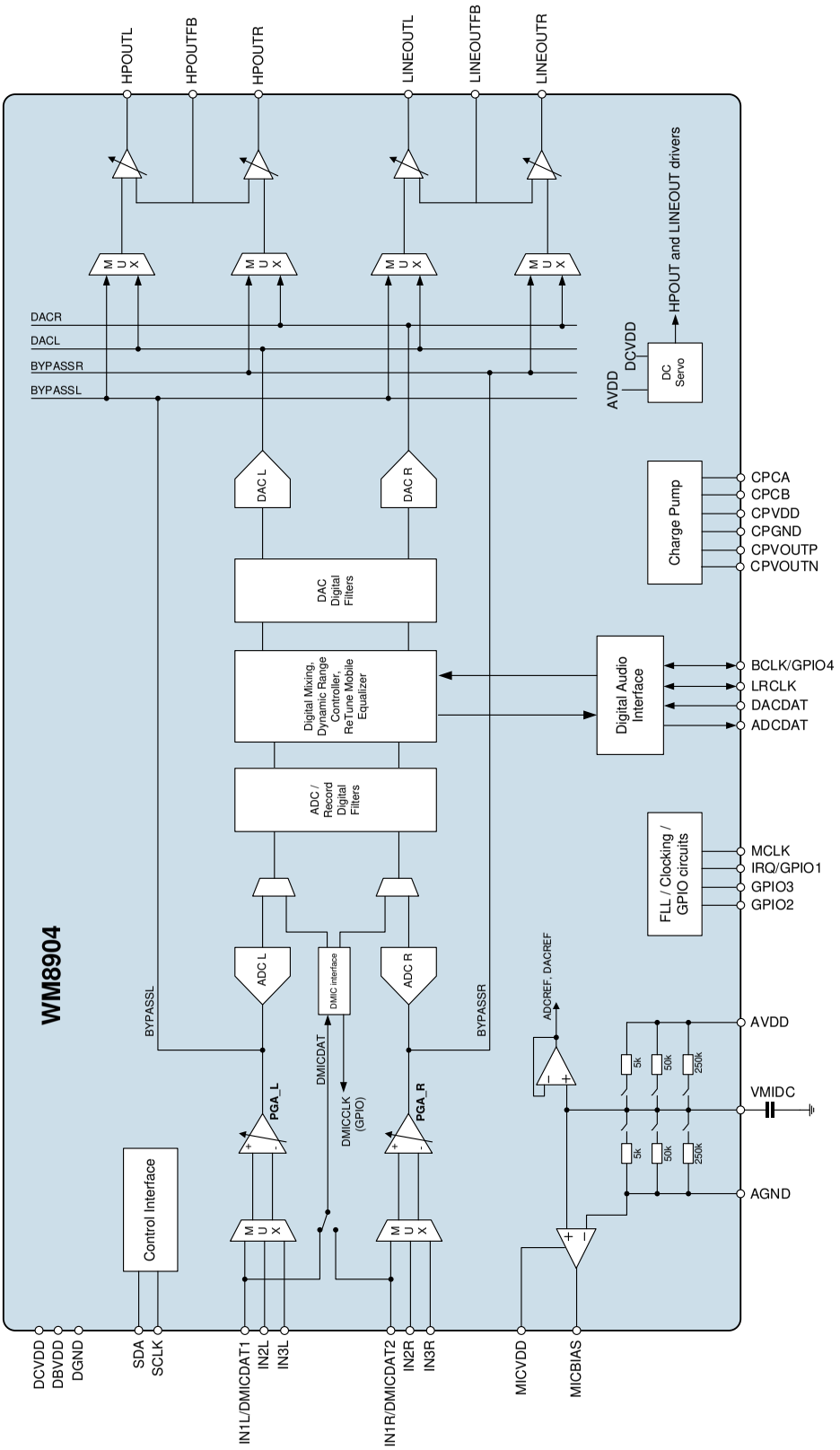
TABLE OF CONTENTS

DESCRIPTION 1
FEATURES 1
APPLICATIONS 1
BLOCK DIAGRAM 2
TABLE OF CONTENTS 3
AUDIO SIGNAL PATHS DIAGRAM 6
PIN CONFIGURATION 7
ORDERING INFORMATION 8
PIN DESCRIPTION 9
ABSOLUTE MAXIMUM RATINGS 10
RECOMMENDED OPERATING CONDITIONS 10
ELECTRICAL CHARACTERISTICS 11
TERMINOLOGY 11
COMMON TEST CONDITIONS 11
INPUT SIGNAL PATH 12
OUTPUT SIGNAL PATH 16
BYPASS PATH 18
CHARGE PUMP 18
FLL 18
OTHER PARAMETERS 19
POWER CONSUMPTION 21
COMMON TEST CONDITIONS 21
POWER CONSUMPTION MEASUREMENTS 21
SIGNAL TIMING REQUIREMENTS 25
COMMON TEST CONDITIONS 25
MASTER CLOCK 25
AUDIO INTERFACE TIMING 26
MASTER MODE 26
SLAVE MODE 27
TDM MODE 28
CONTROL INTERFACE TIMING 29
DIGITAL FILTER CHARACTERISTICS 30
ADC FILTER RESPONSES 31
ADC HIGH PASS FILTER RESPONSES 31
DAC FILTER RESPONSES 32
DE-EMPHASIS FILTER RESPONSES 33
DEVICE DESCRIPTION 34
INTRODUCTION 34
ANALOGUE INPUT SIGNAL PATH 35
INPUT PGA ENABLE 36
INPUT PGA CONFIGURATION 36
SINGLE-ENDED INPUT 38
DIFFERENTIAL LINE INPUT 38
DIFFERENTIAL MICROPHONE INPUT 39
INPUT PGA GAIN CONTROL 39
INPUT PGA COMMON MODE AMPLIFIER 41
ELECTRET CONDENSER MICROPHONE INTERFACE 42
MICBIAS CONTROL 42

MICBIAS CURRENT DETECT 43
MICBIAS CURRENT DETECT FILTERING 43
MICROPHONE HOOK SWITCH DETECTION 45
DIGITAL MICROPHONE INTERFACE 46
ANALOGUE-TO-DIGITAL CONVERTER (ADC) 47
ADC DIGITAL VOLUME CONTROL 48
HIGH PASS FILTER 50
ADC OVERSAMPLING RATIO (OSR) 51
DYNAMIC RANGE CONTROL (DRC) 51
COMPRESSION/LIMITING CAPABILITIES 52
GAIN LIMITS 53
DYNAMIC CHARACTERISTICS 54
ANTI-CLIP CONTROL 54
QUICK RELEASE CONTROL 55
GAIN SMOOTHING 56
INITIALISATION 56
RETUNE™ MOBILE PARAMETRIC EQUALIZER (EQ) 57
DEFAULT MODE (5-BAND PARAMETRIC EQ) 57
RETUNE™ MOBILE MODE 58
EQ FILTER CHARACTERISTICS 58
DIGITAL MIXING 60
DIGITAL MIXING PATHS 60
DAC INTERFACE VOLUME BOOST 62
DIGITAL SIDETONE 62
DIGITAL-TO-ANALOGUE CONVERTER (DAC) 64
DAC DIGITAL VOLUME CONTROL 64
DAC SOFT MUTE AND SOFT UN-MUTE 66
DAC MONO MIX 67
DAC DE-EMPHASIS 67
DAC SLOPING STOPBAND FILTER 68
DAC OVERSAMPLING RATIO (OSR) 68
OUTPUT SIGNAL PATH 69
OUTPUT SIGNAL PATHS ENABLE 70
HEADPHONE / LINE OUTPUT SIGNAL PATHS ENABLE 70
OUTPUT MUX CONTROL 73
OUTPUT VOLUME CONTROL 74
ANALOGUE OUTPUTS 76
HEADPHONE OUTPUTS – HPOUTL AND HPOUTR 76
LINE OUTPUTS – LINEOUTL AND LINEOUTR 76
EXTERNAL COMPONENTS FOR GROUND REFERENCED OUTPUTS 77
REFERENCE VOLTAGES AND MASTER BIAS 77
ANALOGUE REFERENCE AND MASTER BIAS 77
LOW POWER PLAYBACK MODE 79
POP SUPPRESSION CONTROL 80
DISABLED INPUT CONTROL 80
CHARGE PUMP 80
DC SERVO 82
DC SERVO ENABLE AND START-UP 82
DC SERVO ACTIVE MODES 85
DC SERVO READBACK 87
DIGITAL AUDIO INTERFACE 87
MASTER AND SLAVE MODE OPERATION 87
OPERATION WITH TDM 88
BCLK FREQUENCY 89
AUDIO DATA FORMATS (NORMAL MODE) 89

AUDIO DATA FORMATS (TDM MODE) 91
DIGITAL AUDIO INTERFACE CONTROL 93
AUDIO INTERFACE OUTPUT TRI-STATE 94
BCLK AND LRCLK CONTROL 94
COMPANDING 95
LOOPBACK 97
DIGITAL PULL-UP AND PULL-DOWN 97
CLOCKING AND SAMPLE RATES 98
SYSCLK CONTROL 100
CONTROL INTERFACE CLOCKING 100
CLOCKING CONFIGURATION 101
ADC / DAC CLOCK CONTROL 102
OPCLK CONTROL 102
TOCLK CONTROL 103
ADC / DAC OPERATION AT 88.2K / 96K 103
FREQUENCY LOCKED LOOP (FLL) 104
FREE-RUNNING FLL CLOCK 109
GPIO OUTPUTS FROM FLL 109
EXAMPLE FLL CALCULATION 110
EXAMPLE FLL SETTINGS 111
GENERAL PURPOSE INPUT/OUTPUT (GPIO) 112
IRQ/GPIO1 112
GPIO2 113
GPIO3 113
BCLK/GPIO4 114
INTERRUPTS 115
USING IN1L AND IN1R AS INTERRUPT INPUTS 119
CONTROL INTERFACE 120
CONTROL WRITE SEQUENCER 122
INITIATING A SEQUENCE 122
PROGRAMMING A SEQUENCE 123
DEFAULT SEQUENCES 126
START-UP SEQUENCE 126
SHUTDOWN SEQUENCE 128
POWER-ON RESET 129
QUICK START-UP AND SHUTDOWN 131
QUICK START-UP (DEFAULT SEQUENCE) 131
FAST START-UP FROM STANDBY 132
QUICK SHUTDOWN (DEFAULT SEQUENCE) 133
SOFTWARE RESET AND CHIP ID 133
REGISTER MAP 134
REGISTER BITS BY ADDRESS 138
APPLICATIONS INFORMATION 177
RECOMMENDED EXTERNAL COMPONENTS 177
MIC DETECTION SEQUENCE USING MICBIAS CURRENT 179
PACKAGE DIMENSIONS 181
IMPORTANT NOTICE 183
REVISION HISTORY 184

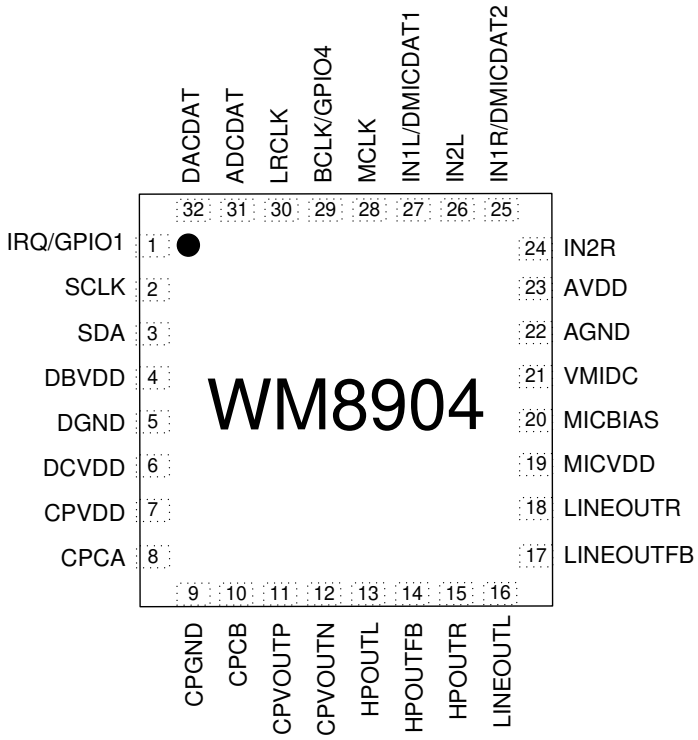
AUDIO SIGNAL PATHS DIAGRAM



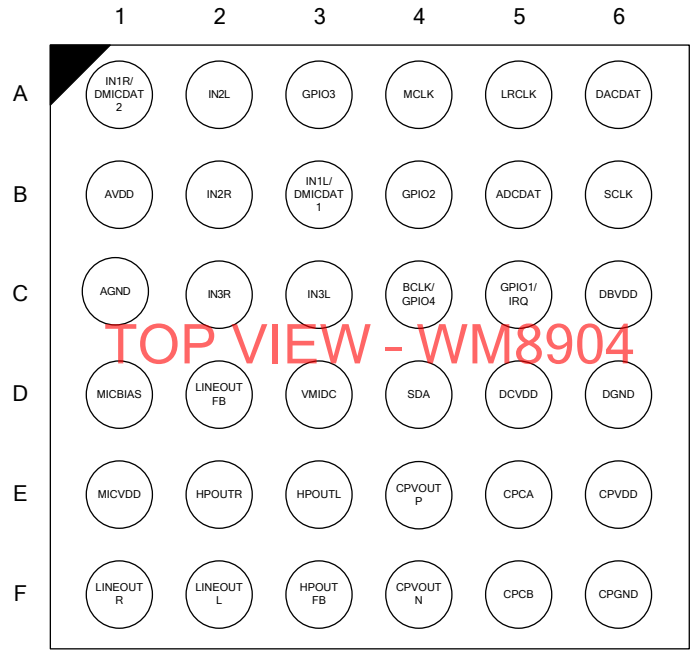
PIN CONFIGURATION

The WM8904 is supplied in a 32-pin QFN package or in a 36-ball CSP format.

The diagram below shows the 32-pin QFN configuration.



The following diagram shows the 36-ball CSP configuration.



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8904CGEFL/V	-40°C to +85°C	32-lead QFN (4 x 4 x 0.75mm, 0.4mm pitch, lead-free)	MSL3	260°C
WM8904CGEFL/RV	-40°C to +85°C	32-lead QFN (4 x 4 x 0.75mm, 0.4mm pitch, lead-free, tape and reel)	MSL3	260°C
WM8904ECS/R	-40°C to +85°C	36-ball W-CSP (2.6 x 2.5 x 0.5mm, 6 x 6 ball grid, 0.4mm pitch, lead-free, tape and reel)	MSL1	260°C

Note:

QFN Reel quantity = 3,500

W-CSP Reel quantity = 3,500

PIN DESCRIPTION

NAME	WLCSP 6×6	QFN-32	TYPE	DESCRIPTION
IN1L / DMICDAT1	B3	27	Analogue / Digital Input	Left channel input 1 / Digital microphone data input 1
IN2L	A2	26	Analogue Input	Left channel input 2
IN3L	C3	n/a	Analogue Input	Left channel input 3
IN1R / DMICDAT2	A1	25	Analogue / Digital Input	Right channel input 1 / Digital microphone data input 2
IN2R	B2	24	Analogue Input	Right channel input 2
IN3R	C2	n/a	Analogue Input	Right channel input 3
MICBIAS	D1	20	Analogue Output	Microphone bias
MICVDD	E1	19	Supply	Microphone bias amp supply
HPOUTL	E3	13	Analogue Output	Left headphone output (line or headphone output)
HPOUTR	E2	15	Analogue Output	Right headphone output (line or headphone output)
HPOUTFB	F3	14	Analogue Input	Headphone output ground loop noise rejection feedback
LINEOUTL	F2	16	Analogue Output	Left line output 1 (line output)
LINEOUTR	F1	18	Analogue Output	Right line output 1 (line output)
LINEOUTFB	D2	17	Analogue Input	Line output ground loop noise rejection feedback
CPVDD	E6	7	Supply	Charge pump power supply
CPGND	F6	9	Supply	Charge pump ground
CPCA	E5	8	Analogue Output	Charge pump flyback capacitor pin
CPCB	F5	10	Analogue Output	Charge pump flyback capacitor pin
CPVOUTP	E4	11	Analogue Output	Charge pump positive supply decoupling (powers HPOUTL/R, LINEOUTL/R)
CPVOUTN	F4	12	Analogue Output	Charge pump negative supply decoupling (powers HPOUTL/R, LINEOUTL/R)
AVDD	B1	23	Supply	Analogue power supply (powers analogue inputs, reference, ADC, DAC)
AGND	C1	22	Supply	Analogue power return
VMIDC	D3	21		Midrail voltage decoupling capacitor
DCVDD	D5	6	Supply	Digital core supply
DBVDD	C6	4	Supply	Digital buffer supply (powers audio interface and control interface)
DGND	D6	5	Supply	Digital ground (return path for DCVDD and DBVDD)
MCLK	A4	28	Digital Input	Master clock for CODEC
BCLK / GPIO4	C4	29	Digital Input / Output	Audio interface bit clock / GPIO4
LRCLK	A5	30	Digital Input / Output	Audio interface left / right clock (common for ADC and DAC)
DACDAT	A6	32	Digital Input	DAC digital audio data
ADCDAT	B5	31	Digital Output	ADC digital audio data
SCLK	B6	2	Digital Input	Control interface clock input
SDA	D4	3	Digital Input / Output	Control interface data input / output
GPIO1 / IRQ	C5	1	Digital Input / Output	GPIO1 / Interrupt
GPIO2	B4	n/a	Digital Input / Output	GPIO2
GPIO3	A3	n/a	Digital Input / Output	GPIO3
GND_PADDLE	n/a	33		Die Paddle

Note:

1. It is recommended that the QFN ground paddle is connected to analogue ground on the application PCB.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus Logic tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
AVDD, DCVDD	-0.3V	+2.5V
DBVDD,	-0.3V	+4.5V
MICVDD	-0.3V	+4.5V
CPVDD	-0.3V	+2.2V
HPOUTL, HPOUTR, LINEOUTL, LINEOUTR	(CPVDD + 0.3V) * -1	CPVDD + 0.3V
Voltage range digital inputs	DGND -0.3V	DBVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Temperature range, T_A	-40°C	+85°C
Storage temperature after soldering	-65°C	+150°C

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other; there is no restriction on power supply sequencing.
3. HPOUTL, HPOUTR, LINEOUTL, LINEOUTR are outputs, and should not normally become connected to DC levels. However, if the limits above are exceeded, then damage to the WM8904 may occur.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD	0.95	1.0	1.98	V
Digital supply range (Buffer)	DBVDD	1.42	1.8	3.6	V
Analogue supplies range	AVDD	1.71	1.8	2.0	V
Charge pump supply range	CPVDD	1.71	1.8	2.0	V
Microphone bias	MICVDD	1.71	2.5	3.6	V
Ground	DGND, AGND, CPGND		0		V
Operating Temperature (ambient)	T_A	-40	+25	+85	°C

ELECTRICAL CHARACTERISTICS

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is the difference in level between a full scale output signal and the device output noise with no signal applied, measured over a bandwidth of 20Hz to 20kHz. This ratio is also called idle channel noise. (No Auto-zero or Automute function is employed).
2. Total Harmonic Distortion (dB) – THD is the difference in level between a 1kHz full scale sinewave output signal and the first seven harmonics of the output signal. The amplitude of the fundamental frequency of the output signal is compared to the RMS value of the next seven harmonics and expressed as a ratio.
3. Total Harmonic Distortion + Noise (dB) – THD+N is the difference in level between a 1kHz full scale sine wave output signal and all noise and distortion products in the audio band. The amplitude of the fundamental reference frequency of the output signal is compared to the RMS value of all other noise and distortion products and expressed as a ratio.
4. Channel Separation (dB) – is a measure of the coupling between left and right channels. A full scale signal is applied to the left channel only, the right channel amplitude is measured. Then a full scale signal is applied to the right channel only and the left channel amplitude is measured. The worst case channel separation is quoted as a ratio.
5. Multi-Path Crosstalk (dB) – is the measured signal level in the idle path at the test signal frequency relative to the signal level at the output of the active path. The active path is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the specified idle path.
6. Channel Level Matching (dB) – measures the difference in gain between the left and the right channels.
7. Power Supply Rejection Ratio (dB) – PSRR is a measure of ripple attenuation between the power supply pin and an output path. With the signal path idle, a small signal sine wave is summed onto the power supply rail, The amplitude of the sine wave is measured at the output port and expressed as a ratio.
8. All performance measurements carried out with 20kHz AES17 low pass filter for distortion measurements, and an A-weighted filter for noise measurement. Failure to use such a filter will result in higher THD and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.

COMMON TEST CONDITIONS

Unless otherwise stated, the following test conditions apply throughout the following sections:

- DCVDD = 1.0V
- DBVDD = 1.8V
- AVDD = CPVDD =1.8V
- Ambient temperature = +25°C
- Audio signal: 1kHz sine wave, sampled at 48kHz with 24-bit data resolution
- SYSCLK_SRC = 0 (system clock comes direct from MCLK, not from FLL).

Additional, specific test conditions are given within the relevant sections below.

INPUT SIGNAL PATH

Single-ended Stereo Line Record - IN1L+IN1R pins to ADC output

Test conditions:

L_MODE = R_MODE = 00b (Single ended)

LIN_VOL = RIN_VOL = 00101b (0dB)

Total signal path gain = 6dB, incorporating 6dB single-ended to differential conversion gain

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Full Scale Input Signal Level (for ADC 0dBFS).				0.50 -6 1.41		Vrms dBV Vpk-pk
Input Resistance	R_{in}		9	12		kΩ
Input Capacitance	C_{in}			10		pF
Signal to Noise Ratio	SNR	A-weighted ADC_OSR128 = 0 ADC_128_OSR_TST_MODE = 1 ADC_BIASx1P5 = 1		80		dB
		A-weighted ADC_OSR128 = 1 ADC_128_OSR_TST_MODE = 0 ADC_BIASx1P5 = 0	80	90		
Total Harmonic Distortion + Noise	THD+N	-7dBV input		-78	-66	dB
Channel Separation		1kHz signal, -7dBV		85		dB
		10kHz signal, -7dBV		80		
Channel Level Matching		1kHz signal, -7dBV		+/-1		dB
Power Supply Rejection Ratio	PSRR	217Hz, 100mVpk-pk		45		dB
		1kHz, 100mV pk-pk		55		

Differential Stereo Line Record - IN2L+IN3L / IN2R+IN3R pins to ADC output

Test conditions:

L_MODE = R_MODE = 01b (Differential Line)

LIN_VOL = RIN_VOL = 00101b (0dB)

Total signal path gain = 0dB

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Line Input Full Scale Signal Level applied to IN2L or IN2R (for ADC 0dBFS output)				1.00 0 2.83		Vrms dBV Vpk-pk
IN3L, IN3R input range						mV
Input Resistance	R_{in}		9	12		kΩ
Input Capacitance	C_{in}			10		pF
Signal to Noise Ratio	SNR	A-weighted ADC_OSR128 = 0 ADC_128_OSR_TST_MODE = 1 ADC_BIASx1P5 = 1		80		dB
		A-weighted Best performance mode:: ADC_OSR128 = 1 ADC_128_OSR_TST_MODE = 0 ADC_BIASx1P5 = 0	81	91		
Total Harmonic Distortion + Noise	THD+N	-1dBV input		-78	-66	dB
Common Mode Rejection Ratio	CMRR	1kHz, 100mV pk-pk		60		dB
Channel Separation		1kHz signal, -1dBV		85		dB
		10kHz signal, -1dBV		80		
Channel Level Matching		1kHz signal, -1dBV		+/-1		dB
Power Supply Rejection Ratio	PSRR	217Hz, 100mVpk-pk		55		dB
		1kHz, 100mV pk-pk		55		

Single-ended Stereo Record from Analogue Microphones - IN2L / IN2R pins to ADC output

Test conditions:

L_MODE = R_MODE = 00b (Single ended)

LIN_VOL = RIN_VOL = 11111b (+28.3dB)

Total signal path gain = +34.3dB, incorporating 6dB single-ended to differential conversion gain

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Single-ended mic input full-scale Signal Level (for ADC 0dBFS output)				0.019 -34.3 0.055		Vrms dBV Vpk-pk
Input Resistance	R_{in}		9	12		kΩ
Input Capacitance	C_{in}			10		pF
Signal to Noise Ratio	SNR	A-weighted ADC_OSR128 = 0 ADC_128_OSR_TST_MODE = 1 ADC_BIASx1P5 = 1		65		dB
		A-weighted Best performance mode:: ADC_OSR128 = 1 ADC_128_OSR_TST_MODE = 0 ADC_BIASx1P5 = 0		73		
Total Harmonic Distortion + Noise	THD+N	-35.3dBV input		-69		dB
Channel Level Matching		1kHz signal, -35.3dBV		+/-3		dB
Power Supply Rejection Ratio	PSRR	217Hz, 100mVpk-pk		45		dB
		1kHz, 100mV pk-pk		55		

Differential Stereo Record from Analogue Microphones - IN1L+IN2L / IN1R+IN2R pins to ADC output **Test conditions:** L_MODE = R_MODE = 10b (Differential mic) LIN_VOL = RIN_VOL = 00111b (+30dB) Total signal path gain = +30dB						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Differential Mic Input Full Scale Signal Level IN1L-IN2L / IN1R-IN2R (for ADC 0dBFS output)				0.032 -30 0.089		Vrms dBV Vpk-pk
Input Resistance	Rin		100	120		kΩ
Input Capacitance	Cin			10		pF
Signal to Noise Ratio	SNR	A-weighted ADC_OSR128 = 0 ADC_128_OSR_TST_MODE = 1 ADC_BIASx1P5 = 1		68		dB
		A-weighted Best performance mode:: ADC_OSR128 = 1 ADC_128_OSR_TST_MODE = 0 ADC_BIASx1P5 = 0	67	77		
Total Harmonic Distortion + Noise	THD+N	-31dBV input		-75	-65	dB
Common Mode Rejection Ratio	CMRR	1kHz, 100mVpk-pk		60		dB
Channel Separation		1kHz signal, -31dBV		85		dB
		10kHz signal, -31dBV		80		
Channel Level Matching		1kHz signal, -31dBV		+/-1		dB
PSRR (Referred to Input)	PSRR	217Hz, 100mVpk-pk		50		dB
		1kHz, 100mV pk-pk		50		

PGA and Microphone Boost					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Minimum PGA gain setting	L_MODE/R_MODE= 00b or 01b		-1.55		dB
	L_MODE/R_MODE= 10b		+12		
Maximum PGA gain setting	L_MODE/R_MODE= 00b or 01b		+28.28		dB
	L_MODE/R_MODE= 10b		+30		
Single-ended to differential conversion gain	L_MODE/R_MODE= 00b		+6		dB
PGA gain accuracy	L_MODE/R_MODE= 00b Gain -1.5 to +6.7dB	-1		+1	dB
	L_MODE/R_MODE= 00b Gain +7.5 to +28.3dB	-1.5		+1.5	
	L_MODE/R_MODE= 1X Gain +12 to +24dB	-1		+1	
	L_MODE/R_MODE= 1X Gain +27 to +30dB	-1.5		+1.5	
Mute attenuation	all modes of operation		100		dB
Equivalent input noise	L_MODE/R_MODE= 00b or 01b		30 214		µVrms nV/√Hz

OUTPUT SIGNAL PATH

High Performance Stereo Playback to Headphones - DAC input to HPOUTL+HPOUTR pins with 15Ω load

Test conditions:

HPOUTL_VOL = HPOUTR_VOL = 111001b (0dB)

Low Power Playback mode disabled. (See Table 49 for details; note that Low Power Playback mode is disabled by default.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Power (per Channel)	P_o	1% THD R_{Load}= 30Ω		28 0.92 -0.76		mW Vrms dBV
		1% THD R_{Load}= 15Ω		32 0.69 -3.19		mW Vrms dBV
DC Offset		DC servo enabled, calibration complete.	-1.5		+1.5	mV
Signal to Noise Ratio	SNR	A-weighted	90	96		dB
Total Harmonic Distortion + Noise	THD+N	R_L=30Ω; P_o=2mW		-91		dB
		R_L=30Ω; P_o=20mW		-84		
		R_L=15Ω; P_o=2mW		-87	-80	
		R_L=15Ω; P_o=20mW		-85		
Channel Separation		1kHz signal, 0dBFS		100		dB
		10kHz signal, 0dBFS		90		
Channel Level Matching		1kHz signal, 0dBFS		+/-1		dB
Power Supply Rejection Ratio	PSRR	217Hz, 100mVpk-pk		75		dB
		1kHz, 100mV pk-pk		70		

Low Power Stereo Playback to Headphones - DAC input to HPOUTL+HPOUTR pins with 15Ω load

Test conditions:

HPOUTL_VOL = HPOUTR_VOL = 111001b (0dB)

Low Power Playback Mode enabled (see Table 48 for details)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Power (per Channel)	P_o	1% THD R_{Load}= 30Ω		27 0.90 -0.92		mW Vrms dBV
		1% THD R_{Load}= 15Ω		30 0.67 -3.5		mW Vrms dBV
Signal to Noise Ratio	SNR	A-weighted		95		dB
Total Harmonic Distortion + Noise	THD+N	R_L=30Ω; P_o=2mW		-91		dB
		R_L=30Ω; P_o=20mW		-83		
		R_L=15Ω; P_o=2mW		-87		
		R_L=15Ω; P_o=20mW		-80		

High Performance Stereo Playback to Line-out - DAC input to LINEOUTL+LINEOUTR pins with 10kΩ / 50pF load **Test conditions:** LINEOUTL_VOL = LINEOUTR_VOL = 111001b (0dB) Low Power Playback mode disabled. (See Table 49 for details; note that Low Power Playback mode is disabled by default.)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Full Scale Output Signal Level		DAC 0dBFS output at 0dB volume		1.0 0 2.83		Vrms dBV Vpk-pk
DC offset		DC servo enabled. Calibration complete.	-1.5		+1.5	mV
Signal to Noise Ratio	SNR	A-weighted	90	96		dB
Total Harmonic Distortion + Noise	THD+N	10kΩ load		-85	-70	dB
Channel Separation		1kHz signal, 0dBFS		100		dB
		10kHz signal, 0dBFS		90		
Channel Level Matching		1kHz signal, 0dBFS		+/-1		dB
Power Supply Rejection Ratio	PSRR	217Hz, 100mVpk-pk		62		dB
		1kHz, 100mV pk-pk		62		

Low Power Stereo Playback to Line-out - DAC input to LINEOUTL+LINEOUTR pins with 10kΩ / 50pF load **Test conditions:** LINEOUTL_VOL = LINEOUTR_VOL = 111001b (0dB), Low Power Playback Mode enabled (see Table 48 for details)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Full Scale Output Signal Level		DAC 0dBFS output at 0dB volume		1.0 0 2.83		Vrms dBV Vpk-pk
Signal to Noise Ratio	SNR	A-weighted		95		dB
Total Harmonic Distortion + Noise	THD+N	10kΩ load		-82		dB

Output PGAs (HP, LINE)					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Minimum PGA gain setting			-57		dB
Maximum PGA gain setting			6		dB
PGA Gain Step Size			1		dB
PGA gain accuracy	+6dB to -40dB	-1.5		+1.5	dB
PGA gain accuracy	-40dB to -57dB	-1		+1	dB
Mute attenuation	HPOUTL/R		85		dB
	LINEOUTL/R		85		dB

BYPASS PATH

Differential Stereo Line Input to Stereo Line Output- IN2L-IN3L / IN2R-IN3R pins to LINEOUTL+LINEOUTR pins with 10kΩ / 50pF load

Test conditions:

L_MODE = R_MODE = 01b (Differential Line)

LIN_VOL = RIN_VOL = 00101b (0dB)

LINEOUTL_VOL = LINEOUTR_VOL = 111001b (0dB)

Total signal path gain = 0dB

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Full Scale Output Signal Level				1.0 0 2.83		Vrms dBV Vpk-pk
Signal to Noise Ratio	SNR	A-weighted	90	100		dBV
Total Harmonic Distortion + Noise	THD+N	-1dBV input		-92	-85	dBV
Channel Separation		1kHz signal, -1dBV		90		dB
		10kHz signal, -1dBV		80		
Channel Level Matching		1kHz signal, -1dBV		+/-1		dB
Power Supply Rejection Ratio	PSRR	217Hz, 100mV pk-pk		45		dB

CHARGE PUMP

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up Time			260		µs
CPCA	Normal mode		CPVDD		V
	Low power mode		CPVDD/2		V
CPCB	Normal mode		-CPVDD		V
	Low power mode		-CPVDD/2		V
External component requirements To achieve specified headphone output power and performance					
Flyback Capacitor (between CPCA and CPCB)	at 2V	1	2.2		µF
CPVOUTN Capacitor	at 2V	2	2.2		µF
CPVOUTP Capacitor	at 2V	2	2.2		µF

FLL

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Frequency	F_{REF}	FLL_CLK_REF_DIV = 00	0.032		13.5	MHz
		FLL_CLK_REF_DIV = 01	0.064		27	MHz
Lock time				2		ms
Free-running mode start-up time		VMID enabled		100		µs
Free-running mode frequency accuracy		Reference supplied initially		+/-10		%
		No reference provided		+/-30		%

OTHER PARAMETERS

VMID Reference					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Midrail Reference Voltage (VMIDC pin)		-3%	AVDD/2	+3%	V
Charge up time (from fully discharged to 10% below VMID)	External capacitor 4.7µF		890		µs

Microphone Bias (for analogue electret condenser microphones)

Additional test conditions: MICBIAS_ENA=1, all parameters measured at the MICBIAS pin

PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Bias Voltage. Note: 7/6 and 9/10 are available only if MICVDD > AVDD. Note: 3/2 and 4/3 are available only if MICVDD ≥ 2.5V.	$V_{MICBIAS}$	MICVDD = 2.5V 3mA load current, MICBIAS_SEL = 1xx	-10%	3/2 x AVDD	+10%	V
		MICBIAS_SEL = 011	-10%	4/3 x AVDD	+10%	
		MICBIAS_SEL = 010	-10%	7/6 x AVDD	+10%	
		MICBIAS_SEL = 001	-10%	10/9 x AVDD	+10%	
		MICBIAS_SEL = 000	-10%	9/10 ×AVDD	+10%	
Drop out voltage between MICVDD and MICBIAS				200		mV
Maximum source current	$I_{MICBIAS}$			4		mA
Noise spectral density		At 1kHz		19		nV/√Hz
Power Supply Rejection Ratio MICVDD to MICBIAS	PSRR	1kHz, 100mV pk-pk MICVDD = 1.71 V		67		dB
		20kHz, 100mV pk-pk MICVDD = 1.71 V		76		
		1kHz, 100mV pk-pk MICVDD = 2.5 V		88		
		20kHz, 100mV pk-pk MICVDD = 2.5 V		84		
		1kHz, 100mV pk-pk MICVDD = 3.6 V		61		
		20kHz, 100mV pk-pk MICVDD = 3.6 V		70		
Power Supply Rejection Ratio MICVDD and AVDD to MICBIAS	PSRR	1kHz, 100mV pk-pk AVDD = MICVDD = 1.8 V		54		dB
		20kHz, 100mV pk-pk AVDD = MICVDD = 1.8 V		79		
MICBIAS Current Detect Function (See Note 1)						
Current Detect Threshold (Microphone insertion)		MICDET_THR = 00			80	µA
Current Detect Threshold (Microphone removal)			60			
Delay Time for Current Detect Interrupt	t_{DET}			3.2		ms
MICBIAS Short Circuit (Hook Switch) Detect Function (See Note 1)						
Short Circuit Detect Threshold (Button press)		MICSHORT_THR = 00			600	µA
Short Circuit Detect Threshold (Button release)			400			
Minimum Delay Time for Short Circuit Detect Interrupt	t_{SHORT}			47		ms

Note 1 : If AVDD ≠ 1.8, current threshold values should be multiplied by (AVDD/1.8)

Digital Inputs / Outputs						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Input HIGH Level (Digital Input)	V_{IH}		0.7×DBVDD			V
Input LOW Level (Digital Input)	V_{IL}				0.3×DBVDD	V
Input HIGH Level (Analogue / Digital Input)	V_{IH}		0.7×AVDD			V
Input LOW Level (Analogue / Digital Input)	V_{IL}				0.3×AVDD	V
Output HIGH Level	V_{OH}	I_{OH} = +1mA	0.9×DBVDD			V
Output LOW Level	V_{OL}	I_{OL} = -1mA			0.1×DBVDD	V

Multi-Path Crosstalk
Test Conditions:
Input Path = IN1L/IN1R to ADC, 0dB gain
Output Path = DAC to HPOUTL/HPOUTR, 0dB gain
Fs = 48kHz

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to ADC Crosstalk		1kHz signal, 0dBFS		-45		dB
ADC to DAC Crosstalk		1kHz signal, -7dBV		-60		dB

POWER CONSUMPTION

The WM8904 power consumption is dependent on many parameters. Most significantly, it depends on supply voltages, sample rates, mode of operation, and output loading.

The power consumption on each supply rail varies approximately with the square of the voltage. Power consumption is greater at fast sample rates than at slower ones. When the digital audio interface is operating in Master mode, the DBVDD current is significantly greater than in Slave mode. (Note also that power savings can be made by using MCLK as the BCLK source in Slave mode.) The output load conditions (impedance, capacitance and inductance) can also impact significantly on the device power consumption.

COMMON TEST CONDITIONS

Unless otherwise stated, the following test conditions apply throughout the following sections:

- Ambient temperature = +25°C
- Audio signal = quiescent (zero amplitude)
- Sample rate = 48kHz
- MCLK = 12.288MHz
- Audio interface mode = Slave (LRCLK_DIR=0, BCLK_DIR=0)
- SYSCLK_SRC = 0 (system clock comes direct from MCLK, not from FLL)

Additional, variant test conditions are quoted within the relevant sections below. Where applicable, power dissipated in the headphone or line loads is included.

POWER CONSUMPTION MEASUREMENTS

Single-ended Stereo Line Record - IN1L/R, IN2L/R or IN3L/R pins to ADC output.

Test conditions:

L_MODE = R_MODE = 00b (Single ended)

LIN_VOL = RIN_VOL = 00101 = +0.0 dB

ADC_OSR128 = 0 (64*fs), ADC_128_OSR_TST_MODE = 1, ADC_BIASx1P5 = 1

MICBIAS = disabled

Variant test conditions	AVDD		DCVDD		DBVDD		CPVDD		MICVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	V	mA	mW
48kHz sample rate	1.80	4.38	1.00	0.80	1.80	0.02	1.80	0.01	1.80	0.01	8.72
8kHz sample rate	1.80	4.25	1.00	0.14	1.80	0.00	1.80	0.01	1.80	0.01	7.81
48kHz -6dBV sine wave	1.80	4.41	1.00	0.80	1.80	0.03	1.80	0.01	1.80	0.01	8.81

Differential Stereo Record from Analogue Microphones - IN1L/R, IN2L/R or IN3L/R pins to ADC out.

Test conditions:

L_MODE = R_MODE = 10b (Differential mic)

LIN_VOL = RIN_VOL = 00111 = +30.0 dB

ADC_OSR128 = 0 (64*fs), ADC_128_OSR_TST_MODE = 1, ADC_BIASx1P5 = 1

MICBIAS_ENA = 1, MICBIAS_SEL = 000, No load connected to MICBIAS

Variant test conditions	AVDD		DCVDD		DBVDD		CPVDD		MICVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	V	mA	mW
48kHz sample rate	1.80	4.38	1.00	0.80	1.80	0.02	1.80	0.01	1.80	0.01	8.73
8kHz sample rate	1.80	4.25	1.00	0.14	1.80	0.00	1.80	0.01	1.80	0.01	7.81
48kHz -30dBV sine wave	1.80	4.39	1.00	0.81	1.80	0.03	1.80	0.01	1.80	0.01	8.78

High Performance Stereo Playback to Headphones - DAC input to HPOUTL+HPOUTR pins with 30Ω load.

Test conditions:

VMID_RES = 01 (for normal operation)

CP_DYN_PWR = 1 (Class-W, Charge pump controlled by real-time audio level)

Low Power Playback mode disabled. (See Table 49 for details; note that Low Power Playback mode is disabled by default.)

Variant test conditions	AVDD		DCVDD		DBVDD		CPVDD		MICVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	V	mA	mW
48kHz sample rate	1.80	1.69	1.00	0.76	1.80	0.00	1.80	0.31	2.50	0.01	4.38
8kHz sample rate	1.80	1.69	1.00	0.18	1.80	0.00	1.80	0.31	2.50	0.01	3.80
48kHz, Po = 0.1mW/channel 1kHz sine wave 0dBFS HPOUT_VOL= -25dB DAC_VOL= 0dB	1.80	1.71	1.00	0.77	1.80	0.00	1.80	1.99	2.50	0.01	7.45
48kHz, Po = 1mW/channel 1kHz sine wave 0dBFS HPOUT_VOL= -15dB DAC_VOL= 0dB	1.80	1.73	1.00	0.77	1.80	0.00	1.80	5.61	2.50	0.01	13.99
48kHz sample rate, Master mode, FLL enabled, MCLK input frequency = 13MHz	1.80	1.82	1.00	1.05	1.80	0.73	1.80	0.30	2.50	0.01	6.18
48kHz sample rate, Master mode, FLL enabled, MCLK input frequency = 32.768kHz	1.80	1.83	1.00	0.94	1.80	0.76	1.80	0.29	2.50	0.01	6.14

Low Power Stereo Playback to Headphones - DAC input to HPOUTL+HPOUTR pins with 30Ω load.

Test conditions:

VMID_RES = 01 (for normal operation)

CP_DYN_PWR = 1 (Class-W, Charge pump controlled by real-time audio level)

Low Power Playback Mode enabled (See Table 48 for details)

SYSCLK = 6.144MHz, CLK_SYS_RATE = 0001b (for 128 fs clocking)

Variant test conditions	AVDD		DCVDD		DBVDD		CPVDD		MICVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	V	mA	mW
48kHz sample rate	1.80	0.99	1.00	0.61	1.80	0.00	1.80	0.31	2.50	0.01	2.98
48kHz, Po = 0.1mW/channel 1kHz sine wave 0dBFS HPOUT_VOL= -25dB DAC_VOL= 0dB	1.80	1.02	1.00	0.62	1.80	0.00	1.80	1.68	2.50	0.01	5.51
48kHz, Po = 1mW/channel 1kHz sine wave 0dBFS HPOUT_VOL= -15dB DAC_VOL= 0dB	1.80	1.04	1.00	0.62	1.80	0.00	1.80	5.23	2.50	0.01	11.93

High Performance Stereo Playback to Line-out - DAC input to LINEOUTL+LINEOUTR or HPOUTL+HPOUTR pins with 10kΩ / 50pF load

Test conditions:

VMID_RES = 01 (for normal operation)

CP_DYN_PWR = 1 (Class-W, Charge pump controlled by real-time audio level)

Low Power Playback mode disabled. (See Table 49 for details; note that Low Power Playback mode is disabled by default.)

Variant test conditions	AVDD		DCVDD		DBVDD		CPVDD		MICVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	V	mA	mW
48kHz sample rate	1.80	1.67	1.00	0.76	1.80	0.00	1.80	0.36	2.50	0.01	4.43
8kHz sample rate	1.80	1.67	1.00	0.18	1.80	0.00	1.80	0.36	2.50	0.01	3.86
48kHz, Po = 0dBFS 1kHz sine wave	1.80	1.78	1.00	0.77	1.80	0.00	1.80	2.27	2.50	0.01	8.09

Low Power Stereo Playback to Line-out - DAC input to LINEOUTL+LINEOUTR or HPOUTL+HPOUTR pins with 10kΩ / 50pF load

Test conditions:

VMID_RES = 01 (for normal operation)

CP_DYN_PWR = 1 (Class-W, Charge pump controlled by real-time audio level)

Low Power Playback Mode enabled (see Table 48 for details)

SYSCLK = 6.144MHz, CLK_SYS_RATE = 0001b (for 128 fs clocking)

Variant test conditions	AVDD		DCVDD		DBVDD		CPVDD		MICVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	V	mA	mW
48kHz sample rate	1.80	0.99	1.00	0.61	1.80	0.00	1.80	0.22	2.50	0.01	2.81
48kHz, Po = 0dBFS 1kHz sine wave	1.80	1.04	1.00	0.62	1.80	0.00	1.80	1.77	2.50	0.01	5.70

Stereo analogue bypass to headphones - IN1L/R, IN2L/R or IN3L/R pins to HPOUTL+HPOUTR pins with 30Ω load.

Test conditions:

LIN_VOL = RIN_VOL = 00101 = +0.0 dB

MCLK = 11.2896MHz

Digital audio interface disabled

Note that the Analogue bypass configuration does not benefit from the Class W dynamic control.

Variant test conditions	AVDD		DCVDD		DBVDD		CPVDD		MICVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	V	mA	mW
Quiescent HPOUTVOL = 000000 (-57dB)	1.8	1.24	1	0.11	1.8	0.00	1.8	0.26	2.5	0.01	2.82
Po = 0.1mW/channel 1kHz sine wave HPOUTVOL = 100000 (-25dB)	1.8	1.29	1	0.11	1.8	0.00	1.8	2.05	2.5	0.01	6.13
Po = 1mW/channel 1kHz sine wave HPOUTVOL = 101010 (-15dB)	1.8	1.30	1	0.11	1.8	0.00	1.8	5.86	2.5	0.01	13.02

Stereo analogue bypass to Line-out - IN1L/R, IN2L/R or IN3L/R pins to LINEOUTL+LINEOUTR pins with 30Ω load.

Test conditions:

LIN_VOL = RIN_VOL = 00101 = +0.0 dB

MCLK = 11.2896MHz

Digital audio interface disabled

Note that the Analogue bypass configuration does not benefit from the Class W dynamic control.

Variant test conditions	AVDD		DCVDD		DBVDD		CPVDD		MICVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	V	mA	mW
Quiescent LINEOUTVOL = 000000 (-57dB)	1.8	1.04	1.0	0.15	1.8	0.00	1.8	0.21	1.8	0.01	2.41
Quiescent LINEOUTVOL = 101011 (-14dB)	1.8	1.04	1.0	0.15	1.8	0.00	1.8	0.63	1.8	0.01	3.18
Quiescent LINEOUTVOL = 111001 (0dB)	1.8	1.04	1.0	0.15	1.8	0.00	1.8	1.25	1.8	0.01	4.28

Off

Note: DC servo calibration is retained in this state as long as DCVDD is supplied. This allows fast, pop suppressed start-up from the off state.

Variant test conditions	AVDD		DCVDD		DBVDD		CPVDD		MICVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	V	mA	mW
Off (default settings) No Clocks applied	1.8	0.01	1	0.00	1.8	0.00	1.8	0.01	2.5	0.01	0.04
Off (default settings) DACDAT, MCLK, BCLK, and LRCLK applied	1.8	0.01	1	0.02	1.8	0.00	1.8	0.01	2.5	0.01	0.06

SIGNAL TIMING REQUIREMENTS

COMMON TEST CONDITIONS

Unless otherwise stated, the following test conditions apply throughout the following sections:

- Ambient temperature = +25°C
- DCVDD = 1.0V
- DBVDD = AVDD = CPVDD = 1.8V
- DGND = AGND = CPGND = 0V

Additional, specific test conditions are given within the relevant sections below.

MASTER CLOCK

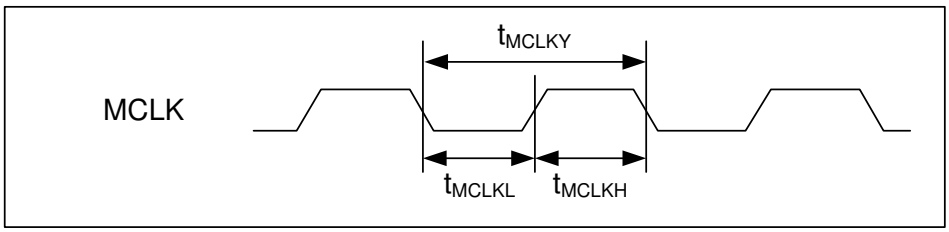


Figure 1 Master Clock Timing

Master Clock Timing						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
MCLK cycle time	T_{MCLKY}	MCLK_DIV=1	40			ns
		MCLK_DIV=0	80			ns
MCLK duty cycle	T_{MCLKDS}		60:40		40:60	