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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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WM8912

Ultra Low Power DAC with Headphone Driver for Portable Audio Applications

DESCRIPTION

The WM8912 is a high performance ultra-low power stereo DAC optimised for portable audio applications.

The device features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques - incorporating an innovative dual-mode charge pump architecture - to optimise efficiency and power consumption during playback. The ground-referenced outputs eliminate headphone coupling capacitors. The outputs include common mode feedback paths to reject ground noise.

Control sequences for audio path setup can be pre-loaded and executed by an integrated control write sequencer to reduce software driver development and minimise pops and clicks via Wolfson's SilentSwitch™ technology.

A dynamic range controller provides compression and level control to support a wide range of portable recording applications. Anti-clip and quick release features offer good performance in the presence of loud impulsive noises. ReTune™ Mobile 5-band parametric equaliser with fully programmable coefficients is integrated for optimization of speaker characteristics.

Common audio sampling frequencies are supported from a wide range of external clocks, either directly or generated using the integrated FLL.

The WM8912 can operate directly from a single 1.8V switched supply. For optimal power consumption, the digital core can be operated from a 1.0V supply.

FEATURES

- 3.8mW quiescent power consumption for DAC to headphone playback
- DAC SNR 96dB typical, THD -86dB typical
- Class W ground-referenced headphone driver
  - 28mW per channel into 30Ω at <1% THD
  - 32mW per channel into 15Ω at <1% THD
- Dynamic range controller
- ReTune™ Mobile parametric equalizer
- Integrated control write sequencer for pop minimised start-up and shutdown
- Single register write for default start-up and shutdown sequences
- On-chip FLL provides all necessary clocks
- DAC supports standard sample rates from 8kHz to 96kHz
- 32-pin QFN package (4x4mm, 0.4mm pitch)

APPLICATIONS

- Portable multimedia players
- Multimedia handsets
- Handheld gaming

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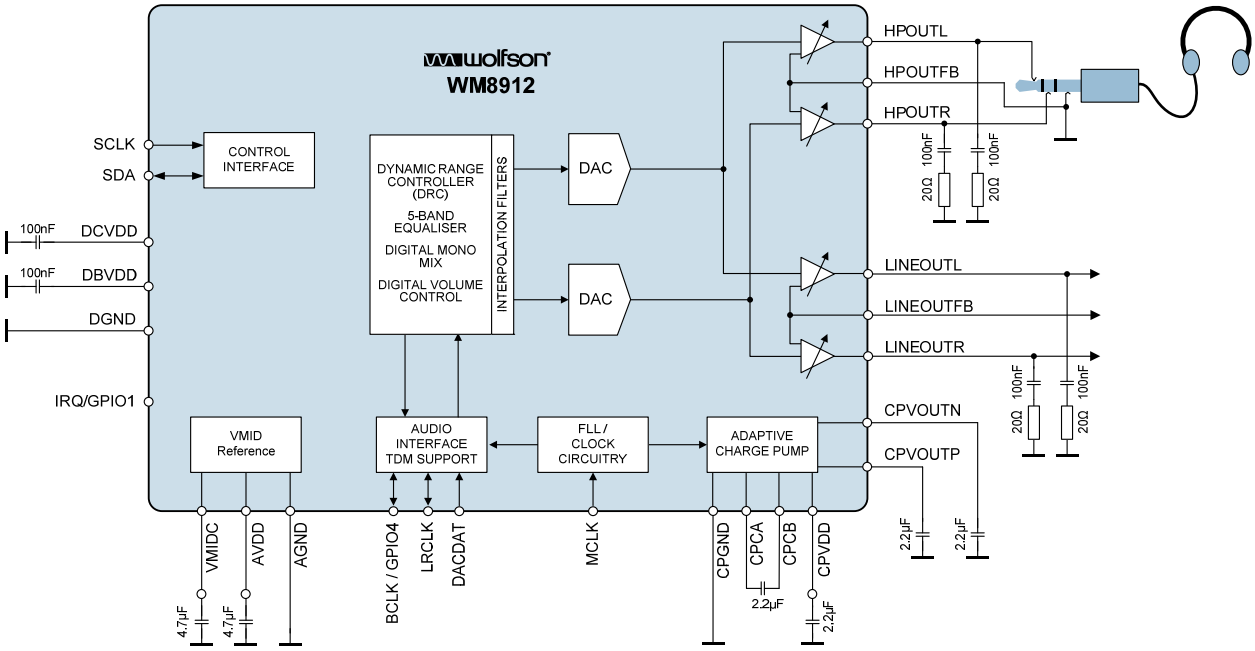
BLOCK DIAGRAM



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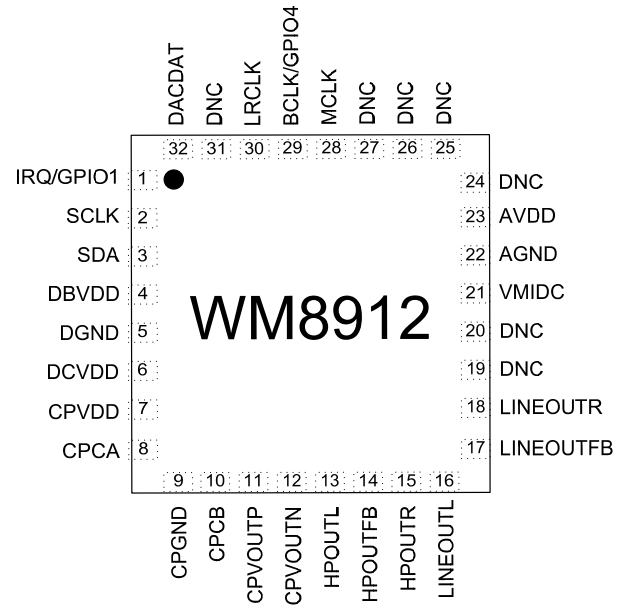
PIN CONFIGURATION

The WM8912 is supplied in a 32-pin QFN package.



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8912CGEFL/V	-40°C to +85°C	32-lead QFN (4x4x0.4mm, lead-free)	MSL3	260°C
WM8912CGEFL/RV	-40°C to +85°C	32-lead QFN (4x4x0.4mm, lead-free, tape and reel)	MSL3	260°C

Note:

Reel quantity = 3,500

PIN DESCRIPTION

NAME	QFN-32	TYPE	DESCRIPTION
IRQ/GPIO1	1	Digital Input / Output	GPIO1 / Interrupt
SCLK	2	Digital Input	Control interface clock input
SDA	3	Digital Input / Output	Control interface data input / output
DBVDD	4	Supply	Digital buffer supply (powers audio interface and control interface)
DGND	5	Supply	Digital ground (return path for DCVDD and DBVDD)
DCVDD	6	Supply	Digital core supply
CPVDD	7	Supply	Charge pump power supply
CPCA	8	Analogue Input	Charge pump flyback capacitor pin
CPGND	9	Supply	Charge pump ground
CPCB	10	Analogue Input	Charge pump flyback capacitor pin
CPVOUTP	11	Analogue Output	Charge pump positive supply decoupling (powers HPOUTL/R, LINEOUTL/R)
CPVOUTN	12	Analogue Output	Charge pump negative supply decoupling (powers HPOUTL/R, LINEOUTL/R)
HPOUTL	13	Analogue Output	Left headphone output (line or headphone output)
HPOUTFB	14	Analogue Output	Headphone output ground loop noise rejection feedback
HPOUTR	15	Analogue Output	Right headphone output (line or headphone output)
LINEOUTL	16	Analogue Output	Left line output 1 (line output)
LINEOUTFB	17	Analogue Output	Line output ground loop noise rejection feedback
LINEOUTR	18	Analogue Output	Right line output 1 (line output)
DNC	19	n/a	Do Not Connect
DNC	20	n/a	Do Not Connect
VMIDC	21	Analogue Output	Midrail voltage decoupling capacitor
AGND	22	Supply	Analogue power return
AVDD	23	Supply	Analogue power supply
DNC	24	n/a	Do Not Connect
DNC	25	n/a	Do Not Connect
DNC	26	n/a	Do Not Connect
DNC	27	n/a	Do Not Connect
MCLK	28	Digital Input	Master clock for DAC
BCLK/GPIO4	29	Digital Input / Output	Audio interface bit clock / GPIO4
LRCLK	30	Digital Input / Output	Audio interface left / right clock
DNC	31	n/a	Do Not Connect
DACDAT	32	Digital Input	DAC digital audio data
GND_PADDLE	33		Die Paddle

Note:

It is recommended that the QFN ground paddle is connected to analogue ground on the application PCB.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
AVDD, DCVDD	-0.3V	+2.5V
DBVDD,	-0.3V	+4.5V
CPVDD	-0.3V	+2.2V
HPOUTL, HPOUTR, LINEOUTL, LINEOUTR	(CPVDD + 0.3V) * -1	CPVDD + 0.3V
Voltage range digital inputs	DGND -0.3V	DBVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Temperature range, T_A	-40°C	+85°C
Storage temperature after soldering	-65°C	+150°C

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other; there is no restriction on power supply sequencing.
3. HPOUTL, HPOUTR, LINEOUTL, LINEOUTR are outputs, and should not normally become connected to DC levels. However, if the limits above are exceeded, then damage to the WM8912 may occur.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD	0.95	1.0	1.98	V
Digital supply range (Buffer)	DBVDD	1.42	1.8	3.6	V
Analogue supplies range	AVDD	1.71	1.8	2.0	V
Charge pump supply range	CPVDD	1.71	1.8	2.0	V
Ground	DGND, AGND, CPGND		0		V
Operating Temperature (ambient)	T_A	-40	+25	+85	°C

ELECTRICAL CHARACTERISTICS

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is the difference in level between a full scale output signal and the device output noise with no signal applied, measured over a bandwidth of 20Hz to 20kHz. This ratio is also called idle channel noise. (No Auto-zero or Automute function is employed).
2. Total Harmonic Distortion (dB) – THD is the difference in level between a 1kHz full scale sinewave output signal and the first seven harmonics of the output signal. The amplitude of the fundamental frequency of the output signal is compared to the RMS value of the next seven harmonics and expressed as a ratio.
3. Total Harmonic Distortion + Noise (dB) – THD+N is the difference in level between a 1kHz full scale sine wave output signal and all noise and distortion products in the audio band. The amplitude of the fundamental reference frequency of the output signal is compared to the RMS value of all other noise and distortion products and expressed as a ratio.
4. Channel Separation (dB) – is a measure of the coupling between left and right channels. A full scale signal is applied to the left channel only, the right channel amplitude is measured. Then a full scale signal is applied to the right channel only and the left channel amplitude is measured. The worst case channel separation is quoted as a ratio.
5. Channel Level Matching (dB) – measures the difference in gain between the left and the right channels.
6. Power Supply Rejection Ratio (dB) – PSRR is a measure of ripple attenuation between the power supply pin and an output path. With the signal path idle, a small signal sine wave is summed onto the power supply rail, The amplitude of the sine wave is measured at the output port and expressed as a ratio.
7. All performance measurements carried out with 20kHz AES17 low pass filter for distortion measurements, and an A-weighted filter for noise measurement. Failure to use such a filter will result in higher THD and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.

COMMON TEST CONDITIONS

Unless otherwise stated, the following test conditions apply throughout the following sections:

- DCVDD = 1.0V
- DBVDD = 1.8V
- AVDD = CPVDD =1.8V
- Ambient temperature = +25°C
- Audio signal: 1kHz sine wave, sampled at 48kHz with 24-bit data resolution
- SYSCLK_SRC = 0 (system clock comes direct from MCLK, not from FLL).

Additional, specific test conditions are given within the relevant sections below.

OUTPUT SIGNAL PATH

Stereo Playback to Headphones - DAC input to HPOUTL+HPOUTR pins with 15Ω load
Test conditions: HPOUTL_VOL = HPOUTR_VOL = 111001b (0dB)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Power (per Channel)	P_o	1% THD R_{Load}= 30Ω		28 0.92 -0.76		mW Vrms dBV
		1% THD R_{Load}= 15Ω		32 0.69 -3.19		mW Vrms dBV
DC Offset		DC servo enabled, calibration complete.	-1.5		+1.5	mV
Signal to Noise Ratio	SNR	A-weighted	90	96		dB
Total Harmonic Distortion + Noise	THD+N	R_L=30Ω; P_o=2mW		-91		dB
		R_L=30Ω; P_o=20mW		-84		
		R_L=15Ω; P_o=2mW		-87	-80	
		R_L=15Ω; P_o=20mW		-85		
Channel Separation		1kHz signal, 0dBFS		100		dB
		10kHz signal, 0dBFS		90		
Channel Level Matching		1kHz signal, 0dBFS		+/-1		dB
Power Supply Rejection Ratio	PSRR	217Hz, 100mVpk-pk		75		dB
		1kHz, 100mV pk-pk		70		

Stereo Playback to Line-out - DAC input to LINEOUTL+LINEOUTR pins with 10kΩ / 50pF load
Test conditions: LINEOUTL_VOL = LINEOUTR_VOL = 111001b (0dB)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Full Scale Output Signal Level		DAC 0dBFS output at 0dB volume		1.0 0 2.83		Vrms dBV Vpk-pk
DC offset		DC servo enabled. Calibration complete.	-1.5		+1.5	mV
Signal to Noise Ratio	SNR	A-weighted	90	96		dB
Total Harmonic Distortion + Noise	THD+N	10kΩ load		-85	-70	dB
Channel Separation		1kHz signal, 0dBFS		100		dB
		10kHz signal, 0dBFS		90		
Channel Level Matching		1kHz signal, 0dBFS		+/-1		dB
Power Supply Rejection Ratio	PSRR	217Hz, 100mVpk-pk		62		dB
		1kHz, 100mV pk-pk		62		

Output PGAs (HP, LINE)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Minimum PGA gain setting			-57		dB
Maximum PGA gain setting			6		dB
PGA Gain Step Size			1		dB
PGA gain accuracy	+6dB to -40dB	-1.5		+1.5	dB
PGA gain accuracy	-40dB to -57dB	-1		+1	dB
Mute attenuation	HPOUTL/R		85		dB
	LINEOUTL/R		85		dB

CHARGE PUMP

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up Time			260		µs
CPCA	Normal mode		CPVDD		V
	Low power mode		CPVDD/2		V
CPCB	Normal mode		-CPVDD		V
	Low power mode		-CPVDD/2		V
External component requirements To achieve specified headphone output power and performance					
Flyback Capacitor (between CPCA and CPCB)	at 2V	1	2.2		µF
CPVOUTN Capacitor	at 2V	2	2.2		µF
CPVOUTP Capacitor	at 2V	2	2.2		µF

FLL

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Frequency	F_{REF}	FLL_CLK_REF_DIV = 00	0.032		13.5	MHz
		FLL_CLK_REF_DIV = 01	0.064		27	MHz
Lock time				2		ms
Free-running mode start-up time		VMID enabled		100		µs
Free-running mode frequency accuracy		Reference supplied initially		+/-10		%
		No reference provided		+/-30		%

OTHER PARAMETERS

VMID Reference					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Midrail Reference Voltage (VMID pin)		-3%	AVDD/2	+3%	V
Charge up time (from fully discharged to +5% or -10% of VMID)	External capacitor 4.7µF		890		µs

Digital Inputs / Outputs						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Input HIGH Level	V_{IH}		0.7×DBVDD			V
Input LOW Level	V_{IL}				0.3×DBVDD	V
Output HIGH Level	V_{OH}	I_{OH} = +1mA	0.9×DBVDD			V
Output LOW Level	V_{OL}	I_{OL} = -1mA			0.1×DBVDD	V

POWER CONSUMPTION

The WM8912 power consumption is dependent on many parameters. Most significantly, it depends on supply voltages, sample rates, mode of operation, and output loading.

The power consumption on each supply rail varies approximately with the square of the voltage. Power consumption is greater at fast sample rates than at slower ones. When the digital audio interface is operating in Master mode, the DBVDD current is significantly greater than in Slave mode. (Note also that power savings can be made by using MCLK as the BCLK source in Slave mode.) The output load conditions (impedance, capacitance and inductance) can also impact significantly on the device power consumption.

COMMON TEST CONDITIONS

Unless otherwise stated, the following test conditions apply throughout the following sections:

- Ambient temperature = +25°C
- Audio signal = quiescent (zero amplitude)
- Sample rate = 48kHz
- MCLK = 12.288MHz
- Audio interface mode = Slave (LRCLK_DIR=0, BCLK_DIR=0)
- SYSCLK_SRC = 0 (system clock comes direct from MCLK, not from FLL)

Additional, variant test conditions are quoted within the relevant sections below. Where applicable, power dissipated in the headphone or line loads is included.

POWER CONSUMPTION MEASUREMENTS

Stereo Playback to Headphones - DAC input to HPOUTL+HPOUTR pins with 30Ω load.

Test conditions:

VMID_RES = 01 (for normal operation)

CP_DYN_PWR = 1 (Class-W, Charge pump controlled by real-time audio level)

Variant test conditions	AVDD		DCVDD		DBVDD		CPVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	mW
48kHz sample rate	1.80	1.69	1.00	0.76	1.80	0.00	1.80	0.31	4.38
8kHz sample rate	1.80	1.69	1.00	0.18	1.80	0.00	1.80	0.31	3.80
48kHz, Po = 0.1mW/channel 1kHz sine wave 0dBFS HPOUT_VOL= -25dB DAC_VOL= 0dB	1.80	1.71	1.00	0.77	1.80	0.00	1.80	1.99	7.45
48kHz, Po = 1mW/channel 1kHz sine wave 0dBFS HPOUT_VOL= -15dB DAC_VOL= 0dB	1.80	1.73	1.00	0.77	1.80	0.00	1.80	5.61	13.99
48kHz sample rate, Master mode, FLL enabled, MCLK input frequency = 13MHz	1.80	1.82	1.00	1.05	1.80	0.73	1.80	0.30	6.18
48kHz sample rate, Master mode, FLL enabled, MCLK input frequency = 32.768kHz	1.80	1.83	1.00	0.94	1.80	0.76	1.80	0.29	6.14

Stereo Playback to Line-out - DAC input to LINEOUTL+LINEOUTR or HPOUTL+HPOUTR pins with 10kΩ / 50pF load

Test conditions :

VMID_RES = 01 (for normal operation)

CP_DYN_PWR = 1 (Class-W, Charge pump controlled by real-time audio level)

Variant test conditions	AVDD		DCVDD		DBVDD		CPVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	mW
48kHz sample rate	1.8	1.67	1	0.76	1.8	0.00	1.8	0.36	4.43
8kHz sample rate	1.8	1.67	1	0.18	1.8	0.00	1.8	0.36	3.86
48kHz, Po = 0dBFS 1kHz sine wave	1.8	1.78	1	0.77	1.8	0.00	1.8	2.27	8.09

Off

Note: DC servo calibration is retained in this state as long as DCVDD is supplied. This allows fast, pop suppressed start-up from the off state.

Variant test conditions	AVDD		DCVDD		DBVDD		CPVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	mW
Off (default settings) No Clocks applied	1.8	0.01	1	0.00	1.8	0.00	1.8	0.01	0.04
Off (default settings) DACDAT, MCLK, BCLK, and LRCLK applied	1.8	0.01	1	0.02	1.8	0.00	1.8	0.01	0.06

SIGNAL TIMING REQUIREMENTS

COMMON TEST CONDITIONS

Unless otherwise stated, the following test conditions apply throughout the following sections:

- Ambient temperature = +25°C
- DCVDD = 1.0V
- DBVDD = AVDD = CPVDD = 1.8V
- DGND = AGND = CPGND = 0V

Additional, specific test conditions are given within the relevant sections below.

MASTER CLOCK

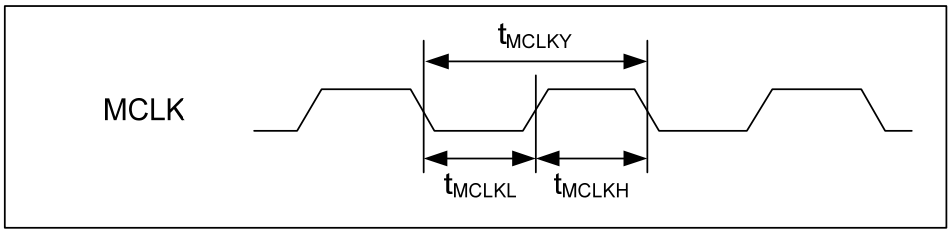


Figure 1 Master Clock Timing

Master Clock Timing						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
MCLK cycle time	T_{MCLKY}	MCLK_DIV=1	40			ns
		MCLK_DIV=0	80			ns
MCLK duty cycle	T_{MCLKDS}		60:40		40:60	

AUDIO INTERFACE TIMING

MASTER MODE

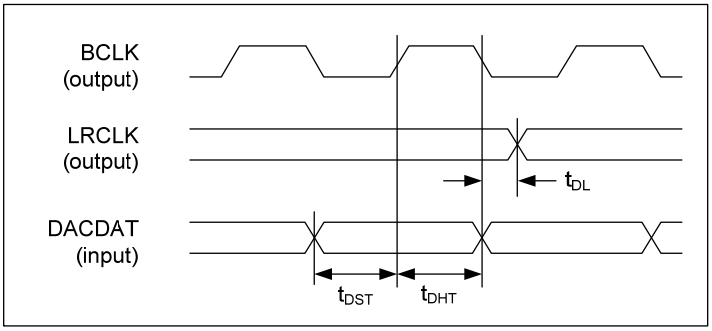


Figure 2 Audio Interface Timing – Master Mode

Test Conditions

DCVDD = 1.0V, AVDD = DBVDD = CPVDD = 1.8V, DGND=AGND=CPGND =0V, T_A = +25°C, Master Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Master Mode					
LRCLK propagation delay from BCLK falling edge	t_{DL}			20	ns
DACDAT setup time to BCLK rising edge	t_{DST}	20			ns
DACDAT hold time from BCLK rising edge	t_{DHT}	10			ns

SLAVE MODE

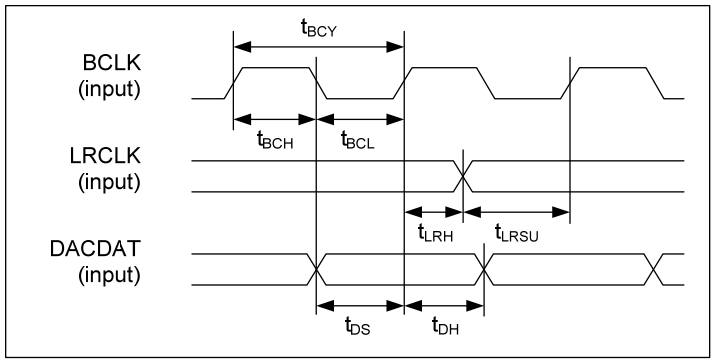


Figure 3 Audio Interface Timing – Slave Mode

Test Conditions

DCVDD = 1.0V, AVDD = DBVDD = CPVDD = 1.8V, DGND=AGND=CPGND =0V, T_A = +25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Slave Mode					
BCLK cycle time	t_{BCY}	50			ns
BCLK pulse width high	t_{BCH}	20			ns
BCLK pulse width low	t_{BCL}	20			ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}	20			ns
LRCLK hold time from BCLK rising edge	t_{LRH}	10			ns
DACDAT hold time from BCLK rising edge	t_{DH}	10			ns
DACDAT set-up time to BCLK rising edge	t_{DS}	20			ns

Note: BCLK period must always be greater than or equal to MCLK period.

CONTROL INTERFACE TIMING

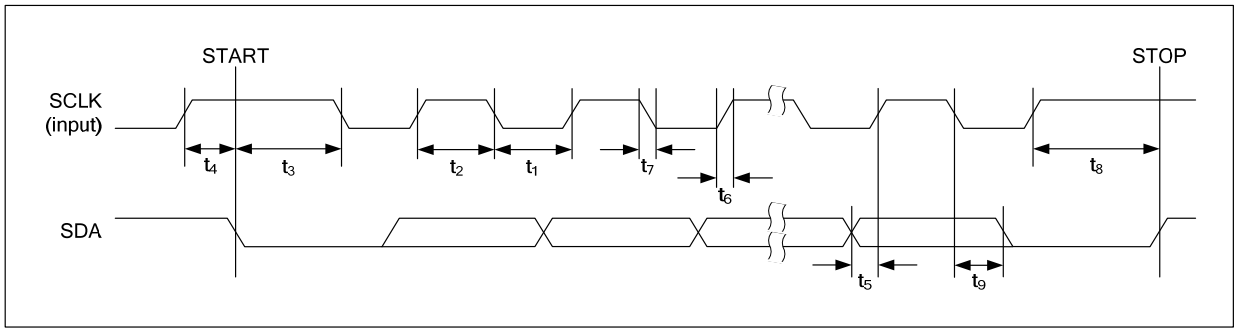


Figure 4 Control Interface Timing

Test Conditions

DCVDD = 1.0V, AVDD = DBVDD = CPVDD = 1.8V, DGND=AGND=CPGND =0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SCLK Frequency				400	kHz
SCLK Low Pulse-Width	t_1	1300			ns
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDA, SCLK Rise Time	t_6			300	ns
SDA, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC Normal Filter					
Passband	+/- 0.05dB	0		0.454 fs	
	-6dB		0.5 fs		
Passband Ripple	0.454 fs			+/- 0.03	dB
Stopband		0.546 fs			
Stopband Attenuation	F > 0.546 fs	-50			dB
DAC Sloping Stopband Filter					
Passband	+/- 0.03dB	0		0.25 fs	
	+/- 1dB	0.25 fs		0.454 fs	
	-6dB		0.5 fs		
Passband Ripple	0.25 fs			+/- 0.03	dB
Stopband 1		0.546 fs		0.7 fs	
Stopband 1 Attenuation	f > 0.546 fs	-60			dB
Stopband 2		0.7 fs		1.4 fs	
Stopband 2 Attenuation	f > 0.7 fs	-85			dB
Stopband 3		1.4 fs			
Stopband 3 Attenuation	F > 1.4 fs	-55			dB

DAC FILTERS	
Mode	**Group Delay**
Normal	16.5 / fs
Sloping Stopband	18 / fs

TERMINOLOGY

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region

DAC FILTER RESPONSES

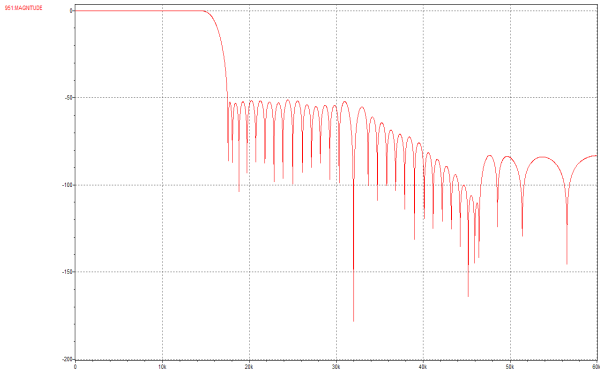


Figure 5 DAC Digital Filter Frequency Response; (Normal Mode); Sample Rate > 24kHz

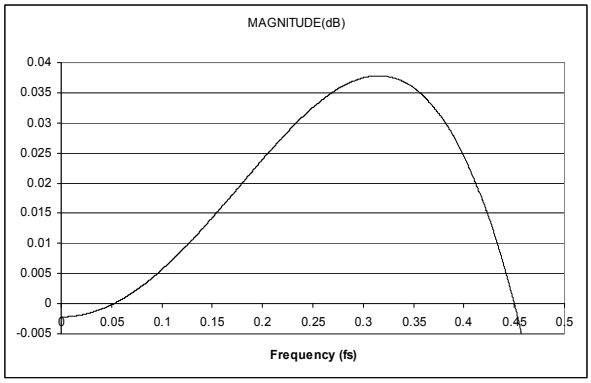


Figure 6 DAC Digital Filter Ripple (Normal Mode)

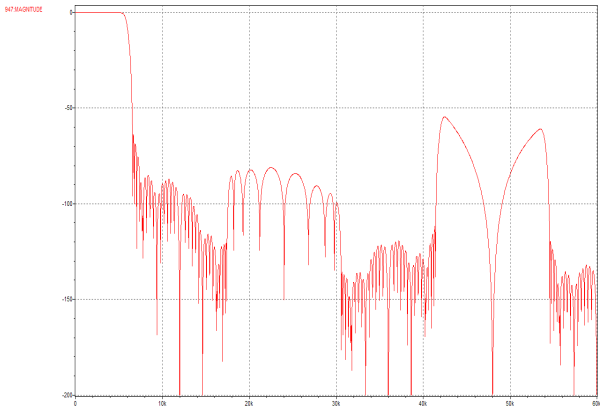


Figure 7 DAC Digital Filter Frequency Response; (Sloping Stopband Mode); Sample Rate <= 24kHz

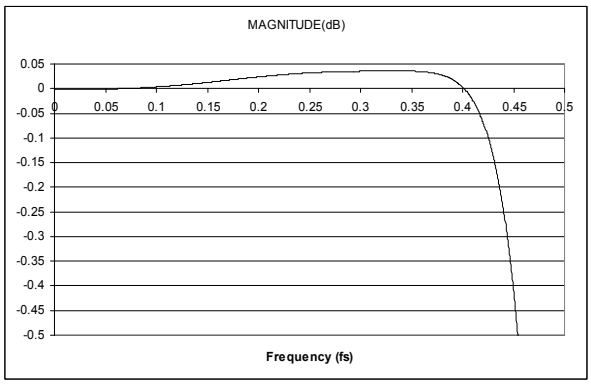


Figure 8 DAC Digital Filter Ripple (Sloping Stopband Mode)

DE-EMPHASIS FILTER RESPONSES

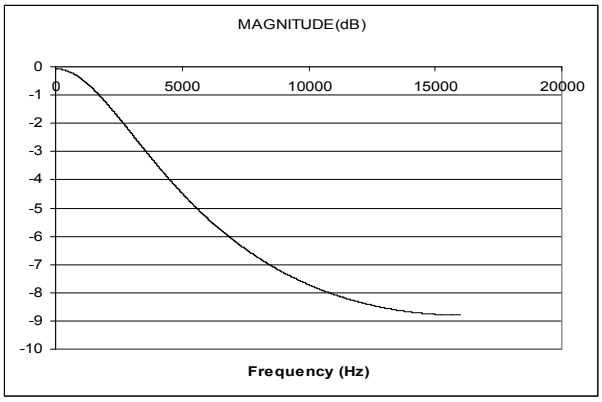


Figure 9 De-Emphasis Digital Filter Response (32kHz)

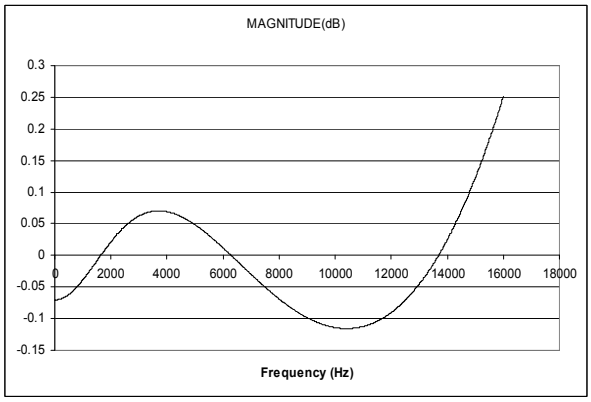


Figure 10 De-Emphasis Error (32kHz)

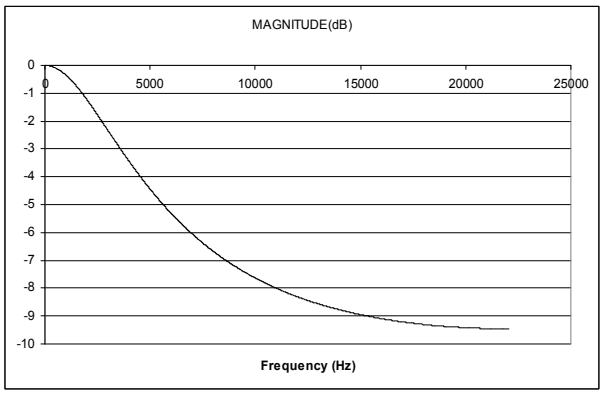


Figure 11 De-Emphasis Digital Filter Response (44.1kHz)

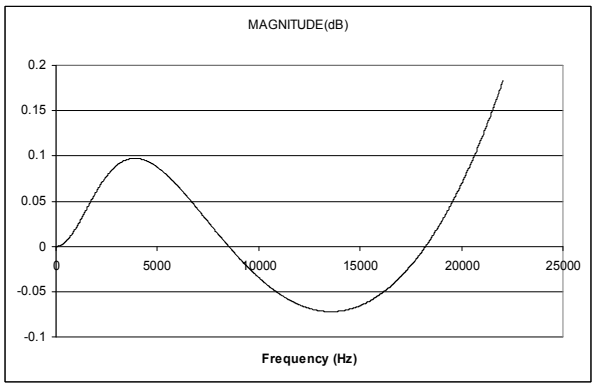


Figure 12 De-Emphasis Error (44.1kHz)

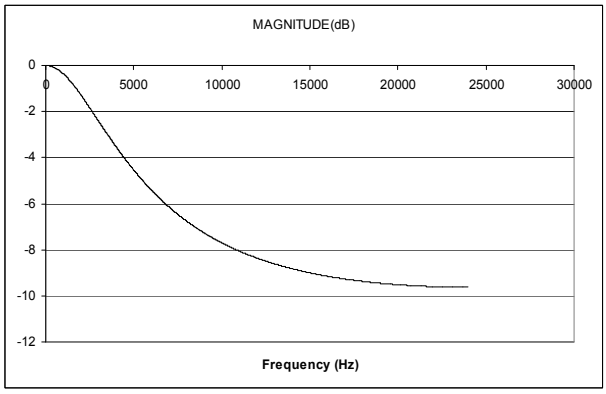


Figure 13 De-Emphasis Digital Filter Response (48kHz)

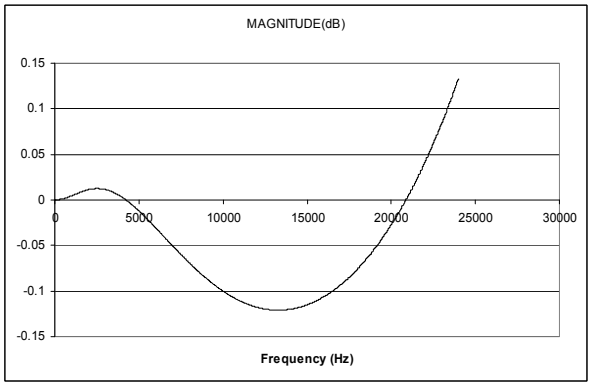


Figure 14 De-Emphasis Error (48kHz)

DEVICE DESCRIPTION

INTRODUCTION

The WM8912 is a high performance ultra-low power stereo DAC optimised for portable audio applications. Powerful digital signal processing (DSP) makes it ideal for small portable devices.

Two stereo pairs of ground-referenced Class-W outputs are provided, suitable for driving a stereo headphone and stereo line load simultaneously. The ground-referenced outputs are powered from an integrated Charge Pump, enabling high quality, power efficient outputs without requirement for DC blocking capacitors. A DC Servo circuit is available for DC offset correction, thereby suppressing pops and further reducing power consumption. Ground loop feedback is provided on the headphone outputs and on the line outputs, providing rejection of noise on the ground connections. All outputs use Wolfson SilentSwitch™ technology for pop and click suppression.

The stereo DACs are of hi-fi quality, using a 24-bit low-order oversampling architecture to deliver optimum performance. A flexible clocking arrangement supports all commonly used DAC sample rates, either directly from an external MCLK or with the use of the integrated Frequency Locked Loop (FLL) for additional flexibility. DAC soft mute and un-mute is available for pop-free music playback.

The integrated Dynamic Range Controller (DRC) and ReTune™ Mobile 5-band parametric equaliser (EQ) provide further processing capability of the digital audio paths. The DRC provides compression and signal level control to improve the handling of unpredictable signal levels. 'Anti-clip' and 'quick release' algorithms improve intelligibility in the presence of transients and impulsive noises. The EQ provides the capability to tailor the audio path according to the frequency characteristics of an earpiece or loudspeaker, and/or according to user preferences.

The WM8912 has a highly flexible digital audio interface, supporting a number of protocols, including I^2S, DSP, MSB-first left/right justified, and can operate in master or slave modes. PCM operation is supported in the DSP mode. A-law and μ-law companding are also supported. Time division multiplexing (TDM) is available to allow multiple devices to stream data simultaneously on the same bus, saving space and power.

The system clock (SYSCLK) provides clocking for the DACs, DSP core, digital audio interface and other circuits. SYSCLK can be derived directly from the MCLK pin or via the integrated FLL, providing flexibility to support a wide range of clocking schemes. Typical portable system MCLK frequencies and commonly used sample rates from 8kHz to 48kHz are all supported. The clocking circuits are configured automatically from the sample rate and from the MCLK / SYSCLK ratio.

The integrated FLL can be used to generate SYSCLK from a wide variety of different reference sources and frequencies. The FLL can accept a wide range of reference frequencies, which may be high frequency (e.g. 13MHz) or low frequency (eg. 32.768kHz). The FLL is tolerant of jitter and may be used to generate a stable SYSCLK from a less stable input signal. The integrated FLL can be used as a free-running oscillator, enabling autonomous clocking of the Headphone Charge Pump and DC Servo if required.

The WM8912 uses a standard 2-wire control interface, providing full software control of all features, together with device register readback. An integrated Control Write Sequencer enables automatic scheduling of control sequences; commonly-used signal configurations may be selected using ready-programmed sequences, including time-optimised control of the WM8912 pop suppression features. It is an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs. Unused circuitry can be disabled under software control, in order to save power; low leakage currents enable extended standby/off time in portable battery-powered applications.

Two GPIO pins may be configured for miscellaneous input/output functions such as button/accessory detect inputs, or for clock, system status, or programmable logic level output for control of additional external circuitry. Interrupt logic, status readback and de-bouncing options are supported within this functionality.

DYNAMIC RANGE CONTROL (DRC)

The dynamic range controller (DRC) is a circuit which can be enabled in the digital DAC playback path. The function of the DRC is to adjust the signal gain in conditions where the input amplitude is unknown or varies over a wide range, e.g. when recording from microphones built into a handheld system. The DRC can apply Compression and Automatic Level Control to the signal path. It incorporates 'anti-clip' and 'quick release' features for handling transients in order to improve intelligibility in the presence of loud impulsive noises.

The DRC is enabled in the digital DAC playback path by setting DRC_ENA and DRC_DAC_PATH, as shown in Table 1. Both bits must be set for DRC operation.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R40 (28h) DRC Control 0	15	DRC_ENA	0	DRC enable 0 = disabled 1 = enabled
	14	DRC_DAC_PATH	0	DRC path select 0 = Reserved 1 = DAC path

Table 1 DRC Enable

COMPRESSION/LIMITING CAPABILITIES

The DRC supports two different compression regions, separated by a "knee" at input amplitude T. For signals above the knee, the compression slope DRC_HI_COMP applies; for signals below the knee, the compression slope DRC_LO_COMP applies.

The overall DRC compression characteristic in "steady state" (i.e. where the input amplitude is near-constant) is illustrated in Figure 15.

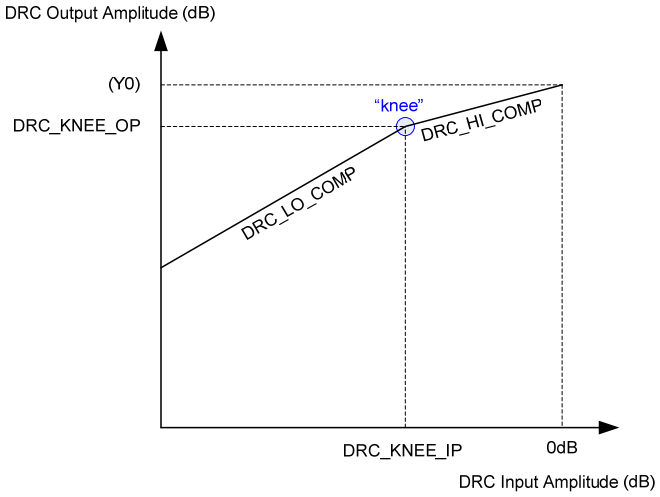


Figure 15 DRC Compression Characteristic

The slope of the DRC response is determined by register fields DRC_HI_COMP and DRC_LO_COMP respectively. A slope of 1 indicates constant gain in this region. A slope less than 1 represents compression (i.e. a change in input amplitude produces only a smaller change in output amplitude). A slope of 0 indicates that the target output amplitude is the same across a range of input amplitudes; this is infinite compression.

The “knee” in Figure 15 is determined by register fields DRC_KNEE_IP and DRC_KNEE_OP.

Parameter Y0, the output level for a 0dB input, is not specified directly, but can be calculated from the other parameters, using the equation.

$$Y0 = DRC\_KNEE\_OP - (DRC\_KNEE\_IP * DRC\_HI\_COMP)$$

The DRC Compression parameters are defined in Table 2.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R43 (2Bh) DRC Control 3	10:5	DRC_KNEE_IP [5:0]	00_0000	Input signal at the Compressor 'knee'. 000000 = 0dB 000001 = -0.75dB 000010 = -1.5dB … (-0.75dB steps) 111100 = -45dB 111101 to 111111 = Reserved
	4:0	DRC_KNEE_OP [4:0]	0_0000	Output signal at the Compressor 'knee'. 00000 = 0dB 00001 = -0.75dB 00010 = -1.5dB … (-0.75dB steps) 11110 = -22.5dB 11111 = Reserved
R42 (2Ah) DRC Control 2	5:3	DRC_HI_COMP [2:0]	000	Compressor slope (upper region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 0 110 to 111 = Reserved
	2:0	DRC_LO_COMP [2:0]	000	Compressor slope (lower region) 000 = 1 (no compression) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 0 101 to 111 = Reserved

Table 2 DRC Compression Control

GAIN LIMITS

The minimum and maximum gain applied by the DRC is set by register fields DRC_MINGAIN and DRC_MAXGAIN. These limits can be used to alter the DRC response from that illustrated in Figure 15. If the range between maximum and minimum gain is reduced, then the extent of the dynamic range control is reduced. The maximum gain prevents quiet signals (or silence) from being excessively amplified.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R41 (29h) DRC Control 1	3:2	DRC_MINGAIN [1:0]	10	Minimum gain the DRC can use to attenuate audio signals 00 = 0dB (default) 01 = -6dB 10 = -12dB 11 = -18dB
	1:0	DRC_MAXGAIN [1:0]	00	Maximum gain the DRC can use to boost audio signals 00 = 12dB 01 = 18dB (default) 10 = 24dB 11 = 36dB

Table 3 DRC Gain Limits

DYNAMIC CHARACTERISTICS

The dynamic behaviour determines how quickly the DRC responds to changing signal levels. Note that the DRC responds to the average (RMS) signal amplitude over a period of time.

DRC_ATK determines how quickly the DRC gain decreases when the signal amplitude is high. DRC_DCY determines how quickly the DRC gain increases when the signal amplitude is low.

These register fields are described in Table 4. Note that the register defaults are suitable for general purpose microphone use.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R41 (29h) DRC Control 1	15:12	DRC_ATK [3:0]	0011	Gain attack rate (seconds/6dB) 0000 = Reserved 0001 = 182µs 0010 = 363µs 0011 = 726µs (default) 0100 = 1.45ms 0101 = 2.9ms 0110 = 5.8ms 0111 = 11.6ms 1000 = 23.2ms 1001 = 46.4ms 1010 = 92.8ms 1011-1111 = Reserved

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	11:8	DRC_DCY [3:0]	0010	Gain decay rate (seconds/6dB) 0000 = 186ms 0001 = 372ms 0010 = 743ms (default) 0011 = 1.49s 0100 = 2.97s 0101 = 5.94s 0110 = 11.89s 0111 = 23.78s 1000 = 47.56s 1001-1111 = Reserved

Table 4 DRC Attack and Decay Rates

Note:

For detailed information about DRC attack and decay rates, please see Wolfson application note WAN0247.

ANTI-CLIP CONTROL

The DRC includes an Anti-Clip feature to avoid signal clipping when the input amplitude rises very quickly. This feature uses a feed-forward technique for early detection of a rising signal level. Signal clipping is avoided by dynamically increasing the gain attack rate when required. The Anti-Clip feature is enabled using the DRC_ANTICLIP bit.

Note that the feed-forward processing increases the latency in the input signal path. For low-latency applications (e.g. telephony), it may be desirable to reduce the delay, although this will also reduce the effectiveness of the anti-clip feature. The latency is determined by the DRC_FF_DELAY bit. If necessary, the latency can be minimised by disabling the anti-clip feature altogether.

The DRC Anti-Clip control bits are described in Table 5.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R40 (28h) DRC Control 0	5	DRC_FF_DELAY	1	Feed-forward delay for anti-clip feature 0 = 5 samples 1 = 9 samples Time delay can be calculated as $5/f_s$ or $9/f_s$, where f_s is the sample rate.
	1	DRC_ANTICLIP	1	Anti-clip enable 0 = disabled 1 = enabled

Table 5 DRC Anti-Clip Control

Note that the Anti-Clip feature operates entirely in the digital domain. It cannot be used to prevent signal clipping in the analogue domain nor in the source signal. Analogue clipping can only be prevented by reducing the analogue signal gain or by adjusting the source signal.