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WM8915

Ultra-Low Power Audio Hub CODEC

DESCRIPTION

The WM8915[1] is an ultra-low power mobile CODEC designed for music phones requiring high quality voice and music playback.

Four DAC channels and four ground-referenced Class W output drivers provide interfaces to a headset connector, earpiece or line output. Ground loop feedback is employed to reduce common mode noise on these outputs.

An advanced micro-power accessory interface provides plug-in / removal and hookswitch button press detection with support for up to seven buttons in parallel with the headset microphone. Load impedance sensing circuits provide support for a wide range of 3.5mm accessory types, including AV connectors.

The digital core is highly optimised to produce very high quality sidetones with low latency filters supporting both wideband and narrowband voice sample rates. Programmable filtering, equalisation and dynamic range control are also available in the record and playback paths. Flexible DAC mixing options are provided to all outputs.

The device integrates PDM interfaces for digital microphones and digital speaker amplifiers.

A MICBIAS with a dedicated LDO provides exceptionally high PSRR and low noise microphone amplifiers provide up to 30dB of gain in the ADC path.

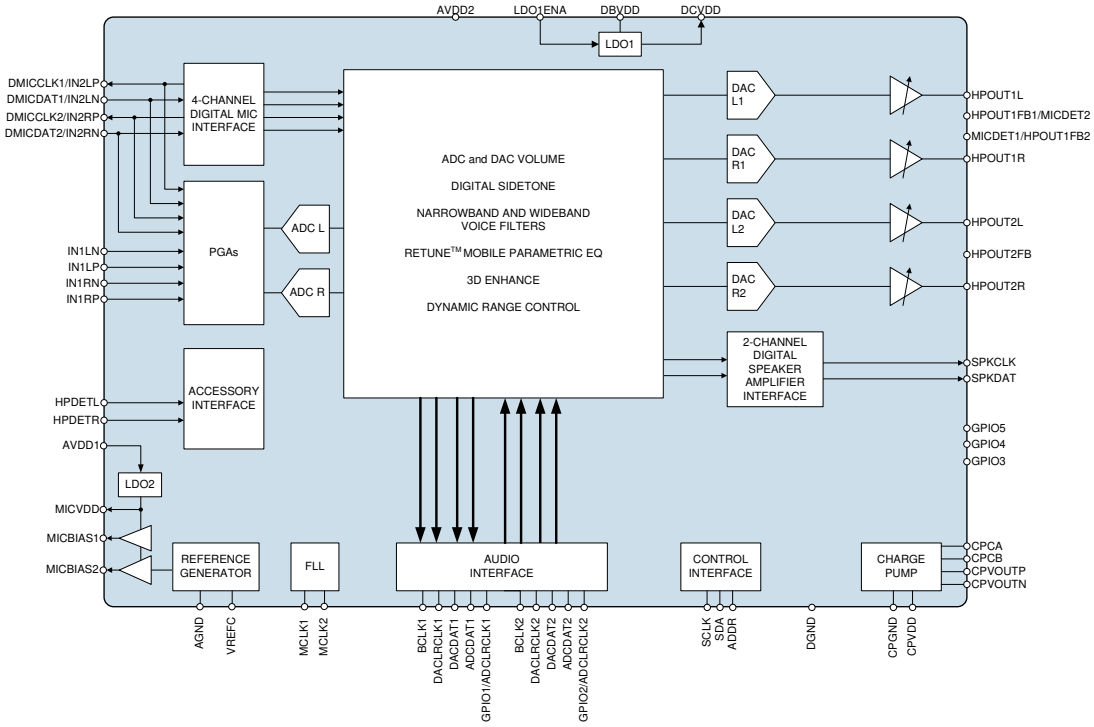
The WM8915 is supplied in a 3.24 x 3.56 x 0.7mm W-CSP package, ideal for portable systems.

FEATURES

- 4-channel DAC with 99dB SNR ('A' weighted)
- Four Class W ground-referenced headphone/line outputs
- 4-channel PDM digital inputs (digital microphone support)
- 2-channel PDM digital outputs (digital speaker amp support)
- Advanced 3.5mm accessory interface
  - Up to seven headset buttons supported
  - Accessory type detection and load impedance sense
  - Ultra-low power plug-in detect and button monitor
  - MICBIAS with dedicated LDO for ultra-high PSRR
- Programmable digital audio interface
  - All standard data formats supported
  - Multi-channel mixed rate TDM support
  - Standard sample rates up to 48kHz
  - Second interface to allow data pass-through
- 5mW total power consumption in playback mode
- Low power FLL
  - Provides all necessary internal clocks
  - 32kHz to 34MHz input frequency support
- 2-wire control interface
- 54-pin W-CSP package (3.24 x 3.56 x 0.58mm, 0.4mm pitch)

APPLICATIONS

- Music phones
- General purpose low power portable CODEC applications



[1] This product is protected by Patents US 7,622,984 and US 7,626,445.

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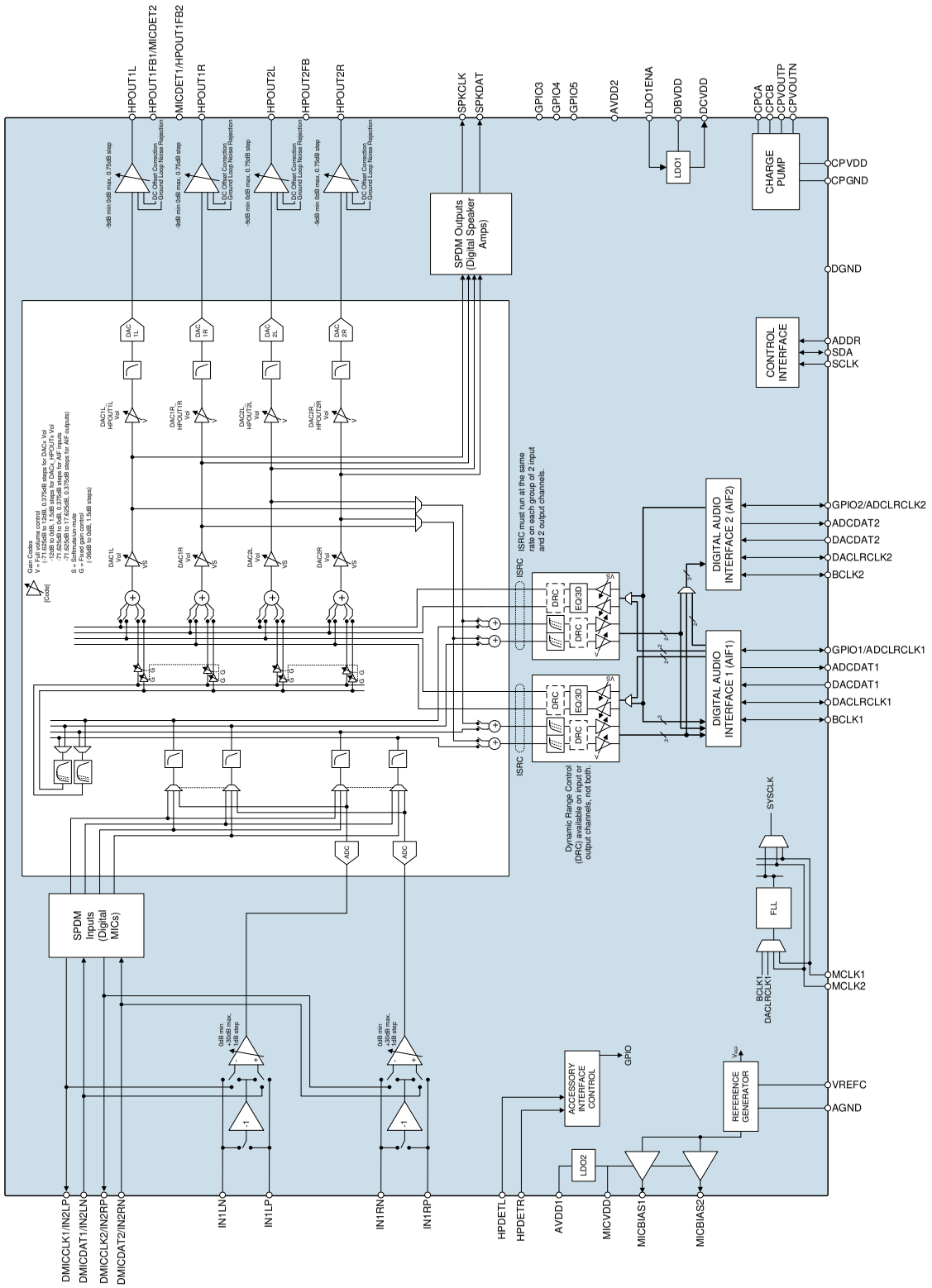
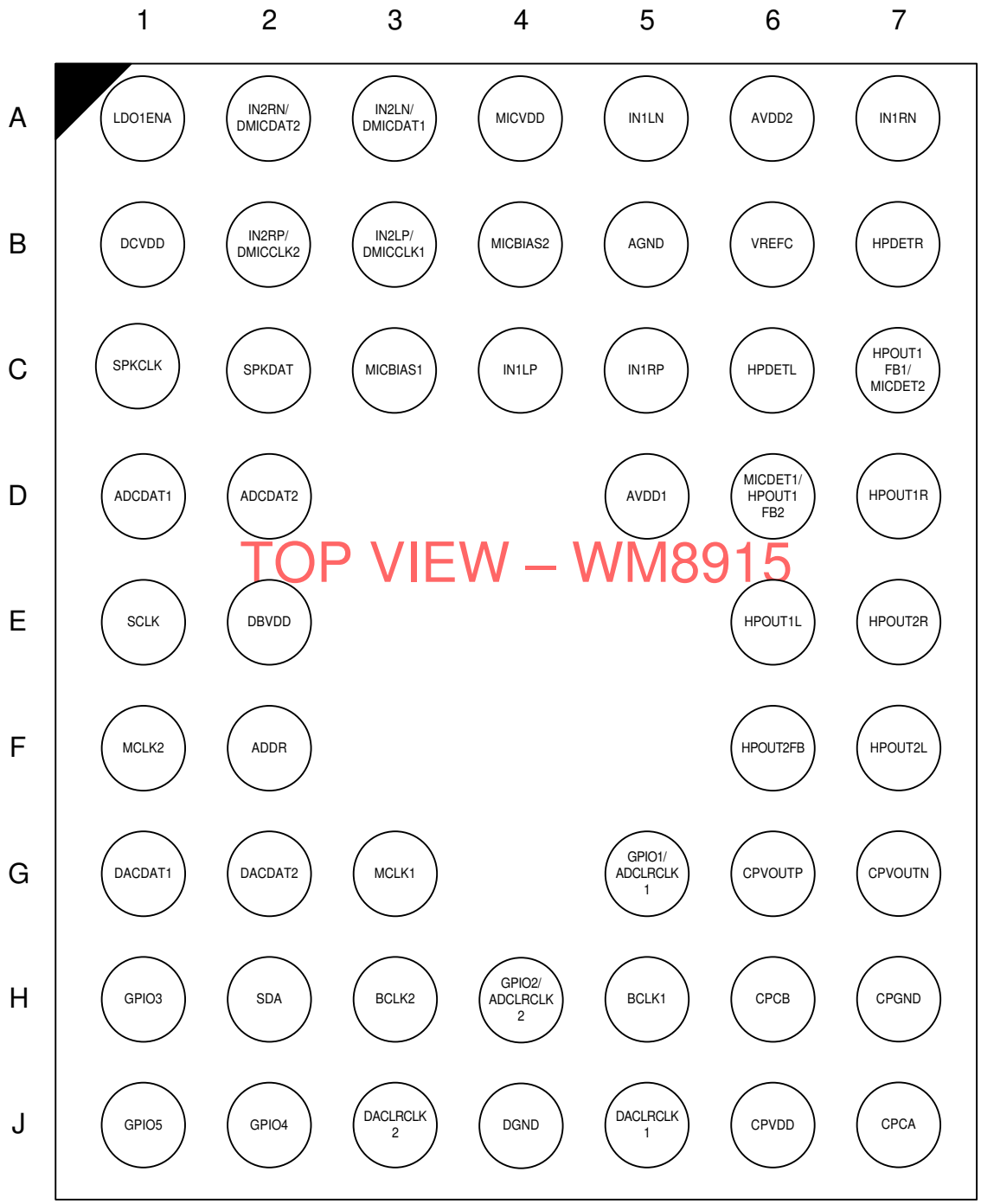
BLOCK DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8915ECSN/R	-40°C to +85°C	54-ball W-CSP (pb-free, tape and reel)	MSL1	260°C

Note:
Reel quantity = 5,000

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
A1	LDO1ENA	Digital Input	Enable pin for LDO1
A2	IN2RN/ DMICDAT2	Analogue Input / Digital Input	Right channel negative differential input 2 / Digital Microphone data input 2
A3	IN2LN/ DMICDAT1	Analogue Input / Digital Input	Left channel negative differential input 2 / Digital Microphone data input 1
A4	MICVDD	Supply / Analogue Output	Microphone supply / LDO2 output
A5	IN1LN	Analogue Input	Left channel inverting single-ended input 1 / Left channel negative differential input 1
A6	AVDD2	Supply	Analogue core supply
A7	IN1RN	Analogue Input	Right channel inverting single-ended input 1 / Right channel negative differential input 1
B1	DCVDD	Supply / Analogue Output	Digital core supply / LDO1 output
B2	IN2RP/ DMICCLK2	Analogue Input / Digital Output	Right channel positive differential input 2/ Digital Microphone clock output 2
B3	IN2LP/ DMICCLK1	Analogue Input / Digital Output	Left channel positive differential input 2/ Digital Microphone clock output 1
B4	MICBIAS2	Analogue Output	Microphone bias 2 (for microphone / accessory detection circuit)
B5	AGND	Supply	Analogue ground (Return path for AVDD1, AVDD2, MICVDD)
B6	VREFC	Analogue Output	Bandgap reference decoupling capacitor
B7	HPDETR	Analogue Input / Output	Headphone Right sense input
C1	SPKCLK	Digital Output	Digital Speaker (PDM) clock output
C2	SPKDAT	Digital Output	Digital Speaker (PDM) data output
C3	MICBIAS1	Analogue Output	Microphone bias 1 (digital microphone supply)
C4	IN1LP	Analogue Input	Left channel non-inverting single-ended input / Left channel positive differential input
C5	IN1RP	Analogue Input	Right channel non-inverting single-ended input / Right channel positive differential input
C6	HPDETL	Analogue Input / Output	Headphone Left sense input
C7	HPOUT1FB1/ MICDET2	Analogue Input	HPOUT1L and HPOUT1R ground feedback pin 1 Microphone & accessory sense input 2
D1	ADCDAT1	Digital Output	Audio interface 1 ADC digital audio data
D2	ADCDAT2	Digital Output	Audio interface 2 ADC digital audio data
D5	AVDD1	Supply	LDO2 input
D6	MICDET1/ HPOUT1FB2	Analogue Input	Microphone & accessory sense input 1 HPOUT1L and HPOUT1R ground feedback pin 2
D7	HPOUT1R	Analogue Output	Right headphone 1 output
E1	SCLK	Digital Input	Control interface clock input
E2	DBVDD	Supply	Digital buffer (I/O) supply / LDO1 input
E6	HPOUT1L	Analogue Output	Left headphone 1 output
E7	HPOUT2R	Analogue Output	Right headphone 2 output
F1	MCLK2	Digital Input	Master clock 2

PIN NO	NAME	TYPE	DESCRIPTION
F2	ADDR	Digital Input	Control interface 1 3-/4-wire (SPI) chip select or 2-wire (I2C) address select
F6	HPOUT2FB	Analogue Input	HPOUT2L and HPOUT2R ground loop noise rejection feedback
F7	HPOUT2L	Analogue Output	Left headphone 2 output
G1	DACDAT1	Digital Input	Audio interface 1 DAC digital audio data
G2	DACDAT2	Digital Input	Audio interface 2 DAC digital audio data
G3	MCLK1	Digital Input	Master clock 1
G5	GPIO1/ ADCLRCLK1	Digital Input / Output	General Purpose pin GPIO 1 / Audio interface 1 ADC (TX) left / right clock
G6	CPVOUTP	Analogue Output	Charge pump positive supply decoupling pin (HPOUT1 / HPOUT2)
G7	CPVOUTN	Analogue Output	Charge pump negative supply decoupling pin (HPOUT1 / HPOUT2)
H1	GPIO3	Digital Input / Output	General Purpose pin GPIO 3
H2	SDA	Digital Input / Output	Control interface data input and output / acknowledge output
H3	BCLK2	Digital Input / Output	Audio interface 2 bit clock
H4	GPIO2/ ADCLRCLK2	Digital Input / Output	General Purpose pin GPIO 2 / Audio interface 2 ADC (TX) left / right clock
H5	BCLK1	Digital Input / Output	Audio interface 1 bit clock
H6	CPCB	Analogue Output	Charge pump fly-back capacitor pin
H7	CPGND	Supply	Charge pump ground (Return path for CPVDD)
J1	GPIO5	Digital Input / Output	General Purpose pin GPIO 5
J2	GPIO4	Digital Input / Output	General Purpose pin GPIO 4
J3	DACLRCLK2	Digital Input / Output	Audio interface 2 DAC (RX) left / right clock (can also be used for ADC (TX) clock)
J4	DGND	Supply	Digital ground (Return path for DCVDD and DBVDD)
J5	DACLRCLK1	Digital Input / Output	Audio interface 1 DAC (RX) left / right clock (can also be used for ADC (TX) clock)
J6	CPVDD	Supply	Charge pump supply
J7	CPCA	Analogue Output	Charge pump fly-back capacitor pin

The following table identifies the power domain and ground reference associated with each of the input / output pins.

PIN NO	NAME	POWER DOMAIN	GROUND DOMAIN
D1	ADCDAT1	DBVDD	DGND
D2	ADCDAT2	DBVDD	DGND
F2	ADDR	DBVDD	DGND
H5	BCLK1	DBVDD	DGND
H3	BCLK2	DBVDD	DGND
G1	DACDAT1	DBVDD	DGND
G2	DACDAT2	DBVDD	DGND
J5	DACLRCLK1	DBVDD	DGND
J3	DACLRCLK2	DBVDD	DGND
G5	GPIO1 / ADCLRCLK1	DBVDD	DGND
H4	GPIO2 / ADCLRCLK2	DBVDD	DGND
H1	GPIO3	DBVDD	DGND
J2	GPIO4	DBVDD	DGND
J1	GPIO5	DBVDD	DGND
A5	IN1LN	AVDD2	AGND
C4	IN1LP	AVDD2	AGND
A7	IN1RN	AVDD2	AGND
C5	IN1RP	AVDD2	AGND
A3	IN2LN / DMICDAT1	AVDD2 (IN2LN) or MICBIAS1 (DMICDAT1)	AGND (IN2LN) or DGND (DMICDAT1)
B3	IN2LP / DMICCLK1	AVDD2 (IN2LP) or MICBIAS1 (DMICCLK1)	AGND (IN2LP) or DGND (DMICCLK1)
A2	IN2RN / DMICDAT2	AVDD2 (IN2RN) or MICBIAS1 (DMICDAT2)	AGND (IN2RN) or DGND (DMICDAT2)
B2	IN2RP / DMICCLK2	AVDD2 (IN2RP) or MICBIAS1 (DMICCLK2)	AGND (IN2RP) or DGND (DMICCLK2)
A1	LDO1ENA	DBVDD	DGND
G3	MCLK1	DBVDD	DGND
F1	MCLK2	DBVDD	DGND
E1	SCLK	DBVDD	DGND
H2	SDA	DBVDD	DGND
C1	SPKCLK	DBVDD	DGND
C2	SPKDAT	DBVDD	DGND

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (AVDD1, MICVDD)	-0.3V	+4.5V
Supply voltages (AVDD2, DCVDD, DBVDD)	-0.3V	+2.5V
Supply voltages (CPVDD)	-0.3V	+2.2V
Voltage range digital inputs	DGND -0.3V	DBVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD2 +0.3V
Operating temperature range, T_A	-40ºC	+85ºC
Junction temperature, T_J	-40ºC	+150ºC
Storage temperature after soldering	-65ºC	+150ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core) See notes 3, 4	DCVDD	0.95	1.0	2.0	V
Digital supply range (I/O)	DBVDD	1.62	1.8	2.0	V
Analogue supply 1 range	AVDD1	1.71	3.0	3.6	V
Analogue supply 2 range	AVDD2	1.71	1.8	2.0	V
Charge Pump supply range	CPVDD	1.71	1.8	2.0	V
Microphone Bias supply See notes 5, 6	MICVDD	1.71	2.5	3.6	V
Ground	DGND, AGND, CPGND		0		V
Operating temperature range	T_A	-40		+85	ºC

Notes:

1. All digital and analogue grounds must always be within 0.3V of each other.
2. There is no power sequencing requirement; the supplies may be enabled in any order.
3. An internal LDO (powered by DBVDD) can be used to provide the DCVDD supply.
4. When DCVDD is supplied externally (not from LDO1), the DBVDD voltage must be greater than or equal to DCVDD.
5. An internal LDO (powered by AVDD1) can be used to provide the MICVDD supply.
6. When MICVDD is supplied externally (not from LDO2), the AVDD1 voltage must be greater than or equal to MICVDD.

ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD=1.0V, AVDD2=DBVDD=CPVDD=1.8V, AVDD1=3.0V, MICVDD=2.5V, AGND=DGND=CPGND=0V,
T_A = +25ºC, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (INxLN, INxLP, INxRN, INxRP)						
A1	Maximum Full-Scale PGA Input Signal Level. Note - for AVDD2<1.8V, the full scale input is reduced in proportion to AVDD2.	Single-ended PGA input (IN1LN, IN1LP, IN1RN, IN1RP)			0.5 -6.02	Vrms dBV
		Differential PGA input			1.0 0	Vrms dBV
B4	Input Resistance	Single-ended PGA input, gain = 0dB	5.25	7.5		kΩ
		Single-ended PGA input, gain = +31dB	1.33	1.9		
B5		Differential PGA input, gain = 0dB	42	60		
		Differential PGA input, gain = +31dB	2.31	3.3		
Input Programmable Gain Amplifiers (PGAs)						
B1	Minimum Programmable Gain			0		dB
B2	Maximum Programmable Gain			31		dB
B3	Programmable Gain Step Size	Guaranteed monotonic		1		dB
Output Programmable Gain Amplifiers (PGAs)						
C1	Minimum Programmable Gain			-9		dB
C2	Maximum Programmable Gain			0		dB
C3	Programmable Gain Step Size	Guaranteed monotonic		0.75		dB
ADC Input Path Performance (Differential Input from IN1LN/P or IN1RN/P)						
D1	SNR	A-weighted, ADC_OSR128=1	90	94		dB
D2	THD	-1dBV input		-83		dB
	THD+N	-1dBV input		-83	-75	dB
D3	Channel separation (L/R)	-1dBV input		-100		dB
D4	Power Supply Rejection Ratio	100mV pk-pk, 217Hz, any supply		80		dB
		100mV pk-pk, 10kHz, any supply		70		
D5	Common Mode Rejection Ratio	0dBV input, 217Hz, PGA in differential mode, gain = 0dB		60		dB
		0dBV input, 217Hz, PGA in differential mode, gain = +30dB		70		
ADC Input Path Performance (Single-Ended Input from IN1LN, IN1LP, IN1RN or IN1RP)						
E1	SNR	A-weighted, ADC_OSR128=1	90	94		dB
E2	THD	-7dBV input		-83		dB
	THD+N	-7dBV input		-81	-72	dB
E3	Channel separation (L/R)	-7dBV input		-100		dB
E4	Power Supply Rejection Ratio	100mV pk-pk, 217Hz, any supply		50		dB
		100mV pk-pk, 10kHz, any supply		50		
ADC Input Path Performance (Differential Input from IN2LN/P or IN2RN/P)						
F1	SNR	A-weighted, ADC_OSR128=1	90	94		dB
F2	THD	-1dBV input		-83		dB
	THD+N	-1dBV input		-83	-75	dB
F3	Channel separation (L/R)	-1dBV input		-100		dB
F4	Power Supply Rejection Ratio	100mV pk-pk, 217Hz, any supply		80		dB
		100mV pk-pk, 10kHz, any supply		70		
F5	Common Mode Rejection Ratio	-20dBV input, 217Hz, PGA in differential mode, gain = 0dB		60		dB
		-20dBV input, 217Hz, PGA in differential mode, gain = +20dB		70		

Test Conditions

DCVDD=1.0V, AVDD2=DBVDD=CPVDD=1.8V, AVDD1=3.0V, MICVDD=2.5V, AGND=DGND=CPGND=0V,
T_A = +25ºC, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

DAC Output Path (HPOUT1L, HPOUT1R, HPOUT2L, HPOUT2R), Line Load R_L = 10kΩ						
G1	SNR	A-weighted, DAC_OSR128=1	92	100		dB
G2	THD	1Vrms output		-81		dB
	THD+N	1Vrms output		-81		dB
G3	Channel Separation (L/R)	1Vrms output		-100		dB
G4	Power Supply Rejection Ratio	100mV pk-pk, 217Hz, any supply		80		dB
		100mV pk-pk, 10kHz, any supply		65		
DAC Output Path (HPOUT1L, HPOUT1R, HPOUT2L, HPOUT2R), Headphone Load R_L = 32Ω						
G6	SNR	A-weighted, DAC_OSR128=1	92	99		dB
G7	THD	P_O = 20mW		-80		dB
	THD+N	P_O = 20mW		-78		dB
	THD	P_O = 5mW		-80		dB
	THD+N	P_O = 5mW		-79		dB
G8	Channel Separation (L/R)	P_O = 20mW		-98		dB
G9	Power Supply Rejection Ratio	100mV pk-pk, 217Hz, any supply		80		dB
		100mV pk-pk, 10kHz, any supply		65		
DAC Output Path (HPOUT1L, HPOUT1R, HPOUT2L, HPOUT2R), Headphone Load R_L = 16Ω						
G11	SNR	A-weighted, DAC_OSR128=1	92	99		dB
G12	THD	P_O = 20mW		-76		dB
	THD+N	P_O = 20mW		-74		dB
	THD	P_O = 5mW		-80	-75	dB
	THD+N	P_O = 5mW		-79	-75	dB
G13	Channel Separation (L/R)	P_O = 20mW		-95		dB
G14	Power Supply Rejection Ratio	100mV pk-pk, 217Hz, any supply		80		dB
		100mV pk-pk, 10kHz, any supply		65		
Headphone Output Driver (HPOUT1L, HPOUT1R, HPOUT2L, HPOUT2R)						
	Minimum output load resistance		15			Ω
	Maximum output load capacitance				2	nF

Test Conditions

DCVDD=1.0V, AVDD2=DBVDD=CPVDD=1.8V, AVDD1=3.0V, MICVDD=2.5V, AGND=DGND=CPGND=0V,
T_A = +25ºC, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Bias (Note: No capacitor on MICBIAS)						
H1	Bias Voltage (Regulator mode) (MICBIAS1 or MICBIAS2, 1.0mA load current)	MICBx_LVL = 000b	-4%	1.5	+4%	V
		MICBx_LVL = 001b	-4%	1.8	+4%	
		MICBx_LVL = 010b	-4%	1.9	+4%	
		MICBx_LVL = 011b	-4%	2.0	+4%	
		MICBx_LVL = 100b	-4%	2.2	+4%	
		MICBx_LVL = 101b	-4%	2.4	+4%	
		MICBx_LVL = 110b	-4%	2.5	+4%	
		MICBx_LVL = 111b	-4%	2.6	+4%	
H2	Bias Voltage (Bypass mode) (MICBIAS1 or MICBIAS2, 1mA load current)		MICVDD - 80mV		MICVDD	V
H3	Bias Current (Regulator Mode)	MICVDD - MICBIASn >200mV			2.4	mA
H4	Bias Current (Bypass mode)				3.6	mA
H5	Output Noise Density @ 1kHz	MICBx_LVL = 100b, Output current = 1mA		60		nV/√Hz
H6	Integrated Noise Voltage (100Hz to 7kHz)	MICBx_LVL = 100b, Output current = 1mA		4.5		uVrms
H7	PSRR (100mV pk-pk on AVDD1)	217Hz		100		dB
		10kHz		80		dB
Digital Input / Output (except DMICDATn and DMICCLKn)						
J1	Input HIGH Level		0.7×DBVDD			V
J2	Input LOW Level				0.3×DBVDD	V
Note that digital input pins should not be left unconnected / floating. Internal pull-up/pull-down resistors may be enabled on GPIO pins if required.						
J3	Output HIGH Level	I_{OH} = 4mA	0.8×DBVDD			V
J4	Output LOW Level	I_{OL} = -4mA			0.2×DBVDD	V
J5	Pin capacitance			10		pF
J6	Pin leakage		-0.9		0.9	uA
Digital Microphone Input / Output (DMICDATn and DMICCLKn)						
J7	DMICDATn input HIGH Level	MICBIAS1 = MICVDD, MICB1_MODE = 1	0.7 × MICBIAS1			V
J8	DMICDATn input LOW Level	MICBIAS1 = MICVDD, MICB1_MODE = 1			0.3 x MICBIAS1	V
J11	Pin capacitance			10		pF
J12	Pin leakage		-0.9		0.9	µA
Note that digital input pins should not be left unconnected / floating. Internal pull-up/pull-down resistors may be enabled on GPIO pins if required.						
J9	DMICCLK output HIGH Level	MICBIAS1 = MICVDD, MICB1_MODE = 1	0.8 × MICBIAS1			V
J10	DMICCLK output LOW Level	MICBIAS1 = MICVDD, MICB1_MODE = 1			0.2 x MICBIAS1	V
Digital Pull-Up / Pull-Down						
	Pull-Up resistance	Measured at HIGH Level output condition	40	60	80	kΩ
	Pull-Down resistance	Measured at LOW Level output condition	40	60	80	kΩ

Test Conditions

DCVDD=1.0V, AVDD2=DBVDD=CPVDD=1.8V, AVDD1=3.0V, MICVDD=2.5V, AGND=DGND=CPGND=0V,
T_A = +25ºC, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FLL						
K4	Lock time	F_{REF} = 13MHz			0.3	ms
		F_{REF} = 32kHz			2	
K5	FLL Clock (GPIO output) duty cycle		45:55		55:45	%
LDO1 Regulator						
L3	Output voltage (DCVDD)		0.9		1.2	V
L1	Start-up Time (for LDO1 output to exceed 0.95V)	VREFC Cap = 1uF, DCVDD Cap = 4.7uF, LDO1 in Bypass Mode			5	ms
LDO2 Regulator						
M3	Output voltage (MICVDD)		1.7		2.8	V
M1	Start-up Time (for LDO2 output to reach 90% of final value)	VREFC Cap = 1uF, MICVDD Cap = 4.7uF, LDO2 in Normal Mode			1.5	ms
		VREFC Cap = 1uF, MICVDD Cap = 4.7uF, LDO2 in Bypass Mode			3	
Charge Pump						
N3	CPVOUTP (CP mode is controlled automatically)	Normal mode		CPVDD		V
		Low power mode		CPVDD/2		
N4	CPVOUTN (CP mode is controlled automatically)	Normal mode		-CPVDD		V
		Low power mode		-CPVDD/2		
N5	Maximum Total Output Power			100		mW
N1	Start-up Time				500	µs
Wired Accessory Interface						
P1	Load impedance detection ranges	HPDETL or HPDETR	-30%	8 to 128	+30%	Ω
	Load impedance ranges for valid button detection (pull-down resistor in headset) Measured on MICDET1 or MICDET2, 2.2kΩ (2%) MICBIAS resistor, MICBn_LVL = 100b (2.2V). Note these characteristics assume no other component is connected to MICDETn. See "Applications Information" for recommended external components when a typical microphone is present.	for MICD_LVL[0] = 1	0		3	Ω
		for MICD_LVL[1] = 1	13.33		15.27	
		for MICD_LVL[2] = 1	27.16		30.96	
		for MICD_LVL[3] = 1	42.48		49.47	
		for MICD_LVL[4] = 1	65		85	
		for MICD_LVL[5] = 1	114		155.24	
		for MICD_LVL[6] = 1	191		329.87	
		for MICD_LVL[8] = 1	475		30000	
P2	Programmable debounce time		0		0.5	s
P3	Programmable debounce step size			1		ms

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum full scale output signal and the output with no input signal applied.
2. Total Harmonic Distortion (dB) – THD is the level of the rms value of the sum of harmonic distortion products relative to the amplitude of the measured output signal.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the level of the rms value of the sum of harmonic distortion products plus noise in the specified bandwidth relative to the amplitude of the measured output signal.
4. Channel Separation (L/R) (dB) – left-to-right and right-to-left channel separation is the measured signal level in the idle channel at the test signal frequency relative to the signal level at the output of the active channel. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
5. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.
6. All performance measurements carried out with 20kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCKS & FREQUENCY LOCKED LOOP (FLL)

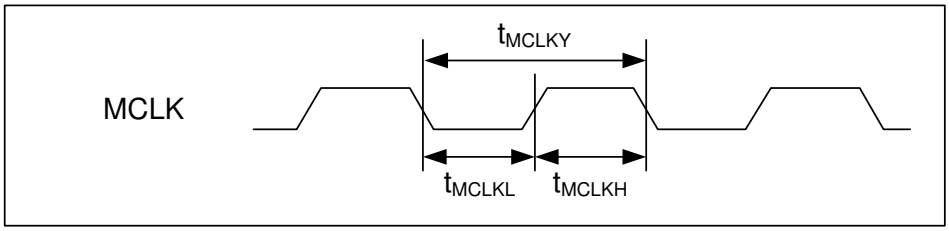


Figure 1 Master Clock Timing

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Master Clock Timing (MCLK1 and MCLK2)						
MCLK cycle time	T_{MCLKY}	MCLK as input to FLL, FLLn_REFCLK_DIV = 10	29.4			ns
		MCLK as input to FLL, FLLn_REFCLK_DIV = 01	37			
		MCLK as input to FLL, FLLn_REFCLK_DIV = 00	74			
		FLL not used, SYSCLK_DIV = 1	40			ns
		FLL not used, SYSCLK_DIV = 0	80			ns
MCLK duty cycle (= T_{MCLKH} : T_{MCLKL})			60:40		40:60	
Frequency Locked Loop (FLL)						
FLL input frequency		FLL_REFCLK_DIV = 00	0.032		13.5	MHz
		FLL_REFCLK_DIV = 01	0.064		27	
		FLL_REFCLK_DIV = 10	0.128		34	
Internal Clocking						
SYSCLK frequency		48kHz (and integer related) audio sample rates		12.288		MHz
		44.1kHz (and integer related) audio sample rates		11.2896		

AUDIO INTERFACE TIMING

DIGITAL MICROPHONE (DMIC) INTERFACE TIMING

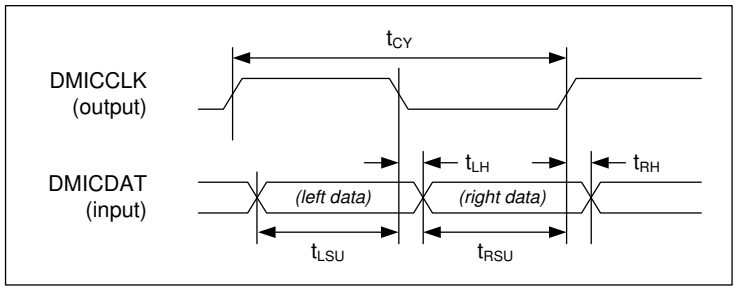


Figure 2 Digital Microphone Interface Timing

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital Microphone Interface Timing					
DMICCLK cycle time	t_{CY}	325		651	ns
DMICDAT (Left) setup time to falling DMICCLK edge	t_{LSU}	15			ns
DMICDAT (Left) hold time from falling DMICCLK edge	t_{LH}	0			ns
DMICDAT (Right) setup time to rising DMICCLK edge	t_{RSU}	15			ns
DMICDAT (Right) hold time from rising DMICCLK edge	t_{RH}	0			ns

DIGITAL SPEAKER (PDM) INTERFACE TIMING

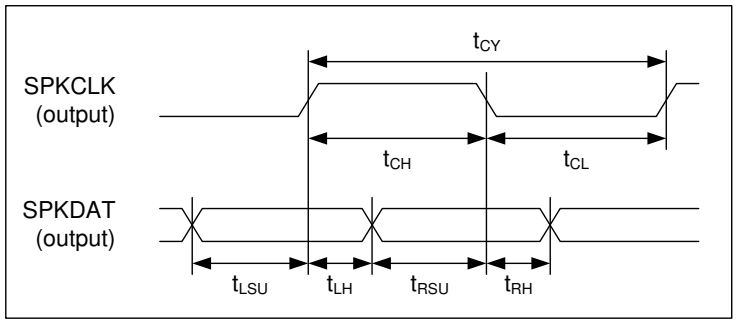


Figure 3 Digital Speaker (PDM) Interface Timing - Mode A

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
PDM Audio Interface Timing					
SPKCLK cycle time	t_{CY}	160	163	340	ns
SPKCLK pulse width high	t_{CH}	70	80		ns
SPKCLK pulse width low	t_{CL}	70	80		ns
SPKDAT set-up time to SPKCLK rising edge (Left channel)	t_{LSU}	30			ns
SPKDAT hold time from SPKCLK rising edge (Left channel)	t_{LH}	30			ns
SPKDAT set-up time to SPKCLK falling edge (Right channel)	t_{RSU}	30			ns
SPKDAT hold time from SPKCLK falling edge (Right channel)	t_{RH}	30			ns

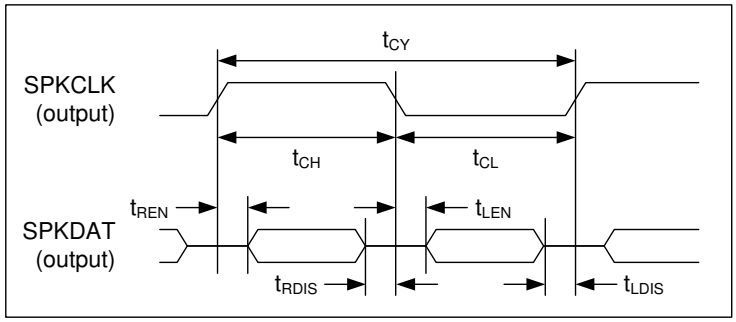


Figure 4 Digital Speaker (PDM) Interface Timing - Mode B

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
PDM Audio Interface Timing					
SPKCLK cycle time	t_{CY}	160	163	340	ns
SPKCLK pulse width high	t_{CH}	70	80		ns
SPKCLK pulse width low	t_{CL}	70	80		ns
SPKDAT enable from SPKCLK rising edge (Right channel)	t_{REN}			15	ns
SPKDAT disable to SPKCLK falling edge (Right channel)	t_{RDIS}			5	ns
SPKDAT enable from SPKCLK falling edge (Left channel)	t_{LEN}			15	ns
SPKDAT disable to SPKCLK rising edge (Left channel)	t_{LDIS}			5	ns

AIF1 / AIF2 - MASTER MODE

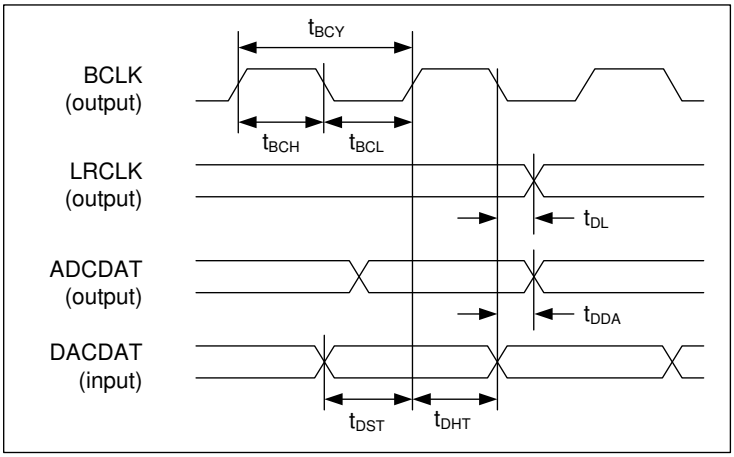


Figure 5 Audio Interface Timing - Master Mode

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Master Mode					
BCLK cycle time	t_{BCY}	160			ns
BCLK pulse width high (SYSCLK_RATE = 1)	t_{BCH}	64			ns
BCLK pulse width low (SYSCLK_RATE = 1)	t_{BCL}	64			ns
BCLK pulse width high (SYSCLK_RATE = 0)	t_{BCH}	72			ns
BCLK pulse width low (SYSCLK_RATE = 0)	t_{BCL}	72			ns
LRCLK propagation delay from BCLK falling edge	t_{DL}			20	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			20	ns
DACDAT setup time to BCLK rising edge	t_{DST}	20			ns
DACDAT hold time from BCLK rising edge	t_{DHT}	10			ns

AIF1 / AIF2 - SLAVE MODE

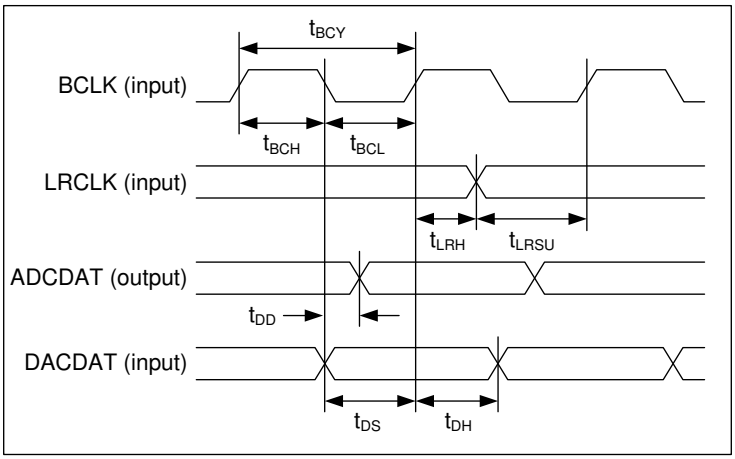


Figure 6 Audio Interface Timing – Slave Mode

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Slave Mode					
BCLK cycle time	t_{BCY}	160			ns
BCLK pulse width high	t_{BCH}	64			ns
BCLK pulse width low	t_{BCL}	64			ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}	20			ns
LRCLK hold time from BCLK rising edge	t_{LRH}	10			ns
DACDAT hold time from BCLK rising edge	t_{DH}	10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			20	ns
DACDAT set-up time to BCLK rising edge	t_{DS}	20			ns

CONTROL INTERFACE TIMING

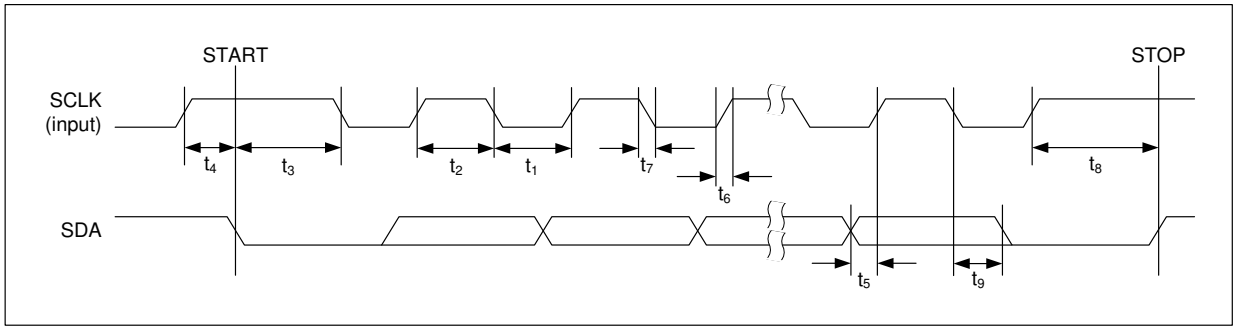


Figure 7 Control Interface Timing

Test Conditions

The following timing information is valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SCLK Frequency				1000	kHz
SCLK Low Pulse-Width	t_1	500			ns
SCLK High Pulse-Width	t_2	260			ns
Hold Time (Start Condition)	t_3	260			ns
Setup Time (Start Condition)	t_4	260			ns
Data Setup Time	t_5	50			ns
SDA, SCLK Rise Time	t_6			120	ns
SDA, SCLK Fall Time	t_7			120	ns
Setup Time (Stop Condition)	t_8	260			ns
Data Hold Time	t_9			450	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		50	ns

DEVICE DESCRIPTION

INTRODUCTION

The WM8915 is a low power, high quality audio codec designed to interface with a wide range of processors and digital audio components. A high level of mixed-signal integration in a very small footprint makes it ideal for portable applications such as mobile phones.

Two separate audio interfaces are available in order to provide independent and fully asynchronous connections to multiple processors. These interfaces provide input and output paths to the ADCs, DACs and digital mixing functions on the WM8915. A flexible signal routing capability between the two interfaces is also provided.

Four digital microphone input channels are available to support advanced multi-microphone applications such as noise reduction. An integrated microphone activity monitor is available to enable the processor to sleep during periods of microphone inactivity, saving power.

Up to four analogue inputs can be connected, to allow interfacing to microphones or line level audio signals. The WM8915 supports single-ended and differential analogue input connections. Signal routing to the output mixers and within the CODEC has been designed for maximum flexibility to support a wide variety of usage modes.

Four DAC channels are available to support use cases requiring up to four headphone output channels. A stereo digital (SPDM) output is provided for connection to external speaker drivers; flexible signal routing is provided between the DACs and the SPDM outputs.

Two pairs of ground-referenced headphone outputs are provided; these are powered from an integrated Charge Pump, enabling high quality, power efficient headphone playback without any requirement for DC blocking capacitors. A DC Servo circuit is available for DC offset correction, suppressing pops and reducing power consumption. Ground loop feedback is available on the headphone outputs, providing rejection of noise on the ground connections. All outputs have integrated pop and click suppression features.

The ADCs and DACs are of hi-fi quality, using a 24-bit low-order oversampling architecture to deliver optimum performance. A flexible clocking arrangement supports mixed sample rates, whilst an integrated ultra-low power FLL provides additional flexibility. A configurable high pass filter is available in all ADC and digital MIC paths for removing DC offsets and suppressing low frequency noise such as mechanical vibration and wind noise. A digital mixing path from the ADC or digital MICs to the DAC provides a sidetone of enhanced quality during voice calls. DAC soft mute and un-mute is available for pop-free music playback.

The integrated Dynamic Range Controllers (DRC) and ReTune™ Mobile 5-band parametric equaliser (EQ) provide further processing capability of the digital audio paths. The DRC provides compression and signal level control to improve the handling of unpredictable signal levels. ‘Anti-clip’ and ‘quick release’ algorithms improve intelligibility in the presence of transients and impulsive noises. The EQ provides the capability to tailor the audio path according to the frequency characteristics of an earpiece or loudspeaker, and/or according to user preferences.

External accessory detection is provided to measure the impedance of headphones and to detect push-switch operation and microphone connection. These features enable intelligent signal path configuration to be implemented according to the status of any external accessory components.

The WM8915 has two highly flexible digital audio interfaces, supporting a number of protocols, including I^2S, DSP and Left-Justified formats, and can operate in master or slave modes. Each interface is independently configurable on the respective transmit and receive paths. Time division multiplexing (TDM) is supported on both interfaces to allow multiple devices to stream data simultaneously on the same bus, saving space and power.

Up to six digital input / output channels can be supported simultaneously via the TDM channels on digital audio interface 1 (AIF1). It is also possible to support different sample rates simultaneously on any of the input or output paths of AIF1.

A powerful digital mixing core allows data from each input channel and from the ADCs and digital MICs to be mixed and re-routed back to a different audio interface and to the 4 DAC output channels.

The system clock (SYSCLK) provides clocking for the ADCs, DACs, DSP core, digital audio interface and other circuits. SYSCLK can be derived directly from the MCLK1 or MCLK2 pins or from the integrated FLL, providing flexibility to support a wide range of clocking schemes. A wide range of typical portable system MCLK frequencies is supported.

The WM8915 uses a standard 2-wire control interface, providing full software control of all features, together with device register readback. An integrated Control Write Sequencer enables automatic scheduling of control sequences; commonly-used signal configurations may be selected using ready-programmed sequences, including time-optimised control of the WM8915 pop suppression features. It is an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs. Unused circuitry can be disabled under software control, in order to save power; low leakage currents enable extended standby/off time in portable battery-powered applications.

Versatile GPIO functionality is provided, with support for button/accessory detect inputs, or for clock, system status, or programmable logic level output for control of additional external circuitry. Interrupt logic, status readback and de-bouncing options are supported within this functionality.

ANALOGUE INPUT SIGNAL PATH

The WM8915 has four dedicated analogue input pins, which may be used to support connections to multiple microphone or line input sources. Analogue input is also supported using the digital microphone interface pins, which may also be configured as analogue inputs if required.

A maximum of two analogue input signal paths may be enabled at once. The left and right input PGAs can each be configured to select a single-ended or a differential input connection. The selected inputs are routed to the Analogue to Digital Converters (ADCs), and can be routed to the Digital Audio Interface output and/or mixed into the Output Signal Paths.

The Left Input PGA can select IN1LN or IN1LP as a single-ended input, or can select a differential input configuration on the IN1LP - IN1LN pins or a differential input on the IN2LP - IN2LN pins.

The Right Input PGA can select IN1RN or IN1RP as a single-ended input, or can select a differential input configuration on the IN1RP - IN1RN pins or a differential input on the IN2RP - IN2RN pins.

Input PGA gain from 0dB to +31dB is available on each input channel.

The WM8915 input signal paths and control registers are illustrated in Figure 8.

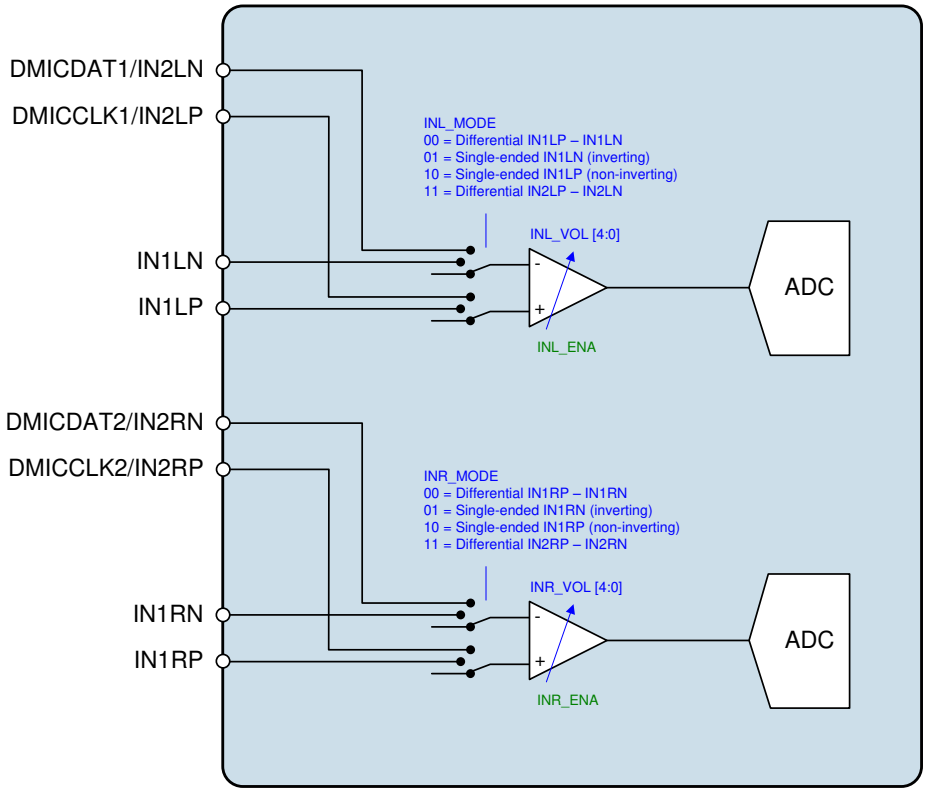


Figure 8 Control Registers for Input Signal Path

MICROPHONE BIAS CONTROL

There are two MICBIAS generators which provide low noise reference voltages suitable for biasing electret condenser (ECM) type microphones via an external resistor. Refer to the “Applications Information” section for recommended external components.

The MICBIAS outputs can be independently enabled using the MICB1_ENA and MICB2_ENA register bits. Under default conditions, a smooth pop-free profile of the MICBIAS outputs is implemented when MICB1_ENA or MICB2_ENA is enabled or disabled; a faster transition can be selected by setting the MICB1_RATE and MICB2_RATE registers as described in Table 1.

When a MICBIAS output is disabled, the output pin can be configured to be floating or to be actively discharged. This is selected using the MICB1_DISCH and MICB2_DISCH register bits.

The MICBIAS generators can each operate as a voltage regulator or in bypass mode.

In Regulator mode, the output voltage is selected using the MICB1_LVL and MICB2_LVL register bits. In this mode, MICVDD must be at least 200mV greater than the required MICBIAS output voltages. The MICBIAS outputs are powered from the MICVDD supply pin, and use the internal bandgap circuit as a reference.

Note that, in Regulator mode, the MICBIAS regulators are designed to operate without external decoupling capacitors. It is important that parasitic capacitances on the MICBIAS1 or MICBIAS2 pins do not exceed 50pF in Regulator mode.

In Bypass mode, the output pin (MICBIAS1 or MICBIAS2) is connected directly to MICVDD. This enables a low power operating state. Note that, if a capacitive load is connected to MICBIAS1 or MICBIAS2 (eg. for a digital microphone supply), then the respective MICBIAS generator must be configured in Bypass mode.

The MICBIAS configuration is illustrated in Figure 9.

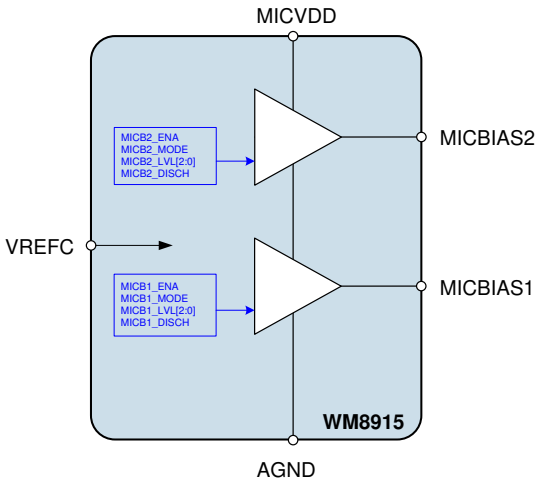


Figure 9 MICBIAS Generator