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WM8918

Ultra Low Power DAC for Portable Audio Applications

DESCRIPTION

The WM8918 is a high performance ultra-low power stereo DAC optimised for portable audio applications.

The device features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques - incorporating an innovative dual-mode charge pump architecture - to optimise efficiency and power consumption during playback. The ground-referenced headphone and line outputs eliminate AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise.

Control sequences for audio path setup can be pre-loaded and executed by an integrated control write sequencer to reduce software driver development and minimise pops and clicks via Wolfson's SilentSwitch™ technology.

The analogue input stage can be configured for single ended or differential inputs. Up to 3 stereo microphone or line inputs may be connected. The input impedance is constant with PGA gain setting.

A stereo digital microphone interface is provided, with a choice of two inputs. The analogue or digital microphone inputs can be mixed into the headphone or line output paths.

A dynamic range controller provides compression and level control to support a wide range of portable recording applications in conjunction with the digital microphone interface. Anti-clip and quick release features offer good performance in the presence of loud impulsive noises.

ReTune™ Mobile 5-band parametric equaliser with fully programmable coefficients is integrated for optimization of speaker characteristics. Programmable dynamic range control is also available for maximizing loudness, protecting speakers from clipping and preventing premature shutdown due to battery droop.

Common audio sampling frequencies are supported from a wide range of external clocks, either directly or generated via the FLL.

The WM8918 can operate directly from a single 1.8V switched supply. For optimal power consumption, the digital core can be operated from a 1.0V supply.

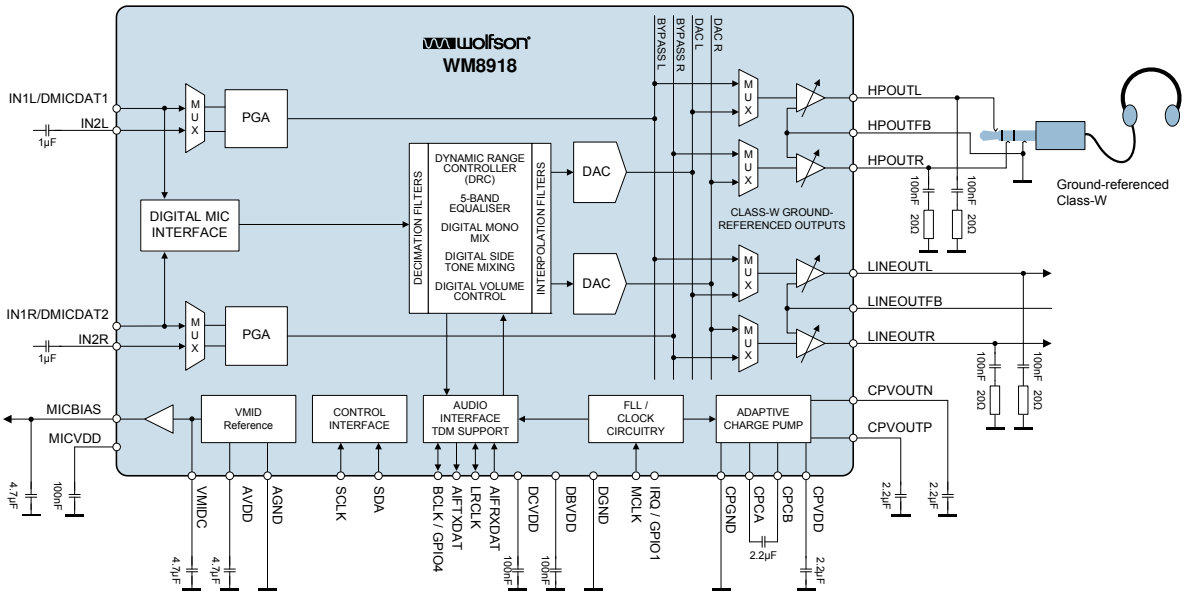
FEATURES

- 3.8mW quiescent power consumption for DAC to headphone playback
- DAC SNR 96dB typical, THD -86dB typical
- 2.4mW quiescent power consumption for analogue bypass playback
- Control write sequencer for pop minimised start-up and shutdown
- Single register write for default start-up sequence
- Integrated FLL provides all necessary clocks
  - Self-clocking modes allow processor to sleep
  - All standard sample rates from 8kHz to 96kHz
- Stereo digital microphone input
- 3 single ended inputs per stereo channel
- 1 fully differential mic / line input per stereo channel
- Digital Dynamic Range Controller (compressor / limiter)
- Digital sidetone mixing
- Ground-referenced headphone driver
- Ground-referenced line outputs
- 32-pin QFN package (4x4mm, 0.4mm pitch)

APPLICATIONS

- Wireless headsets
- Portable multimedia players
- Handheld gaming

BLOCK DIAGRAM



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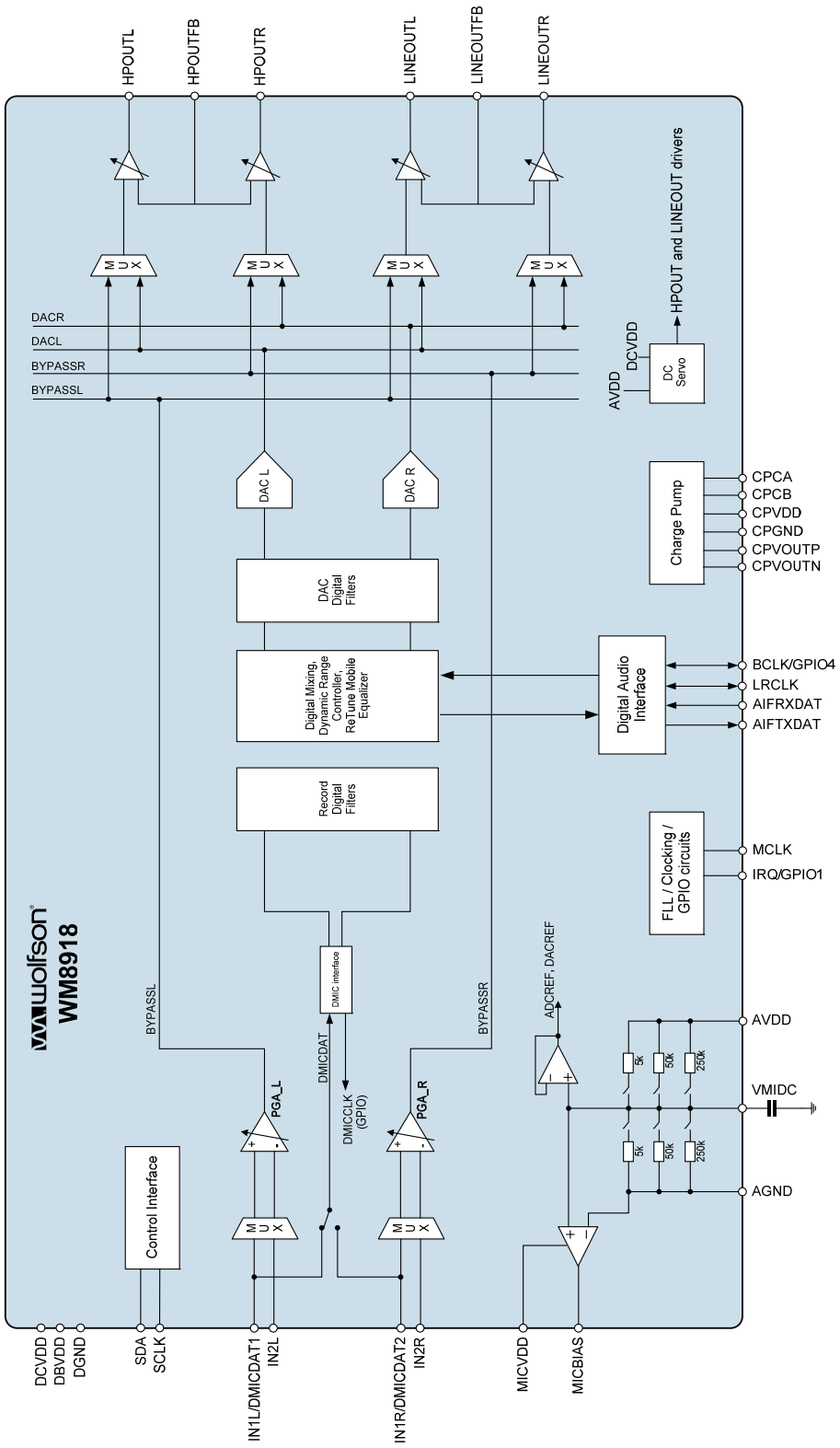
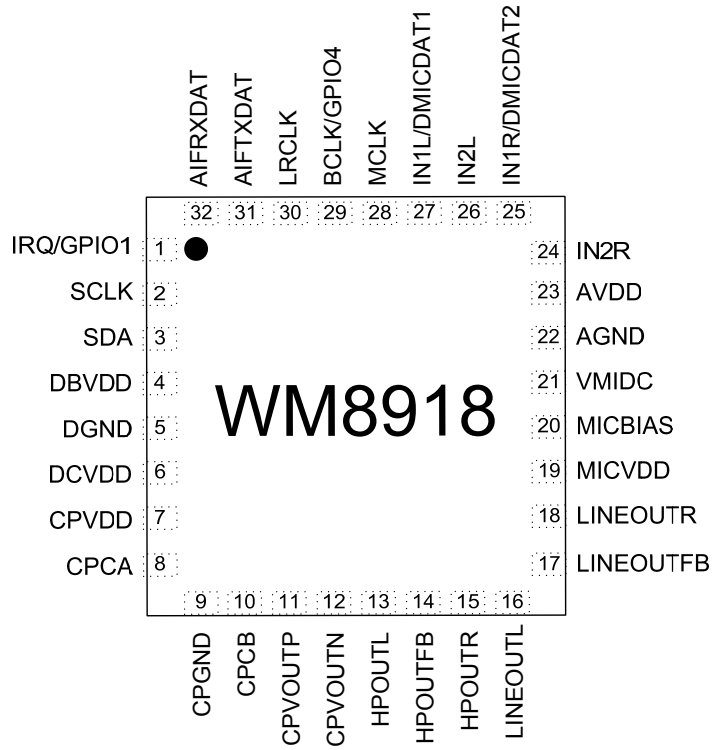
AUDIO SIGNAL PATHS DIAGRAM



PIN CONFIGURATION

The WM8918 is supplied in a 32-pin QFN package.



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8918CGEFL/V	-40°C to +85°C	32-lead QFN (4x4x0.4mm, lead-free)	MSL3	260°C
WM8918CGEFL/RV	-40°C to +85°C	32-lead QFN (4x4x0.4mm, lead-free, tape and reel)	MSL3	260°C

Note:

Reel quantity = 3,500

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	IRQ / GPIO1	Digital Input / Output	Interrupt / GPIO1
2	SCLK	Digital Input	Control interface clock input
3	SDA	Digital Input / Output	Control interface data input / output
4	DBVDD	Supply	Digital buffer supply (powers audio interface and control interface)
5	DGND	Supply	Digital ground (return path for DCVDD and DBVDD)
6	DCVDD	Supply	Digital core supply
7	CPVDD	Supply	Charge pump power supply
8	CPCA	Analogue Output	Charge pump flyback capacitor pin
9	CPGND	Supply	Charge pump ground
10	CPCB	Analogue Output	Charge pump flyback capacitor pin
11	CPVOUTP	Analogue Output	Charge pump positive supply decoupling (powers HPOUTL/R, LINEOUTL/R)
12	CPVOUTN	Analogue Output	Charge pump negative supply decoupling (powers HPOUTL/R, LINEOUTL/R)
13	HPOUTL	Analogue Output	Left headphone output (line or headphone output)
14	HPOUTFB	Analogue Input	Headphone output ground loop noise rejection feedback
15	HPOUTR	Analogue Output	Right headphone output (line or headphone output)
16	LINEOUTL	Analogue Output	Left line output 1 (line output)
17	LINEOUTFB	Analogue Input	Line output ground loop noise rejection feedback
18	LINEOUTR	Analogue Output	Right line output 1 (line output)
19	MICVDD	Supply	Microphone bias amp supply
20	MICBIAS	Analogue Output	Microphone bias
21	VMIDC	Analogue Output	Midrail voltage decoupling capacitor
22	AGND	Supply	Analogue power return
23	AVDD	Supply	Analogue power supply (powers analogue inputs, reference, DAC)
24	IN2R	Analogue Input	Right channel input 2
25	IN1R / DMICDAT2	Analogue / Digital Input	Right channel input 1 / Digital microphone data input 2
26	IN2L	Analogue Input	Left channel input 2
27	IN1L / DMICDAT1	Analogue / Digital Input	Left channel input 1 / Digital microphone data input 1
28	MCLK	Digital Input	Master clock
29	BCLK / GPIO4	Digital Input / Output	Audio interface bit clock / GPIO4
30	LRCLK	Digital Input / Output	Audio interface left / right clock (common for TX and RX)
31	AIFTXDAT	Digital Output	TX digital audio data (digital microphone data)
32	AIFRXDAT	Digital Input	RX digital audio data (DAC digital playback data)

Note:

1. It is recommended that the QFN ground paddle is connected to analogue ground on the application PCB.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
AVDD, DCVDD	-0.3V	+2.5V
DBVDD	-0.3V	+4.5V
MICVDD	-0.3V	+4.5V
CPVDD	-0.3V	+2.2V
HPOUTL, HPOUTR, LINEOUTL, LINEOUTR	(CPVDD + 0.3V) * -1	CPVDD + 0.3V
Voltage range digital inputs	DGND -0.3V	DBVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Temperature range, T_A	-40°C	+85°C
Storage temperature after soldering	-65°C	+150°C

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other; there is no restriction on power supply sequencing.
3. HPOUTL, HPOUTR, LINEOUTL, LINEOUTR are outputs, and should not normally become connected to DC levels. However, if the limits above are exceeded, then damage to the WM8918 may occur.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD	0.95	1.0	1.98	V
Digital supply range (Buffer)	DBVDD	1.42	1.8	3.6	V
Analogue supplies range	AVDD	1.71	1.8	2.0	V
Charge pump supply range	CPVDD	1.71	1.8	2.0	V
Microphone bias	MICVDD	1.71	2.5	3.6	V
Ground	DGND, AGND, CPGND		0		V
Operating Temperature (ambient)	T_A	-40	+25	+85	°C

ELECTRICAL CHARACTERISTICS

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is the difference in level between a full scale output signal and the device output noise with no signal applied, measured over a bandwidth of 20Hz to 20kHz. This ratio is also called idle channel noise. (No Auto-zero or Automute function is employed).
2. Total Harmonic Distortion (dB) – THD is the difference in level between a 1kHz full scale sinewave output signal and the first seven harmonics of the output signal. The amplitude of the fundamental frequency of the output signal is compared to the RMS value of the next seven harmonics and expressed as a ratio.
3. Total Harmonic Distortion + Noise (dB) – THD+N is the difference in level between a 1kHz full scale sine wave output signal and all noise and distortion products in the audio band. The amplitude of the fundamental reference frequency of the output signal is compared to the RMS value of all other noise and distortion products and expressed as a ratio.
4. Channel Separation (dB) – is a measure of the coupling between left and right channels. A full scale signal is applied to the left channel only, the right channel amplitude is measured. Then a full scale signal is applied to the right channel only and the left channel amplitude is measured. The worst case channel separation is quoted as a ratio.
5. Channel Level Matching (dB) – measures the difference in gain between the left and the right channels.
6. Power Supply Rejection Ratio (dB) – PSRR is a measure of ripple attenuation between the power supply pin and an output path. With the signal path idle, a small signal sine wave is summed onto the power supply rail, The amplitude of the sine wave is measured at the output port and expressed as a ratio.
7. All performance measurements carried out with 20kHz AES17 low pass filter for distortion measurements, and an A-weighted filter for noise measurement. Failure to use such a filter will result in higher THD and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.

COMMON TEST CONDITIONS

Unless otherwise stated, the following test conditions apply throughout the following sections:

- DCVDD = 1.0V
- DBVDD = 1.8V
- AVDD = CPVDD =1.8V
- Ambient temperature = +25°C
- Audio signal: 1kHz sine wave, sampled at 48kHz with 24-bit data resolution
- SYSCLK_SRC = 0 (system clock comes direct from MCLK, not from FLL).

Additional, specific test conditions are given within the relevant sections below.

INPUT SIGNAL PATH

PGA and Microphone Boost					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Minimum PGA gain setting	L_MODE/R_MODE= 00b or 01b		-1.55		dB
	L_MODE/R_MODE= 10b		+12		
Maximum PGA gain setting	L_MODE/R_MODE= 00b or 01b		+28.28		dB
	L_MODE/R_MODE= 10b		+30		
Single-ended to differential conversion gain	L_MODE/R_MODE= 00b		+6		dB
PGA gain accuracy	L_MODE/R_MODE= 00b Gain -1.5 to +6.7dB	-1		+1	dB
	L_MODE/R_MODE= 00b Gain +7.5 to +28.3dB	-1.5		+1.5	
	L_MODE/R_MODE= 1X Gain +12 to +24dB	-1		+1	
	L_MODE/R_MODE= 1X Gain +27 to +30dB	-1.5		+1.5	
Mute attenuation	all modes of operation		100		dB
Equivalent input noise	L_MODE/R_MODE= 00b or 01b		30 214		µVrms nV/√Hz

OUTPUT SIGNAL PATH

Stereo Playback to Headphones - DAC input to HPOUTL+HPOUTR pins with 15Ω load
Test conditions: HPOUTL_VOL = HPOUTR_VOL = 111001b (0dB)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Power (per Channel)	P_o	1% THD R_{Load}= 30Ω		28 0.92 -0.76		mW Vrms dBV
		1% THD R_{Load}= 15Ω		32 0.69 -3.19		mW Vrms dBV
DC Offset		DC servo enabled, calibration complete.	-1.5		+1.5	mV
Signal to Noise Ratio	SNR	A-weighted	90	96		dB
Total Harmonic Distortion + Noise	THD+N	R_L=30Ω; P_o=2mW		-91		dB
		R_L=30Ω; P_o=20mW		-84		
		R_L=15Ω; P_o=2mW		-87	-80	
		R_L=15Ω; P_o=20mW		-85		
Channel Separation		1kHz signal, 0dBFS		100		dB
		10kHz signal, 0dBFS		90		
Channel Level Matching		1kHz signal, 0dBFS		+/-1		dB
Power Supply Rejection Ratio	PSRR	217Hz, 100mVpk-pk		75		dB
		1kHz, 100mV pk-pk		70		

Stereo Playback to Line-out - DAC input to LINEOUTL+LINEOUTR pins with 10kΩ / 50pF load

Test conditions: LINEOUTL_VOL = LINEOUTR_VOL = 111001b (0dB)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Full Scale Output Signal Level		DAC 0dBFS output at 0dB volume		1.0 0 2.83		Vrms dBV Vpk-pk
DC offset		DC servo enabled. Calibration complete.	-1.5		+1.5	mV
Signal to Noise Ratio	SNR	A-weighted	90	96		dB
Total Harmonic Distortion + Noise	THD+N	10kΩ load		-85	-70	dB
Channel Separation		1kHz signal, 0dBFS		100		dB
		10kHz signal, 0dBFS		90		
Channel Level Matching		1kHz signal, 0dBFS		+/-1		dB
Power Supply Rejection Ratio	PSRR	217Hz, 100mVpk-pk		62		dB
		1kHz, 100mV pk-pk		62		

Output PGAs (HP, LINE)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Minimum PGA gain setting			-57		dB
Maximum PGA gain setting			6		dB
PGA Gain Step Size			1		dB
PGA gain accuracy	+6dB to -40dB	-1.5		+1.5	dB
	-40dB to -57dB	-1		+1	
Mute attenuation	HPOUTL/R		85		dB
	LINEOUTL/R		85		dB

BYPASS PATH

Differential Stereo Line Input to Stereo Line Output- IN1L-IN2L / IN1R-IN2R pins to LINEOUTL+LINEOUTR pins with 10kΩ / 50pF load

Test conditions:

L_MODE = R_MODE = 01b (Differential Line)

LIN_VOL = RIN_VOL = 00101b (0dB)

LINEOUTL_VOL = LINEOUTR_VOL = 111001b (0dB)

Total signal path gain = 0dB

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Full Scale Output Signal Level				1.0 0 2.83		Vrms dBV Vpk-pk
Signal to Noise Ratio	SNR	A-weighted	90	100		dBV
Total Harmonic Distortion + Noise	THD+N	-1dBV input		-92	-85	dBV
Channel Separation		1kHz signal, -1dBV		90		dB
		10kHz signal, -1dBV		80		
Channel Level Matching		1kHz signal, -1dBV		+/-1		dB
Power Supply Rejection Ratio	PSRR	217Hz, 100mV pk-pk		45		dB

CHARGE PUMP

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up Time			260		µs
CPCA	Normal mode		CPVDD		V
	Low power mode		CPVDD/2		V
CPCB	Normal mode		-CPVDD		V
	Low power mode		-CPVDD/2		V
External component requirements To achieve specified headphone output power and performance					
Flyback Capacitor (between CPCA and CPCB)	at 2V	1	2.2		µF
CPVOUTN Capacitor	at 2V	2	2.2		µF
CPVOUTP Capacitor	at 2V	2	2.2		µF

FLL

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Frequency	F_{REF}	FLL_CLK_REF_DIV = 00	0.032		13.5	MHz
		FLL_CLK_REF_DIV = 01	0.064		27	MHz
Lock time				2		ms
Free-running mode start-up time		VMID enabled		100		µs
Free-running mode frequency accuracy		Reference supplied initially		+/-10		%
		No reference provided		+/-30		%

OTHER PARAMETERS

VMID Reference					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Midrail Reference Voltage (VMIDC pin)		-3%	AVDD/2	+3%	V
Charge up time (from fully discharged to 10% below VMID)	External capacitor 4.7µF		890		µs

Microphone Bias (for analogue electret condenser microphones) Additional test conditions: MICBIAS_ENA=1, all parameters measured at the MICBIAS pin						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Bias Voltage. Note: 7/6 and 9/10 are available only if MICVDD > AVDD. Note: 3/2 and 4/3 are available only if MICVDD ≥ 2.5V.	$V_{MICBIAS}$	MICVDD = 2.5V 3mA load current, MICBIAS_SEL = 1xx	-10%	3/2 x AVDD	+10%	V
		MICBIAS_SEL = 011	-10%	4/3 x AVDD	+10%	
		MICBIAS_SEL = 010	-10%	7/6 x AVDD	+10%	
		MICBIAS_SEL = 001	-10%	10/9 x AVDD	+10%	
		MICBIAS_SEL = 000	-10%	9/10 ×AVDD	+10%	
Drop out voltage between MICVDD and MICBIAS				200		mV
Maximum source current	$I_{MICBIAS}$			4		mA
Noise spectral density		At 1kHz		19		nV/√Hz
Power Supply Rejection Ratio MICVDD to MICBIAS	PSRR	1kHz, 100mV pk-pk MICVDD = 1.71 V		67		dB
		20kHz, 100mV pk-pk MICVDD = 1.71 V		76		
		1kHz, 100mV pk-pk MICVDD = 2.5 V		88		
		20kHz, 100mV pk-pk MICVDD = 2.5 V		84		
		1kHz, 100mV pk-pk MICVDD = 3.6 V		61		
		20kHz, 100mV pk-pk MICVDD = 3.6 V		70		
Power Supply Rejection Ratio MICVDD and AVDD to MICBIAS	PSRR	1kHz, 100mV pk-pk AVDD = MICVDD = 1.8 V		54		dB
		20kHz, 100mV pk-pk AVDD = MICVDD = 1.8 V		79		
MICBIAS Current Detect Function (See Note 1)						
Current Detect Threshold (Microphone insertion)		MICDET_THR = 00			80	µA
Current Detect Threshold (Microphone removal)			60			
Delay Time for Current Detect Interrupt	t_{DET}			3.2		ms
MICBIAS Short Circuit (Hook Switch) Detect Function (See Note 1)						
Short Circuit Detect Threshold (Button press)		MICSHORT_THR = 00			600	µA
Short Circuit Detect Threshold (Button release)			400			
Minimum Delay Time for Short Circuit Detect Interrupt	t_{SHORT}			47		ms

Note:

1. If AVDD ≠ 1.8, current threshold values should be multiplied by (AVDD/1.8)

Digital Inputs / Outputs						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Input HIGH Level (Digital Input)	V_{IH}		0.7×DBVDD			V
Input LOW Level (Digital Input)	V_{IL}				0.3×DBVDD	V
Input HIGH Level (Analogue / Digital Input)	V_{IH}		0.7×AVDD			V
Input LOW Level (Analogue / Digital Input)	V_{IL}				0.3×AVDD	V
Output HIGH Level	V_{OH}	I_{OH} = +1mA	0.9×DBVDD			V
Output LOW Level	V_{OL}	I_{OL} = -1mA			0.1×DBVDD	V

POWER CONSUMPTION

The WM8918 power consumption is dependent on many parameters. Most significantly, it depends on supply voltages, sample rates, mode of operation, and output loading.

The power consumption on each supply rail varies approximately with the square of the voltage. Power consumption is greater at fast sample rates than at slower ones. When the digital audio interface is operating in Master mode, the DBVDD current is significantly greater than in Slave mode. (Note also that power savings can be made by using MCLK as the BCLK source in Slave mode.) The output load conditions (impedance, capacitance and inductance) can also impact significantly on the device power consumption.

COMMON TEST CONDITIONS

Unless otherwise stated, the following test conditions apply throughout the following sections:

- Ambient temperature = +25°C
- Audio signal = quiescent (zero amplitude)
- Sample rate = 48kHz
- MCLK = 12.288MHz
- Audio interface mode = Slave (LRCLK_DIR=0, BCLK_DIR=0)
- SYSCLK_SRC = 0 (system clock comes direct from MCLK, not from FLL)

Additional, variant test conditions are quoted within the relevant sections below. Where applicable, power dissipated in the headphone or line loads is included.

POWER CONSUMPTION MEASUREMENTS

Stereo Playback to Headphones - DAC input to HPOUTL+HPOUTR pins with 30Ω load.
Test conditions:
VMID_RES = 01 (for normal operation)
CP_DYN_PWR = 1 (Class-W, Charge pump controlled by real-time audio level)

Variant test conditions	AVDD		DCVDD		DBVDD		CPVDD		MICVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	V	mA	mW
48kHz sample rate	1.80	1.69	1.00	0.76	1.80	0.00	1.80	0.31	2.50	0.01	4.38
8kHz sample rate	1.80	1.69	1.00	0.18	1.80	0.00	1.80	0.31	2.50	0.01	3.80
48kHz, Po = 0.1mW/channel 1kHz sine wave 0dBFS HPOUT_VOL= -25dB DAC_VOL= 0dB	1.80	1.71	1.00	0.77	1.80	0.00	1.80	1.99	2.50	0.01	7.45
48kHz, Po = 1mW/channel 1kHz sine wave 0dBFS HPOUT_VOL= -15dB DAC_VOL= 0dB	1.80	1.73	1.00	0.77	1.80	0.00	1.80	5.61	2.50	0.01	13.99
48kHz sample rate, Master mode, FLL enabled, MCLK input frequency = 13MHz	1.80	1.82	1.00	1.05	1.80	0.73	1.80	0.30	2.50	0.01	6.18
48kHz sample rate, Master mode, FLL enabled, MCLK input frequency = 32.768kHz	1.80	1.83	1.00	0.94	1.80	0.76	1.80	0.29	2.50	0.01	6.14

Stereo Playback to Line-out - DAC input to LINEOUTL+LINEOUTR or HPOUTL+HPOUTR pins with 10kΩ / 50pF load

Test conditions:

VMID_RES = 01 (for normal operation)

CP_DYN_PWR = 1 (Class-W, Charge pump controlled by real-time audio level)

Variant test conditions	AVDD		DCVDD		DBVDD		CPVDD		MICVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	V	mA	mW
48kHz sample rate	1.8	1.67	1	0.76	1.8	0.00	1.8	0.36	2.5	0.01	4.43
8kHz sample rate	1.8	1.67	1	0.18	1.8	0.00	1.8	0.36	2.5	0.01	3.86
48kHz, Po = 0dBFS 1kHz sine wave	1.8	1.78	1	0.77	1.8	0.00	1.8	2.27	2.5	0.01	8.09

Stereo analogue bypass to headphones - IN1L/R or IN2L/R pins to HPOUTL+HPOUTR pins with 30Ω load.

Test conditions:

LIN_VOL = RIN_VOL = 00101 = +0.0 dB

MCLK = 11.2896MHz

Digital audio interface disabled

Note that the Analogue bypass configuration does not benefit from the Class W dynamic control.

Variant test conditions	AVDD		DCVDD		DBVDD		CPVDD		MICVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	V	mA	mW
Quiescent HPOUTVOL = 000000 (-57dB)	1.8	1.24	1	0.11	1.8	0.00	1.8	0.26	2.5	0.01	2.82
Po = 0.1mW/channel 1kHz sine wave HPOUTVOL = 100000 (-25dB)	1.8	1.29	1	0.11	1.8	0.00	1.8	2.05	2.5	0.01	6.13
Po = 1mW/channel 1kHz sine wave HPOUTVOL = 101010 (-15dB)	1.8	1.30	1	0.11	1.8	0.00	1.8	5.86	2.5	0.01	13.02

Stereo analogue bypass to Line-out - IN1L/R or IN2L/R pins to LINEOUTL+LINEOUTR pins with 30Ω load.

Test conditions:

LIN_VOL = RIN_VOL = 00101 = +0.0 dB

MCLK = 11.2896MHz

Digital audio interface disabled

Note that the Analogue bypass configuration does not benefit from the Class W dynamic control.

Variant test conditions	AVDD		DCVDD		DBVDD		CPVDD		MICVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	V	mA	mW
Quiescent LINEOUTVOL = 000000 (-57dB)	1.8	1.04	1.0	0.15	1.8	0.00	1.8	0.21	1.8	0.01	2.41
Quiescent LINEOUTVOL = 101011 (-14dB)	1.8	1.04	1.0	0.15	1.8	0.00	1.8	0.63	1.8	0.01	3.18
Quiescent LINEOUTVOL = 111001 (0dB)	1.8	1.04	1.0	0.15	1.8	0.00	1.8	1.25	1.8	0.01	4.28

Off

Note: DC servo calibration is retained in this state as long as DCVDD is supplied. This allows fast, pop suppressed start-up from the off state.

Variant test conditions	AVDD		DCVDD		DBVDD		CPVDD		MICVDD		TOTAL
	V	mA	V	mA	V	mA	V	mA	V	mA	mW
Off (default settings) No Clocks applied	1.8	0.01	1	0.00	1.8	0.00	1.8	0.01	2.5	0.01	0.04
Off (default settings) AIFRXDAT, MCLK, BCLK, and LRCLK applied	1.8	0.01	1	0.02	1.8	0.00	1.8	0.01	2.5	0.01	0.06

SIGNAL TIMING REQUIREMENTS

COMMON TEST CONDITIONS

Unless otherwise stated, the following test conditions apply throughout the following sections:

- Ambient temperature = +25°C
- DCVDD = 1.0V
- DBVDD = AVDD = CPVDD = 1.8V
- DGND = AGND = CPGND = 0V

Additional, specific test conditions are given within the relevant sections below.

MASTER CLOCK

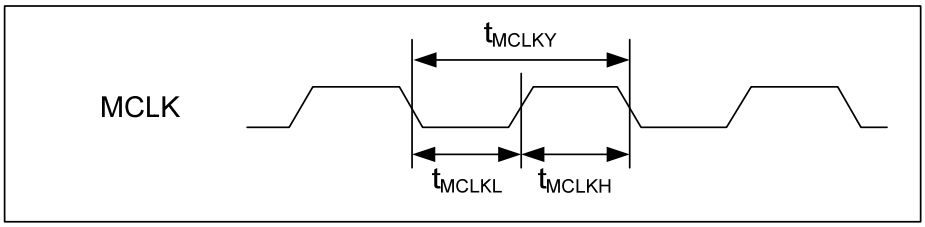


Figure 1 Master Clock Timing

Master Clock Timing						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
MCLK cycle time	T_{MCLKY}	MCLK_DIV=1	40			ns
		MCLK_DIV=0	80			ns
MCLK duty cycle	T_{MCLKDS}		60:40		40:60	

AUDIO INTERFACE TIMING

MASTER MODE

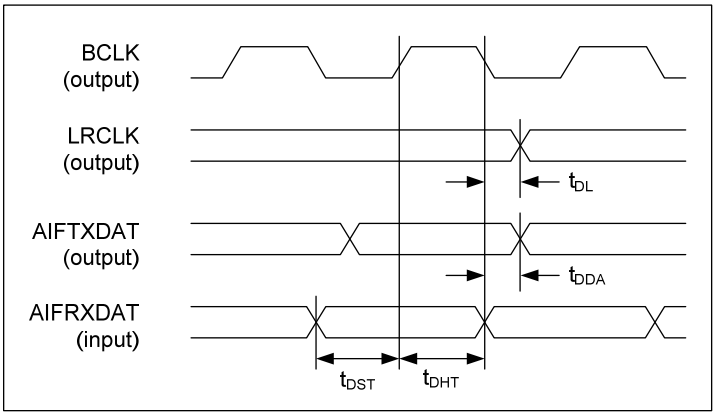


Figure 2 Audio Interface Timing – Master Mode

Test Conditions

DCVDD = 1.0V, AVDD = DBVDD = CPVDD = 1.8V, DGND=AGND=CPGND =0V, T_A = +25°C, Master Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Master Mode					
LRCLK propagation delay from BCLK falling edge	t_{DL}			20	ns
AIFTXDAT propagation delay from BCLK falling edge	t_{DDA}			20	ns
AIFRXDAT setup time to BCLK rising edge	t_{DST}	20			ns
AIFRXDAT hold time from BCLK rising edge	t_{DHT}	10			ns

SLAVE MODE

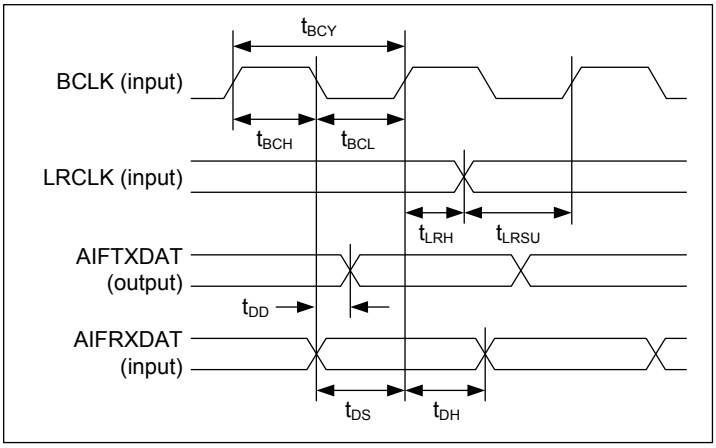


Figure 3 Audio Interface Timing – Slave Mode

Test Conditions

DCVDD = 1.0V, AVDD = DBVDD = CPVDD = 1.8V, DGND=AGND=CPGND =0V, T_A = +25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Slave Mode					
BCLK cycle time	t_{BCY}	50			ns
BCLK pulse width high	t_{BCH}	20			ns
BCLK pulse width low	t_{BCL}	20			ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}	20			ns
LRCLK hold time from BCLK rising edge	t_{LRH}	10			ns
AIFRXDAT hold time from BCLK rising edge	t_{DH}	10			ns
AIFTXDAT propagation delay from BCLK falling edge	t_{DD}			20	ns
AIFRXDAT set-up time to BCLK rising edge	t_{DS}	20			ns

Note: BCLK period must always be greater than or equal to MCLK period.

TDM MODE

In TDM mode, it is important that two devices do not attempt to drive the AIFTXDAT pin simultaneously. The timing of the WM8918 AIFTXDAT tri-stating at the start and end of the data transmission is described below.

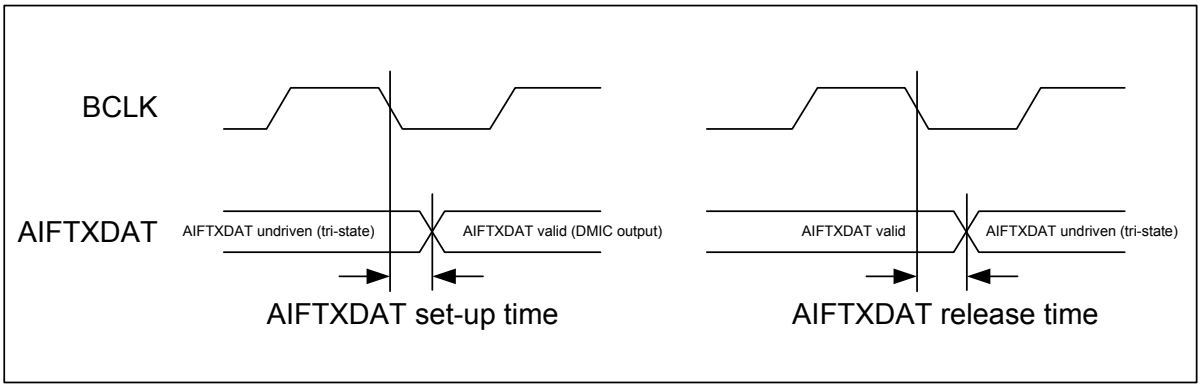


Figure 4 Audio Interface Timing - TDM Mode

Test Conditions

AVDD = CPVDD = 1.8V , DGND=AGND=CPGND= =0V, T_A = +25°C, Master Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Timing Information					
AIFTXDAT setup time from BCLK falling edge	DCVDD =2.0V DBVDD = 3.6V		5		ns
	DCVDD = 1.08V DBVDD = 1.62V		15		ns
AIFTXDAT release time from BCLK falling edge	DCVDD = 2.0V DBVDD = 3.6V		5		ns
	DCVDD = 1.08V DBVDD = 1.62V		15		ns

CONTROL INTERFACE TIMING

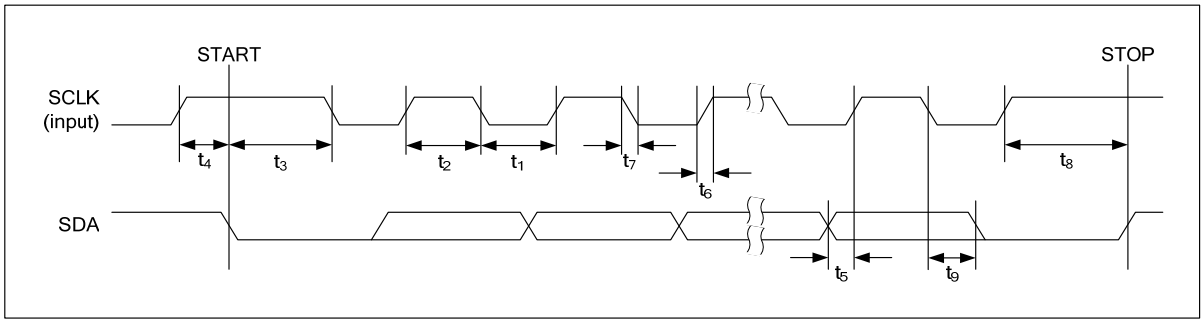


Figure 5 Control Interface Timing

Test Conditions

DCVDD = 1.0V, AVDD = DBVDD = CPVDD = 1.8V, DGND=AGND=CPGND =0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SCLK Frequency				400	kHz
SCLK Low Pulse-Width	t_1	1300			ns
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDA, SCLK Rise Time	t_6			300	ns
SDA, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Microphone (DMIC) Filter					
Passband	+/- 0.05dB	0		0.454 fs	
	-6dB		0.5 fs		
Passband Ripple				+/- 0.05	dB
Stopband		0.546 fs			
Stopband Attenuation	f > 0.546 fs	-60			dB
DAC Normal Filter					
Passband	+/- 0.05dB	0		0.454 fs	
	-6dB		0.5 fs		
Passband Ripple	0.454 fs			+/- 0.03	dB
Stopband		0.546 fs			
Stopband Attenuation	f > 0.546 fs	-50			dB
DAC Sloping Stopband Filter					
Passband	+/- 0.03dB	0		0.25 fs	
	+/- 1dB	0.25 fs		0.454 fs	
	-6dB		0.5 fs		
Passband Ripple	0.25 fs			+/- 0.03	dB
Stopband 1		0.546 fs		0.7 fs	
Stopband 1 Attenuation	f > 0.546 fs	-60			dB
Stopband 2		0.7 fs		1.4 fs	
Stopband 2 Attenuation	f > 0.7 fs	-85			dB
Stopband 3		1.4 fs			
Stopband 3 Attenuation	F > 1.4 fs	-55			dB

DAC FILTERS		DMIC FILTERS	
Mode	**Group Delay**	**Mode**	**Group Delay**
Normal	16.5 / fs	Normal	16.5 / fs
Sloping Stopband	18 / fs		

TERMINOLOGY

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region

DMIC FILTER RESPONSES

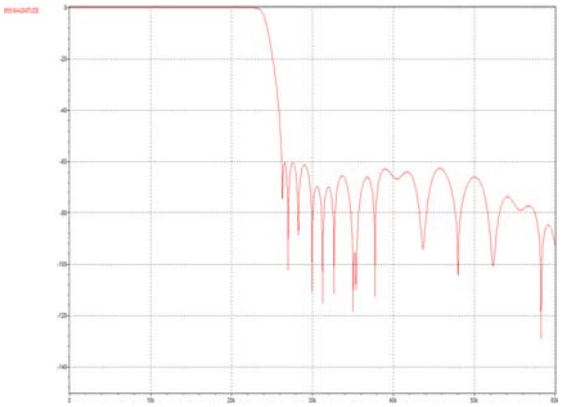


Figure 6 DMIC Digital Filter Frequency Response

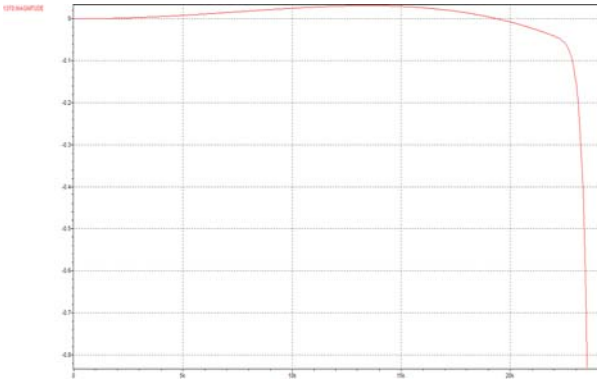


Figure 7 DMIC Digital Filter Ripple

DMIC HIGH PASS FILTER RESPONSES

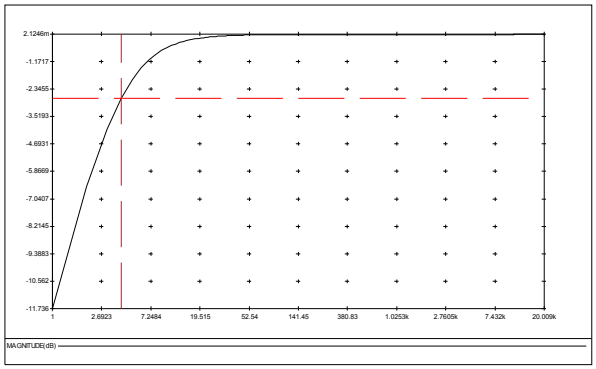


Figure 8 DMIC Digital High Pass Filter Frequency Response (48kHz, Hi-Fi Mode, DMIC_HPF_CUT[1:0]=00)

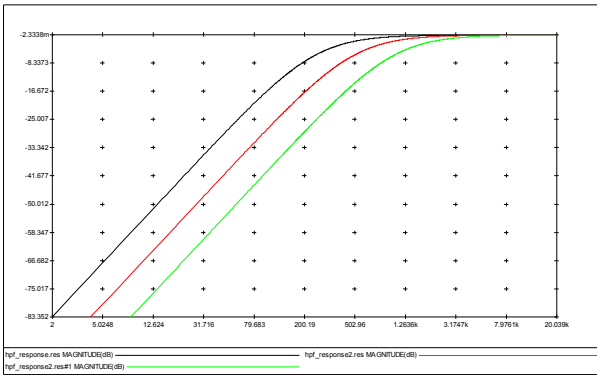


Figure 9 DMIC Digital High Pass Filter Ripple (48kHz, Voice Mode, DMIC_HPF_CUT=01, 10 and 11)

DAC FILTER RESPONSES

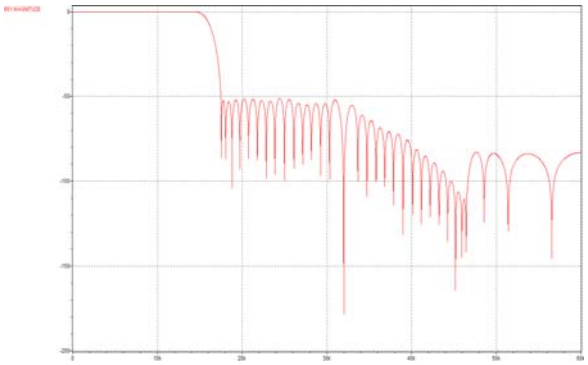


Figure 10 DAC Digital Filter Frequency Response; (Normal Mode); Sample Rate > 24kHz

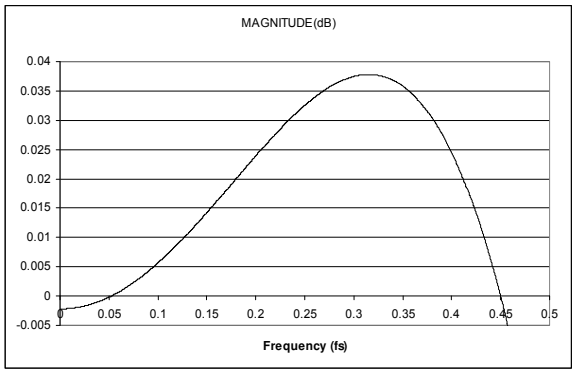


Figure 11 DAC Digital Filter Ripple (Normal Mode)

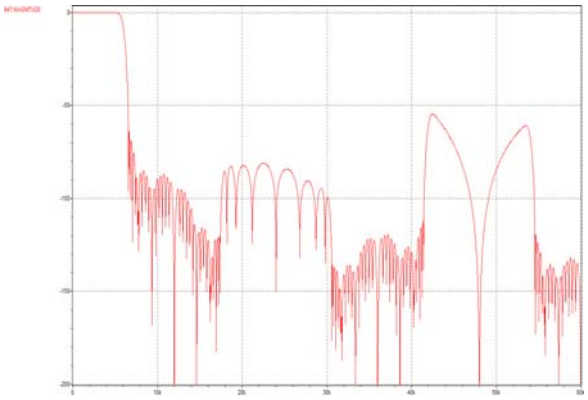


Figure 12 DAC Digital Filter Frequency Response; (Sloping Stopband Mode); Sample Rate <= 24kHz

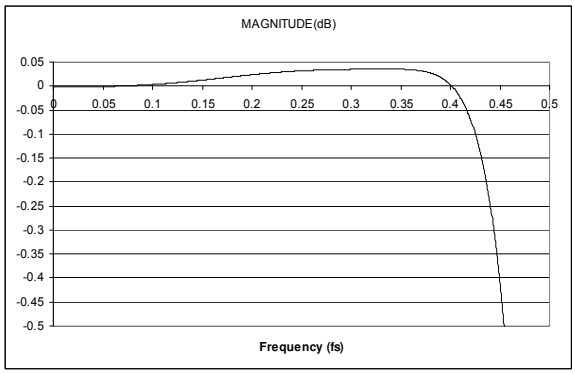


Figure 13 DAC Digital Filter Ripple (Sloping Stopband Mode)