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WM8944B

Mono Low-Power CODEC with Video Buffer

DESCRIPTION

The WM8944B is a highly integrated low power hi-fi CODEC designed for portable devices such as digital still cameras.

Up to 2 analogue inputs may be connected; a stereo digital microphone interface is also provided. Flexible output mixing options support single-ended and differential configurations, with outputs derived from the digital audio paths or from analogue bypass paths. Mono line output and mono BTL headphone/speaker drive is supported.

Flexible digital mixing and powerful DSP functions are available. Programmable filters and other processes may be applied to the ADC and DAC signal paths simultaneously. The DSP functions include 5 notch filters, 5-band EQ, dynamic range control and the ReTune™ feature.

The ReTune™ feature is a sophisticated digital filter that can compensate for imperfect characteristics of the housing, loudspeaker or microphone components in an application. The ReTune algorithm can provide acoustic equalisation and selective phase (delay) control of specific frequency bands.

The WM8944B is controlled via a I2C or SPI interface. Additional functions include Digital beep generator, Video buffer, programmable GPIO functions, Frequency Locked Loop (FLL) for flexible clocking support and integrated LDO for low noise supply regulation.

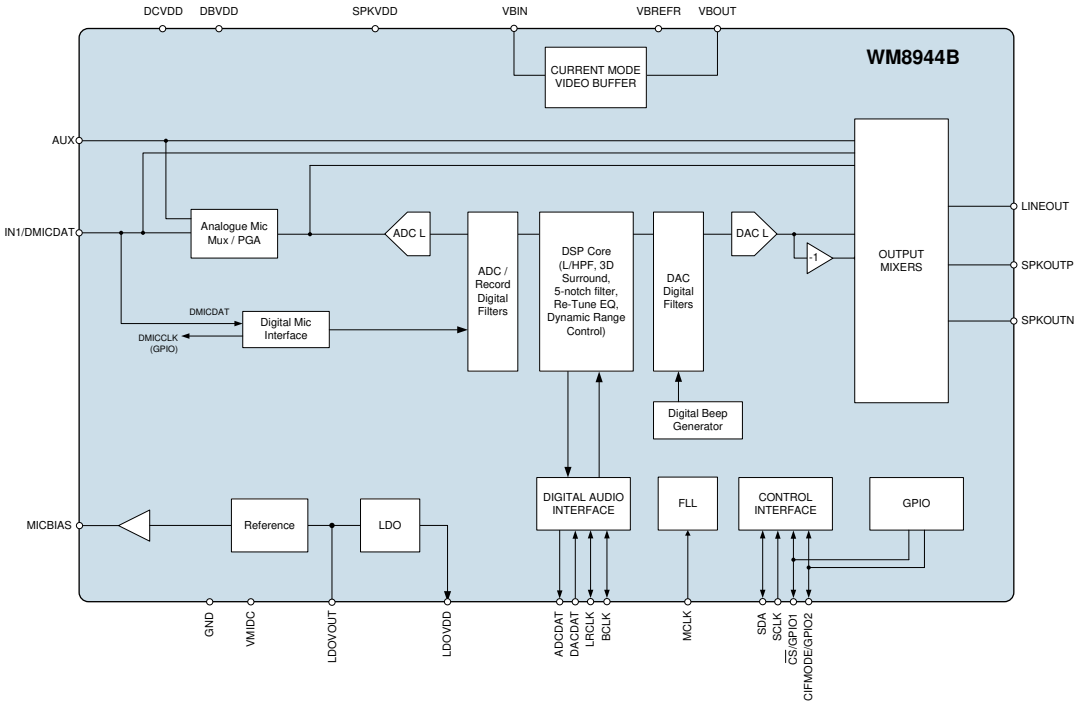
The WM8944B is supplied in 25-ball W-CSP package, ideal for portable systems.

FEATURES

- Hi-fi audio CODEC
  - 94dB SNR during ADC recording ('A' weighted)
  - 96dB SNR during DAC playback ('A' weighted)
- 2 analogue audio inputs
- Integrated bias reference for electret microphones
- Digital microphone interface (Stereo)
- Powerful digital mixing / DSP functions:
  - 5-notch filters
  - 5-band equalizer (EQ)
  - ReTune™ parametric filter
  - Dynamic range control and noise gate
  - Low-pass/High-pass filters
  - Direct Form 1 (DF1) programmable digital filter
  - 3D stereo enhancement (for digital mic input)
- Digital beep generator
- Mono line output
- Mono BTL headphone/speaker output driver
- I2S digital audio interface - sample rates 8kHz to 48kHz
- Frequency Locked Loop (FLL) frequency conversion / filter
- Video buffer function
- Integrated LDO low-noise voltage regulator
- 25-ball W-CSP package (2.41 x 2.41 x 0.55mm, 0.5mm pitch)

APPLICATIONS

- Digital Still Cameras (DSC)
- Multimedia phones



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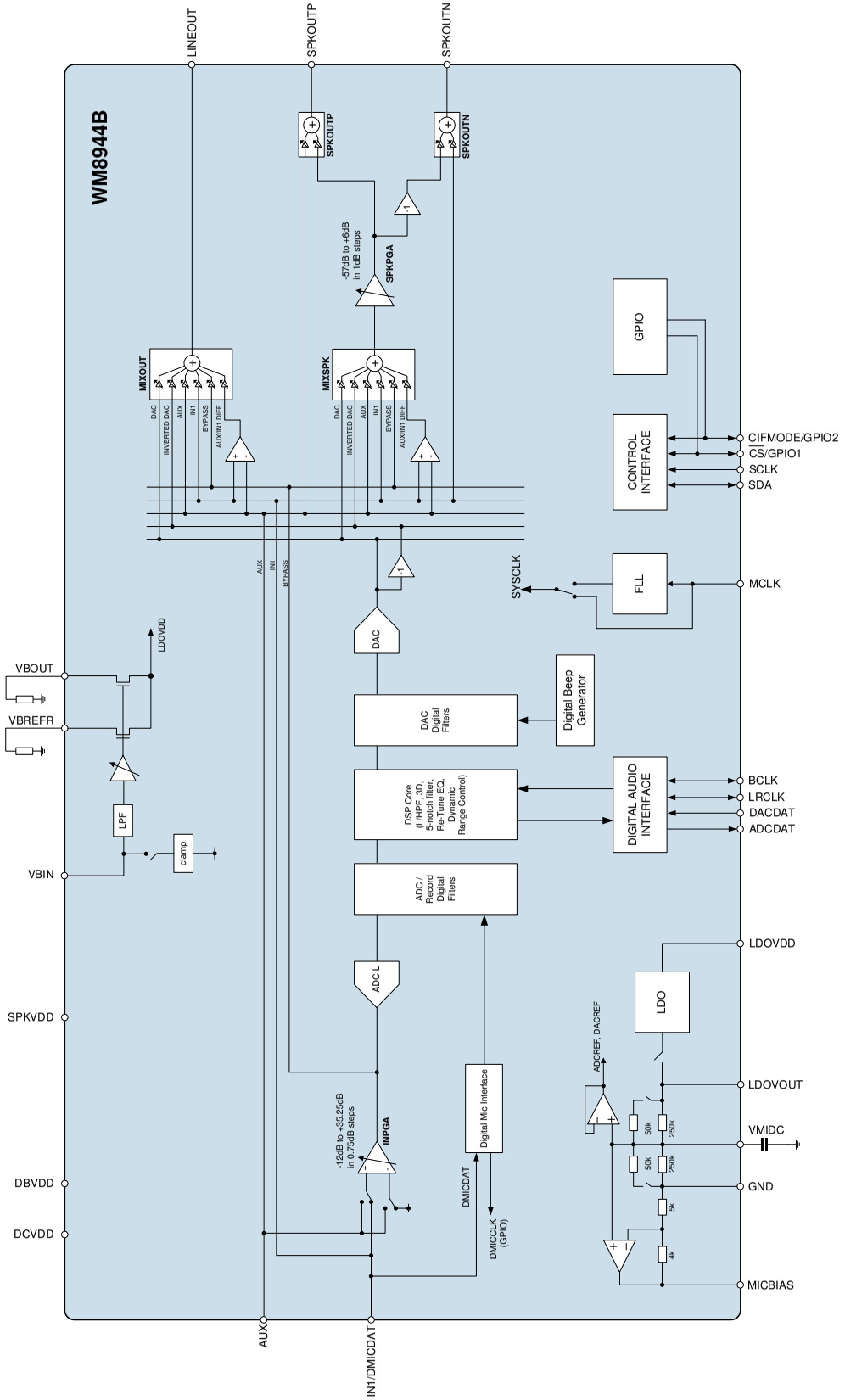
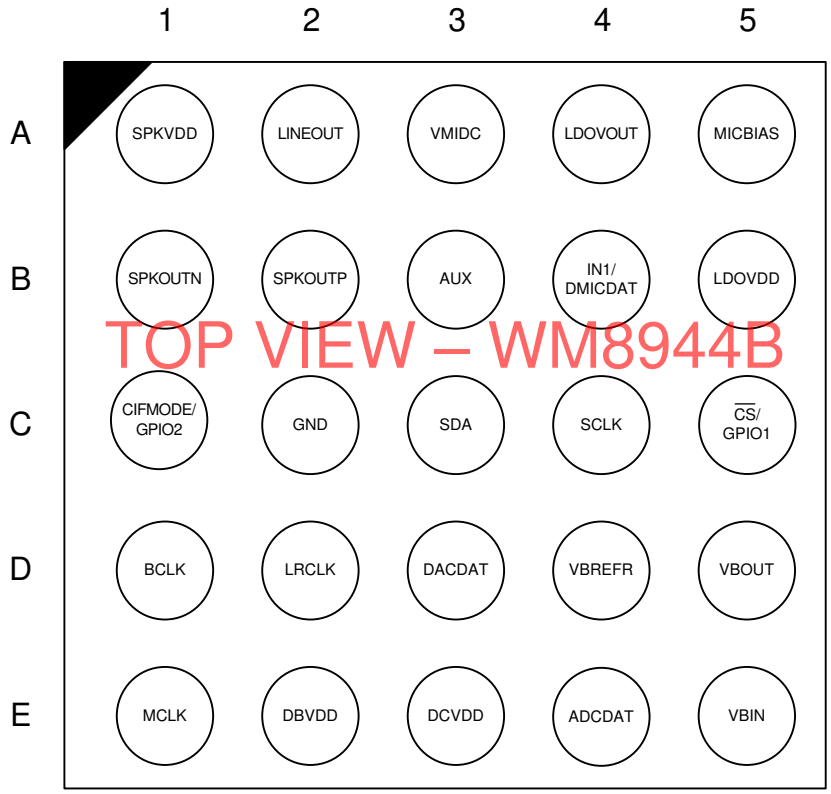
BLOCK DIAGRAM



PIN CONFIGURATION

The WM8944B is supplied in a 25-ball CSP format. The pin configuration is illustrated below, showing the top-down view from above the chip.



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8944BECS/R	-40°C to +85°C	25-ball W-CSP (Pb-free, tape and reel)	MSL1	260°C

Note:
Reel quantity = 3500

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
A1	SPKVDD	Supply	Supply for speaker driver
A2	LINEOUT	Analogue Output	Line mixer output
A3	VMIDC	Analogue Output	Midrail voltage decoupling capacitor
A4	LDOVOUT	Supply	LDO output voltage
A5	MICBIAS	Analogue Output	Microphone bias output voltage
B1	SPKOUTN	Analogue Output	Negative speaker mixer output
B2	SPKOUTP	Analogue Output	Positive speaker mixer output
B3	AUX	Analogue Input	Aux audio input
B4	IN1/DMICDAT	Analogue Input / Digital Input	Analogue input / Digital Microphone data input
B5	LDOVDD	Supply	LDO supply input
C1	CIFMODE/GPIO2	Digital Input / Output	Control interface mode select / GPIO2
C2	GND	Supply	Ground
C3	SDA	Digital Input / Output	Control interface data input / output
C4	SCLK	Digital Input	Control interface clock input
C5	CS/GPIO1	Digital Input / Output	3-wire (SPI) Control Mode Chip Select / GPIO1
D1	BCLK	Digital Input / Output	Audio interface bit clock
D2	LRCLK	Digital Input / Output	Audio interface left / right clock
D3	DACDAT	Digital Input	DAC digital audio data input
D4	VBREFR	Analogue Output	Video buffer current reference resistor connection
D5	VBOUT	Analogue Output	Video buffer output
E1	MCLK	Digital Input	Master clock input
E2	DBVDD	Supply	Digital buffer (I/O) supply
E3	DCVDD	Supply	Digital core supply
E4	ADCDAT	Digital Output	ADC / Digital Microphone digital audio data output
E5	VBIN	Analogue Input	Video buffer input

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus Logic tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (DCVDD)	-0.3V	2.5V
Supply voltages (LDOVDD, DBVDD, SPKVDD)	-0.3V	4.5V
Voltage range digital inputs	-0.7V	DBVDD +0.7V
Voltage range analogue inputs	-0.7V	LDOVDD +0.7V
Operating temperature range, T_A	-40ºC	+85ºC
Junction temperature, T_{JMAX}	-40ºC	+150ºC
Storage temperature after soldering	-65ºC	+150ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD	1.62	1.8	1.98	V
Digital supply range (I/O)	DBVDD	1.62	3.3	3.6	V
Analogue supply	LDOVDD	2.4	3.3	3.6	V
Speaker supply range	SPKVDD	1.71	3.3	3.6	V
Ground	GND		0		V

THERMAL PERFORMANCE

Thermal analysis should be performed in the intended application to prevent the WM8944B from exceeding maximum junction temperature. Several contributing factors affect thermal performance most notably the physical properties of the mechanical enclosure, location of the device on the PCB in relation to surrounding components and the number of PCB layers. Connecting the GND balls through thermal vias and into a large ground plane will aid heat extraction.

Three main heat transfer paths exist to surrounding air as illustrated below in Figure 1:

- Package top to air (radiation).
- Package bottom to PCB (radiation).
- Package balls to PCB (conduction).

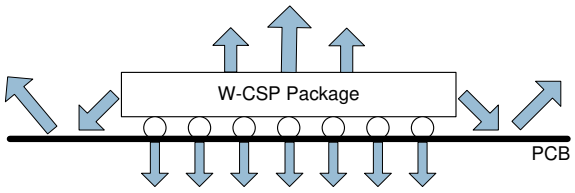


Figure 1 Heat Transfer Paths

The temperature rise T_R is given by $T_R = P_D * \Theta_{JA}$

P_D is the power dissipated in the device.

Θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature and is therefore a measure of heat transfer from the die to surrounding air. Θ_{JA} is determined with reference to JEDEC standard JESD51-9.

The junction temperature T_J is given by $T_J = T_A + T_R$, where T_A is the ambient temperature.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Operating temperature range	T_A	-40		85	°C
Operating junction temperature	T_J	-40		125	°C
Thermal Resistance (Junction to Board)	Θ_{JB}		26		°C/W
Thermal Resistance (Junction to Ambient)	Θ_{JA}		70		°C/W

Note:

1. Junction temperature is a function of ambient temperature and of the device operating conditions. The ambient temperature limits and junction temperature limits must both be observed.

ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD = 1.8V, DBVDD = LDOVDD = SPKVDD = 3.3V, LDOVOUT = 3.0V, GND = 0V,
T_A = +25ºC, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (IN1, AUX)						
Maximum input signal level (changes in proportion to LDOVOUT)		Single-ended input INPGA_VOL = 0dB		1.0 0		Vrms dBV
		Pseudo-differential input INPGA_VOL = 0dB		0.7 -3.1		Vrms dBV
Input resistance (IN1/DMICDAT)		Input PGA path (+35.25dB)		4.5		kΩ
		Input PGA path (0dB)		105		
		Input PGA path (-12dB)		160		
		Output mixer path (0dB)		15		
		Output mixer path (-6dB)		30		
		Direct speaker (0dB)		10		
		Direct speaker (-6dB)		20		
Input resistance (AUX)		Input PGA path (All gain settings)		96		kΩ
Input capacitance				10		pF
Analogue Inputs Programmable Gain Amplifier (PGA)						
Minimum programmable gain				-12		dB
Maximum programmable gain				35.25		dB
Gain step size		Guaranteed monotonic		0.75		dB
Mute attenuation				92		dB
Common Mode Rejection Ratio		1kHz input		110		dB
Speaker Output Programmable Gain Amplifier (PGA)						
Minimum programmable gain				-57		dB
Maximum programmable gain				6		dB
Gain step size		Guaranteed monotonic		1		dB
Mute attenuation				71		dB
ADC Input Path Performance (Input PGA to ADC)						
SNR (A-weighted)			84	94		dB
THD		-1dBFS input		-83	-72	dB
THD+N		-1dBFS input		-77	-70	dB
PSRR (with respect to LDOVDD)		217Hz, 100mV pk-pk		77		dB
		1kHz, 100mV pk-pk		90		

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Bypass to Line Output (IN1/AUX to LINEMIX Differential Input to LINEOUT, 10kΩ / 50pF)						
SNR (A-weighted)		INPGA_VOL = 0dB	90	98		dB
THD+N		INPGA_VOL = 0dB		-89.5	-80	dB
Bypass to Speaker Output (IN1/AUX to SPKMIX Differential Input to SPKOUTP/SPKOUTN, 8R BTL)						
SNR (A-weighted)		SPKVOL = 0dB	90	96		dB
THD+N		SPKVOL = 0dB		-75	-65	dB
DAC Output Path Performance (DAC to LINEOUT, 10kΩ / 50pF)						
Maximum output signal level (changes in proportion to LDOVOUT)				1		Vrms
SNR (A-weighted)			85	96		dB
THD				-80	-71	dB
THD+N				-78	-70	dB
Mute attenuation				125		dB
PSRR (with respect to LDOVDD)		217Hz, 100mV pk-pk		48		dB
		1kHz, 100mV pk-pk		60		
Line Output Resistance				10		kΩ
Line Output Capacitance				50		pF
DAC Output Path Performance (DAC to SPKOUTP or SPKOUTN, 10kΩ / 50pF)						
Maximum output signal level (changes in proportion to LDOVOUT)				1		Vrms
SNR (A-weighted)			85	96		dB
THD				-78	-68	dB
THD+N				-76	-66	dB
Speaker Output Performance (Speaker Output SPKOUTP/SPKOUTN, 8Ω BTL)						
SNR (A-weighted)			90	96		dB
THD		P_O=150mW		0.03 -68		% dB
		P_O=350mW		2.944 -30.6		% dB
THD+N		P_O=150mW		0.05 -66		% dB
		P_O=350mW		3.72 -28.6		% dB
Mute attenuation				92		dB
PSRR (with respect to LDOVDD)		217Hz		48		dB
		1kHz		60		
PSRR (with respect to SPKVDD)		217Hz, 100mV pk-pk		89		dB
		1kHz, 100mV pk-pk		79		
Speaker Resistance				8		Ω
Speaker Capacitance				50		pF

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Inputs/Outputs						
Input high level			0.7×DBVDD			V
Input low level					0.3×DBVDD	V
Output high level		I_{OL} = 1mA	0.8×DBVDD			V
Output low level		I_{OH} = -1mA			0.2×DBVDD	V
Input capacitance				10		pF
Input leakage		All digital pins except CIFMODE	-900		900	nA
		CIFMODE pin	-90		90	uA
LDO Regulator						
Input voltage	LDOVDD		2.4	3.3	3.6	V
Output voltage	LDOVOUT	LDO_REF_SEL = 0		3.0		V
Dropout Voltage	LDOVDD-LDOVOUTLDOVDD - LDOVOUT	I_{LOAD}=50mA, LDOVOUT>2.4V		200		mV
		I_{LOAD}=50mA, LDOVOUT≤2.4V		400		mV
Maximum output current (see note)				50		mA
Output voltage accuracy		I_{LOAD} = 50mA		2		%
Quiescent current		No Load		55		µA
Leakage current				1		µA
PSRR (with respect to LDOVDD)		217Hz, 100mV pk-pk		40		dB
		1kHz, 100mV pk-pk		49		
Video Buffer						
Maximum output voltage swing	Vom	f=100kHz, THD=1%	1.10	1.25	1.50	V pk-pk
Voltage gain	Av	VB_GAIN = 1, R_{REF}=187Ω, R_{LOAD}=75Ω, R_{SOURCE}=75Ω	5.08	6	7.94	dB
		VB_GAIN = 0, R_{REF}=187Ω, R_{LOAD}=75Ω, R_{SOURCE}=75Ω	-0.92	0	1.94	dB
Gain step size				6		dB
Differential gain	DG	Vin = 1V pk-pk	-2.0	0.3	+2.0	%
Differential phase	DP	Vin = 1V pk-pk	-2.0	0	+2.0	Deg
SNR	VSNR		40	60	100	dB
SYNC tip offset above GND		VB_PD = 0 VB_GAIN = 1 (+6dB)	0	40	75	mV
Third order Low Pass Filter response (referenced to 100kHz) R_{REF}=187Ω, R_{LOAD}=75Ω, R_{SOURCE}=75Ω, 0dB gain		2.4MHz	-0.5	0	0.5	dB
		5.13MHz	-0.5	-0.2	0.5	dB
		9.04MHz	-3.0	-1.6	0	dB
		13.32MHz	-11.0	-7.0	-3.0	dB
PSRR (with respect to LDOVDD)	PSRR	100kHz, 50mV pk-pk		60		dB
Clocking						
MCLK frequency			30Hz		27MHz	Hz
FLL output frequency			2.045		50	MHz
FLL lock time				2		ms

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MICBIAS						
Bias voltage (changes in proportion to LDOVOUT)	MICBIAS	MICB_LVL = 0	2.55	2.7	2.85	V
		MICB_LVL = 1		1.95		V
Bias Current source		$V_{MICBIAS}$ within +/-3%			3	mA
Output noise spectral density		1kHz to 20kHz		40		nV/√Hz
PSRR (with respect to LDOVDD)		217Hz, 100mV pk-pk		70		dB
		1kHz, 100mV pk-pk		85		
Bandgap Reference						
Bandgap Voltage			-10%	1.5	+10%	V
Analogue Reference Levels						
Midrail Reference Voltage (changes in proportion to LDOVOUT)	VMID	VMID_REF_SEL = 1 VMID_CTRL=1		1.5		V
Bandgap Reference		BG_VSEL=01010	-10%	1.5	+10%	V

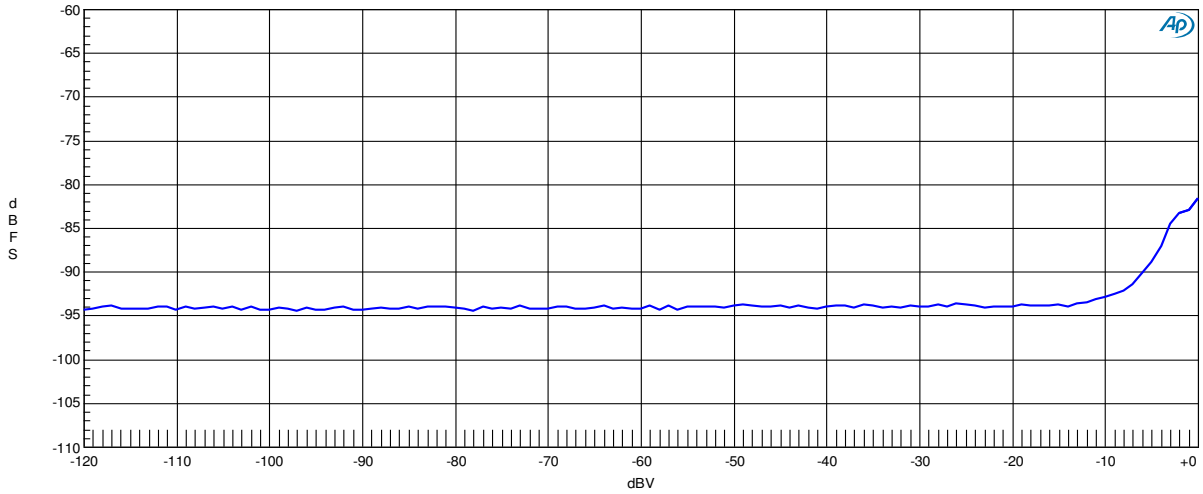
Note:
The maximum LDO output current is the total internal and external load capability; internal circuits of the WM8944B will typically account for 25mA of this capacity.

TERMINOLOGY

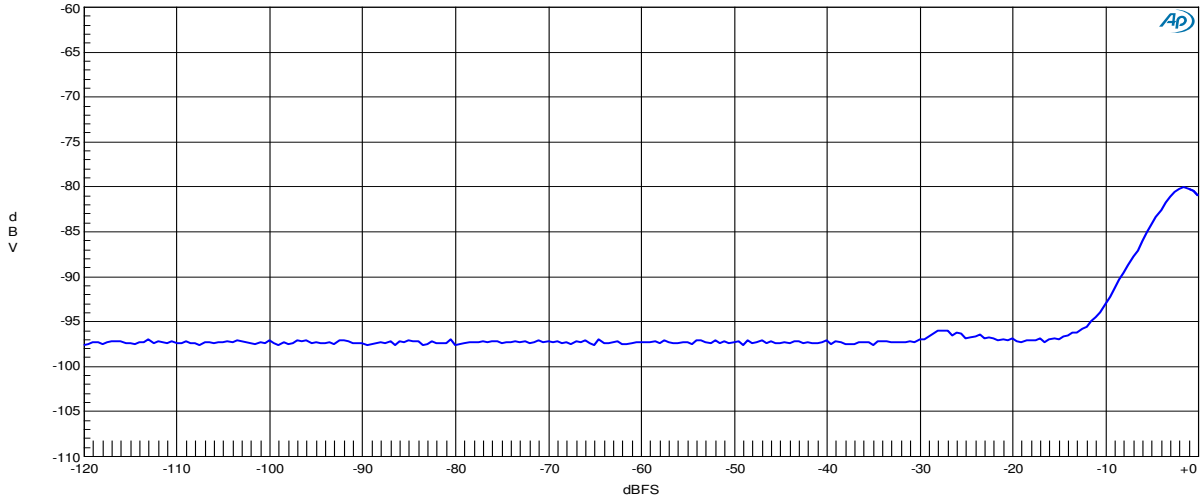
1. Signal-to-Noise Ratio (dB) – SNR is the difference in level between a full scale output signal and the device output noise with no signal applied, measured over a bandwidth of 20Hz to 20kHz. This ratio is also called idle channel noise. (No Auto-zero or Mute function is employed).
2. Total Harmonic Distortion (dB) – THD is the difference in level between a 1kHz reference sine wave output signal and the first seven harmonics of the output signal. The amplitude of the fundamental frequency of the output signal is compared to the RMS value of the next seven harmonics and expressed as a ratio.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the difference in level between a 1kHz reference sine wave output signal and all noise and distortion products in the audio band. The amplitude of the fundamental reference frequency of the output signal is compared to the RMS value of all other noise and distortion products and expressed as a ratio.
4. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.
5. Power Supply Rejection Ratio (dB) – PSRR is a measure of ripple attenuation between a power supply rail and a signal output path. With the signal path idle, a small sine wave ripple is applied to power supply rail. The amplitude of the supply ripple is compared to the amplitude of the output signal generated and is expressed as a ratio.
6. All performance measurements are carried out with 20kHz AES17 low pass filter for distortion measurements, and an A-weighted filter for noise measurement. Failure to use such a filter will result in higher THD and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out-of-band noise; although it is not audible, it may affect dynamic specification values.

TYPICAL PERFORMANCE

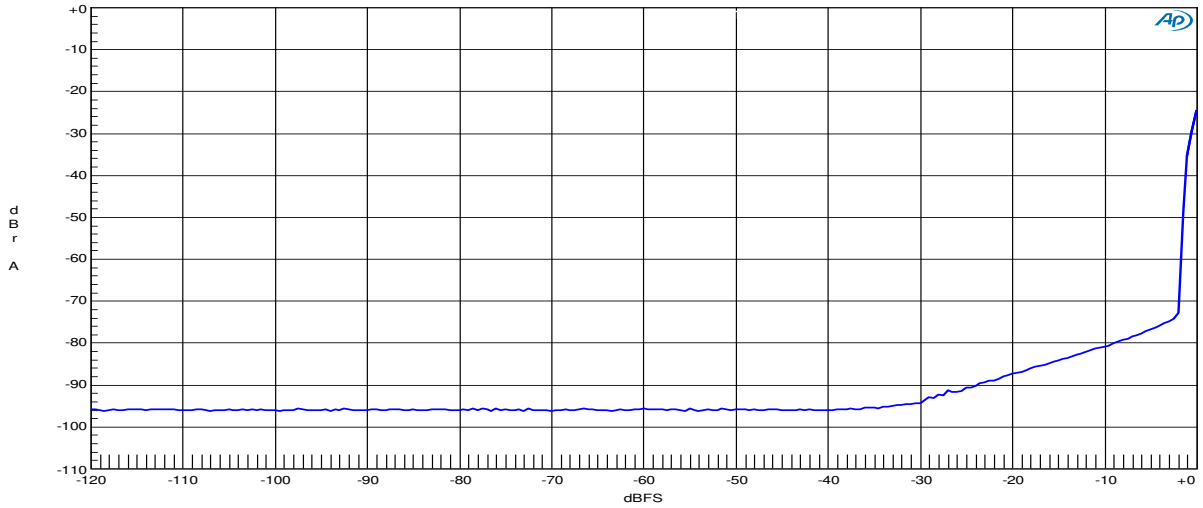
WM8944B_IN1_ADC_THD+NvsAmpl



WM8944B_DAC_Lineout_THD+NvsAmpl



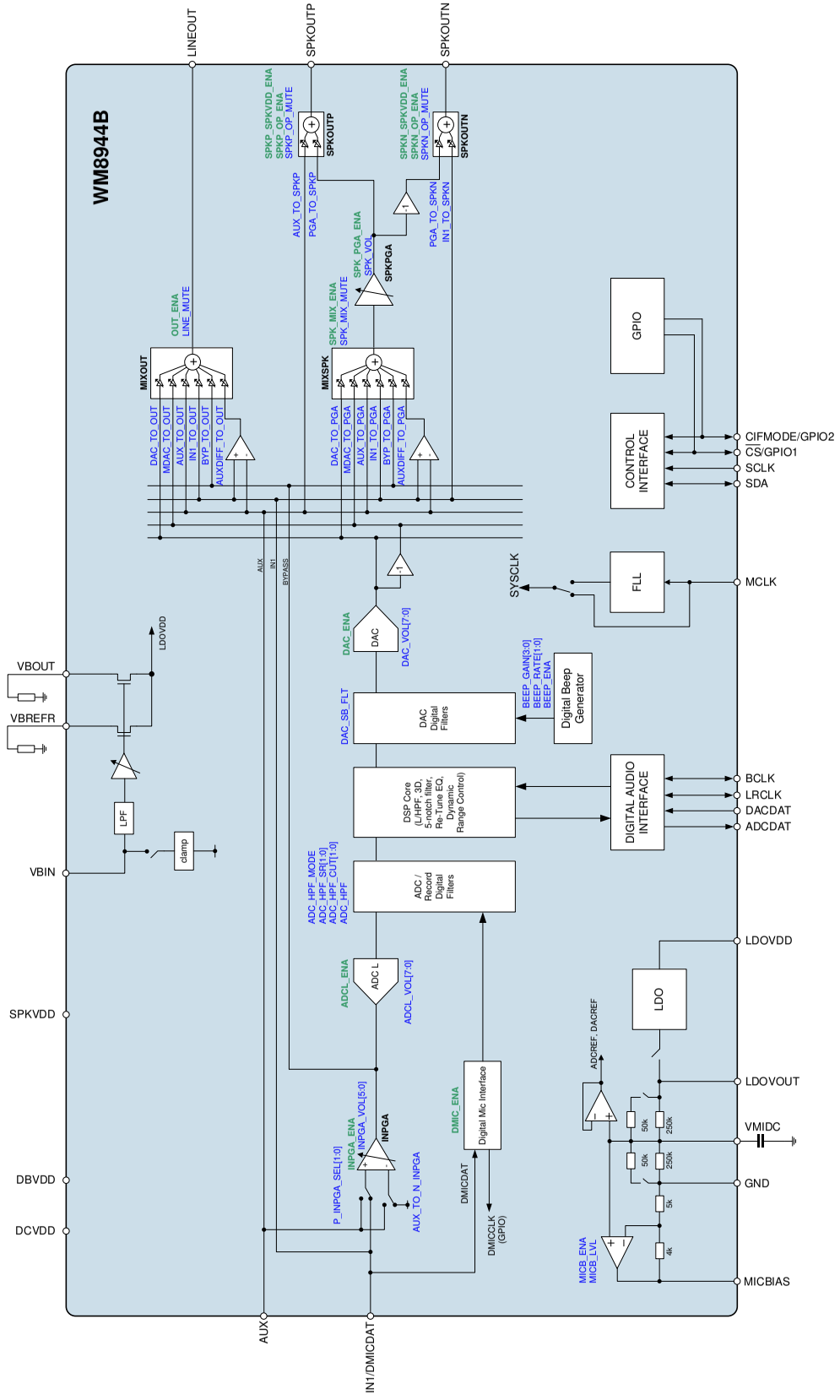
WM8944B_DAC_Spkout_8BTL_350mW_THD+NvsAmpl



TYPICAL POWER CONSUMPTION

Condition	DCVDD (mA) 1.8	DBVDD (mA) 3.3	LDOVDD (mA) 3.3	SPKVDD (mA) 3.3	Total (mA)	Power (mW)
Powerdown						
Supplies are all off except SPKVDD	--	--	--	5.776E-05	--	0.000
Powerdown (register settings are default value, no MCLK, THERR_ACT=0, CIFMODE/GPIO2 configured as an input)	0.0016	0.007	0.00717	0.00133	0.017	0.054
Powerdown (register settings are default value, MCLK=12.288MHz, THERR_ACT=0, CIFMODE/GPIO2 configured as an input)	0.113	0.012	0.00679	0.00138	0.133	0.270
Powerdown (register settings are default value, MCLK=24.576MHz, THERR_ACT=0, CIFMODE/GPIO2 configured as an input)	0.245	0.017	0.00717	0.00133	0.271	0.525
Playback						
Playback to Lineout (SE_CONFIG=DSP playback, no data)	2.55	0.127	1.5	0.00146	4.18	9.964
Playback to Speaker 8ohm BTL (SE_CONFIG=DSP playback, no data)	2.55	0.127	1.64	5.48	9.80	28.505
Playback (Low VMID)						
Playback to Speaker 8ohm BTL with Low VMID (SE_CONFIG=DSP playback, no data)	2.55	0.127	1.99	5.32	9.99	29.132
Record						
IN1 to Record (SE_CONFIG=DSP record, no data)	2.85	0.127	3.87	0.00134	8.7	18.325
Record and Playback						
IN1 to Record + Playback to Lineout + Speaker 8ohm BTL + MICBIAS (SE_CONFIG=DSP playback / record, no data)	4.01 / 5.03	0.126	6.22	5.48	15.8	46.2 / 48.1
IN1 to Record + Playback to Lineout + Speaker 8ohm BTL + MICBIAS + FLL (SE_CONFIG=DSP playback / record, no data)	5.32 / 6.29	0.265	6.22	5.48	17.3	49.1 / 50.8
IN1 to Record + Playback to Lineout + Speaker 8ohm BTL + MICBIAS + FLL + Video Buffer (SE_CONFIG=DSP playback / record, no data)	5.32 / 6.29	0.264	7.21	5.48	18.3	52.3 / 54.1
Record and Playback (Low VMID)						
IN1 to Record + Playback to Lineout + Speaker 8ohm BTL with Low VMID + MICBIAS + FLL + Video Buffer (SE_CONFIG=DSP playback / record, no data)	5.32 / 6.27	0.264	7.56	5.32	18.5	53.0 / 54.7
IN1 to Record + Playback to Lineout + Speaker 8ohm BTL with Low VMID + MICBIAS + FLL + Video Buffer + Bandgap (SE_CONFIG=DSP playback / record, no data)	5.30 / 6.27	0.265	7.5	5.31	18.4	52.7 / 54.4

AUDIO SIGNAL PATHS DIAGRAM



SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

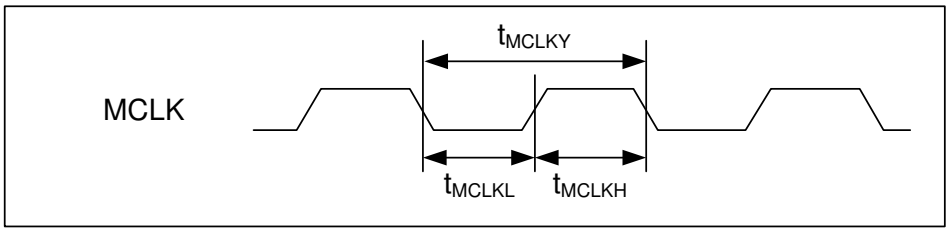


Figure 2 Master Clock Timing

Test Conditions

DCVDD = 1.8V, DBVDD = LDOVDD = SPKVDD = 3.3V, LDOVOUT = 3.0V, GND = 0V, T_A = +25ºC.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Master Clock Timing						
MCLK cycle time	T_{MCLKY}		0.037µs			s
MCLK duty cycle (= T_{MCLKH} : T_{MCLKL})			60:40		40:60	

AUDIO INTERFACE TIMING

MASTER MODE

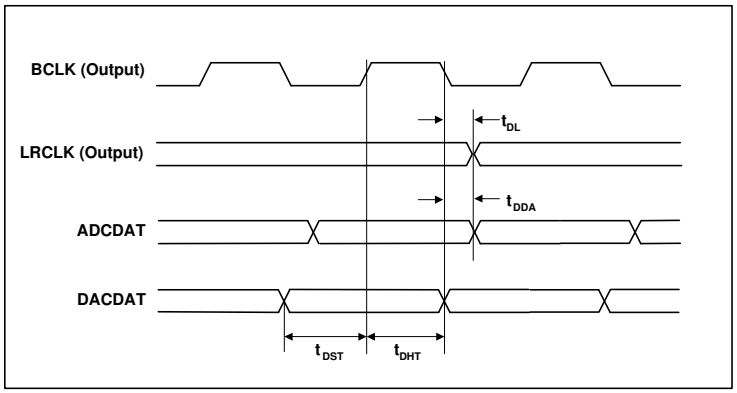


Figure 3 Audio Interface Timing - Master Mode

Test Conditions

DCVDD = 1.8V, DBVDD = LDOVDD = SPKVDD = 3.3V, LDOVOUT = 3.0V, GND = 0V,
T_A = +25ºC, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Master Mode					
LRCLK propagation delay from BCLK falling edge	t_{DL}			20	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			20	ns
DACDAT setup time to BCLK rising edge	t_{DST}	20			ns
DACDAT hold time from BCLK rising edge	t_{DHT}	10			ns

SLAVE MODE

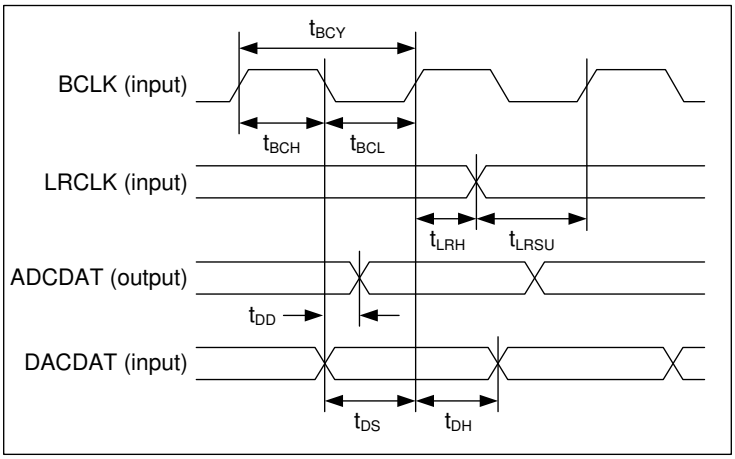


Figure 4 Audio Interface Timing – Slave Mode

Test Conditions

DCVDD = 1.8V, DBVDD = LDOVDD = SPKVDD = 3.3V, LDOVOUT = 3.0V, GND = 0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Slave Mode					
BCLK cycle time	t_{BCY}	50			ns
BCLK pulse width high	t_{BCH}	20			ns
BCLK pulse width low	t_{BCL}	20			ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}	20			ns
LRCLK hold time from BCLK rising edge	t_{LRH}	10			ns
DACDAT hold time from BCLK rising edge	t_{DH}	10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			20	ns
DACDAT set-up time to BCLK rising edge	t_{DS}	20			ns

Note: BCLK period must always be greater than or equal to MCLK period.

CONTROL INTERFACE TIMING

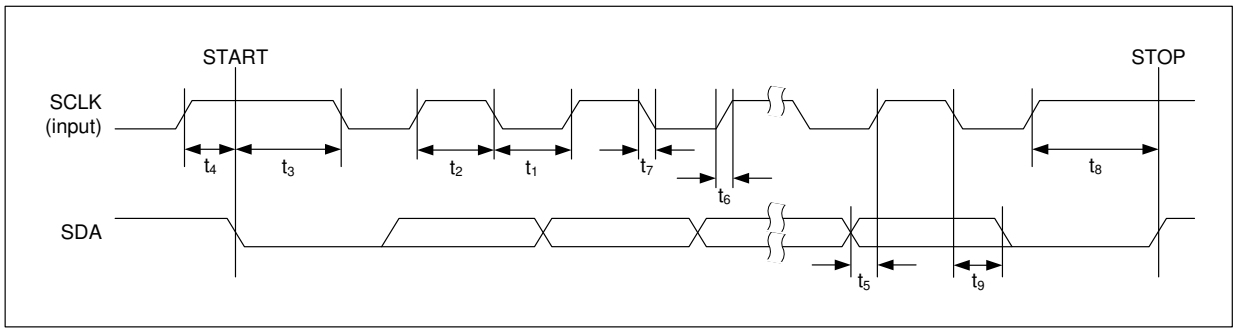


Figure 5 Control Interface Timing - 2-wire (I2C) Control Mode

Test Conditions

DCVDD = 1.8V, DBVDD = LDOVDD = SPKVDD = 3.3V, LDOVOUT = 3.0V, GND = 0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SCLK Frequency				400	kHz
SCLK Low Pulse-Width	t_1	1300			ns
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDA, SCLK Rise Time	t_6			300	ns
SDA, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

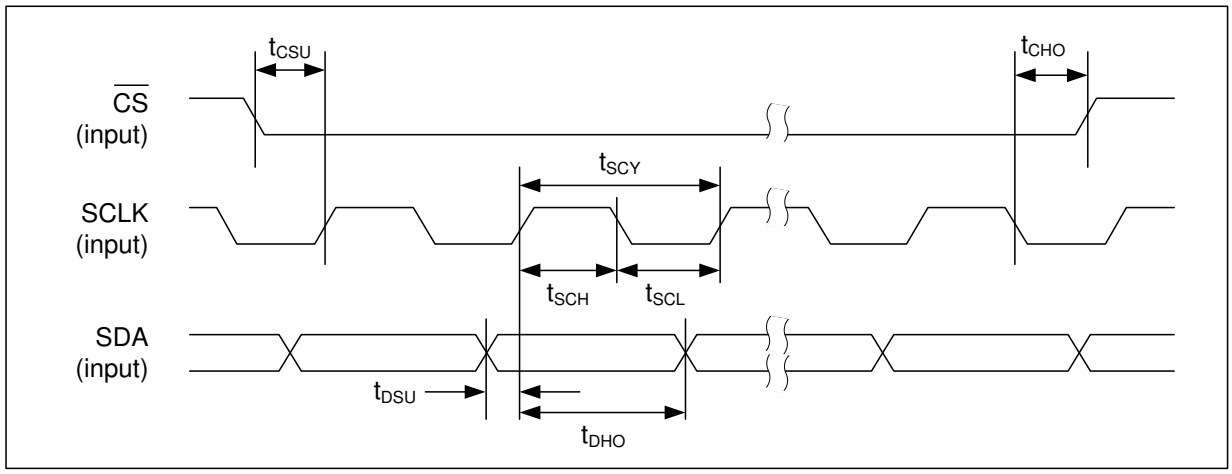


Figure 6 Control Interface Timing - 3-wire (SPI) Control Mode (Write Cycle)

Note: The data is latched on the 32nd falling edge of SCLK after 32 bits have been clocked into the device.

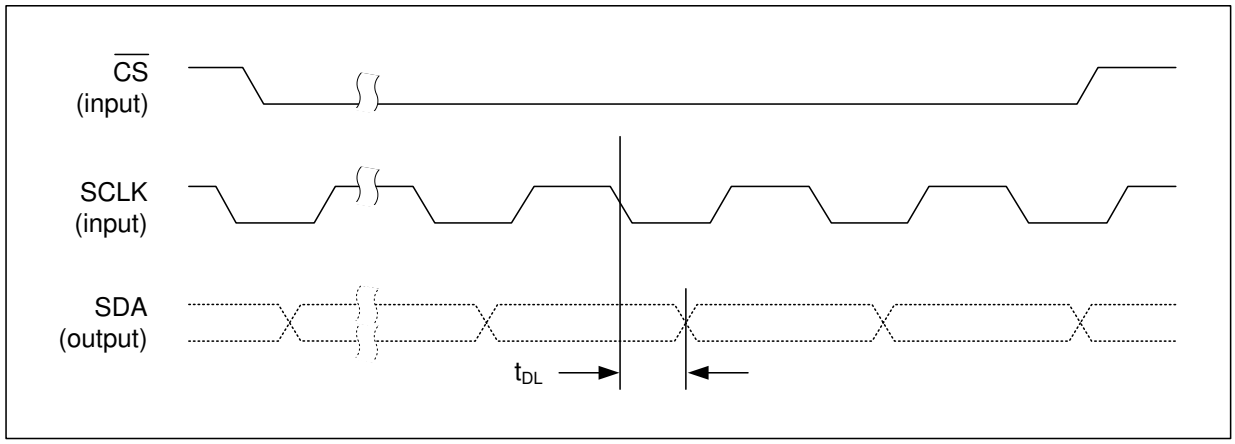


Figure 7 Control Interface Timing - 3-wire (SPI) Control Mode (Read Cycle)

Test Conditions

DCVDD = 1.8V, DBVDD = LDOVDD = SPKVDD = 3.3V, LDOVOUT = 3.0V, GND = 0V,
T_A = +25ºC, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CS falling edge to SCLK rising edge	t_{CSU}	40			ns
SCLK falling edge to CS rising edge	t_{CHO}	10			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDA to SCLK set-up time	t_{DSU}	40			ns
SDA to SCLK hold time	t_{DHO}	10			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns
SCLK falling edge to SDA output transition	t_{DL}			40	ns

DEVICE DESCRIPTION

INTRODUCTION

The WM8944B is a highly integrated low power hi-fi CODEC designed for portable devices such as digital still cameras and multimedia phones. Flexible analogue interfaces and powerful digital signal processing (DSP) in a 2.41 x 2.41mm footprint make it ideal for small portable devices.

The WM8944B supports up to 2 analogue audio inputs. One single-ended or pseudo differential microphone / line input may be selected as the ADC input source. The analogue inputs can also be configured as inputs to the output mixers, either as two single ended inputs or as a differential pair. An integrated bias reference is provided to power standard electret microphones. A stereo digital microphone interface is also supported, with direct input to the DSP core.

The hi-fi ADC and DAC operate at sample rates from 8kHz up to 48kHz. A high pass filter is available in the ADC path for removing DC offsets and suppressing low frequency noise such as mechanical vibration and wind noise. A digital tone ('beep') generator allows audio tones to be injected into the DAC output path.

The WM8944B provides a powerful DSP capability for configurable filtering and processing of the digital audio path. The DSP provides low-pass / high-pass filtering, notch filters, 5-band EQ, dynamic range control (DRC) and a programmable DF1 digital filter. The tuned notch filters allow narrow frequency bands to be attenuated, to provide filtering of motor noise or other unwanted sounds; the 5-band EQ allows the signal to be adjusted for user-preferences. The dynamic range control provides a range of compression, limiting and noise gate functions to support optimum configuration for recording or playback modes. The DF1 filter allows user-specified filters to be implemented in the digital signal chain. 3D stereo enhancement is provided; this may be used on the stereo digital microphone input path.

The ReTune™ feature is a highly-configurable DSP algorithm which can be tailored to cancel or compensate for imperfect characteristics of the housing, loudspeaker or microphone components in the target application. The ReTune algorithm coefficients and register contents are calculated using Cirrus Logic's WISCE™ software; lab bench tests and audio reference measurements must be performed in order to determine the optimum settings.

The digital signal routing between the ADC, DAC and I2S digital audio interface can be configured in different ways according to the application requirements. The DSP functions may be applied to the ADC record path, the DAC playback path, or split between the two paths (refer to the DSP Configuration Modes section).

Two analogue output mixers are provided, connected to 3 analogue output pins. A mono line output and mono BTL speaker may be connected to these outputs.

The WM8944B incorporates an LDO regulator for compatibility with a wide range of supply rails; the internal LDO can also reduce any interference resulting from a noisy supply rail. The LDO regulator can also be used to provide a regulated supply voltage to other circuits.

I2C or SPI control interface modes for read/write access to the register map. A single external clock provides timing reference for all the digital functions; an integrated Frequency Locked Loop (FLL) also provides flexibility to perform frequency conversions and to remove noise/jitter from the external clock. The FLL can be configured for reduced power consumption, or for different filtering requirements of the reference source.

Additional functions include a current-mode video buffer providing excellent video signal reproduction at low operating voltages. Up to 2 GPIO pins may be configured for miscellaneous input/output, or for status indications from the temperature monitoring functions.

ANALOGUE INPUT SIGNAL PATH

The WM8944B has two analogue input pins, which may be selected in different configurations. The analogue input paths can support line and microphone inputs, in single-ended or pseudo-differential modes. The analogue inputs IN1/DMICDAT AUX may be configured as inputs to the input PGA or to the output mixers as single-ended or differential signals.

The input PGA (PGA) is routed to the Analogue to Digital converter (ADC). There is also a bypass path, enabling the signal to be routed directly to the output mixers.

The WM8944B input signal paths and control registers are illustrated in Figure 8.

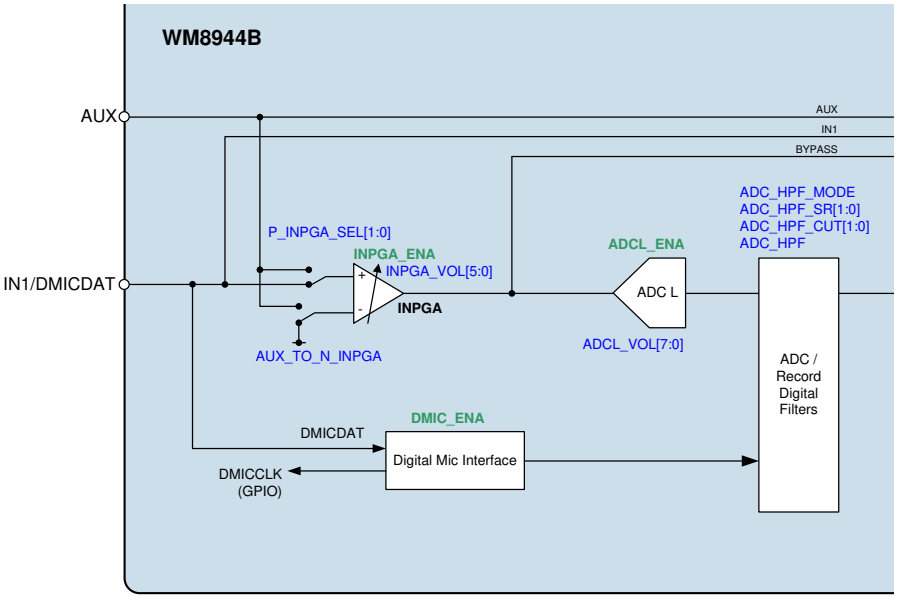


Figure 8 Input Signal Paths

INPUT PGA ENABLE

The input PGA (Programmable Gain Amplifier) is enabled using the register bit INPGA_ENA, as described in Table 1.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) Power Management 1	12	INPGA_ENA	0	Input PGA Enable 0 = Disabled 1 = Enabled

Table 1 Input PGA Enable

To enable the input PGA, the reference voltage VMID and the bias current must also be enabled. See “Reference Voltages and Master Bias” for details of the associated controls VMID_SEL and BIAS_ENA.

INPUT PGA CONFIGURATION

Microphone and Line level audio inputs can be connected to the WM8944B in single-ended or differential configurations. (These two configurations are illustrated in Figure 55 and Figure 56 in the section describing the external components requirements - see “Applications Information”.)

For single-ended microphone inputs, the microphone signal is connected to the non-inverting input of the PGA (IN1/DMICDAT), whilst the inverting input of the PGA is connected to VMID. For differential microphone inputs, the non-inverted microphone signal is connected to the non-inverting input of the PGA (IN1/DMICDAT), whilst the inverted (or ‘noisy ground’) signal is connected to the inverting input pin (AUX).

Line level inputs are connected in the same way as a single-ended microphone signal.

The non-inverting input of the PGA (IN1/DMICDAT) is configured using the P_INPGA_SEL register bit. This register allows the selection of the two possible input pins to the PGA. The inverting input is configured using the AUX_TO_N_INPGA register bit. The registers for configuring the Input PGA are described in Table 2.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R39 (27h) Input ctrl	9	AUX_TO_N_INPGA	0	Input PGA Inverting Input Select 0 = Connected to VMID 1 = Connected to AUX
	1:0	P_INPGA_SEL [1:0]	01	Input PGA Non-Inverting Input Select 00 = Reserved 01 = Connected to IN1/DMICDAT 10 = Connected to AUX 11 = Reserved

Table 2 Input PGA Configuration

MICROPHONE BIAS CONTROL

The WM8944B provides a low noise reference voltage suitable for biasing electret condenser (ECM) type microphones via an external resistor. Refer to the “Applications Information” section for recommended components. The MICBIAS voltage is enabled using the MICB_ENA register bit; the voltage can be selected using the MICB_LVL bit, as described in Table 3.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) Power Management 1	4	MICB_ENA	0	Microphone Bias Enable 0 = Disabled 1 = Enabled
R39 (27h) Input Ctrl	6	MICB_LVL	0	Microphone Bias Voltage control 0 = 0.9 x LDOVOUT 1 = 0.65 x LDOVOUT

Table 3 Microphone Bias Control

INPUT PGA GAIN CONTROL

The volume control gain for the PGA is adjusted using the INPGA_VOL register field as described in Table 4. The gain range is -12dB to +35.25dB in 0.75dB steps. The gains on the inverting and non-inverting inputs to the PGA are always equal. The input PGA can be muted using the INPGA_MUTE mute bit.

To prevent "zipper noise", a zero-cross function is provided on the input PGA. When this feature is enabled, volume updates will not take place until a zero-crossing is detected. The Input PGA volume control register fields are described in Table 4.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R40 (28h) Input PGA gain ctrl	7	INPGA_ZC	0	Input PGA Zero Cross Detector 0 = Change gain immediately 1 = Change gain on zero cross only
	6	INPGA_MUTE	1	Input PGA Mute 0 = Disable Mute 1 = Enable Mute
	5:0	INPGA_VOL [5:0]	01_0000 (0dB)	Input PGA Volume 00_0000 = -12dB 00_0001 = -11.25dB … 01_0000 = 0dB ... 11_1111 = +35.25 (See Table 5 for volume range)

Table 4 Input PGA Volume Control

INPGA_VOL[5:0]	VOLUME (dB)	INPGA_VOL[5:0]	VOLUME (dB)
00_0000	-12	10_0000	12
00_0001	-11.25	10_0001	12.75
00_0010	-10.5	10_0010	13.5
00_0011	-9.75	10_0011	14.25
00_0100	-9	10_0100	15
00_0101	-8.25	10_0101	15.75
00_0110	-7.5	10_0110	16.5
00_0111	-6.75	10_0111	17.25
00_1000	-6	10_1000	18
00_1001	-5.25	10_1001	18.75
00_1010	-4.5	10_1010	19.5
00_1011	-3.75	10_1011	20.25
00_1100	-3	10_1100	21
00_1101	-2.25	10_1101	21.75
00_1110	-1.5	10_1110	22.5
00_1111	-0.75	10_1111	23.25
01_0000	0	11_0000	24
01_0001	0.75	11_0001	24.75
01_0010	1.5	11_0010	25.5
01_0011	2.25	11_0011	26.25
01_0100	3	11_0100	27
01_0101	3.75	11_0101	27.75
01_0110	4.5	11_0110	28.5
01_0111	5.25	11_0111	29.25
01_1000	6	11_1000	30
01_1001	6.75	11_1001	30.75
01_1010	7.5	11_1010	31.5
01_1011	8.25	11_1011	32.25
01_1100	9	11_1100	33
01_1101	9.75	11_1101	33.75
01_1110	10.5	11_1110	34.5
01_1111	11.25	11_1111	35.25

Table 5 Input PGA Volume Range