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WM8946

Stereo Low-Power CODEC with Video Buffer

DESCRIPTION

The WM8946 is a highly integrated low power hi-fi CODEC designed for portable devices such as digital still cameras.

Up to 6 analogue inputs may be connected; a 2-channel digital microphone interface is also provided. Flexible output mixing options support single-ended and differential configurations, with outputs derived from the digital audio paths or from analogue bypass paths. Twin stereo outputs or stereo line and mono BTL headphone/speaker drive may be supported.

Flexible digital mixing and powerful DSP functions are available. Programmable filters and other processes may be applied to the ADC or DAC signal paths. The DSP functions include 3D-stereo enhancement, 5 notch filters, 5-band EQ, dynamic range control and the ReTune™ feature.

The ReTune™ feature is a sophisticated digital filter that can compensate for imperfect characteristics of the housing, loudspeaker or microphone components in an application. The ReTune™ algorithm can provide acoustic equalisation and selective phase (delay) control of specific frequency bands.

The WM8946 is controlled via a I2C or SPI interface. Additional functions include Digital beep generator, Video buffer, programmable GPIO functions, Frequency Locked Loop (FLL) for flexible clocking support and integrated LDO for low noise supply regulation.

The WM8946 is supplied in 36-ball W-CSP package, ideal for portable systems.

FEATURES

- Hi-fi audio CODEC
  - 94dB SNR during ADC recording ('A' weighted)
  - 96dB SNR during DAC playback ('A' weighted)
- 6 analogue audio inputs
- Integrated bias reference for electret microphones
- 2-channel digital microphone interface
- Powerful digital mixing / DSP functions:
  - 3D-stereo enhancement
  - 5-notch filters
  - 5-band equalizer (EQ)
  - ReTune™ parametric filter
  - Dynamic range control and noise gate
  - Low-pass/High-pass filters
  - Direct Form 1 (DF1) programmable digital filter
- Digital beep generator
- 4 analogue audio outputs
- Stereo line output
- Mono BTL headphone/speaker output driver
- I2S digital audio interface - sample rates 8kHz to 48kHz
- Frequency Locked Loop (FLL) frequency conversion / filter
- Video buffer function
- Integrated LDO low-noise voltage regulator
- 36-ball W-CSP package (2.97 x 3.07 x 0.7mm, 0.5mm pitch)

APPLICATIONS

- Digital Still Cameras (DSC)
- Multimedia phones

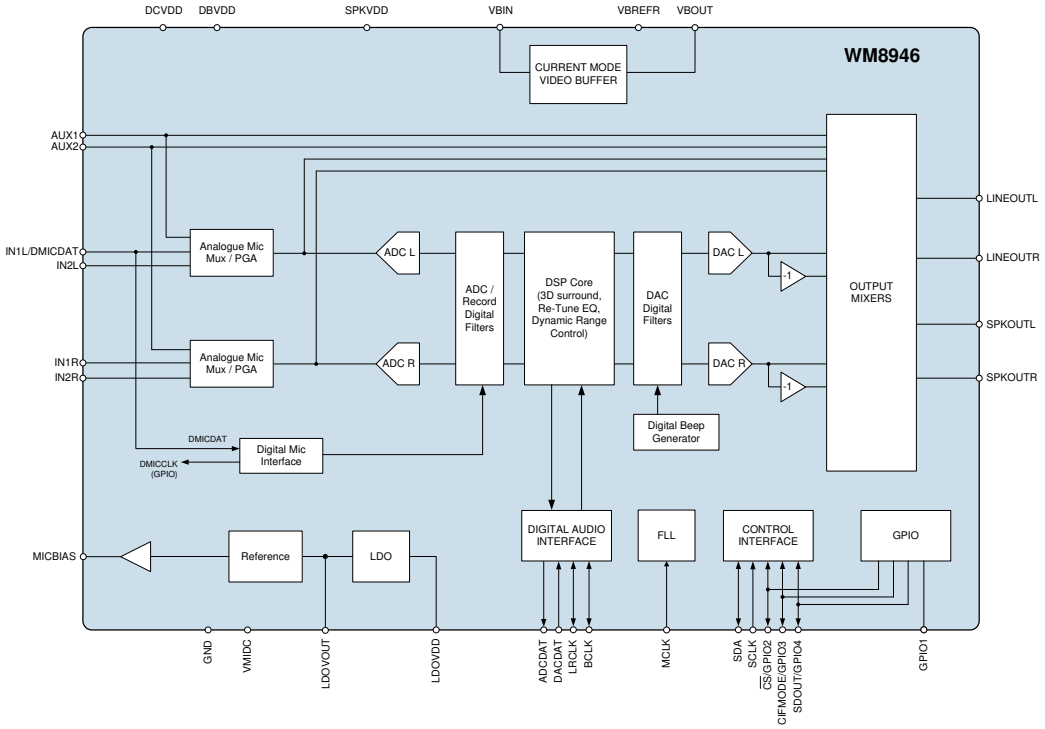
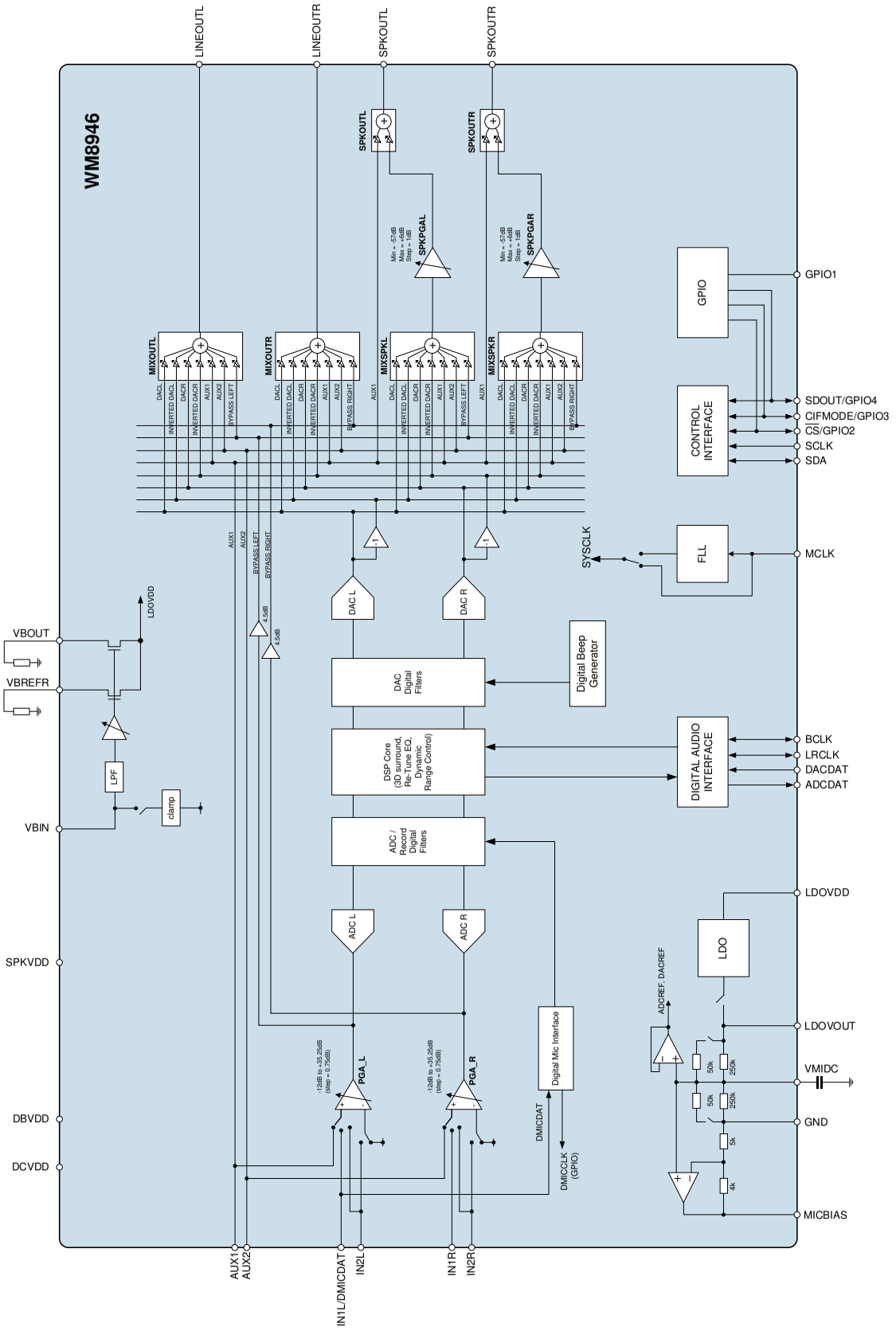


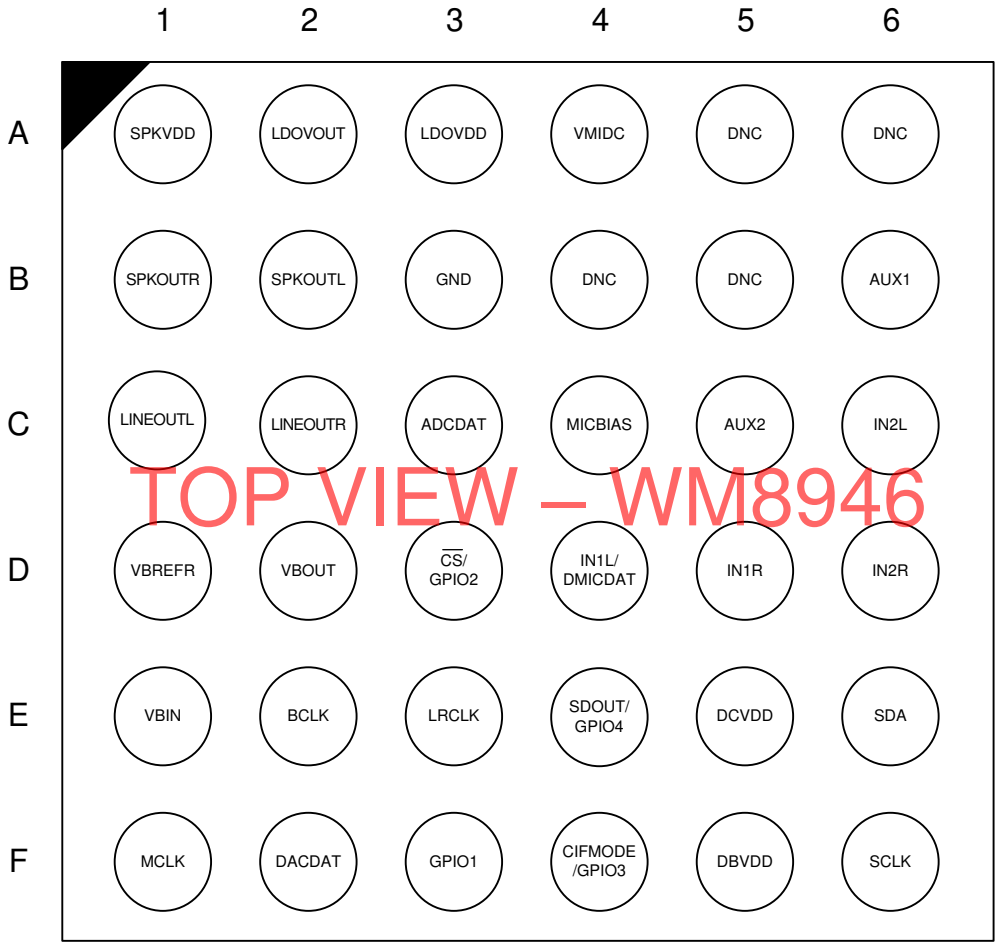
TABLE OF CONTENTS

BLOCK DIAGRAM



PIN CONFIGURATION

The WM8946 is supplied in a 36-pin CSP format. The pin configuration is illustrated below, showing the top-down view from above the chip.



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8946ECS/R	-40°C to +85°C	36-ball W-CSP (Pb-free, tape and reel)	MSL1	260°C

Note:
Reel quantity = 5000

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
A1	SPKVDD	Supply	Supply for speaker driver
A2	LDOVOUT	Supply	LDO output
A3	LDOVDD	Supply	LDO supply input
A4	VMIDC	Analogue Output	Midrail voltage decoupling capacitor
A5	DNC	N/A	Do Not Connect
A6	DNC	N/A	Do Not Connect
B1	SPKOUTR	Analogue Output	Right speaker mixer output
B2	SPKOUTL	Analogue Output	Left speaker mixer output
B3	GND	Supply	Ground
B4	DNC	N/A	Do Not Connect
B5	DNC	N/A	Do Not Connect
B6	AUX1	Analogue Input	Aux audio input
C1	LINEOUTL	Analogue Output	Left line mixer output
C2	LINEOUTR	Analogue Output	Right line mixer output
C3	ADCDAT	Digital Output	ADC / Digital Microphone digital audio data
C4	MICBIAS	Analogue Output	Microphone bias
C5	AUX2	Analogue Input	Aux audio input
C6	IN2L	Analogue Input	Left input 2
D1	VBREFR	Analogue Output	Video buffer current reference resistor connection
D2	VBOUT	Analogue Output	Video buffer output
D3	$\overline{CS}$/GPIO2	Digital Input / Output	Chip Select / GPIO2
D4	IN1L/DMICDAT	Analogue Input / Digital Input	Left input 1 / Digital Microphone data input
D5	IN1R	Analogue Input	Right input 1
D6	IN2R	Analogue Input	Right input 2
E1	VBIN	Analogue Input	Video buffer input
E2	BCLK	Digital Input / Output	Audio interface bit clock
E3	LRCLK	Digital Input / Output	Audio interface left / right clock
E4	SDOUT/GPIO4	Digital Input / Output	Control interface data output / GPIO4
E5	DCVDD	Supply	Digital core supply
E6	SDA	Digital Input / Output	Control interface data input / output
F1	MCLK	Digital Input	Master clock
F2	DACDAT	Digital Input	DAC digital audio data
F3	GPIO1	Digital Input / Output	GPIO1
F4	CIFMODE/GPIO3	Digital Input / Output	Control interface mode select / GPIO3
F5	DBVDD	Supply	Digital buffer (I/O) supply
F6	SCLK	Digital Input	Control interface clock input

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus Logic tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (DCVDD)	-0.3V	2.5V
Supply voltages (LDOVDD, DBVDD, SPKVDD)	-0.3V	4.5V
Voltage range digital inputs	-0.7V	DBVDD +0.7V
Voltage range analogue inputs	-0.7V	LDOVDD +0.7V
Operating temperature range, T_A	-40ºC	+85ºC
Junction temperature, T_{JMAX}	-40ºC	+150ºC
Storage temperature after soldering	-65ºC	+150ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD	1.62	1.8	1.98	V
Digital supply range (I/O)	DBVDD	1.71	3.3	3.6	V
Analogue supply	LDOVDD	2.4	3.3	3.6	V
Speaker supply range	SPKVDD	1.71	3.3	3.6	V
Ground	GND		0		V

Note:

To ensure pop-free device start-up, LDOVDD must be enabled before SPKVDD

THERMAL PERFORMANCE

Thermal analysis should be performed in the intended application to prevent the WM8946 from exceeding maximum junction temperature. Several contributing factors affect thermal performance most notably the physical properties of the mechanical enclosure, location of the device on the PCB in relation to surrounding components and the number of PCB layers. Connecting the GND balls through thermal vias and into a large ground plane will aid heat extraction.

Three main heat transfer paths exist to surrounding air as illustrated below in Figure 1:

- Package top to air (radiation).
- Package bottom to PCB (radiation).
- Package balls to PCB (conduction).

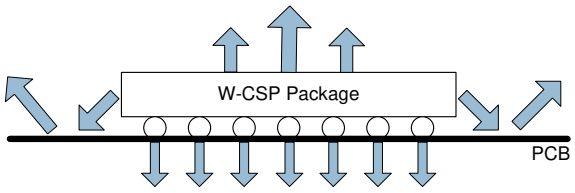


Figure 1 Heat Transfer Paths

The temperature rise T_R is given by $T_R = P_D * \Theta_{JA}$

- P_D is the power dissipated in the device.
- Θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature and is therefore a measure of heat transfer from the die to surrounding air. Θ_{JA} is determined with reference to JEDEC standard JESD51-9.

The junction temperature T_J is given by $T_J = T_A + T_R$, where T_A is the ambient temperature.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Operating temperature range	T_A	-40		85	°C
Operating junction temperature	T_J	-40		125	°C
Thermal Resistance (Junction to Case)	Θ_{JC}		30		°C/W
Thermal Resistance (Junction to Ambient)	Θ_{JA}		60		°C/W

Notes:

1. Junction temperature is a function of ambient temperature and of the device operating conditions. The ambient temperature limits and junction temperature limits must both be observed.

ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD = 1.8V, DBVDD = LDOVDD = SPKVDD = 3.3V, LDOVOUT = 3.0V, GND = 0V,
T_A = +25ºC, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (IN1L, IN2L, IN1R, IN2R)						
Maximum input signal level (changes in proportion to LDOVOUT)		Single-ended input		1.0 0		Vrms dBV
		Pseudo-differential input		0.7 -3.1		Vrms dBV
Input resistance (IN1L, IN1R)		+35.25dB gain		3.5		kΩ
		0dB gain		104		kΩ
		-12dB gain		166		kΩ
Input resistance (IN2L, IN2R)		All gain settings		96		kΩ
Input capacitance				10		pF
Analogue Inputs (AUX1, AUX2)						
Maximum input signal level (changes in proportion to LDOVOUT)		AUX1 or AUX2 enabled as audio input		1.0 0		Vrms dBV
Input resistance		Input mixer path (0dB)		100		kΩ
		Output mixer / direct speaker path (0dB)		15		kΩ
		Output mixer / direct speaker path (-6dB)		30		kΩ
Input capacitance				10		pF
Analogue Inputs Programmable Gain Amplifiers (PGAs)						
Minimum programmable gain				-12		dB
Maximum programmable gain				35.25		dB
Gain step size		Guaranteed monotonic		0.75		dB
Mute attenuation				92		dB
Common Mode Rejection Ratio		1kHz input		110		dB
Speaker Output Programmable Gain Amplifiers (PGAs)						
Minimum programmable gain				-57		dB
Maximum programmable gain				6		dB
Gain step size		Guaranteed monotonic		1		dB
Mute attenuation				71		dB
ADC Input Path Performance (Input PGAs to ADC)						
SNR (A-weighted)			84	94		dB
THD		-1dBFS input		-83	-75	dB
THD+N		-1dBFS input		-77	-70	dB
Channel separation (Left/Right)				95		dB
PSRR (with respect to LDOVDD)		217Hz 1kHz		77 90		dB

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Bypass to Line Output (Single-ended IN2L, IN2R to Input PGA to Line Output, 10kΩ / 50pF)						
SNR (A-weighted)		PGA Gain = 0dB INPPGAVOL = 0dB	90	98		dB
THD+N		PGA Gain = 0dB INPPGAVOL = 0dB		-89.5	-82	dB
Bypass to Speaker Output (Single-ended AUX1, AUX2 to Input PGA to SPKMIX to Speaker Output, 10kΩ / 50pF)						
SNR (A-weighted)		PGA Gain = 0dB INPPGAVOL = 0dB	90	96		dB
THD+N		PGA Gain = 0dB INPPGAVOL = 0dB		-86.5	-77	dB
DAC Output Path Performance (DAC to Line Output, 10kΩ / 50pF)						
Maximum output signal level (changes in proportion to LDOVOUT)				1		Vrms
SNR (A-weighted)			85	96		dB
THD				-78	-72	dB
THD+N				-76	-70	dB
Channel separation (Left/Right)				90		dB
Mute attenuation				125		dB
PSRR (with respect to LDOVDD)				48 60		dB
Line Output Resistance				10		kΩ
Line Output Capacitance				50		pF
DAC Output Path Performance (DAC to Speaker Output, 10kΩ / 50pF)						
Maximum output signal level (changes in proportion to LDOVOUT)				1		Vrms
SNR (A-weighted)				96		dB
THD				-78		dB
THD+N				-76		dB
Speaker Output Performance (Speaker Output, 8Ω BTL)						
SNR (A-weighted)			90	96		dB
THD		P_O=150mW		0.03 -68		% dB
		P_O=350mW		2.944 -30.6		% dB
THD+N		P_O=150mW		0.05 -66		% dB
		P_O=350mW		3.72 -28.6		% dB
Channel separation (Left/Right)				90		dB
Mute attenuation				92		dB
PSRR (with respect to LDOVDD)		217Hz 1kHz		48 60		dB
PSRR (with respect to SPKVDD)		217Hz 1kHz		89 79		dB
Speaker Resistance				8		Ω
Speaker Capacitance				50		pF

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Inputs/Outputs						
Input high level			0.7×DBVDD			V
Input low level					0.3×DBVDD	V
Output high level		I_{OL} = 1mA	0.8×DBVDD			V
Output low level		I_{OH} = -1mA			0.2×DBVDD	V
Input capacitance				10		pF
Input leakage		All digital pins except CIFMODE	-900		900	nA
		CIFMODE pin	-90		90	nA
LDO Regulator						
Input voltage	LDOVDD		2.4	3.3	3.6	V
Output voltage	LDOVOUT	LDO_REF_SEL = 0		3.0		V
Maximum output current (see note)				50		mA
Output voltage accuracy		I_{LOAD} = 50mA		2		%
Quiescent current		No Load		55		µA
Leakage current				1		µA
PSRR (with respect to LDOVDD)		217Hz 1kHz		40 49		dB
Video Buffer						
Maximum output voltage swing	Vom	f=100kHz, THD=1%	1.10	1.25	1.50	V pk-pk
Voltage gain	Av	VB_GAIN = 1, R_{REF}=187Ω, R_{LOAD}=75Ω, R_{SOURCE}=75Ω	5.08	6	7.94	dB
		VB_GAIN = 0, R_{REF}=187Ω, R_{LOAD}=75Ω, R_{SOURCE}=75Ω	-0.92	0	1.94	dB
Gain step size				6		dB
Differential gain	DG	Vin = 1V pk-pk	-2.0	0.3	+2.0	%
Differential phase	DP	Vin = 1V pk-pk	-2.0%	0.7	+2.0	Deg
SNR	VSNR		40	60	100	dB
SYNC tip offset above GND		VB_PD = 0 VB_GAIN = 1	0	40	75	mV
Third order Low Pass Filter response (referenced to 100kHz) R_{REF}=187Ω, R_{LOAD}=75Ω, R_{SOURCE}=75Ω, 0dB gain		2.4MHz	-0.5	0	0.5	dB
		5.13MHz	-0.5	-0.2	0.5	dB
		9.04MHz	-3.0	-1.6	0	dB
		13.32MHz	-11.0	-7.0	-3.0	dB
PSRR (with respect to LDOVOUT)		100kHz		60		dB
Clocking						
MCLK frequency			30Hz		27MHz	Hz
FLL output frequency			2.045		50	MHz
FLL lock time				2		ms
MICBIAS						
Bias voltage (changes in proportion to LDOVOUT)	MICBIAS	MICB_LVL = 0		2.7		V
		MICB_LVL = 1		1.95		V
Bias Current source					3	mA
Output noise spectral density		1kHz to 20kHz		15		nV/√Hz
PSRR (with respect to LDOVDD)		217Hz 1kHz		70 85		dB

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Reference Levels						
Midrail Reference Voltage (changes in proportion to LDOVOUT)	VMID	VMID_REF_SEL = 1 VMID_CTRL=1		1.5		V
Bandgap Reference		BG_VSEL=01010	-10%	1.5	+10%	V

Note:

The maximum LDO output current is the total internal and external load capability; internal circuits of the WM8946 will typically account for 25mA of this capacity.

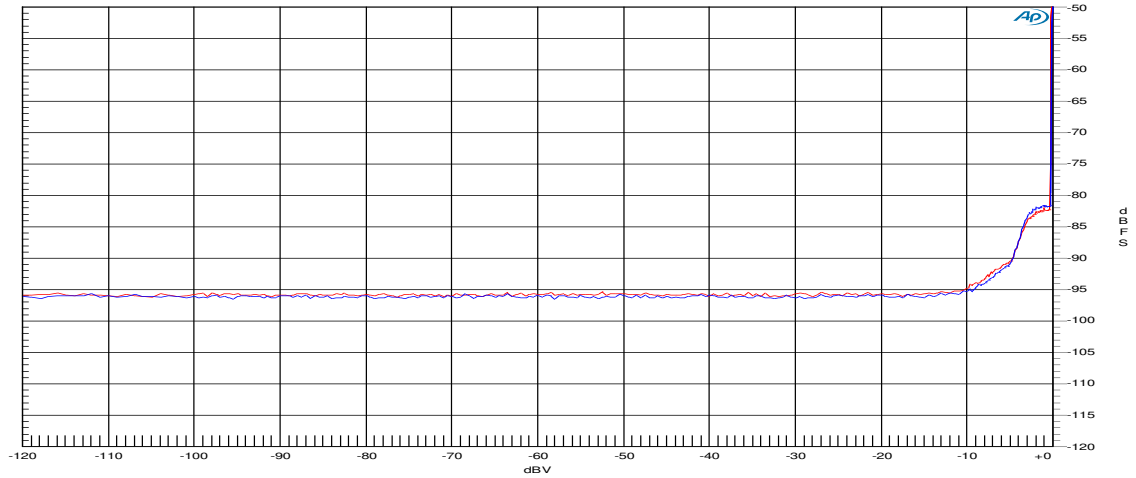
TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is the difference in level between a full scale output signal and the device output noise with no signal applied, measured over a bandwidth of 20Hz to 20kHz. This ratio is also called idle channel noise. (No Auto-zero or Mute function is employed).
2. Total Harmonic Distortion (dB) – THD is the difference in level between a 1kHz reference sine wave output signal and the first seven harmonics of the output signal. The amplitude of the fundamental frequency of the output signal is compared to the RMS value of the next seven harmonics and expressed as a ratio.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the difference in level between a 1kHz reference sine wave output signal and all noise and distortion products in the audio band. The amplitude of the fundamental reference frequency of the output signal is compared to the RMS value of all other noise and distortion products and expressed as a ratio.
4. Channel Separation (L/R) (dB) – is a measure of the coupling between left and right channels. A full scale signal is applied to the left channel only, and the right channel amplitude is measured. Next, a full scale signal is applied to the right channel only, and the left channel amplitude is measured. The worst case channel separation is quoted; this is the difference in level between the full-scale output and the cross-channel output signal level, expressed as a ratio.
5. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.
6. Power Supply Rejection Ratio (dB) – PSRR is a measure of ripple attenuation between a power supply rail and a signal output path. With the signal path idle, a small sine wave ripple is applied to power supply rail. The amplitude of the supply ripple is compared to the amplitude of the output signal generated and is expressed as a ratio.
7. All performance measurements are carried out with 20kHz AES17 low pass filter for distortion measurements, and an A-weighted filter for noise measurement. Failure to use such a filter will result in higher THD and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out-of-band noise; although it is not audible, it may affect dynamic specification values.

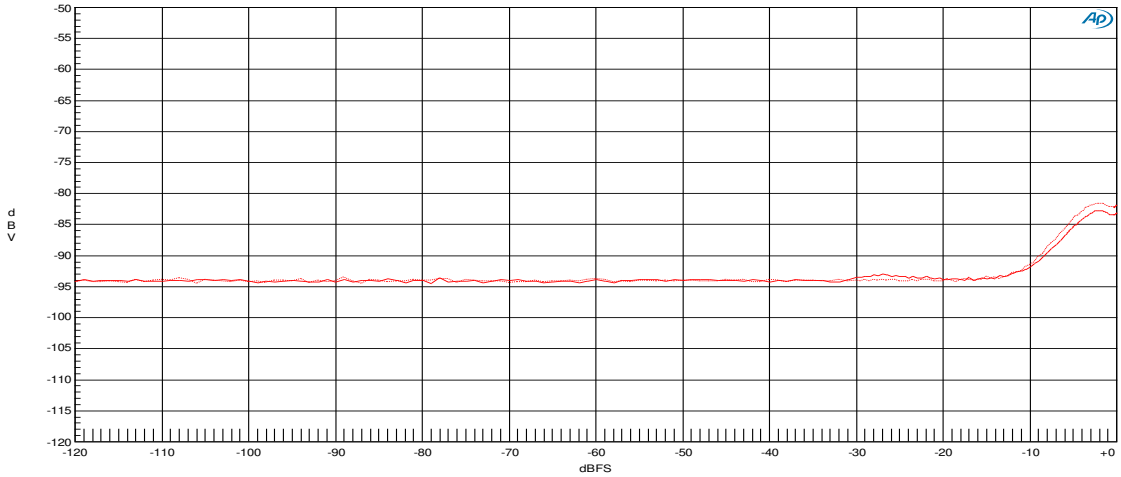
TYPICAL PERFORMANCE

INPUT PATH / OUTPUT PATH PERFORMANCE

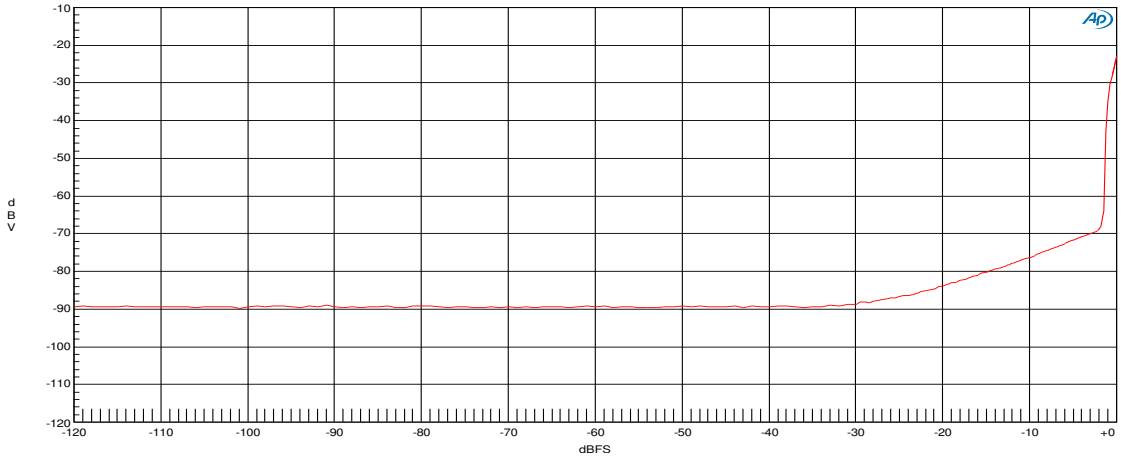
WM8946 ADC - THD+N v Ampltiude - ADC - Slave Mode



WM8946 - DAC to LINEOUT THD+N v Amplitude - Slave



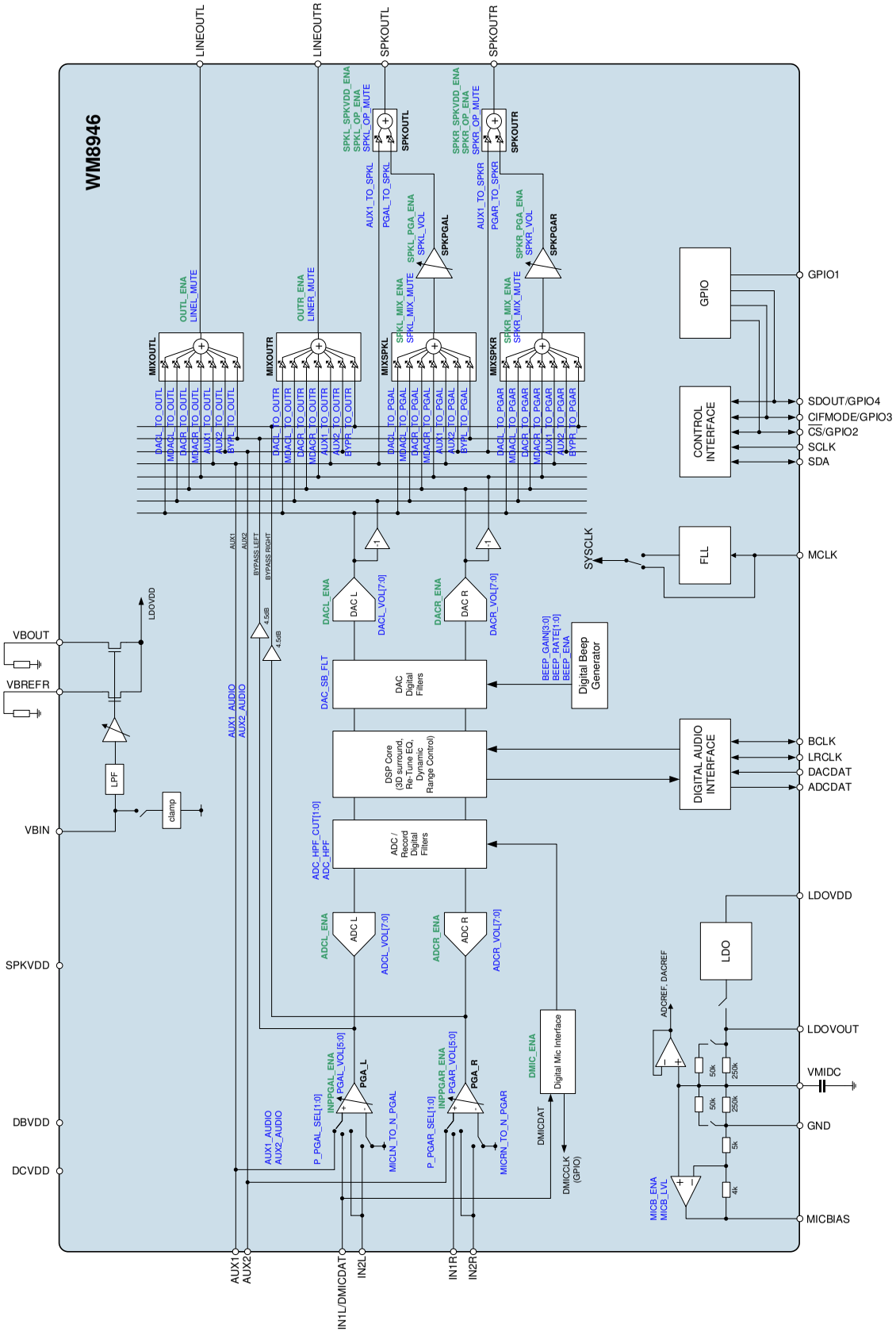
WM8946 - DAC to SPKOUT 8ohm BTL
THD+N v Amplitude - 48kHz



TYPICAL POWER CONSUMPTION

Condition	DCVDD Current @ 1.8V	DBVDD Current @ 3.3V	LDOVDD Current @ 3.3V	SPKVDD Current @ 3.3V	Total Current (mA)	Total Power (mW)
Powerdown (no data)	0.178	0.062	0.007	0.002	0.249	0.555
Powerdown (+Master BIAS)	0.178	0.062	0.021	0.002	0.263	0.601
Powerdown (+Master BIAS+VMID buffer)	0.178	0.062	0.142	0.002	0.384	1.000
Powerdown (+Master BIAS+VMID buffer+VMID)	0.178	0.063	1.092	0.002	1.335	4.139
Playback to Lineout (no data)	4.272	0.057	2.336	0.007	6.672	15.610
Playback to Lineout (with data)	4.293	0.062	2.356	0.007	6.718	15.730
Video Buffer Only	0.178	0.062	5.088	0.020	5.348	17.381
Playback to Speaker (no data)	4.272	0.057	2.877	4.707	11.913	32.905
Playback to Speaker (with data)	4.294	0.062	2.895	4.730	11.981	33.096
Playback to Speaker (with data) 32ohm	4.295	0.062	2.895	5.790	13.042	36.596
Playback to Speaker (with data) 16ohm	4.295	0.062	2.896	6.275	13.528	38.200
Mono Record (nodata)	2.992	0.088	3.728	0.007	6.815	18.002
Mono Record (with data)	2.999	0.100	3.727	0.007	6.833	18.050
Stereo Record (no data)	4.652	0.128	6.692	0.007	11.479	30.903
Stereo Record (with data)	4.654	0.128	6.692	0.007	11.481	30.906
Playback and Record (no data)	5.673	0.120	10.054	4.408	20.255	58.332
All On	5.408	0.099	62.323	4.211	24.253	71.923

AUDIO SIGNAL PATHS DIAGRAM



SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

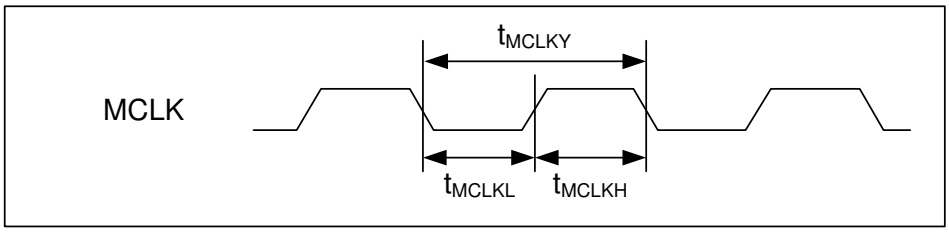


Figure 2 Master Clock Timing

Test Conditions

DCVDD = 1.8V, DBVDD = LDOVDD = SPKVDD = 3.3V, LDOVOUT = 3.0V, GND = 0V, T_A = +25°C.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Master Clock Timing						
MCLK cycle time	T_{MCLKY}		0.037µs			s
MCLK duty cycle (= T_{MCLKH} : T_{MCLKL})			60:40		40:60	

AUDIO INTERFACE TIMING

MASTER MODE

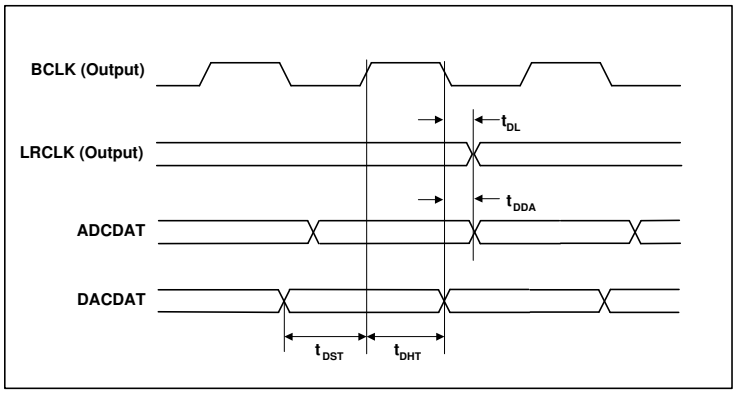


Figure 3 Audio Interface Timing - Master Mode

Test Conditions

DCVDD = 1.8V, DBVDD = LDOVDD = SPKVDD = 3.3V, LDOVOUT = 3.0V, GND = 0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Master Mode					
LRCLK propagation delay from BCLK falling edge	t_{DL}			20	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			20	ns
DACDAT setup time to BCLK rising edge	t_{DST}	20			ns
DACDAT hold time from BCLK rising edge	t_{DHT}	10			ns

SLAVE MODE

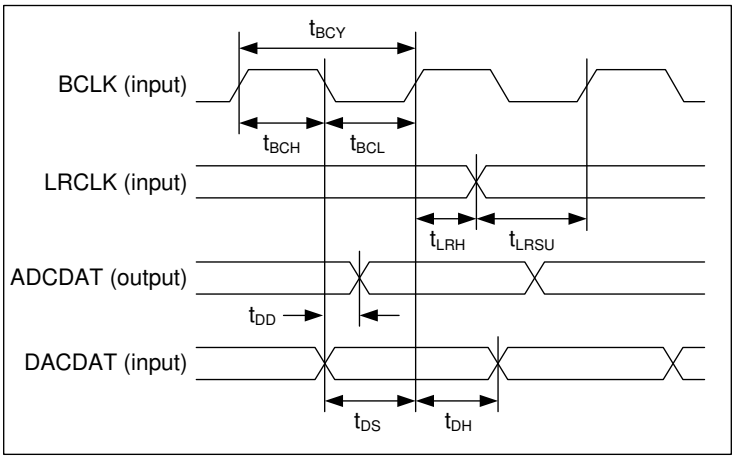


Figure 4 Audio Interface Timing – Slave Mode

Test Conditions

DCVDD = 1.8V, DBVDD = LDOVDD = SPKVDD = 3.3V, LDOVOUT = 3.0V, GND = 0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Interface Timing - Slave Mode					
BCLK cycle time	t_{BCY}	50			ns
BCLK pulse width high	t_{BCH}	20			ns
BCLK pulse width low	t_{BCL}	20			ns
LRCLK set-up time to BCLK rising edge	t_{LRSU}	20			ns
LRCLK hold time from BCLK rising edge	t_{LRH}	10			ns
DACDAT hold time from BCLK rising edge	t_{DH}	10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			20	ns
DACDAT set-up time to BCLK rising edge	t_{DS}	20			ns

Note: BCLK period must always be greater than or equal to MCLK period.

CONTROL INTERFACE TIMING

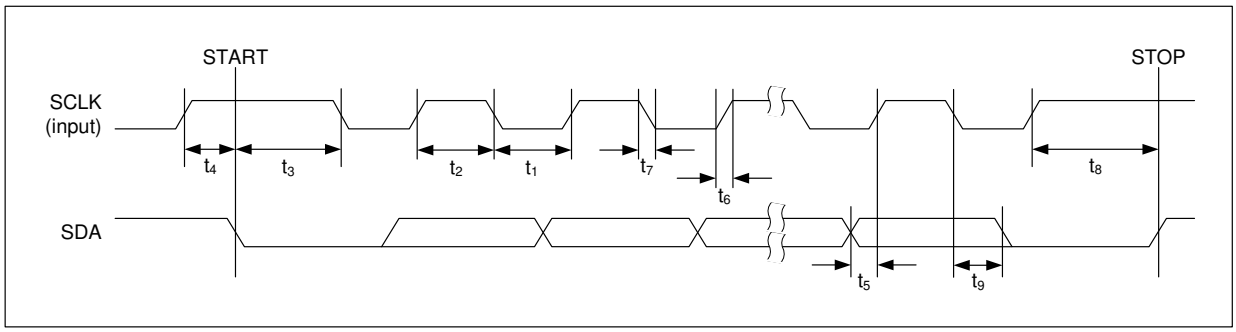


Figure 5 Control Interface Timing - 2-wire (I2C) Control Mode

Test Conditions

DCVDD = 1.8V, DBVDD = LDOVDD = SPKVDD = 3.3V, LDOVOUT = 3.0V, GND = 0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SCLK Frequency				400	kHz
SCLK Low Pulse-Width	t_1	1300			ns
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDA, SCLK Rise Time	t_6			300	ns
SDA, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

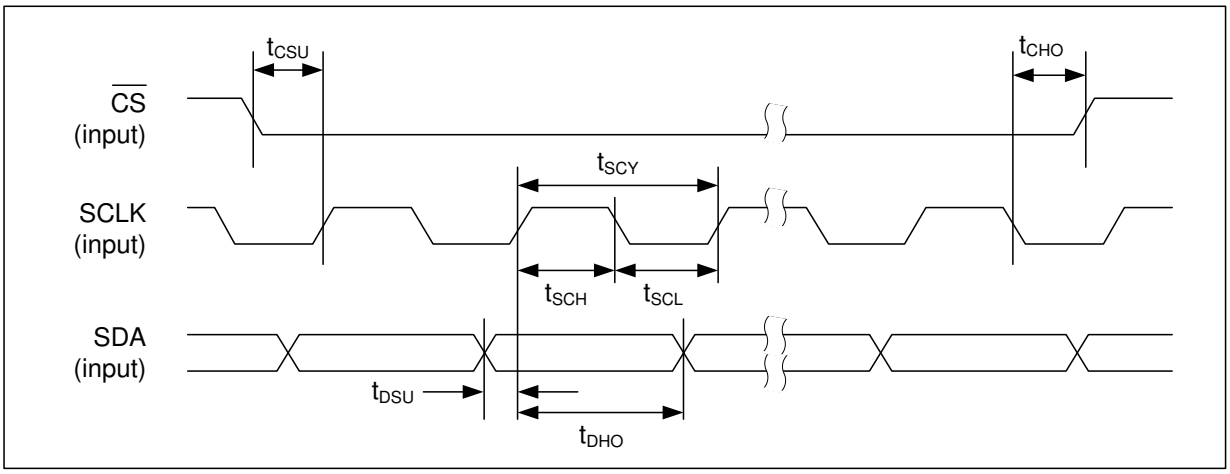


Figure 6 Control Interface Timing - 3-wire (SPI) Control Mode (Write Cycle)

Note: The data is latched on the 32nd falling edge of SCLK after 32 bits have been clocked into the device.

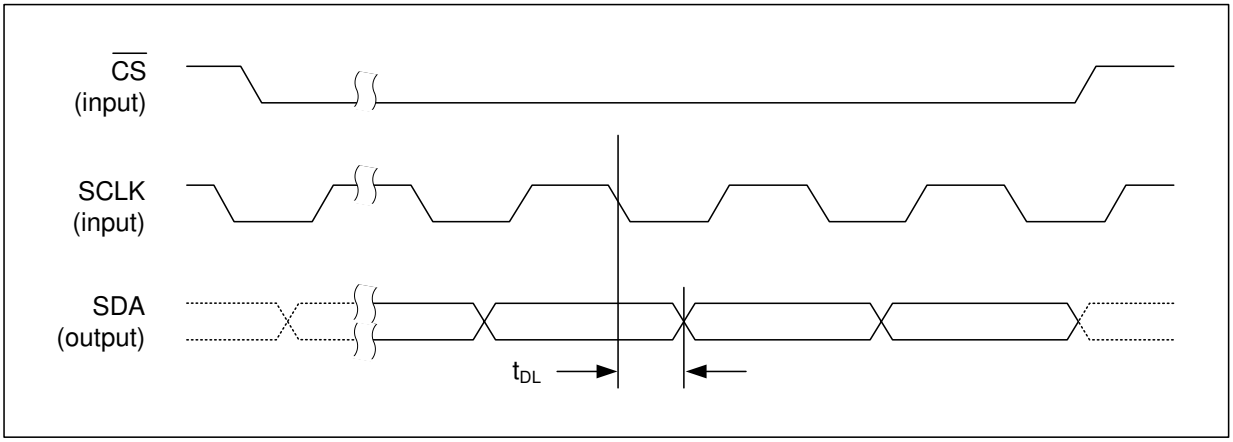


Figure 7 Control Interface Timing - 3-wire (SPI) Control Mode (Read Cycle)

Test Conditions

DCVDD = 1.8V, DBVDD = LDOVDD = SPKVDD = 3.3V, LDOVOUT = 3.0V, GND = 0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CS falling edge to SCLK rising edge	t_{CSU}	40			ns
SCLK falling edge to CS rising edge	t_{CHO}	10			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDA to SCLK set-up time	t_{DSU}	40			ns
SDA to SCLK hold time	t_{DHO}	10			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns
SCLK falling edge to SDA output transition	t_{DL}			40	ns

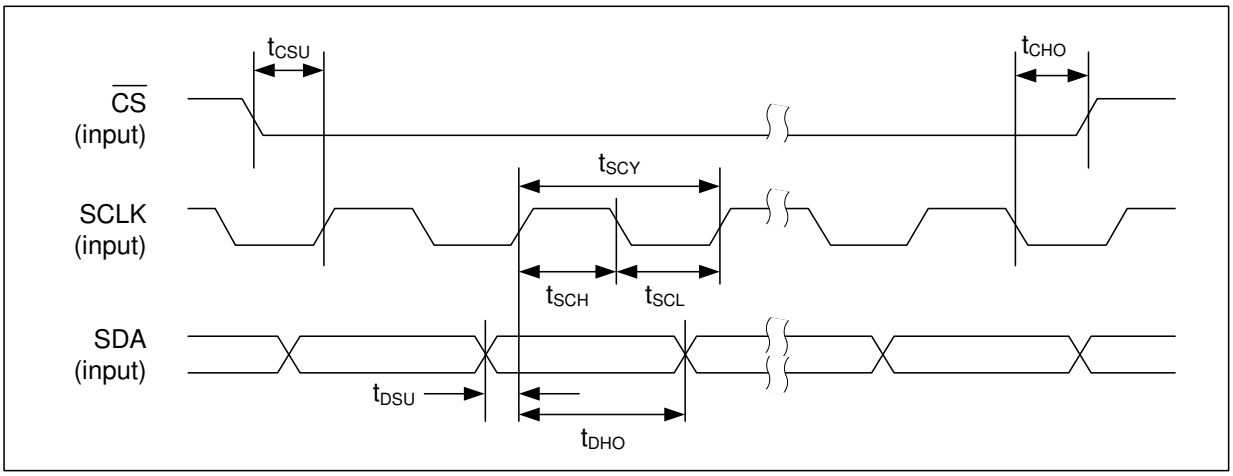


Figure 8 Control Interface Timing - 4-wire (SPI) Control Mode (Write Cycle)

Note: The data is latched on the 32nd falling edge of SCLK after 32 bits have been clocked into the device.

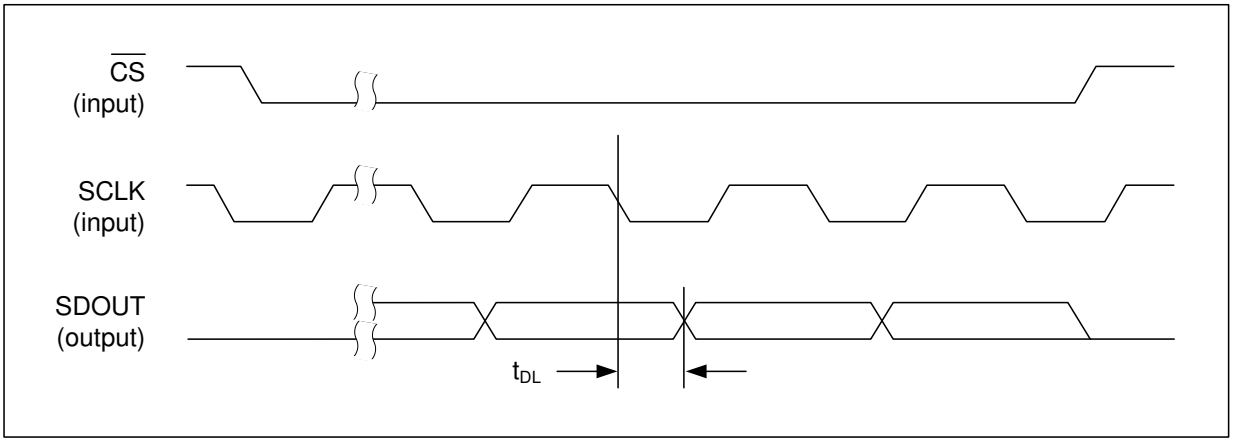


Figure 9 Control Interface Timing - 4-wire (SPI) Control Mode (Read Cycle)

Test Conditions

DCVDD = 1.8V, DBVDD = LDOVDD = SPKVDD = 3.3V, LDOVOUT = 3.0V, GND = 0V,
T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CS falling edge to SCLK rising edge	t_{CSU}	40			ns
SCLK falling edge to CS rising edge	t_{CHO}	10			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDA to SCLK set-up time	t_{DSU}	40			ns
SDA to SCLK hold time	t_{DHO}	10			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns
SCLK falling edge to SDOUT transition	t_{DL}			40	ns

DEVICE DESCRIPTION

INTRODUCTION

The WM8946 is a highly integrated low power hi-fi CODEC designed for portable devices such as digital still cameras and multimedia phones. Flexible analogue interfaces and powerful digital signal processing (DSP) in a 2.96 x 3.06mm footprint make it ideal for small portable devices.

The WM8946 supports up to 6 analogue audio inputs. One pair of single-ended or pseudo differential microphone / line inputs is selected as the ADC input source. The two auxiliary inputs can be selected as line inputs to the ADC, or as direct signal paths to the output mixers. An integrated bias reference is provided to power standard electret microphones. A two-channel digital microphone interface is also supported, with direct input to the DSP core via the ADCs.

The stereo hi-fi ADCs and DACs operate at sample rates from 8kHz up to 48kHz. A high pass filter is available in the ADC path for removing DC offsets and suppressing low frequency noise such as mechanical vibration and wind noise. A digital tone ('beep') generator allows audio tones to be injected into the DAC output path.

The WM8946 provides a powerful DSP capability for configurable filtering and processing of the digital audio paths. The DSP provides low-pass / high-pass filtering, 3D stereo enhancement, notch filters, 5-band EQ, dynamic range control and a programmable DF1 digital filter. The tuned notch filters allow narrow frequency bands to be attenuated, to provide filtering of motor noise or other unwanted sounds; the 5-band EQ allows the signal to be adjusted for user-preferences. The dynamic range control provides a range of compression, limiting and noise gate functions to support optimum configuration for recording or playback modes. The DF1 filter allows user-specified algorithms to be implemented in the digital signal chain.

The ReTune™ feature is a highly-configurable DSP algorithm which can be tailored to cancel or compensate for imperfect characteristics of the housing, loudspeaker or microphone components in the target application. The ReTune™ algorithm coefficients and register contents are calculated using Cirrus Logic's WISCE™ software; lab bench tests and audio reference measurements must be performed in order to determine the optimum settings.

The digital signal routing between the ADCs, DACs and I2S digital audio interface can be configured in different ways according to the application requirements. The DSP functions may be applied to the ADC record path, or the DAC record path, or may be distributed between these two paths.

Four analogue output mixers are provided, connected to 4 analogue output pins. Twin stereo outputs or stereo headphone/line and mono BTL speaker may be connected to these outputs.

The WM8946 incorporates an LDO regulator for compatibility with a wide range of supply rails; the internal LDO can also reduce any interference resulting from a noisy supply rail. The LDO regulator can also be used to provide a regulated supply voltage to other circuits.

I2C or SPI control interface modes for read/write access to the register map. A single external clock provides timing reference for all the digital functions; an integrated Frequency Locked Loop (FLL) also provides flexibility to perform frequency conversions and to remove noise/jitter from the external clock. The FLL can be configured for reduced power consumption, or for different filtering requirements of the reference source.

Additional functions include a current-mode video buffer providing excellent video signal reproduction at low operating voltages. Up to 4 GPIO pins may be configured for miscellaneous input/output, or for status indications from the temperature monitoring functions.

ANALOGUE INPUT SIGNAL PATH

The WM8946 has six analogue input pins, which may be selected in many different configurations. The analogue input paths can support line and microphone inputs, in single-ended or pseudo-differential modes. The auxiliary input pins (AUX1 and AUX2) may be configured as inputs to the input PGAs or to the output mixers.

The Left and Right input PGA audio channels are routed to the Analogue to Digital converters (ADCs). There is also a bypass path for each channel, enabling the signal to be routed directly to the output mixers.

The WM8946 input signal paths and control registers are illustrated in Figure 10.

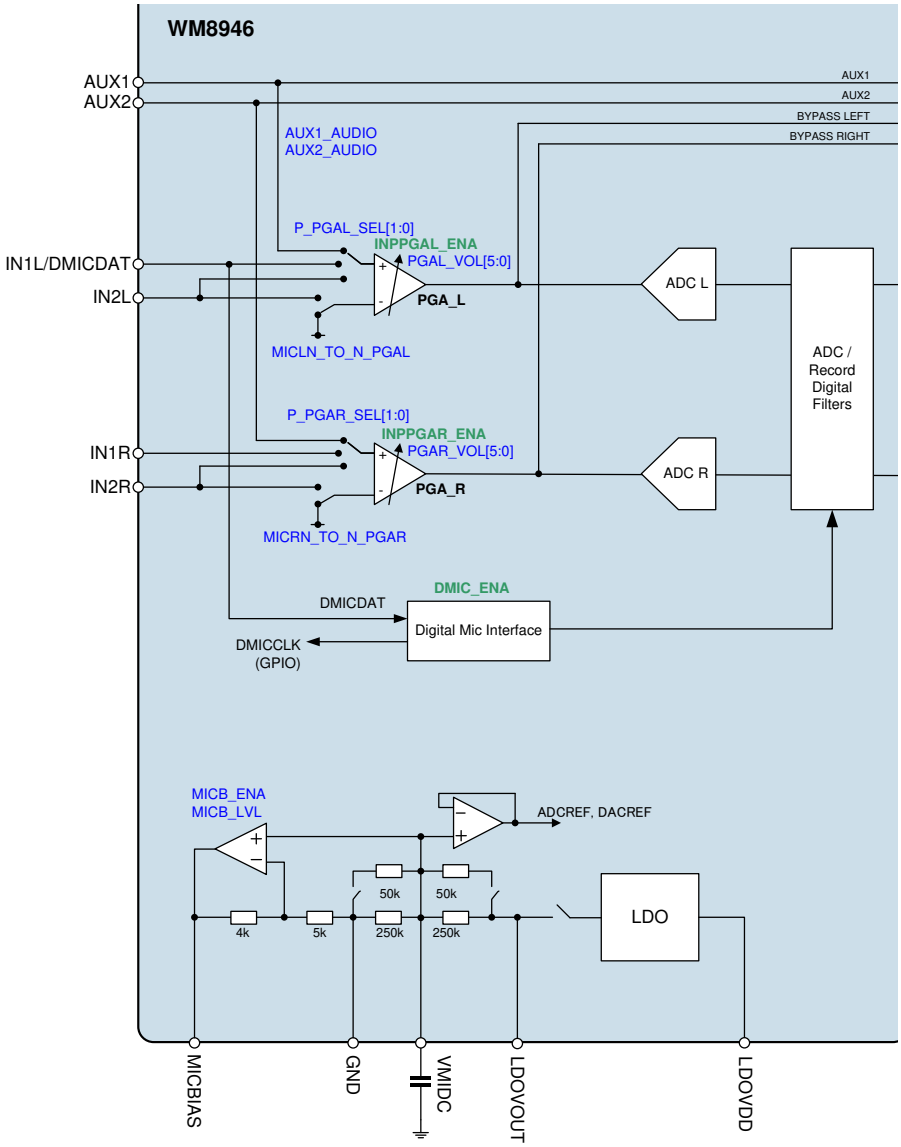


Figure 10 Input Signal Paths

INPUT PGA ENABLE

The input PGAs (Programmable Gain Amplifiers) are enabled using register bits INPPGAR_ENA and INPPGAL_ENA, as described in Table 1.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) Power Management 1	13	INPPGAR_ENA	0	Right Input PGA Enable 0 = Disabled 1 = Enabled
	12	INPPGAL_ENA	0	Left Input PGA Enable 0 = Disabled 1 = Enabled

Table 1 Input PGA Enable

To enable the input PGAs, the reference voltage VMID and the bias current must also be enabled. See "Reference Voltages and Master Bias" for details of the associated controls VMID_SEL and BIAS_ENA.

INPUT PGA CONFIGURATION

Microphone and Line level audio inputs can be connected to the WM8946 in single-ended or differential configurations. (These two configurations are illustrated in Figure 57 and Figure 58 in the section describing the external components requirements - see "Applications Information".)

For single-ended microphone inputs, the microphone signal is connected to the non-inverting input of the PGAs, whilst the inverting inputs of the PGAs are connected to VMID. For differential microphone inputs, the non-inverted microphone signal is connected to the non-inverting input of the PGAs, whilst the inverted (or 'noisy ground') signal is connected to the inverting input pins.

Line level inputs are connected in the same way as a single-ended microphone signal.

The non-inverting input of the PGAs is configured using the P_PGAR_SEL and P_PGAL_SEL registers. These registers allow the selection of three possible input pins to the associated PGA. When the AUX1 or AUX2 pin is used as an audio input, that pin must be configured for audio using the AUX1_AUDIO or AUX2_AUDIO register bits.

The inverting input of the PGAs is configured using MICRN_TO_N_PGAR and MICLN_TO_N_PGAL. These registers allow the PGA to operate in either single-ended or pseudo-differential configuration.

The registers for configuring the Input PGAs are described in Table 2.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R39 (27h) Input Ctrl	8	AUX2_AUDIO	0	AUX2 pin configuration 0 = Non-Audio signal 1 = AC-coupled Audio signal
	7	AUX1_AUDIO	0	AUX1 pin configuration 0 = Non-Audio signal 1 = AC-coupled Audio signal
	5	MICRN_TO_N_PGAR	1	Right Input PGA Inverting Input Select 0 = Connected to VMID 1 = Connected to IN2R
	4	MICLN_TO_N_PGAL	1	Left Input PGA Inverting Input Select 0 = Connected to VMID 1 = Connected to IN2L

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3:2	P_PGAR_SEL [1:0]	01	Right Input PGA Non-Inverting Input Select 00 = Connected to IN2R 01 = Connected to IN1R 10 = Connected to AUX2 11 = Reserved
	1:0	P_PGAL_SEL [1:0]	01	Left Input PGA Non-Inverting Input Select 00 = Connected to IN2L 01 = Connected to IN1L 10 = Connected to AUX1 11 = Reserved

Table 2 Input PGA Configuration

MICROPHONE BIAS CONTROL

The WM8946 provides a low noise reference voltage suitable for biasing electret condenser (ECM) type microphones via an external resistor. Refer to the "Applications Information" section for recommended components. The MICBIAS voltage is enabled using the MICB_ENA register bit; the voltage can be selected using the MICB_LVL bit, as described in Table 3.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 (02h) Power Management 1	4	MICB_ENA	0	Microphone Bias Enable 0 = Disabled 1 = Enabled
R39 (27h) Input Ctrl	6	MICB_LVL	0	Microphone Bias Voltage control 0 = 0.9 x LDOVOUT 1 = 0.65 x LDOVOUT

Table 3 Microphone Bias Control

INPUT PGA GAIN CONTROL

The volume control gain for the Left and Right channels can be independently adjusted using the PGAL_VOL and PGAR_VOL register fields as described in Table 4. The gain range is -12dB to +35.25dB in 0.75dB steps. The gains on the inverting and non-inverting inputs to the PGAs are always equal. Each input PGA can be independently muted using the PGA mute bits.

To prevent "zipper noise", a zero-cross function is provided on the input PGAs. When this feature is enabled, volume updates will not take place until a zero-crossing is detected. In the case of a long period without zero-crossings, a timeout function is provided. When the zero-cross function is enabled, the volume will update after the timeout period if no earlier zero-cross has occurred. The timeout clock is enabled using TOCLK_ENA. See "Clocking and Sample Rates" for the definition of this bit. Note that the zero-cross function can be supported without TOCLK enabled, but the timeout function will not be provided in this case.

The PGA_VU bits control the loading of the input PGA volume data. When PGA_VU is set to 0, the PGA volume data will be loaded into the respective control register, but will not actually change the gain setting. The left and right input PGA volume settings are both updated when a 1 is written to PGA_VU; this makes it possible to update the gain of the left and right signal paths simultaneously.

Note that SYSCLK must be enabled when writing to the PGA_VU bits. (See "Clocking and Sample Rates" for details of SYSCLK.)