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WM8950

ADC with Microphone Input and Programmable Digital Filters

DESCRIPTION

The WM8950 is a low power, high quality mono ADC designed for portable applications such as Digital Still Camera, Digital Voice Recorder or games console accessories.

The device integrates support for a differential or single ended mic. External component requirements are reduced as no separate microphone amplifiers are required.

Advanced Sigma Delta Converters are used along with digital decimation filters to give high quality audio at sample rates from 8 to 48ks/s. Additional digital filtering options are available, to cater for application filtering such as wind noise reduction, noise rejection, plus an advanced mixed signal ALC function with noise gate is provided.

An on-chip PLL is provided to generate the required Master Clock from an external reference clock. The PLL clock can also be output if required elsewhere in the system.

The WM8950 operates at supply voltages from 2.5 to 3.6V, although the digital supplies can operate at voltages down to 1.71V to save power. Different sections of the chip can also be powered down under software control by way of the selectable two or three wire control interface.

WM8950 is supplied in a very small 4x4mm QFN package, offering high levels of functionality in minimum board area, with high thermal performance.

FEATURES

Mono ADC:

- Audio sample rates:8, 11.025, 16, 22.05, 24, 32, 44.1, 48kHz
- SNR 94dB, THD -83dB (‘A’-weighted @ 8 – 48ks/s)
- Multiple auxiliary analogue inputs

Mic Preamps:

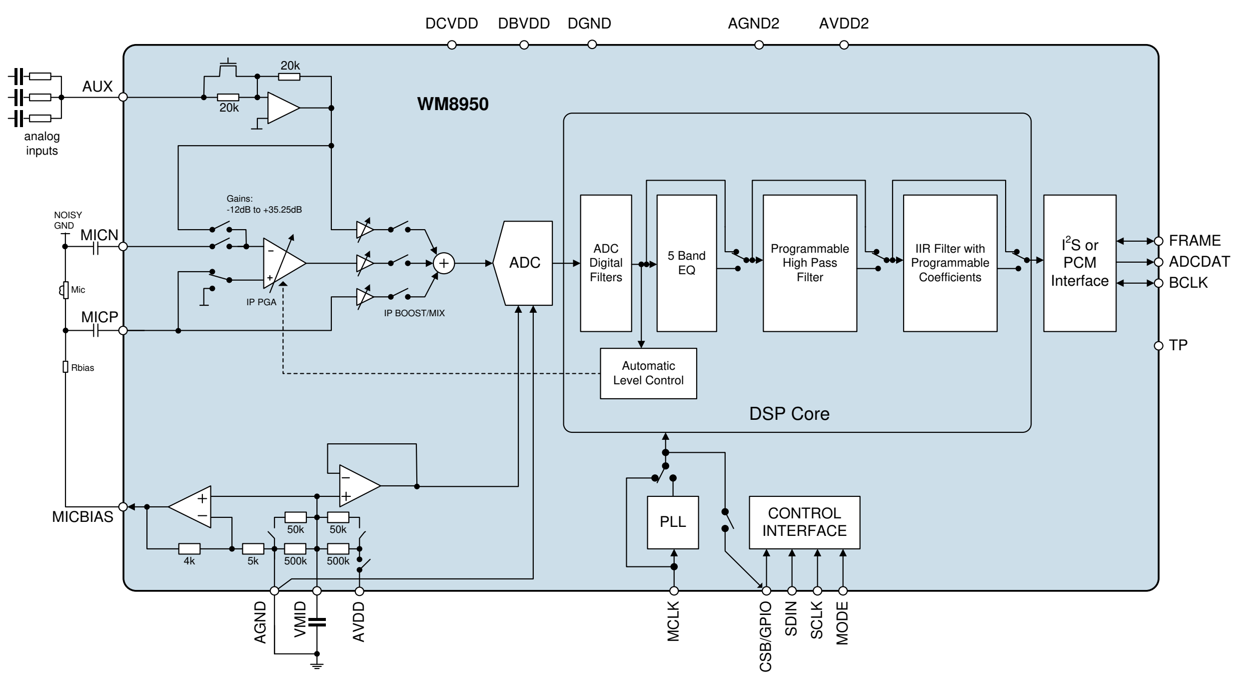
- Differential or single end Microphone Interface
  - Programmable preamp gain
  - Pseudo differential inputs with common mode rejection
  - Programmable ALC / Noise Gate in ADC path
- Low-noise bias supplied for electret microphones

OTHER FEATURES

- 5 band EQ
- Programmable High-Pass Filter (wind noise reduction)
- Fully Programmable IIR Filter (notch filter)
- On-chip PLL
- Low power, low voltage
  - 2.5V to 3.6V (digital: 1.71V to 3.6V)
  - power consumption 10mA all-on 48ks/s mode
- 4x4x0.9mm 24 lead QFN package

APPLICATIONS

- Digital Still Camera
- General Purpose low power audio ADC
- Games console accessories
- Voice recorders



Rev 4.5
AUG ‘16

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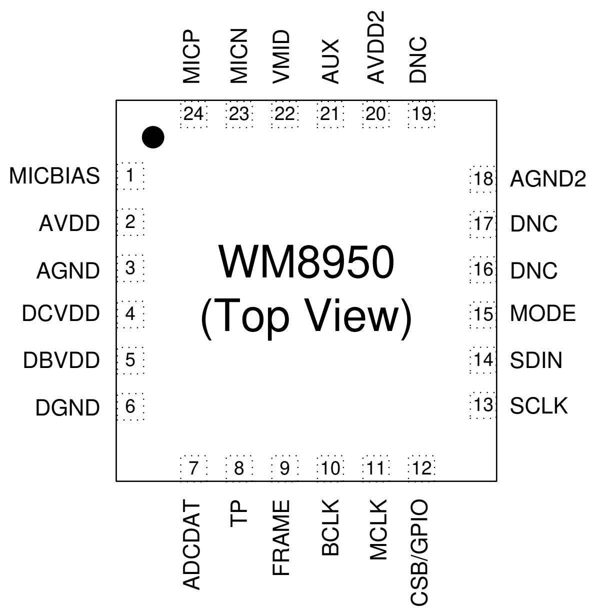
PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PACKAGE BODY TEMPERATURE
WM8950CGEFL/V	-40°C to +85°C	24-lead QFN (4x4x0.9mm) (Pb-free)	MSL3	260ºC
WM8950CGEFL/RV	-40°C to +85°C	24-lead QFN (4x4x0.9mm) (Pb-free, tape and reel)	MSL3	260ºC

Note:

Reel Quantity = 3,500

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
1	MICBIAS	Analogue Output	Microphone bias
2	AVDD	Supply	Analogue supply (feeds ADC)
3	AGND	Supply	Analogue ground (feeds ADC)
4	DCVDD	Supply	Digital core supply
5	DBVDD	Supply	Digital buffer (input/output) supply
6	DGND	Supply	Digital ground
7	ADCDAT	Digital Output	ADC digital audio data output
8	TP	Test Pin	Connect to ground
9	FRAME	Digital Input / Output	ADC sample rate clock or frame synch
10	BCLK	Digital Input / Output	Digital audio bit clock
11	MCLK	Digital Input	Master clock input
12	CSB/GPIO	Digital Input / Output	3-Wire MPU chip select or general purpose input/output pin.
13	SCLK	Digital Input	3-Wire MPU clock Input / 2-Wire MPU Clock Input
14	SDIN	Digital Input / Output	3-Wire MPU data Input / 2-Wire MPU Data Input
15	MODE	Digital Input	Control interface mode selection pin.
16	DNC	Do not connect	Leave this pin floating
17	DNC	Do not connect	Leave this pin floating
18	AGND2	Supply	Analogue ground
19	DNC	Do not connect	Leave this pin floating
20	AVDD2	Supply	Analogue supply
21	AUX	Analogue Input	Auxiliary analogue input
22	VMID	Reference	Decoupling for midrail reference voltage
23	MICN	Analogue Input	Microphone negative input
24	MICP	Analogue Input	Microphone positive input (common mode)

Note:

It is recommended that the QFN ground paddle should be connected to analogue ground on the application PCB.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus Logic tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
DBVDD, DCVDD, AVDD, AVDD2 supply voltages	-0.3V	+4.2
Voltage range digital inputs	DGND -0.3V	DVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Operating temperature range, T_A	-40°C	+85°C
Storage temperature prior to soldering	30°C max / 85% RH max	
Storage temperature after soldering	-65°C	+150°C

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD	1.71		3.6	V
Digital supply range (Buffer)	DBVDD	1.71		3.6	V
Analogue supplies range	AVDD, AVDD2	2.5		3.6	V
Ground	DGND, AGND, AGND2		0		V

Notes:

1. When using PLL, DCVDD must be 1.9V or higher.
2. AVDD must be ≥ DBVDD and DCVDD.
3. DBVDD must be ≥ DCVDD.
4. When using PLL, DCVDD must be ≥ 1.9V.

ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD = 1.8V, AVDD = DBVDD = 3.3V, SPKVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Inputs (MICN, MICP)						
Full-scale Input Signal Level (Note 1) – note this changes with AVDD	V_{INFS}	PGABOOST = 0dB INPPGAVOL = 0dB		1.0 0		Vrms dBV
Mic PGA equivalent input noise	At 35.25dB gain			150		uV
Input resistance	R_{MICIN}	Gain set to 35.25dB		1.6		kΩ
Input resistance	R_{MICIN}	Gain set to 0dB		47		kΩ
Input resistance	R_{MICIN}	Gain set to -12dB		75		kΩ
Input resistance	R_{MICIP}	(Constant for all gain settings)		94		kΩ
Input Capacitance	C_{MICIN}			10		pF
MIC Input Programmable Gain Amplifier (PGA)						
Maximum Programmable Gain				35.25		dB
Minimum Programmable Gain				-12		dB
Programmable Gain Step Size		Guaranteed monotonic		0.75		dB
Mute Attenuation				108		dB
Selectable Input Gain Boost (0/+20dB)						
Gain Boost			0		20	dB
Automatic Level Control (ALC)/Limiter						
Target Record Level			-28.5		-6	dB
Maximum Programmable Gain				35.25		dB
Minimum Programmable Gain				-12		dB
Programmable Gain Step Size		Guaranteed Monotonic		0.75		dB
Gain Hold Time (Note 2)	t_{HOLD}	MCLK=12.288MHz (Note 4)		0, 2.67, 5.33, 10.67, … , 43691 (time doubles with each step)		ms
Gain Ramp-Up (Decay) Time (Note 3)	t_{DCY}	ALCMODE=0 (ALC), MCLK=12.288MHz (Note 4)		3.3, 6.6, 13.1, … , 3360 (time doubles with each step)		ms
		ALCMODE=1 (limiter), MCLK=12.288MHz (Note 4)		0.73, 1.45, 2.91, … , 744 (time doubles with each step)		
Gain Ramp-Down (Attack) Time (Note 3)	t_{ATK}	ALCMODE=0 (ALC), MCLK=12.288MHz (Note 4)		0.83, 1.66, 3.33, … , 852 (time doubles with each step)		ms
		ALCMODE=1 (limiter), MCLK=12.288MHz (Note 4)		0.18, 0.36, 0.73, … , 186 (time doubles with each step)		
Analogue to Digital Converter (ADC)						
Signal to Noise Ratio (Note 5, 6)		A-weighted, 0dB PGA gain	85	94		dB
Total Harmonic Distortion + Noise (Note 6)	THD+N	-1dBFS input 0dB PGA gain	-75	-83		dB
Auxiliary Analogue Input (AUX)						
Full-scale Input Signal Level (0dB) – note this changes with AVDD	V_{INFS}			1.0 0		Vrms dBV
Input Resistance	R_{AUXIN}	AUXMODE=0		20		kΩ
Input Capacitance	C_{AUXIN}			10		pF

Test Conditions

DCVDD = 1.8V, AVDD = DBVDD = 3.3V, SPKVDD = 3.3V, T_A = +25ºC, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Bias						
Bias Voltage (MBVSEL=0)	$V_{MICBIAS}$			0.9 x AVDD		V
Bias Voltage (MBVSEL=1)	$V_{MICBIAS}$			0.75 x AVDD		V
Bias Current Source	$I_{MICBIAS}$				3	mA
Output Noise Voltage	Vn	1K to 20kHz		15		nV/√Hz
Digital Input / Output						
Input HIGH Level	V_{IH}		0.7 × DVDD			V
Input LOW Level	V_{IL}				0.3 × DVDD	V
Output HIGH Level	V_{OH}	I_{OL}=1mA	0.9 × DVDD			V
Output LOW Level	V_{OL}	I_{OH}-1mA			0.1 x DVDD	V

TERMINOLOGY

1. MICN input only in single ended microphone configuration. Maximum input signal to MICP without distortion is -3dBV.
2. Hold Time is the length of time between a signal detected being too quiet and beginning to ramp up the gain. It does not apply to ramping down the gain when the signal is too loud, which happens without a delay.
3. Ramp-up and Ramp-Down times are defined as the time it takes for the PGA to change its gain by 6dB.
4. All hold, ramp-up and ramp-down times scale proportionally with MCLK
5. Signal-to-noise ratio (dB) – SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
6. THD+N (dB) – THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

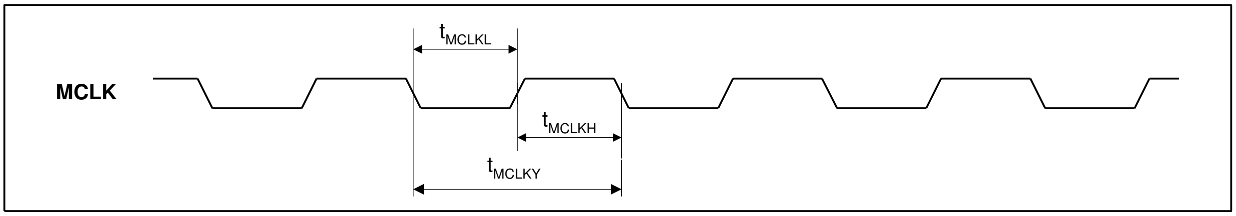


Figure 1 System Clock Timing Requirements

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD=3.3V, DGND=AGND=SPKGND=0V, T_A = +25°C, Slave Mode fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK cycle time	T_{MCLKY}	MCLK as direct SYSCLK source (CLKSEL=0)	81.38			ns
		MCLK as input to PLL (see note) (CLKSEL=1)	20			ns
MCLK duty cycle	T_{MCLKDS}		60:40		40:60	

Note: PLL pre-scaling and PLL N and K values should be set appropriately so that SYSCLK is no greater than 12.288MHz.

AUDIO INTERFACE TIMING – MASTER MODE

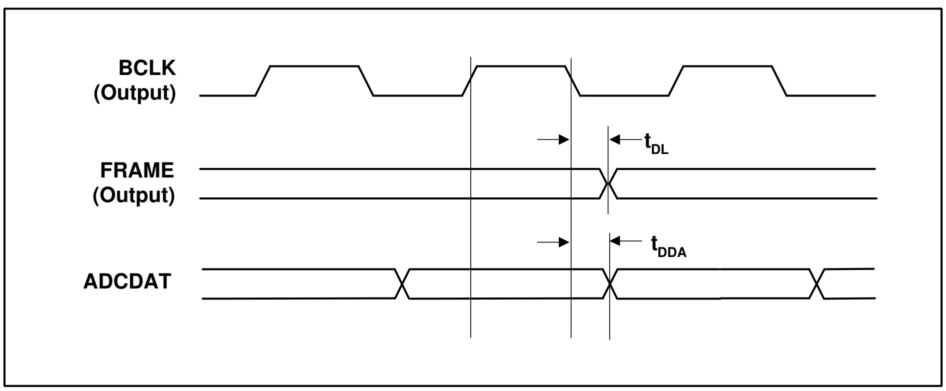


Figure 2 Digital Audio Data Timing – Master Mode (see Control Interface)

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD=3.3V, DGND=AGND=SPKGND=0V, T_A = +25°C, Master Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
FRAME propagation delay from BCLK falling edge	t_{DL}			10	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			10	ns

AUDIO INTERFACE TIMING – SLAVE MODE

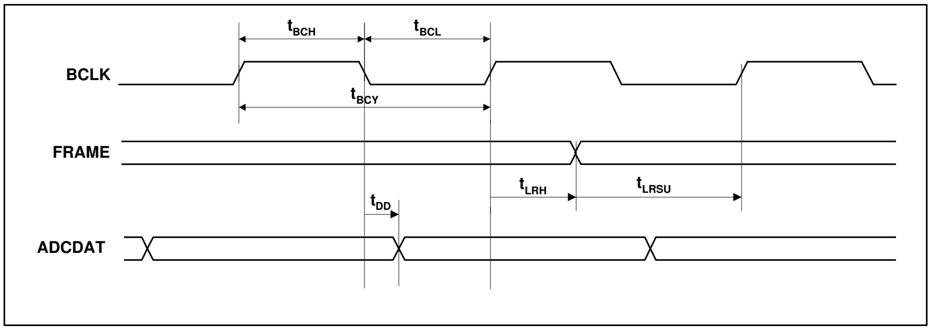


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD=3.3V, DGND=AGND=SPKGND=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK= 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t_{BCY}	50			ns
BCLK pulse width high	t_{BCH}	20			ns
BCLK pulse width low	t_{BCL}	20			ns
FRAME set-up time to BCLK rising edge	t_{LRSU}	10			ns
FRAME hold time from BCLK rising edge	t_{LRH}	10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			20	ns

Note: BCLK period should always be greater than or equal to MCLK period.

CONTROL INTERFACE TIMING – 3-WIRE MODE

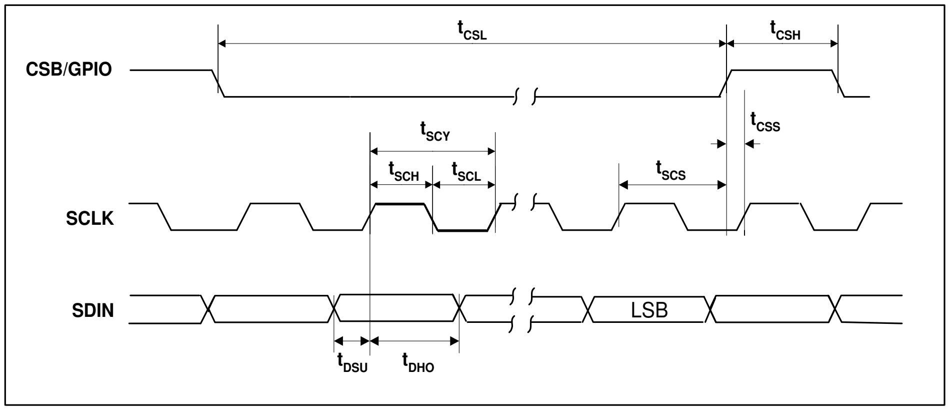


Figure 4 Control Interface Timing – 3-Wire Serial Control Mode

Test Conditions

DCVDD = 1.8V, DBVDD = AVDD = SPKVDD = 3.3V, DGND = AGND = SPKGND = 0V, T_A = +25ºC, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB rising edge	t_{SCS}	80			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDIN to SCLK set-up time	t_{DSU}	40			ns
SCLK to SDIN hold time	t_{DHO}	40			ns
CSB pulse width low	t_{CSL}	40			ns
CSB pulse width high	t_{CSH}	40			ns
CSB rising to SCLK rising	t_{CSS}	40			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

CONTROL INTERFACE TIMING – 2-WIRE MODE

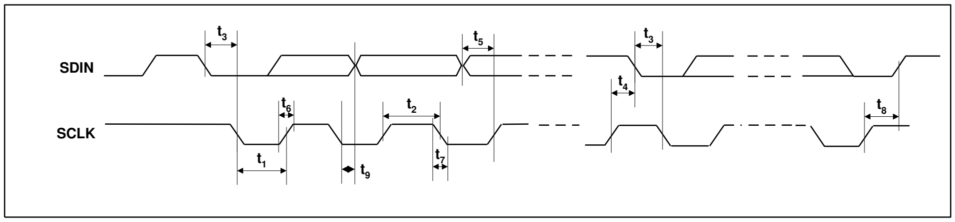


Figure 5 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD=3.3V, DGND=AGND=SPKGND=0V, T_A = +25ºC, Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency		0		526	kHz
SCLK Low Pulse-Width	t_1	1.3			us
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDIN, SCLK Rise Time	t_6			300	ns
SDIN, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

DEVICE DESCRIPTION

INTRODUCTION

The WM8950 is a low power audio ADC, with flexible line and microphone input. Applications for this device include games console accessories, digital still cameras, voice recorders and other general purpose audio applications.

The chip offers great flexibility in use, and so can support many different modes of operation as follows:

MICROPHONE INPUTS

Microphone inputs are provided, allowing for either a differential microphone input or a single ended microphone to be connected. These inputs have a user programmable gain range of -12dB to +35.25dB using internal resistors. After the input PGA stage comes a boost stage which can add a further 20dB of gain. A microphone bias is output from the chip which can be used to bias the microphones. The signal routing can be configured to allow manual adjustment of mic levels, or to allow the ALC loop to control the level of mic signal that is transmitted.

Total gain through the microphone paths of up to +55.25dB can be selected.

PGA AND ALC OPERATION

A programmable gain amplifier is provided in the input path to the ADC. This may be used manually or in conjunction with a mixed analogue/digital automatic level control (ALC) which keeps the recording volume constant.

AUX INPUT

The device includes a mono input, AUX, that can be used as an input for warning tones (beep) etc. This path can also be summed into the input in a flexible fashion, either to the input PGA as a second microphone input or as a line input. The configuration of this circuit, with integrated on-chip resistors allows several analogue signals to be summed into the single AUX input if required.

ADC

The mono ADC uses a multi-bit high-order oversampling architecture to deliver optimum performance with low power consumption. Various sample rates are supported, from the 8ks/s rate typically used in voice dictation, up to the 48ks/s rate used in high quality audio applications.

DIGITAL FILTERING

Advanced Sigma Delta Converters are used along with digital decimation and interpolation filters to give high quality audio at sample rates from 8ks/s to 48ks/s.

Application specific digital filters are also available which help to reduce the effect of specific noise sources such as 'wind noise'. The filters include a programmable ADC high-pass filter, an IIR filter with fully programmable coefficients, and a 5-band equaliser that can be applied to the record path in order to improve the overall audio sound from the device.

AUDIO INTERFACES

The WM8950 has a standard audio interface, to support the transmission of audio data from the chip. This interface is a 4 wire standard audio interface which supports a number of audio data formats including I^2S, DSP Mode, MSB-First, left justified and MSB-First, right justified, and can operate in master or slave modes.

CONTROL INTERFACES

To allow full software control over all its features, the WM8950 offers a choice of 2 or 3 wire MPU control interface. It is fully compatible and an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs. The selection between 2-wire mode and 3-wire mode is determined by the state of the MODE pin. If MODE is high then 3-wire control mode is selected, if MODE is low then 2-wire control mode is selected.

In 2 wire mode, only slave operation is supported, and the address of the device is fixed as 0011010.

CLOCKING SCHEMES

WM8950 offers the normal audio clocking scheme operation, where 256fs MCLK is provided to the ADC.

However, a PLL is also included which may be used to generate the internal master clock frequency in the event that this is not available from the system controller. The PLL uses an input reference (typically, the 12MHz USB clock) to generate high quality audio clocks. If the PLL is not required for generation of these clocks, it can be reconfigured to generate alternative clocks which may then be output on the CSB/GPIO pin and used elsewhere in the system.

POWER CONTROL

The design of the WM8950 has given much attention to power consumption without compromising performance. It operates at low supply voltages, and includes the facility to power off any unused parts of the circuitry under software control, includes standby and power off modes.

INPUT SIGNAL PATH

The WM8950 has 3 flexible analogue inputs: two microphone inputs, and an auxiliary input. These inputs can be used in a variety of ways. The input signal path before the ADC has a flexible PGA block which then feeds into a gain boost/mixer stage.

MICROPHONE INPUTS

The WM8950 can accommodate a variety of microphone configurations including single ended and differential inputs. The inputs through the MICN, MICP and optionally AUX pins are amplified through the input PGA as shown in Figure 6 .

A pseudo differential input is the preferential configuration where the positive terminal of the input PGA is connected to the MICP input pin by setting MICP2INPPGA=1. The microphone ground should then be connected to MICN (when MICN2INPPGA=1) or optionally to AUX (when AUX2INPPGA=1) input pins.

Alternatively a single ended microphone can be connected to the MICN input with MICN2INPPGA set to 1. The non-inverting terminal of the input PGA should be connected internally to VMID by setting MICP2INPPGA to 0.

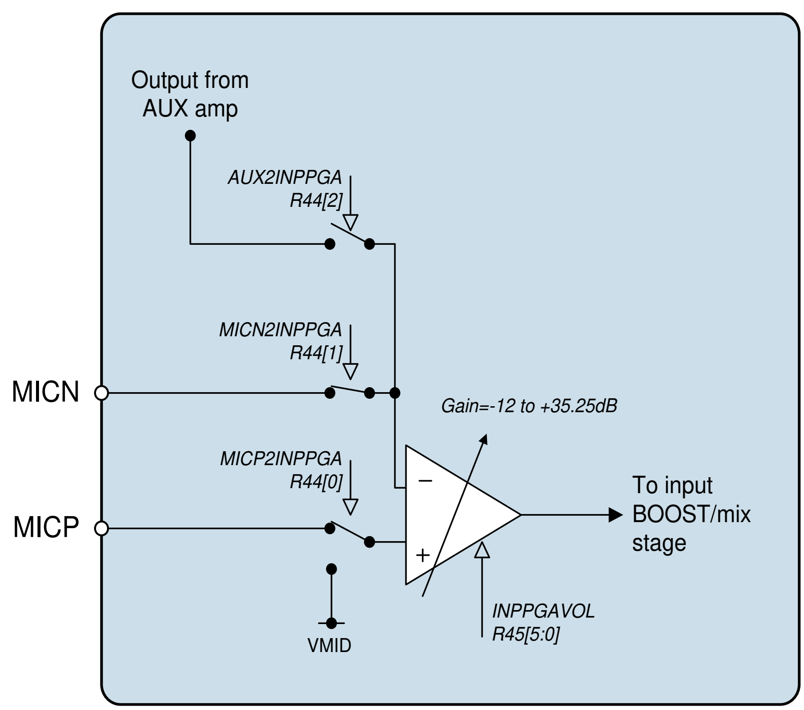


Figure 6 Microphone Input PGA Circuit (switch positions shown are for differential mic input)

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R44 Input Control	0	MICP2INPPGA	1	Connect input PGA amplifier positive terminal to MICP or VMID. 0 = input PGA amplifier positive terminal connected to VMID 1 = input PGA amplifier positive terminal connected to MICP through variable resistor string
	1	MICN2INPPGA	1	Connect MICN to input PGA negative terminal. 0=MICN not connected to input PGA 1=MICN connected to input PGA amplifier negative terminal.
	2	AUX2INPPGA	0	Select AUX amplifier output as input PGA signal source. 0=AUX not connected to input PGA 1=AUX connected to input PGA amplifier negative terminal.

The input PGA is enabled by the IPPGAEN register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 Power Management 2	2	INPPGAEN	0	Input microphone PGA enable 0 = disabled 1 = enabled

INPUT PGA VOLUME CONTROL

The input microphone PGA has a gain range from -12dB to +35.25dB in 0.75dB steps. The gain from the MICN input to the PGA output and from the AUX amplifier to the PGA output are always common and controlled by the register bits INPPGAVOL[5:0]. These register bits also affect the MICP pin when MICP2INPPGA=1.

When the Automatic Level Control (ALC) is enabled the input PGA gain is then controlled automatically and the INPPGAVOL bits should not be used.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R45 Input PGA volume control	5:0	INPPGAVOL	010000	Input PGA volume 000000 = -12dB 000001 = -11.25dB . 010000 = 0dB . 111111 = 35.25dB
	6	INPPGAMUTE	0	Mute control for input PGA: 0=Input PGA not muted, normal operation 1=Input PGA muted (and disconnected from the following input BOOST stage).
	7	INPPGAZC	0	Input PGA zero cross enable: 0=Update gain when gain register changes 1=Update gain on 1st zero cross after gain register write.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 ALC control 1	8	ALCSEL	0	ALC function select: 0=ALC off (PGA gain set by INPPGAVOL register bits) 1=ALC on (ALC controls PGA gain)

Table 1 Input PGA Volume Control

AUXILIARY INPUT

An auxiliary input circuit (Figure 7) is provided which consists of an amplifier which can be configured either as an inverting buffer for a single input signal or as a mixer/summer for multiple inputs with the use of external resistors. The circuit is enabled by the register bit AUXEN.

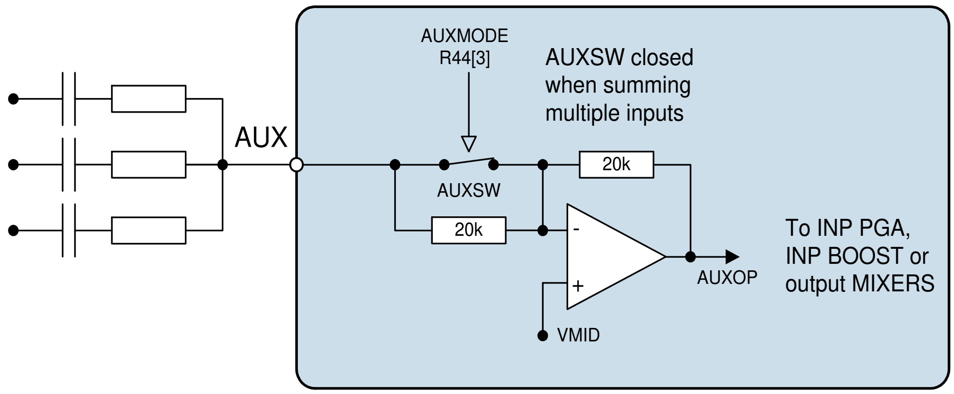


Figure 7 Auxiliary Input Circuit

The AUXMODE register bit controls the auxiliary input mode of operation:

In buffer mode (AUXMODE=0) the switch labelled AUXSW in Figure 7 is open and the signal at the AUX pin will be buffered and inverted through the aux circuit using only the internal components.

In mixer mode (AUXMODE=1) the on-chip input resistor is bypassed, this allows the user to sum in multiple inputs with the use of external resistors. When used in this mode there will be gain variations through this path from part to part due to the variation of the internal 20kΩ resistors relative to the higher tolerance external resistors.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 Power management 1	6	AUXEN	0	Auxiliary input buffer enable 0 = OFF 1 = ON
R44 Input control	3	AUXMODE	0	0 = inverting buffer 1 = mixer (on-chip input resistor bypassed)

Table 2 Auxiliary Input Buffer Control

INPUT BOOST

The input BOOST circuit has 3 selectable inputs: the input microphone PGA output, the AUX amplifier output and the MICP input pin (when not using a differential microphone configuration). These three inputs can be mixed together and have individual gain boost/adjust as shown in Figure 8.

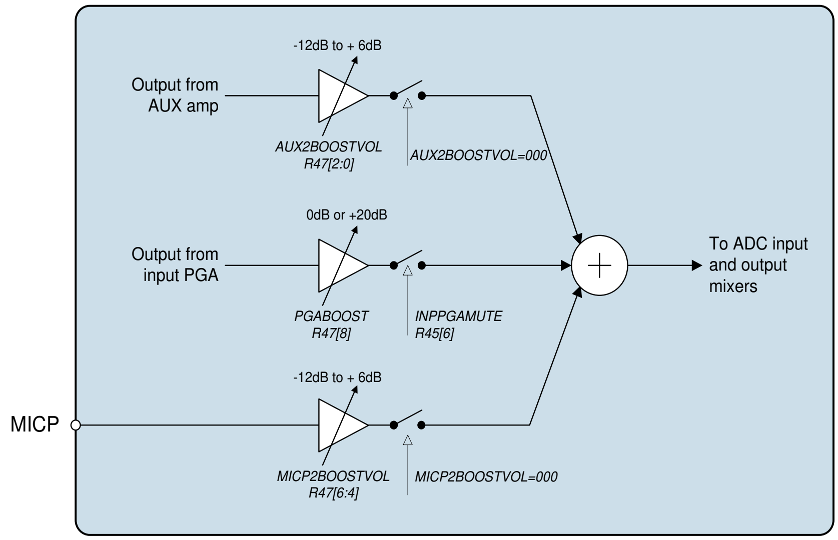


Figure 8 Input Boost Stage

The input PGA path can have a +20dB boost (PGABOOST=1) a 0dB pass through (PGABOOST=0) or be completely isolated from the input boost circuit (INPPGAMUTE=1).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R45 Input PGA gain control	6	INPPGAMUTE	0	Mute control for input PGA: 0=Input PGA not muted, normal operation 1=Input PGA muted (and disconnected from the following input BOOST stage).
R47 Input BOOST control	8	PGABOOST	1	0 = PGA output has +0dB gain through input BOOST stage. 1 = PGA output has +20dB gain through input BOOST stage.

Table 3 Input BOOST Stage Control

The Auxiliary amplifier path to the BOOST stage is controlled by the AUX2BOOSTVOL[2:0] register bits. When AUX2BOOSTVOL=000 this path is completely disconnected from the BOOST stage. Settings 001 through to 111 control the gain in 3dB steps from -12dB to +6dB.

The MICP path to the BOOST stage is controlled by the MICP2BOOSTVOL[2:0] register bits. When MICP2BOOSTVOL=000 this input pin is completely disconnected from the BOOST stage. Settings 001 through to 111 control the gain in 3dB steps from -12dB to +6dB.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R47 Input BOOST control	2:0	AUX2BOOSTVOL	000	Controls the auxiliary amplifier to the input boost stage: 000=Path disabled (disconnected) 001=-12dB gain through boost stage 010=-9dB gain through boost stage … 111=+6dB gain through boost stage
	6:4	MICP2BOOSTVOL	000	Controls the MICP pin to the input boost stage (NB, when using this path set MICPZIUNPPGA=0): 000=Path disabled (disconnected) 001=-12dB gain through boost stage 010=-9dB gain through boost stage … 111=+6dB gain through boost stage

Table 4 Input BOOST Stage Control

The BOOST stage is enabled under control of the BOOSTEN register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 Power management 2	4	BOOSTEN	0	Input BOOST enable 0 = Boost stage OFF 1 = Boost stage ON

Table 5 Input BOOST Enable Control

MICROPHONE BIASING CIRCUIT

The MICBIAS output provides a low noise reference voltage suitable for biasing electret type microphones and the associated external resistor biasing network. Refer to the Applications Information section for recommended external components. The MICBIAS voltage can be altered via the MBVSEL register bit. If MBVSEL = 0, the MICBIAS voltage is 0.9 x AVDD. If MBVSEL = 1, the MICBIAS voltage is 0.75 x AVDD. The output can be enabled or disabled using MICBEN.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R1 Power management 1	4	MICBEN	0	Microphone Bias Enable 0 = OFF (high impedance output) 1 = ON

Table 6 Microphone Bias Enable

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R44 Input Control	8	MBVSEL	0	Microphone Bias Voltage Control 0 = 0.9 x AVDD 1 = 0.75 x AVDD

Table 7 Microphone Bias Voltage Control

The internal MICBIAS circuitry is shown in Figure 9. Note that the maximum source current capability for MICBIAS is 3mA. The external biasing resistors therefore must be large enough to limit the MICBIAS current to 3mA.

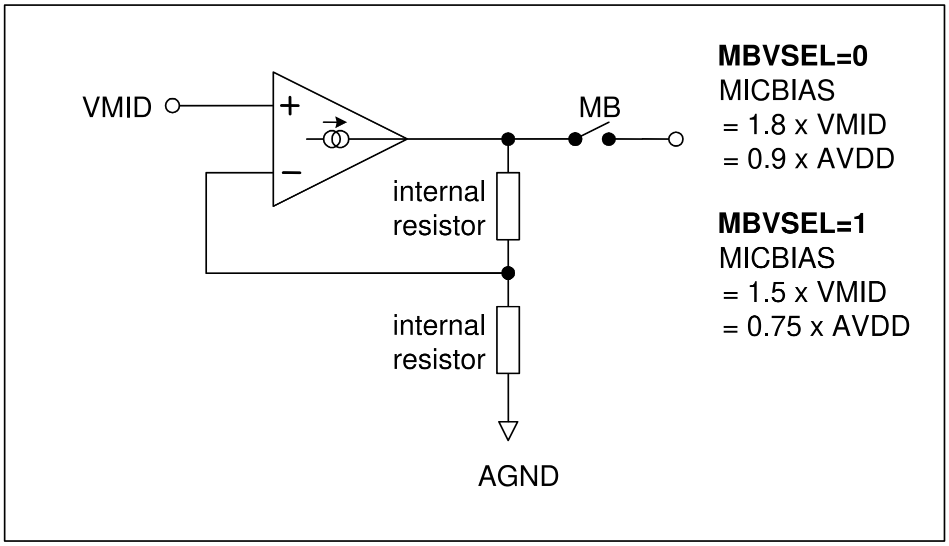


Figure 9 Microphone Bias Schematic

ANALOGUE TO DIGITAL CONVERTER (ADC)

The WM8950 uses a multi-bit, oversampled sigma-delta ADC channel. The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise. The ADC Full Scale input level is proportional to AVDD. With a 3.3V supply voltage, the full scale level is $1.0V_{rms}$. Any voltage greater than -1dBfs may overload the ADC and cause distortion.

ADC DIGITAL FILTERS

The ADC filters perform true 24 bit signal processing to convert the raw multi-bit oversampled data from the ADC to the correct sampling frequency to be output on the digital audio interface. The digital filter path is illustrated in Figure 10 **.**

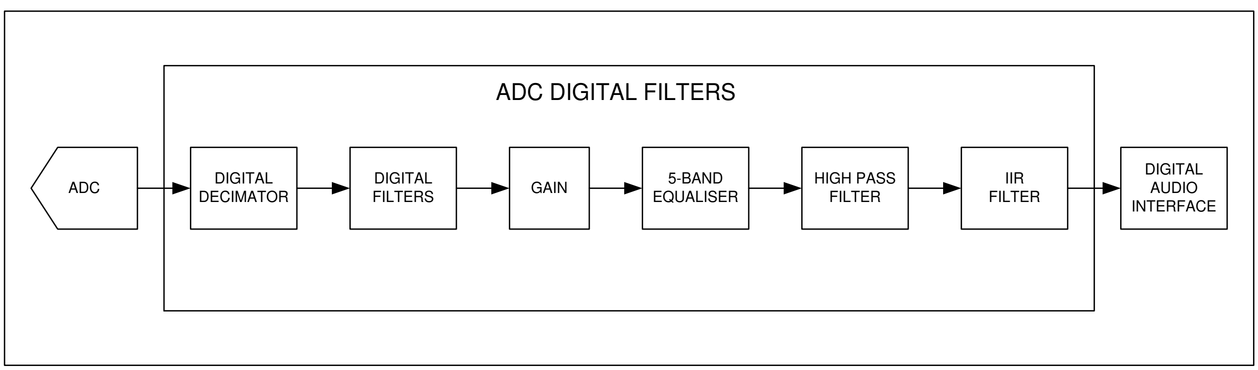


Figure 10 ADC Digital Filter Path

The ADC is enabled by the ADCEN register bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 Power management 2	0	ADCEN	0	0 = ADC disabled 1 = ADC enabled

Table 8 ADC Enable

The polarity of the output signal can also be changed under software control using the ADCPOL register bit. The oversampling rate of the ADC can be adjusted using the ADCOSR register bit. With ADCOSR=0 the oversample rate is 64x which gives lowest power operation and when ADCOSR=1 the oversample rate is 128x which gives best performance.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R14 ADC Control	3	ADCOSR	0	ADC oversample rate select: 0=64x (lower power) 1=128x (best performance)
	0	ADCPOL	0	0=normal 1=inverted

Table 9 ADC Oversample Rate Select

SELECTABLE HIGH-PASS FILTER

A selectable high-pass filter is provided. To disable this filter set HPFEN=0. The filter has two modes controlled by HPFAPP. In Audio Mode (HPFAPP=0) the filter is first order, with a cut-off frequency of 3.7Hz. In Application Mode (HPFAPP=1) the filter is second order, with a cut-off frequency selectable via the HPFCUT register. The cut-off frequencies when HPFAPP=1 are shown in Table 11.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R14 ADC Control	8	HPFEN	1	High-Pass Filter Enable 0=disabled 1=enabled
	7	HPFAPP	0	Select audio mode or application mode 0=Audio mode (1^{st} order, fc = ~3.7Hz) 1=Application mode (2^{nd} order, fc = HPFCUT)
	6:4	HPFCUT	000	Application mode cut-off frequency See Table 11 for details.

Table 10 ADC Filter Select

HPFCUT [2:0]	SAMPLE FREQUENCY (kHz)								
	8	11.025	12	16	22.05	24	32	44.1	48
	SR=101/100			SR=011/010			SR=001/000		
000	82	113	122	82	113	122	82	113	122
001	102	141	153	102	141	153	102	141	153
010	131	180	196	131	180	196	131	180	196
011	163	225	245	163	225	245	163	225	245
100	204	281	306	204	281	306	204	281	306
101	261	360	392	261	360	392	261	360	392
110	327	450	490	327	450	490	327	450	490
111	408	563	612	408	563	612	408	563	612

Table 11 High-Pass Filter Cut-off Frequencies (HPFAPP=1) Values in Hz

Note that the High-Pass filter values (when HPFAPP=1) work on the basis that the SR register bits are set correctly for the actual sample rate as shown in Table 11.

PROGRAMMABLE IIR FILTER

An IIR filter with fully programmable coefficients is provided, typically used as a notch filter for removing narrow band noise at a given frequency. This notch filter has a variable centre frequency and bandwidth, programmable via two coefficients, a0 and a1. These coefficients should be converted to 2's complement numbers to determine the register values. a0 and a1 are represented by the register bits NFA0[13:0] and NFA1[13:0]. Because these coefficient values require four register writes to setup there is an NFU (Notch Filter Update) flag which should be set only when all four registers are setup.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R27 Notch Filter 1	6:0	NFA0[13:7]	0	Notch filter a0 coefficient, bits [13:7]
	7	NFEN	0	Notch filter enable: 0=Disabled 1=Enabled
	8	NFU	0	Notch filter update. The notch filter values used internally only update when one of the NFU bits is set high.
R28 Notch Filter 2	6:0	NFA0[6:0]	0	Notch filter a0 coefficient, bits [6:0]
	8	NFU]	0	Notch filter update. The notch filter values used internally only update when one of the NFU bits is set high.
R29 Notch Filter 3	6:0	NFA1[13:7]	0	Notch filter a1 coefficient, bits [13:7]
	8	NFU	0	Notch filter update. The notch filter values used internally only update when one of the NFU bits is set high.
R30 Notch Filter 4	6:0	NFA1[6:0]	0	Notch filter a1 coefficient, bits [6:0]
	8	NFU	0	Notch filter update. The notch filter values used internally only update when one of the NFU bits is set high.

Table 12 Notch Filter Function

The coefficients are calculated as follows:

$$a_0 = \frac{1-\tan(w_b/2)}{1+\tan(w_b/2)}$$

$$a_1 = -(1+a_0)\cos(w_0)$$

Where:

$$w_0 = 2\pi f_c / f_s$$

$$w_b = 2\pi f_b / f_s$$

f_c = centre frequency in Hz, f_b = -3dB bandwidth in Hz, f_s = sample frequency in Hz

The coefficients are calculated as follows:

NFA0 = -a0 x 2^{13}

NFA1 = -a1 x 2^{12}

These values are then converted to 2's complement notation to determine the register values.

NOTCH FILTER WORKED EXAMPLE

The following example illustrates how to calculate the a0 and a1 coefficients for a desired centre frequency and -3dB bandwidth.

fc = 1000 Hz

fb = 100 Hz

fs = 48000 Hz

$w_0 = 2\pi f_c / f_s = 2\pi$ x (1000 / 48000) = 0.1308996939 rads

$w_b = 2\pi f_b / f_s = 2\pi$ x (100 / 48000) = 0.01308996939 rads

$$a_0 = \frac{1 - \tan(w_b/2)}{1 + \tan(w_b/2)} = \frac{1 - \tan(0.0130899693\ 9/2)}{1 + \tan(0.0130899693\ 9/2)} = 0.9869949627$$

$$a_1 = -(1 + a_0)\cos(w_0) = -(1 + 0.9869949627\ )\cos(0.1308996939\ ) = -1.969995945$$

NFn_A0 = -a0 x 213 = -8085 (rounded to nearest whole number)

NFn_A1 = -a1 x 212 = 8069 (rounded to nearest whole number)

These values are then converted to 2's complement:

NFA0 = 14'h206B = 14'b10000001101011

NFA1 = 14'h1F85 = 14'b01111110000101

DIGITAL ADC VOLUME CONTROL

The output of the ADCs can be digitally attenuated over a range from –127dB to 0dB in 0.5dB steps. The gain for a given eight-bit code X is given by:

Gain = 0.5 x (x–255) dB for 1 ≤ x ≤ 255, MUTE for x = 0

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R15 ADC Digital Volume	7:0	ADCVOL [7:0]	11111111 (0dB)	ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -127dB 0000 0010 = -126.5dB ... 0.5dB steps up to 1111 1111 = 0dB

Table 13 ADC Volume

INPUT AUTOMATIC LEVEL CONTROL (ALC)

The WM8950 has an automatic PGA gain control circuit, which can function as an input peak limiter or as an automatic level control (ALC).

The Automatic Level Control (ALC) provides continuous adjustment of the input PGA in response to the amplitude of the input signal. A digital peak detector monitors the input signal amplitude and compares it to a register defined threshold level (ALCLVL).

If the signal is below the threshold, the ALC will increase the gain of the PGA at a rate set by ALCDCY. If the signal is above the threshold, the ALC will reduce the gain of the PGA at a rate set by ALCATK.

The ALC has two modes selected by the ALCMODE register: normal mode and peak limiter mode. The ALC/limiter function is enabled by setting the register bit R32[8] ALCSEL.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (20h) ALC Control 1	2:0	ALCMIN [2:0]	000 (-12dB)	Set minimum gain of PGA 000 = -12dB 001 = -6dB 010 = 0dB 011 = +6dB 100 = +12dB 101 = +18dB 110 = +24dB 111 = +30dB
	5:3	ALCMAX [2:0]	111 (+35.25dB)	Set Maximum Gain of PGA 111 = +35.25dB 110 = +29.25dB 101 = +23.25dB 100 = +17.25dB 011 = +11.25dB 010 = +5.25dB 001 = -0.75dB 000 = -6.75dB
	8	ALCSEL	0	ALC function select 0 = ALC disabled 1 = ALC enabled
R33 (21h) ALC Control 2	3:0	ALCLVL [3:0]	1011 (-12dB)	ALC target – sets signal level at ADC input 1111 = -6dBFS 1110 = -7.5dBFS 1101 = -9dBFS 1100 = -10.5dBFS 1011 = -12dBFS 1010 = -13.5dBFS 1001 = -15dBFS 1000 = -16.5dBFS 0111 = -18dBFS 0110 = -19.5dBFS 0101 = -21dBFS 0100 = -22.5dBFS 0011 = -24dBFS 0010 = -25.5dBFS 0001 = -27dBFS 0000 = -28.5dBFS

<table>
<tr><th>REGISTER ADDRESS</th><th>BIT</th><th>LABEL</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td></td><td>8</td><td>ALCZC</td><td>0 (zero cross off)</td><td>ALC uses zero cross detection circuit.
0 = Disabled (recommended)
1 = Enabled</td></tr>
<tr><td></td><td>7:4</td><td>ALCHLD [3:0]</td><td>0000
(0ms)</td><td>ALC hold time before gain is increased.
0000 = 0ms
0001 = 2.67ms
0010 = 5.33ms
0011 = 10.66ms
0100 = 21.32ms
0101 = 42.64ms
0110 = 85.28ms
0111 = 0.17s
1000 = 0.34s
1001 = 0.68s
1010 or higher = 1.36s</td></tr>
<tr><td>R34 (22h)
ALC Control 3</td><td>8</td><td>ALCMODE</td><td>0</td><td>Determines the ALC mode of operation:
0 = ALC mode (Normal Operation)
1 = Limiter mode.</td></tr>
<tr><td></td><td>7:4</td><td>ALCDCY [3:0]</td><td>0011
(26ms/6dB)</td><td>Decay (gain ramp-up) time
(ALCMODE ==0)
<table>
<tr><th></th><th>Per step</th><th>Per 6dB</th><th>90% of range</th></tr>
<tr><td>0000</td><td>410us</td><td>3.38ms</td><td>23.6ms</td></tr>
<tr><td>0001</td><td>820us</td><td>6.56ms</td><td>47.2ms</td></tr>
<tr><td>0010</td><td>1.64ms</td><td>13.1ms</td><td>94.5ms</td></tr>
<tr><td colspan="4">… (time doubles with every step)</td></tr>
<tr><td>1010 or higher</td><td>420ms</td><td>3.36s</td><td>24.2s</td></tr>
</table></td></tr>
<tr><td></td><td></td><td></td><td>0011
(5.8ms/6dB)</td><td>Decay (gain ramp-up) time
(ALCMODE ==1)
<table>
<tr><th></th><th>Per step</th><th>Per 6dB</th><th>90% of range</th></tr>
<tr><td>0000</td><td>90.8us</td><td>726us</td><td>5.23ms</td></tr>
<tr><td>0001</td><td>182us</td><td>1.45ms</td><td>10.5ms</td></tr>
<tr><td>0010</td><td>363us</td><td>2.91ms</td><td>20.9ms</td></tr>
<tr><td colspan="4">… (time doubles with every step)</td></tr>
<tr><td>1010</td><td>93ms</td><td>744ms</td><td>5.36s</td></tr>
</table></td></tr>
<tr><td></td><td>3:0</td><td>ALCATK [3:0]</td><td>0010
(3.3ms/6dB)</td><td>ALC attack (gain ramp-down) time
(ALCMODE == 0)
<table>
<tr><th></th><th>Per step</th><th>Per 6dB</th><th>90% of range</th></tr>
<tr><td>0000</td><td>104us</td><td>832us</td><td>6ms</td></tr>
<tr><td>0001</td><td>208us</td><td>1.66ms</td><td>12ms</td></tr>
<tr><td>0010</td><td>416us</td><td>3.33ms</td><td>24ms</td></tr>
<tr><td colspan="4">… (time doubles with every step)</td></tr>
<tr><td>1010 or higher</td><td>106ms</td><td>852ms</td><td>6.13s</td></tr>
</table></td></tr>
</table>

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
			0010 (726us/6dB)	ALC attack (gain ramp-down) time (ALCMODE == 1)

	Per step	Per 6dB	90% of range
0000	22.7us	182.4us	1.31ms
0001	45.4us	363us	2.62ms
0010	90.8us	726us	5.23ms
… (time doubles with every step)			
1010 or higher	23.2ms	186ms	1.34s

Table 14 ALC Control Registers

When the ALC is disabled, the input PGA remains at the last controlled value of the ALC. An input gain update must be made by writing to the INPPGAVOLL/R register bits.

NORMAL MODE

In normal mode, the ALC will attempt to maintain a constant signal level by increasing or decreasing the gain of the PGA. The following diagram shows an example of this.

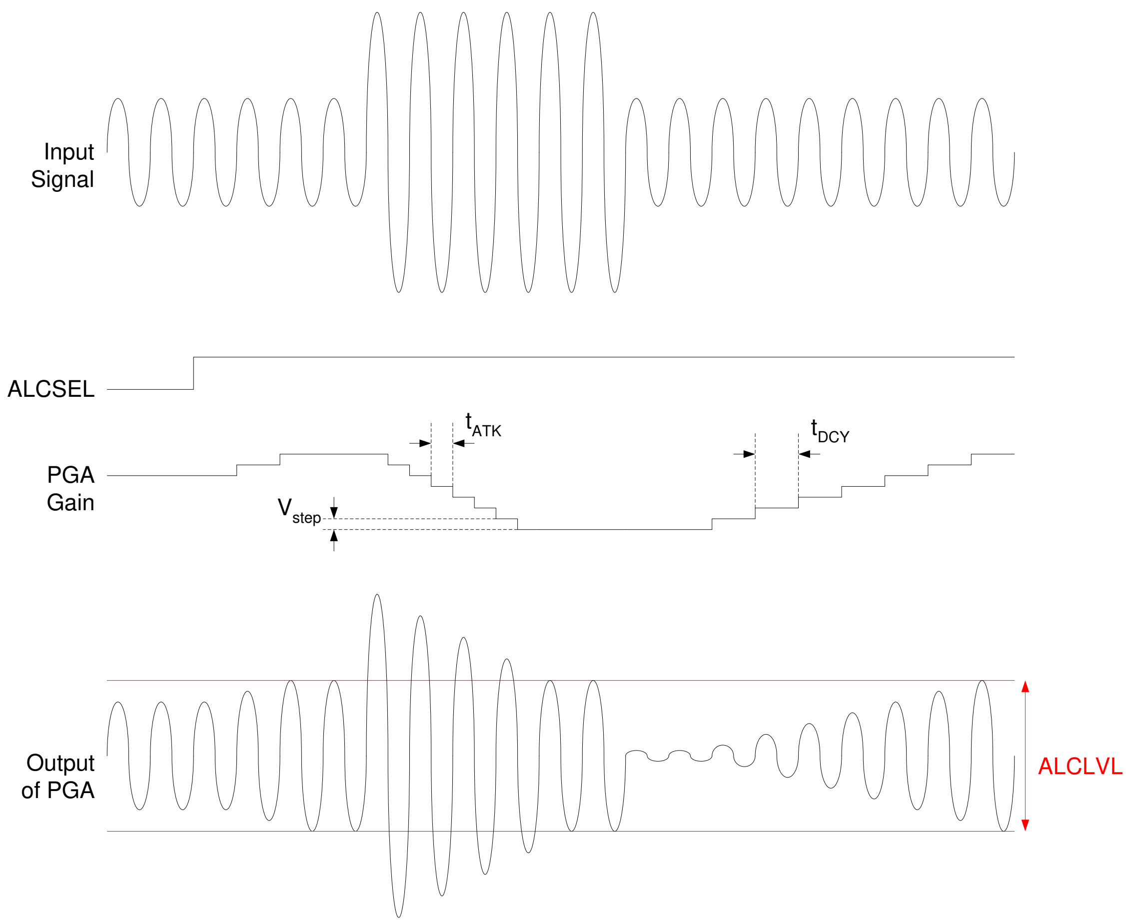


Figure 11 ALC Normal Mode Operation

LIMITER MODE

In limiter mode, the ALC will reduce peaks that go above the threshold level, but will not increase the PGA gain beyond the starting level. The starting level is the PGA gain setting when the ALC is enabled in limiter mode. If the ALC is started in limiter mode, this is the gain setting of the PGA at start-up. If the ALC is switched into limiter mode after running in ALC mode, the starting gain will be the gain at switchover. The diagram below shows an example of limiter mode.

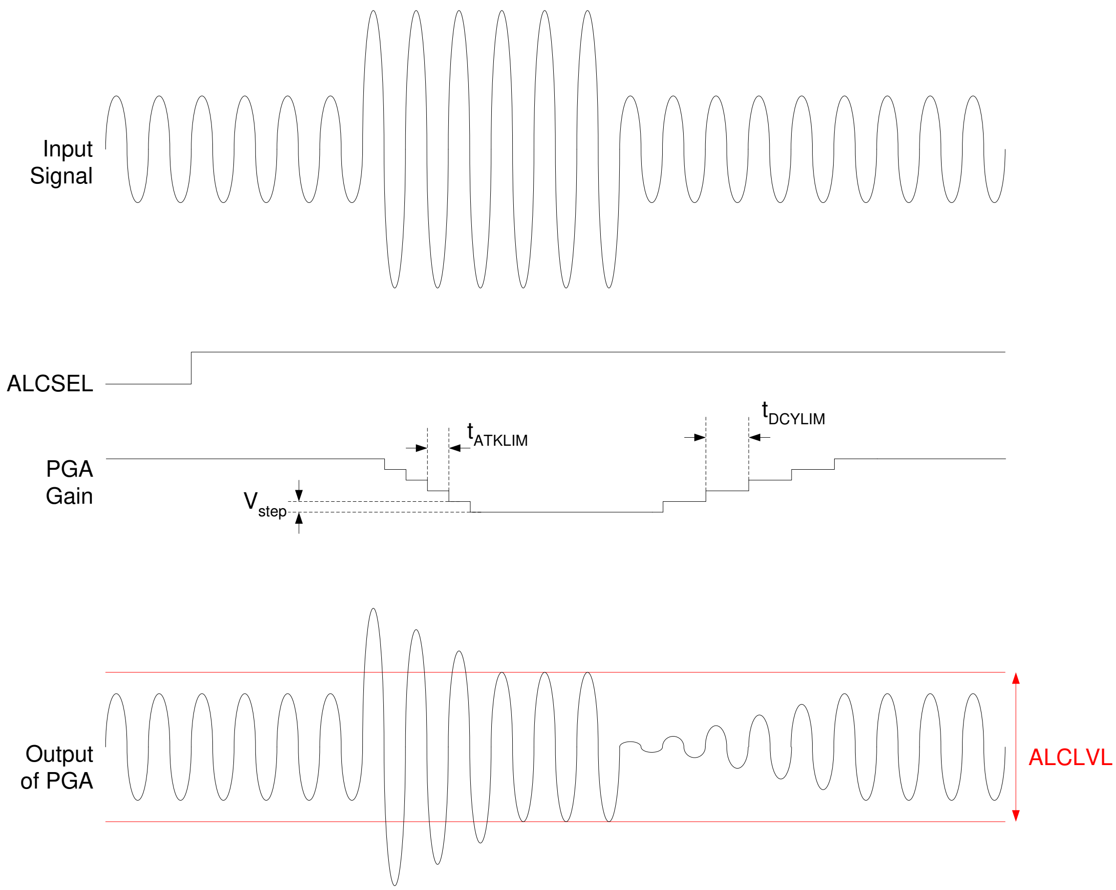


Figure 12 ALC Limiter Mode Operation

ATTACK AND DECAY TIMES

The attack and decay times set the update times for the PGA gain. The attack time is the time constant used when the gain is reducing. The decay time is the time constant used when the gain is increasing. In limiter mode, the time constants are faster than in ALC mode. The time constants are shown below in terms of a single gain step, a change of 6dB and a change of 90% of the PGAs gain range.

Note that, these times will vary slightly depending on the sample rate used (specified by the SR register).