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WM8953

Low Power Stereo ADC with PLL and TDM Interface

DESCRIPTION

The WM8953 is a low power high performance stereo ADC designed for mobile handsets and other portable devices.

Four single-ended or differential input connections are provided, with up to 60dB of analogue gain in each input path. Stereo 24-bit sigma-delta ADCs provide hi-fi quality audio recording of microphones or line input. A programmable high pass filter is available in the ADC path for removing DC offsets and suppressing wind and other low frequency noise.

A low noise microphone bias with programmable current detect and short-circuit detect is provided.

A flexible digital audio interface supports most commonly-used clocking schemes. The audio interface supports TDM and tristate outputs allow multiple devices to share the same interface.

An integrated low power PLL provides support for most commonly-used audio sample rates.

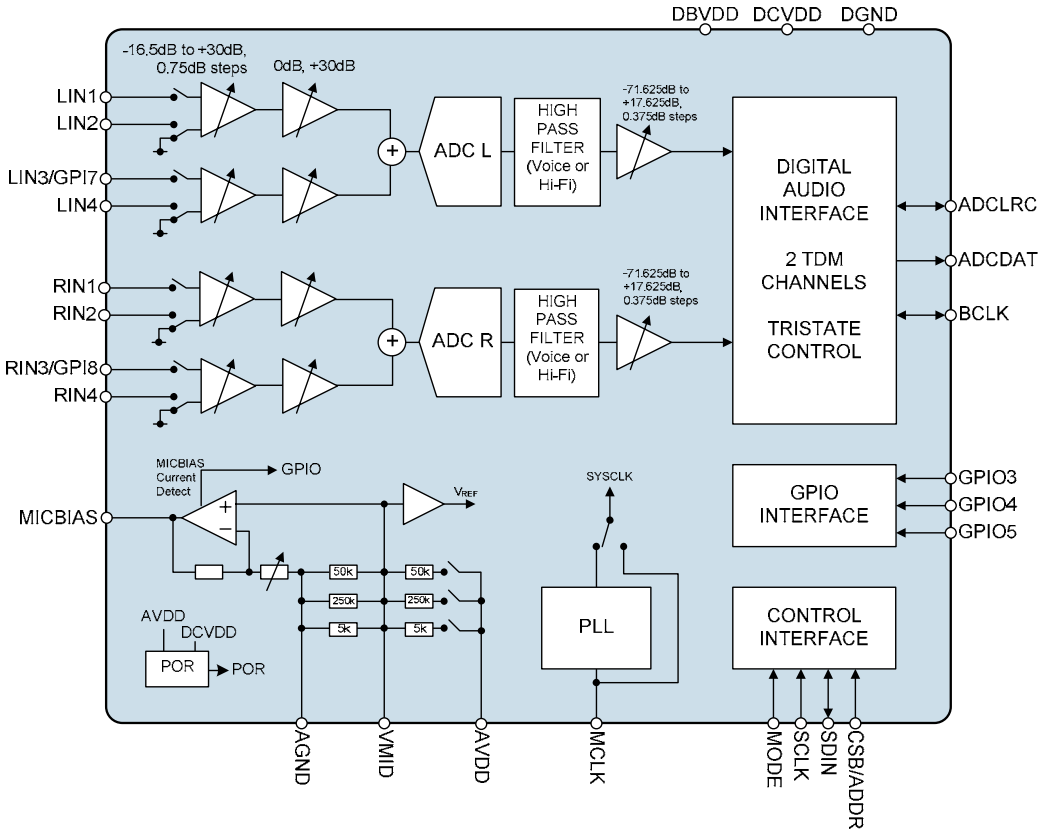
The WM8953 is supplied in very small and thin 42-ball WCSP package, ideal for portable systems.

FEATURES

- SNR 94dB ('A' weighted)
- THD -82dB at 48kHz, 3.3V
- Full stereo microphone / line input interface
- Low noise MICBIAS
- Low power consumption
- Full analogue and digital volume control
- PLL provides flexible clocking scheme
- 2-wire, 3-wire or 4-wire control
- Sample rates: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48kHz
- GPIO functions available
- Digital supply: 1.71V – 3.6V
- Analogue supply: 2.7V – 3.6V
- W-CSP package (3.226 x 3.44 x 0.7mm, 0.5mm pitch)

APPLICATIONS

- Multimedia phones
- General purpose low power audio ADC



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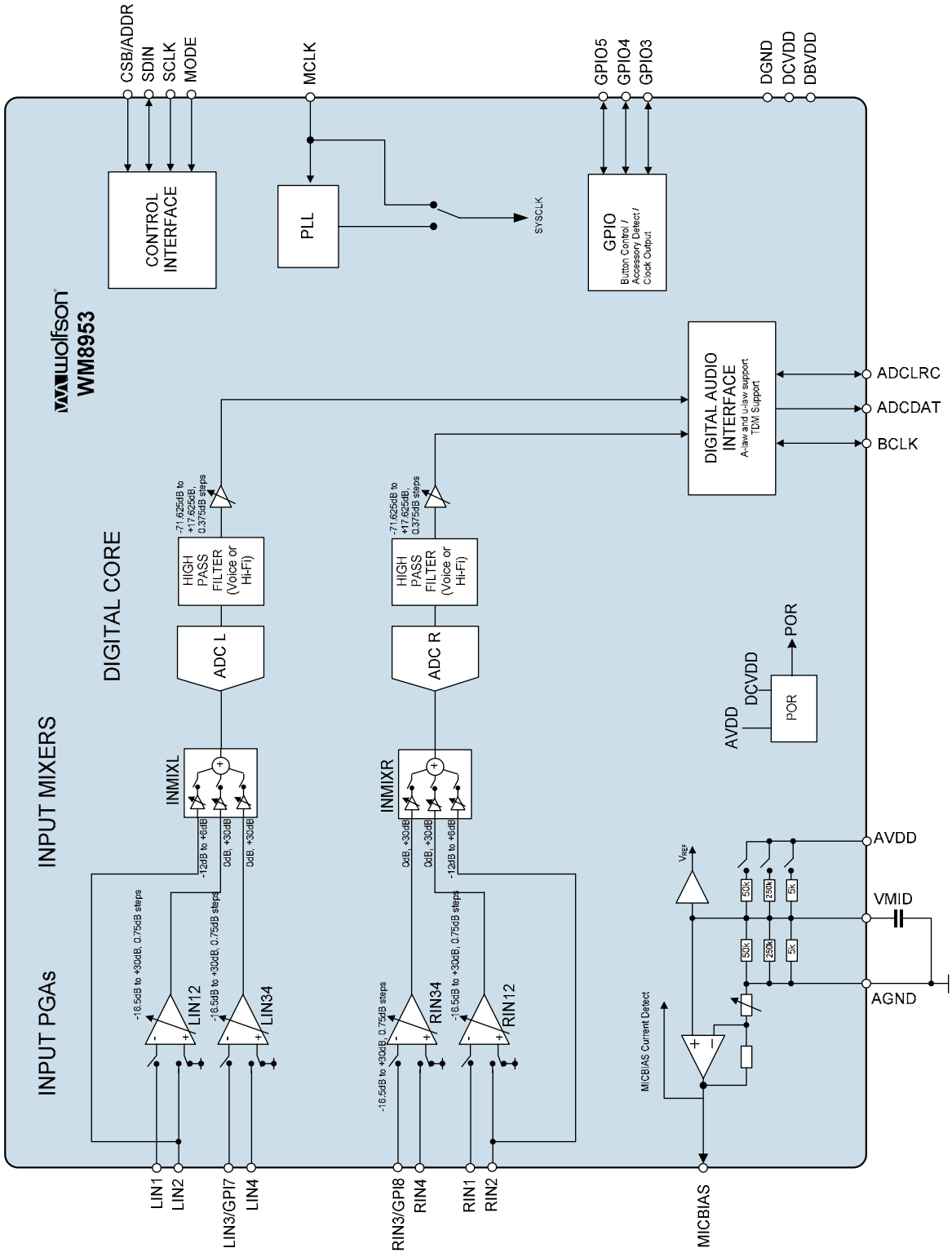
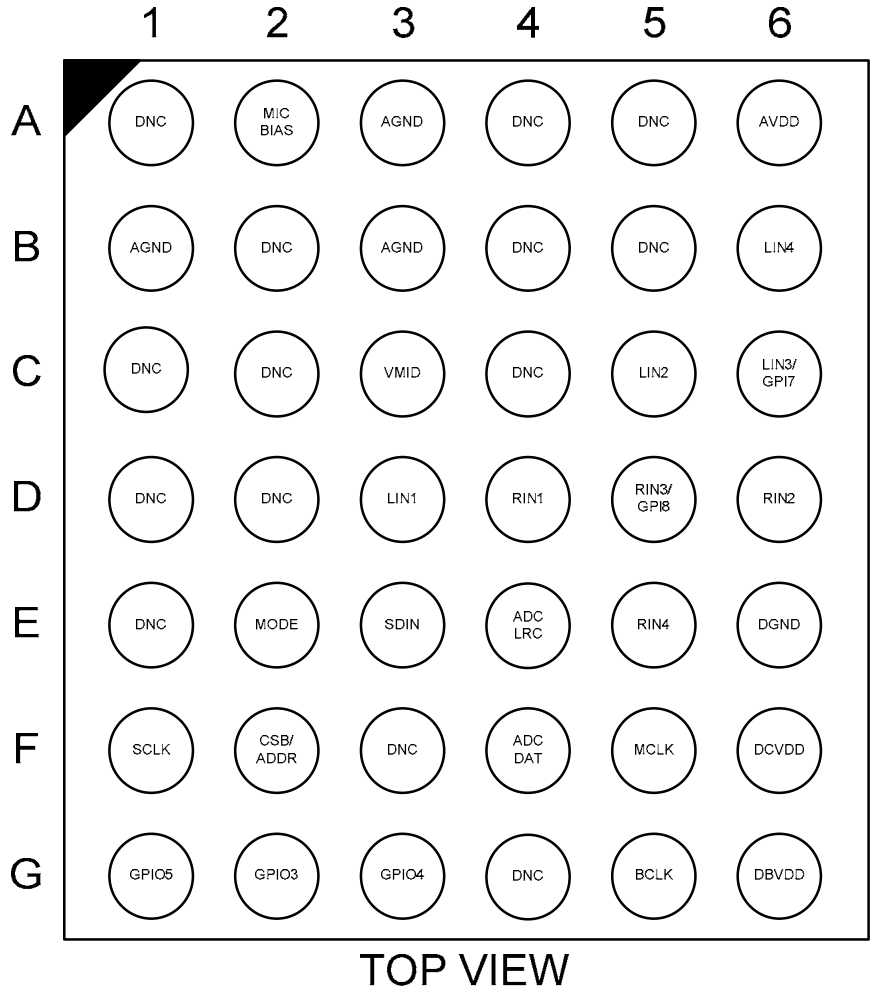
BLOCK DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8953ECS/RV	-40°C to +85°C	42-ball W-CSP (Pb-free, Tape and reel)	MSL3	260°C

Note:

Reel quantity = 3500

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
A2	MICBIAS	Analogue Output	Microphone bias
D3	LIN1	Analogue Input	Left channel single-ended MIC input / Left channel negative differential MIC input
C5	LIN2	Analogue Input	Left channel line input / Left channel positive differential MIC input
C6	LIN3 / GPI7	Analogue Input / Digital Input	Left channel line input / Left channel negative differential MIC input / Accessory or button detect input pin
B6	LIN4	Analogue Input	Left channel line input / Left channel positive differential MIC input /
D4	RIN1	Analogue Input	Right channel single-ended MIC input / Right channel negative differential MIC input
D6	RIN2	Analogue Input	Right channel line input / Right channel positive differential MIC input
D5	RIN3 / GPI8	Analogue Input / Digital Input	Right channel line input / Right channel negative differential MIC input / Accessory or button detect input pin
E5	RIN4	Analogue Input	Left channel line input / Left channel positive differential MIC input /
F6	DCVDD	Supply	Digital core supply
E6	DGND	Supply	Digital ground (Return path for both DCVDD and DBVDD)
G6	DBVDD	Supply	Digital buffer (I/O) supply
A6	AVDD	Supply	Analogue supply
A3, B1, B3	AGND	Supply	Analogue ground (Return path for AVDD)
F5	MCLK	Digital Input	Master clock
G5	BCLK	Digital Input / Output	Audio interface bit clock
E4	ADCLRC	Digital Input / Output	Audio interface ADC left / right clock
F4	ADCDAT	Digital Output	ADC digital audio data
E2	MODE	Digital Input	Selects 2-wire or 3/4 -wire control
F2	CSB / ADDR	Digital Input	3/4 -wire chip select or 2-wire address select
F1	SCLK	Digital Input	Control interface clock input
E3	SDIN	Digital Input / Output	Control interface data input / 2-wire acknowledge output
C3	VMID	Analogue Output	Midrail voltage decoupling capacitor
G2	GPIO3	Digital Input / Output	GPIO pin
G3	GPIO4	Digital Input / Output	GPIO pin
G1	GPIO5	Digital Input / Output	GPIO pin
A1, A4, A5, B2, B4, B5, C1, C2, C4, D1, D2, E1, F3, G4	DNC	Do Not Connect	

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages	-0.3V	+4.5V
Voltage range digital inputs	DGND -0.3V	DBVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Operating temperature range, T_A	-40ºC	+85ºC
Junction temperature, T_{JMAX}	-40ºC	+150ºC
Storage temperature after soldering	-65ºC	+150ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD	1.71		3.6	V
Digital supply range (Buffer)	DBVDD	1.71		3.6	V
Analogue supply range	AVDD	2.7		3.6	V
Ground	DGND, AGND		0		V

Notes

1. Analogue and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other (i.e. not internally connected).
3. DCVDD must be less than or equal to AVDD.
4. DCVDD must be less than or equal to DBVDD.

THERMAL PERFORMANCE

Thermal analysis should be performed in the intended application to prevent the WM8953 from exceeding maximum junction temperature. Several contributing factors affect thermal performance most notably the physical properties of the mechanical enclosure, location of the device on the PCB in relation to surrounding components and the number of PCB layers. Connecting the GND balls through thermal vias and into a large ground plane will aid heat extraction.

Three main heat transfer paths exist to surrounding air as illustrated below in Figure 1:

- Package top to air (radiation).
- Package bottom to PCB (radiation).
- Package balls to PCB (conduction).

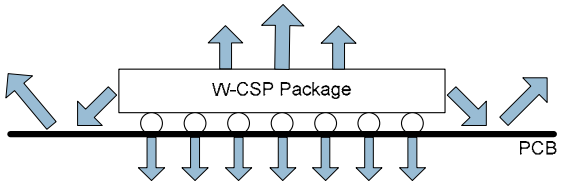


Figure 1 Heat Transfer Paths

The temperature rise T_R is given by $T_R = P_D * \Theta_{JA}$

- P_D is the power dissipated in the device.
- Θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature and is therefore a measure of heat transfer from the die to surrounding air. Θ_{JA} is determined with reference to JEDEC standard JESD51-9.

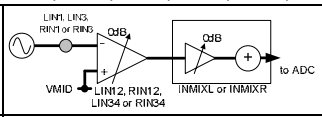
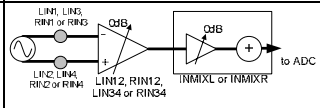
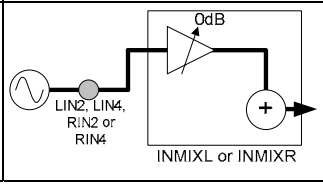
The junction temperature T_J is given by $T_J = T_A + T_R$, where T_A is the ambient temperature.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Operating temperature range	T_A	-40		85	°C
Operating junction temperature	T_J	-40		100	°C
Thermal Resistance	Θ_{JA}		43		°C/W

ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz,
PGA gain = 0dB, 24-bit audio data unless otherwise stated.

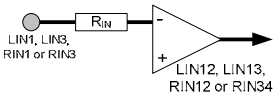
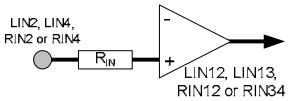
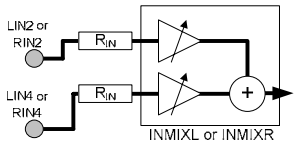
PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Analogue Input Pin Maximum Signal Levels (LIN1, LIN2, LIN3, LIN4, RIN1, RIN2, RIN3, RIN4)						
Maximum Full-Scale PGA Input Signal Level Note 1; Note 2; Note 3	Single-ended PGA input on LIN1, LIN3, RIN1 or RIN3, output to INMIXL or INMIXR			1.0 0		Vrms dBV
	Differential PGA input on LIN1/LIN2, LIN3/LIN4, RIN1/RIN2 or RIN3/RIN4, output to INMIXL or INMIXR			1.0 0		Vrms dBV
Maximum Full-Scale Line Input Signal Level Note 1; Note 2; Note 3	Line input on LIN2, LIN4, RIN2 or RIN4 to INMIXL or INMIXR			1.0 0		Vrms dBV

Notes

1. Maximum full scale signal changes in proportion to AVDD (AVDD/3.3).
2. When mixing input PGA outputs and line inputs, the total signal must not exceed 1Vrms (0dBV).
3. A 1.0Vrms differential signal equates to 0.5Vrms/-6dBV per input.

Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz,
PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Analogue Input Pin Impedances (LIN1, LIN2, LIN3, LIN4, RIN1, RIN2, RIN3, RIN4)						
PGA Input Resistance Note: this will be seen in parallel with the resistance of other enabled input paths from the same pin	LIN1, LIN3, RIN1 or RIN3 (PGA Gain = -16.5dB)			57		kΩ
	LIN1, LIN3, RIN1 or RIN3 (PGA Gain = 0dB)			33		kΩ
	LIN1, LIN3, RIN1 or RIN3 (PGA Gain = +30dB)			2		kΩ
	LIN2, LIN4, RIN2 or RIN4 (Constant for all gains)			65		kΩ
Line Input Resistance Note: this will be seen in parallel with the resistance of other enabled input paths from the same pin	LIN2 or RIN2 to INMIXL or INMIXR (-12dB)			60		kΩ
	LIN2 or RIN2 to INMIXL or INMIXR (0dB)			15		kΩ
	LIN2 or RIN2 to INMIXL or INMIXR (+6dB)			7.5		kΩ
Input Capacitance	All analogue input pins			10		pF

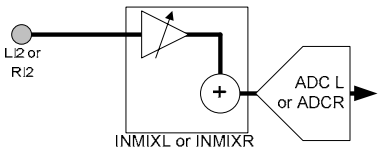
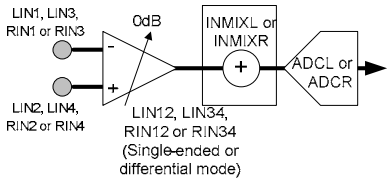
Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz,
PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Programmable Gain Amplifiers (PGAs) LIN12, LIN34, RIN12 and RIN34					
Minimum Programmable Gain			-16.5		dB
Maximum Programmable Gain			30		dB
Programmable Gain Step Size	Guaranteed monotonic		1.5		dB
Mute Attenuation	Inputs disconnected		90		dB
Common Mode Rejection Ratio (1kHz input)	Single PGA in differential mode, gain = +30dB		60		dB
	Single PGA in differential mode, gain = 0dB		50		
	Single PGA in differential mode, gain = -16.5dB		50		
Input Mixers INMIXL and INMIXR					
Minimum Programmable Gain	PGA Outputs to INMIXL and INMIXR		0		dB
Maximum Programmable Gain	PGA Outputs to INMIXL and INMIXR		+30		dB
Programmable Gain Step Size	PGA Outputs to INMIXL and INMIXR		30		dB
Minimum Programmable Gain	Line Inputs to INMIXL and INMIXR		-12		dB
Maximum Programmable Gain	Line Inputs to INMIXL and INMIXR		+6		dB
Programmable Gain Step Size	Line Inputs to INMIXL and INMIXR		3		dB
Mute attenuation			95		dB

Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz,
PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
ADC Input Path Performance						
SNR (A-weighted)	Line inputs to ADC via INMIXL and INMIXR, AVDD = 3.3V		84	94		dB
THD (-1dBFS input)				-84	-75	dB
THD+N (-1dBFS input)				-82	-73	dB
Crosstalk (L/R)				-100		dB
AVDD PSRR (217Hz)				45		dB
DCVDD PSRR (217Hz)				80		dB
SNR (A-weighted)	Line inputs to ADC via INMIXL and INMIXR, AVDD = 2.7V			93		dB
THD (-1dBFS input)				-78		dB
THD+N (-1dBFS input)				-76		dB
SNR (A-weighted)	Input PGAs to ADC via INMIXL or INMIXR, AVDD = 3.3V		84	94		dB
THD (-1dBFS input)				-84	-75	dB
THD+N (-1dBFS input)				-82	-73	dB
Crosstalk (L/R)				-100		dB
AVDD PSRR (217Hz)				45		dB
SNR (A-weighted)	Input PGAs to ADC via INMIXL or INMIXR, AVDD = 2.7V			92		dB
THD (-1dBFS input)				-78		dB
THD+N (-1dBFS input)				-76		dB

Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz,
PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Reference Levels					
VMID Midrail Reference Voltage		-3%	AVDD/2	+3%	V
Microphone Bias					
Bias Voltage	3mA load current MBSEL=0	-5%	0.9×AVDD	+5%	V
	3mA load current MBSEL=1	-5%	0.65×AVDD	+5%	V
Bias Current Source				3	mA
Output Noise Density	1kHz to 20kHz		100		nV/√Hz
AVDD PSRR (217Hz)	100mV pk-pk @217Hz on AVDD		45		dB
Digital Input / Output					
Input HIGH Level		0.7×DBVDD			V
Input LOW Level				0.3×DBVDD	V
Note that digital input pins should not be left unconnected / floating. Internal pull-up/pull-down resistors may be enabled on GPIO3, GPIO4 and GPIO5 if required.					
Output HIGH Level	I_{OL}=1mA	0.9×DBVDD			V
Output LOW Level	I_{OH}=-1mA			0.1×DBVDD	V
Input capacitance			10		pF
Input leakage		-0.9		0.9	uA
PLL					
Input Frequency	PRESCALE = 0b	7.7		18	MHz
	PRESCALE = 1b	14.4		36	MHz
Lock time			200		us
GPIO					
Clock output duty cycle (Integer OPCLKDIV)	SYSCLK=MCLK; OPCLKDIV=0000	35		65	%
	SYSCLK=MCLK; OPCLKDIV=1000	45		55	%
	SYSCLK=PLL output; OPCLKDIV=0000	45		55	%
	SYSCLK=PLL output; OPCLKDIV=1000	45		55	%
Clock output duty cycle (Non-integer OPCLKDIV)	SYSCLK=MCLK; OPCLKDIV=0100	33		66	%
	SYSCLK=PLL output; OPCLKDIV=0100	33		66	%
Interrupt response time for accessory / button detect	Input de-bounced	2^{21} / f_{SYSCLK}		2^{22} / f_{SYSCLK}	s
	Input de-bounced TOCLKSEL=1	2^{19} / f_{SYSCLK}		2^{20} / f_{SYSCLK}	s
	Input not de-bounced		0		s

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum theoretical full scale output signal and the output with no input signal applied.
2. Total Harmonic Distortion (dB) – THD is the level of the rms value of the sum of harmonic distortion products relative to the amplitude of the measured output signal.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the level of the rms value of the sum of harmonic distortion products plus noise in the specified bandwidth relative to the amplitude of the measured output signal.
4. Crosstalk (L/R) (dB) – left-to-right and right-to-left channel crosstalk is the measured signal level in the idle channel at the test signal frequency relative to the signal level at the output of the active channel. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel. For example, measured signal level on the output of the idle right channel (RIN2 to ADCR) with a full scale signal level at the output of the active left channel (LIN1 to ADCL).
5. Multi-Path Channel Separation (dB) – is the measured signal level in the idle path at the test signal frequency relative to the signal level at the output of the active path. The active path is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the specified idle path.
6. All performance measurements carried out with 20kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
7. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.

TYPICAL POWER CONSUMPTION

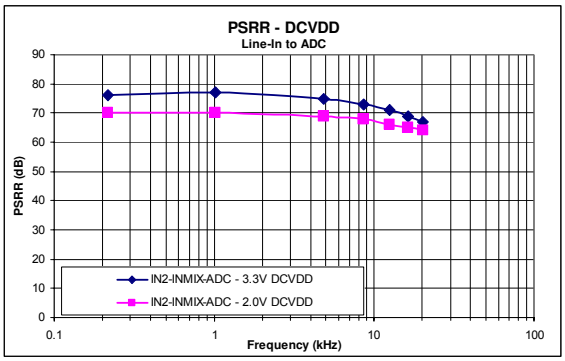
Mode	Other settings	AVDD (V)	DBVDD (V)	DCVDD (V)	IAVDD (mA)	IDBVDD (mA)	IDCVDD (mA)	Total Power (mW)
Standby/Sleep								
OFF (default state at power-up)	No Clocks	2.7	1.8	1.8	0.028	0.000	0.000	0.075
		3.0	2.5	2.5	0.029	0.000	0.000	0.087
		3.3	3.3	3.3	0.030	0.000	0.000	0.099
		3.6	3.6	3.6	0.031	0.000	0.000	0.114
OFF (thermal sensor disabled)	No Clocks	2.7	1.8	1.8	0.008	0.000	0.000	0.020
		3.0	2.5	2.5	0.008	0.000	0.000	0.024
		3.3	3.3	3.3	0.009	0.000	0.000	0.029
		3.6	3.6	3.6	0.009	0.000	0.000	0.035
SLEEP (VMID enabled, thermal sensor anabled)	With Clocks	2.7	1.8	1.8	0.087	0.004	0.459	1.068
		3.0	2.5	2.5	0.096	0.008	0.694	2.044
		3.3	3.3	3.3	0.106	0.014	1.025	3.780
		3.6	3.6	3.6	0.117	0.017	1.162	4.667
ADC Record								
Stereo Line Record (L/RIN2 to INMIXL/R bypassing PGA)	fs=44.1kHz	2.7	1.8	1.8	5.272	0.023	2.285	18.389
		3.0	2.5	2.5	5.603	0.039	3.317	25.199
		3.3	3.3	3.3	5.927	0.060	4.728	35.358
		3.6	3.6	3.6	6.261	0.063	5.295	41.830
Stereo Line Record (L/RIN2 to INMIXL/R bypassing PGA)	fs=8kHz	2.7	1.8	1.8	5.125	0.017	0.758	15.233
		3.0	2.5	2.5	5.434	0.027	1.123	19.177
		3.3	3.3	3.3	5.738	0.061	1.634	24.528
		3.6	3.6	3.6	6.053	0.062	1.841	28.642

Notes:

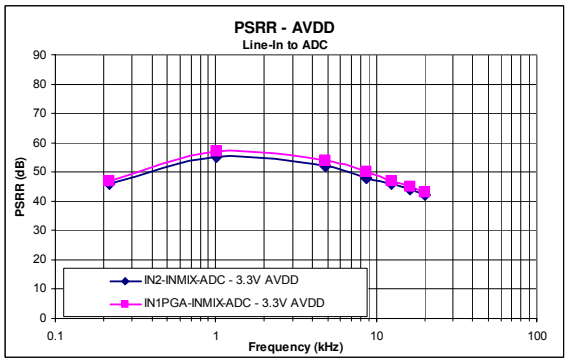
1. All figures are quoted at T_A = +25ºC
2. All figures are quoted as quiescent current unless otherwise stated.

PSRR PERFORMANCE

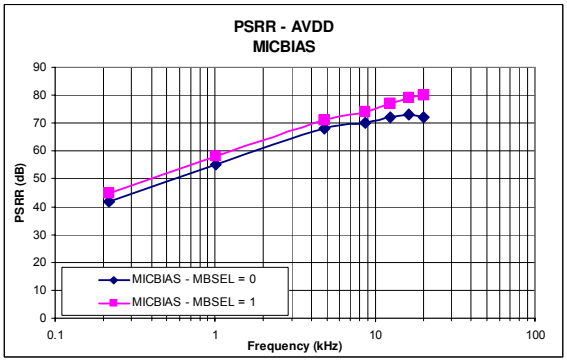
DCVDD – Line-In to ADC



AVDD – Line-In to ADC

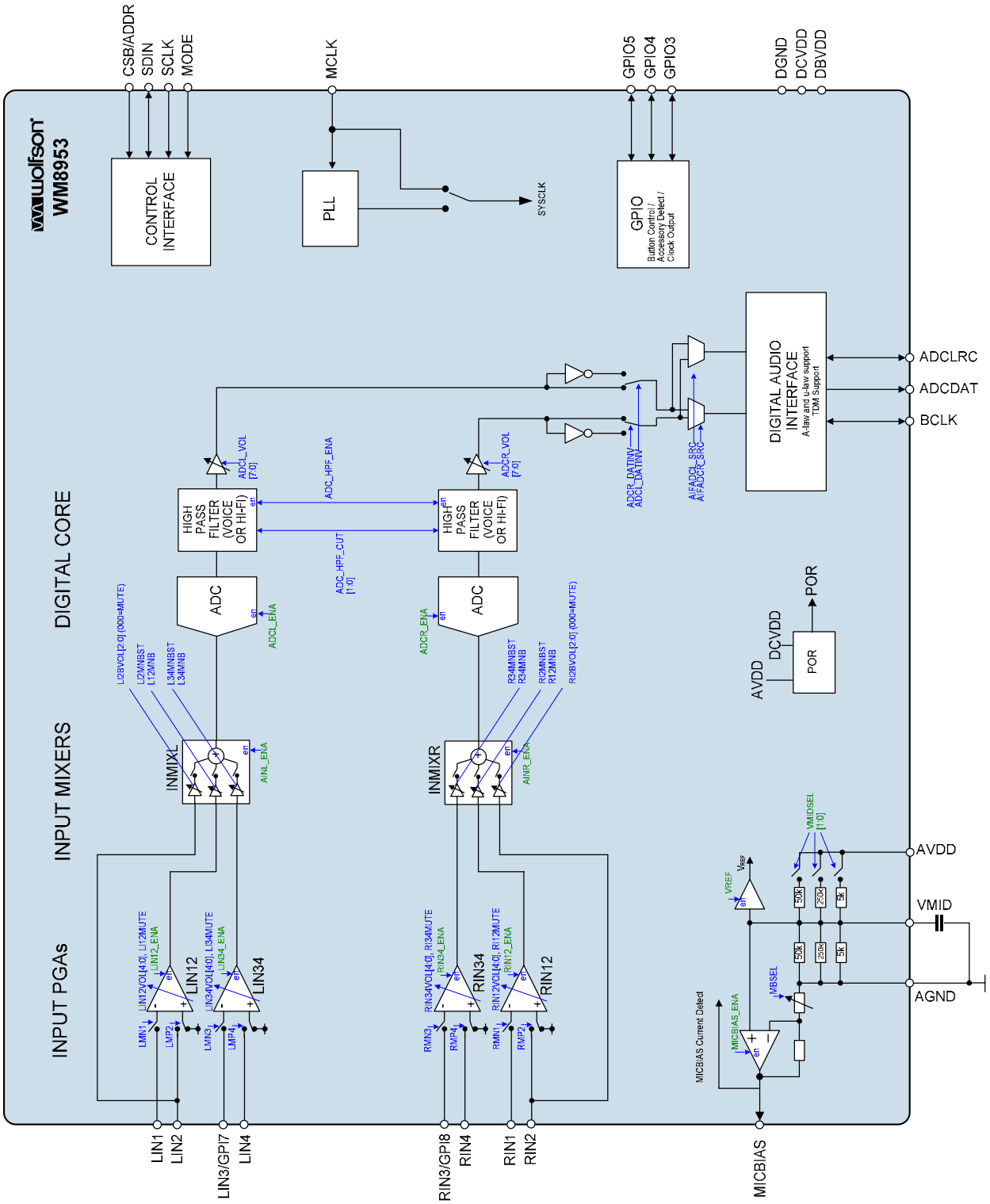


AVDD – MICBIAS



Note: All figures based on 100mVp-p injected on the supply at the relevant test frequency.

AUDIO SIGNAL PATHS



SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

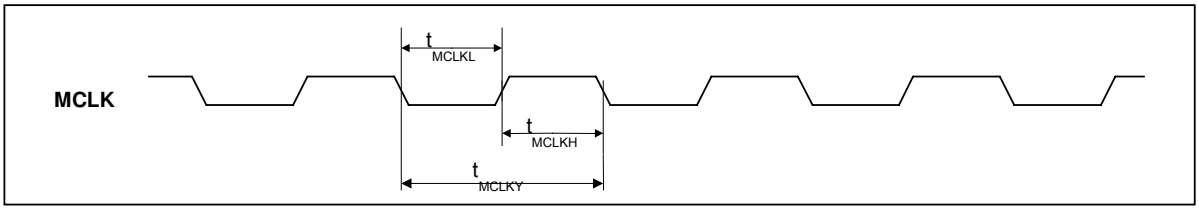


Figure 2 System Clock Timing Requirements

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=3.3V, DGND=AGND=0V, T_A = +25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK cycle time	T_{MCLKY}		33.33			ns
MCLK duty cycle		= T_{MCLKH}/T_{MCLKL}	60:40		40:60	

AUDIO INTERFACE TIMING – MASTER MODE

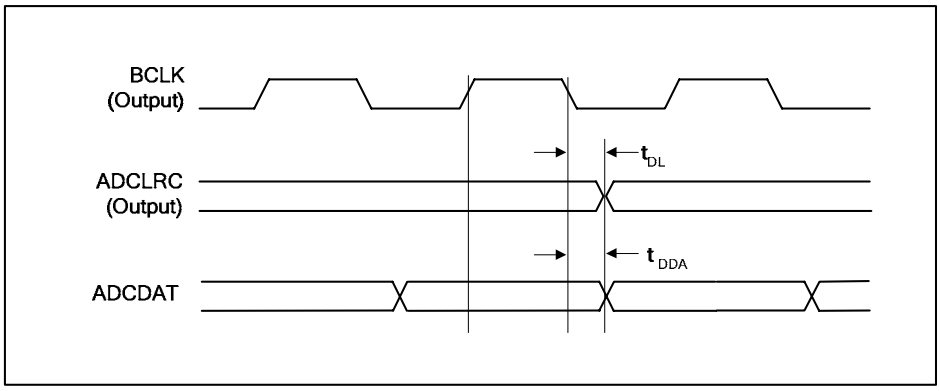


Figure 3 Digital Audio Data Timing - Master Mode (see Control Interface)

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=3.3V, DGND=AGND=0V, T_A=+25°C, Master Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Timing Information					
ADCLRC propagation delay from BCLK falling edge	t_{DL}			20	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			20	ns

AUDIO INTERFACE TIMING – SLAVE MODE

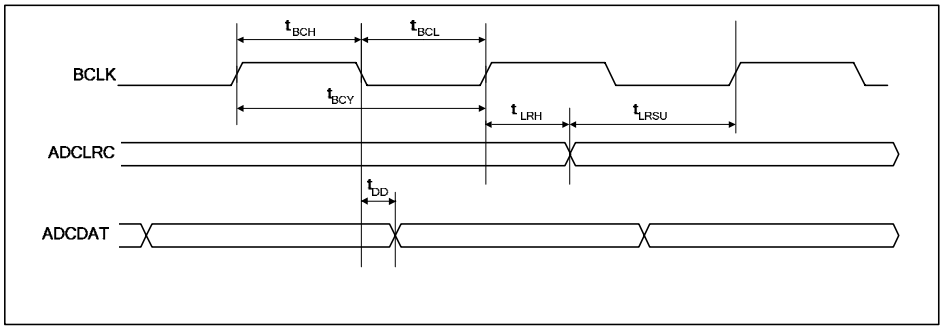


Figure 4 Digital Audio Data Timing – Slave Mode

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=3.3V, DGND=AGND=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t_{BCY}	50			ns
BCLK pulse width high	t_{BCH}	20			ns
BCLK pulse width low	t_{BCL}	20			ns
ADCLRC set-up time to BCLK rising edge	t_{LRSU}	20			ns
ADCLRC hold time from rising edge	t_{LRH}	10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			20	ns

Note:

BCLK period should always be greater than or equal to MCLK period.

AUDIO INTERFACE TIMING – TDM MODE

In TDM mode, it is important that two ADC devices to not attempt to drive the ADCDAT pin simultaneously. The timing of the WM8953 ADCDAT tri-stating at the start and end of the data transmission is described in Figure 5 and the table below.

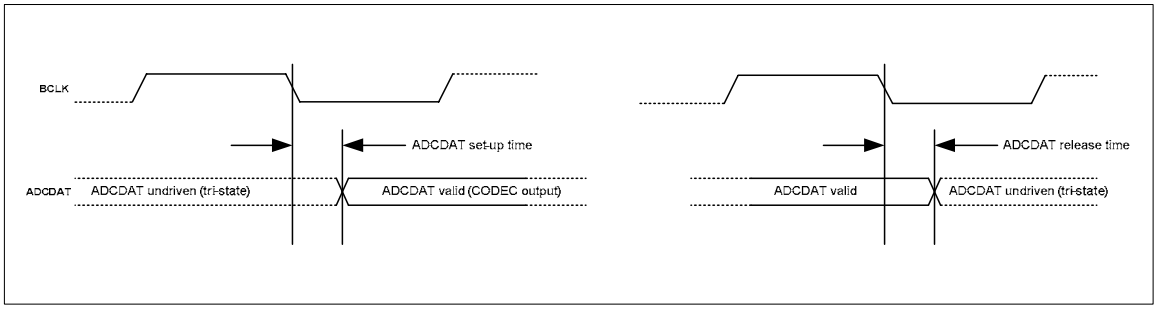


Figure 5 Digital Audio Data Timing - TDM Mode

Test Conditions

AVDD=3.3V, DGND=AGND=0V, T_A=+25°C, Master Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Timing Information					
ADCDAT setup time from BCLK falling edge	DCVDD = DBVDD = 3.6V		5		ns
	DCVDD = DBVDD = 1.71V		15		ns
ADCDAT release time from BCLK falling edge	DCVDD = DBVDD = 3.6V		5		ns
	DCVDD = DBVDD = 1.71V		15		ns

CONTROL INTERFACE TIMING – 2-WIRE MODE

2-wire mode is selected by connecting the MODE pin low.

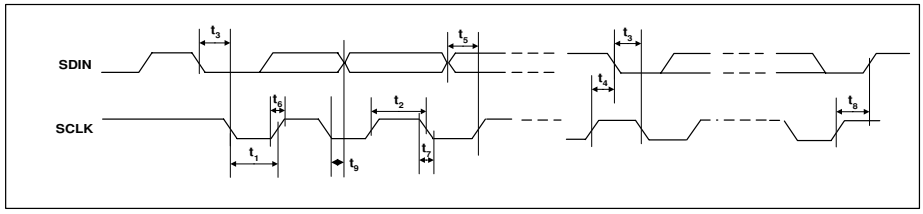


Figure 6 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=3.3V, DGND=AGND=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency				526	kHz
SCLK Low Pulse-Width	t_1	1.3			us
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDIN, SCLK Rise Time	t_6			300	ns
SDIN, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

CONTROL INTERFACE TIMING – 3-WIRE MODE

3-wire mode is selected by connecting the MODE pin high.

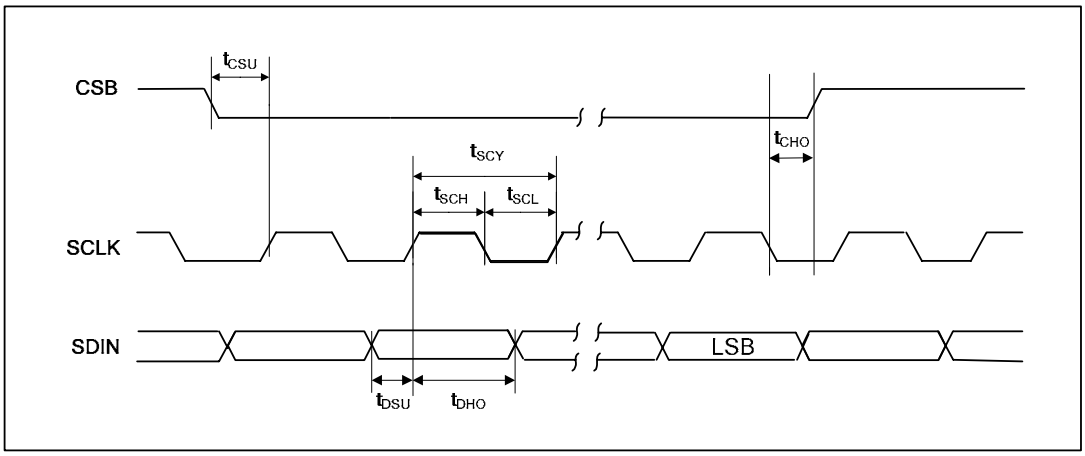


Figure 7 Control Interface Timing – 3-Wire Serial Control Mode (Write Cycle)

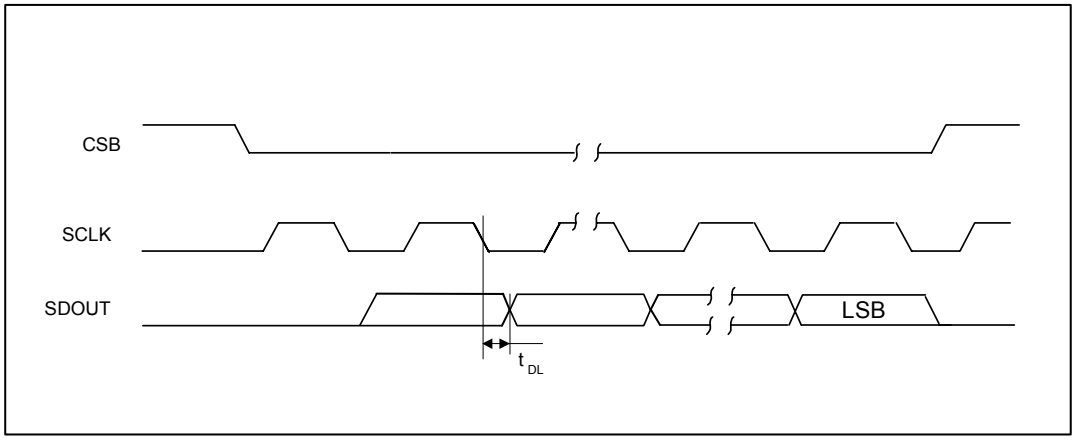


Figure 8 Control Interface Timing – 3-Wire Serial Control Mode (Read Cycle)

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=3.3V, DGND=AGND=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
CSB falling edge to SCLK rising edge	t_{CSU}	40			ns
SCLK falling edge to CSB rising edge	t_{CHO}	40			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDIN to SCLK set-up time	t_{DSU}	40			ns
SDIN to SCLK hold time	t_{DHO}	10			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns
SCLK falling edge to SDOUT transition	t_{DL}			40	ns

CONTROL INTERFACE TIMING – 4-WIRE MODE

4-wire mode supports readback via SDOUT which is available as a GPIO pin function.

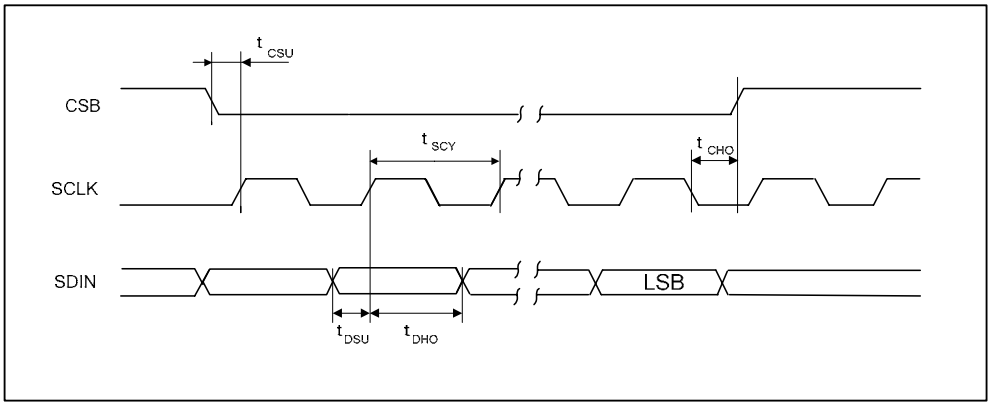


Figure 9 Control Interface Timing – 4-Wire Serial Control Mode (Write Cycle)

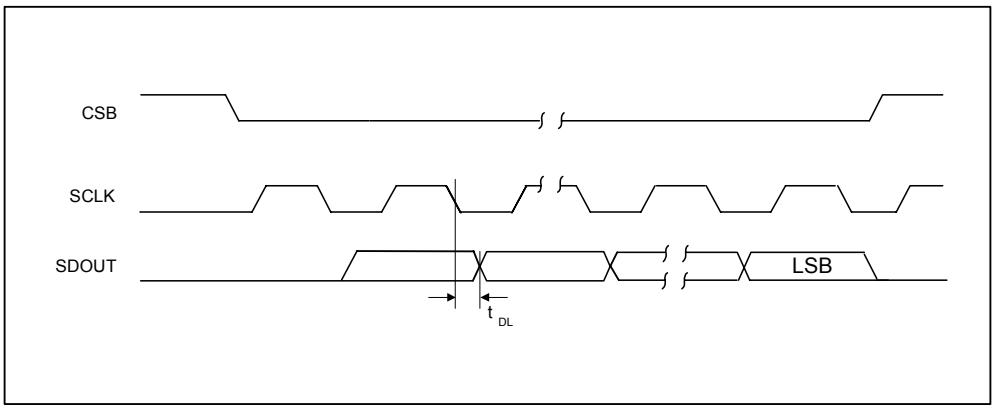


Figure 10 Control Interface Timing – 4-Wire Serial Control Mode (Read Cycle)

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=3.3V, DGND=AGND=0V, T_A =+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB falling edge	t_{CSU}	40			ns
SCLK falling edge to CSB rising edge	t_{CHO}	40			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDIN to SCLK set-up time	t_{DSU}	40			ns
SDIN to SCLK hold time	t_{DHO}	10			ns
SDOUT propagation delay from SCLK rising edge	t_{DL}			10	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns
SCLK falling edge to SDOUT transition	t_{DL}			40	ns

INTERNAL POWER ON RESET CIRCUIT

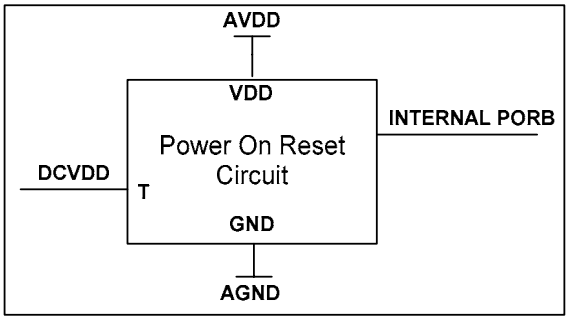


Figure 11 Internal Power on Reset Circuit Schematic

The WM8953 includes an internal Power-On-Reset Circuit, as shown in Figure 11, which is used to reset the digital logic into a default state after power up. The POR circuit is powered from AVDD and monitors DCVDD. It asserts PORB low if AVDD or DCVDD is below a minimum threshold.

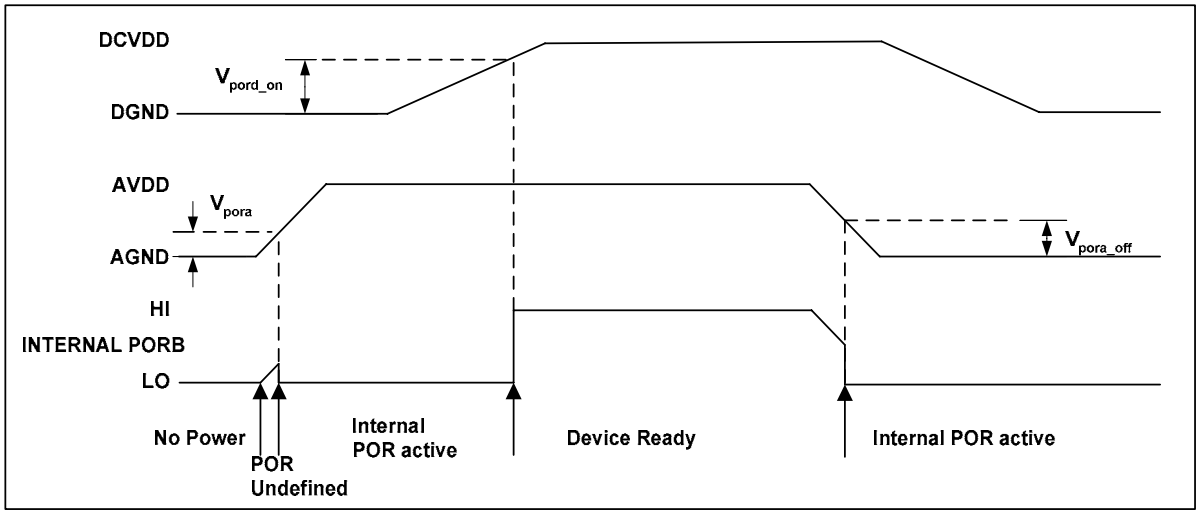


Figure 12 Typical Power up Sequence where AVDD is Powered before DCVDD

Figure 12 shows a typical power-up sequence where AVDD comes up first. When AVDD goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. Now AVDD is at full supply level. Next DCVDD rises to V_{pord_on} and PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where AVDD falls first, PORB is asserted low whenever AVDD drops below the minimum threshold V_{pora_off}.

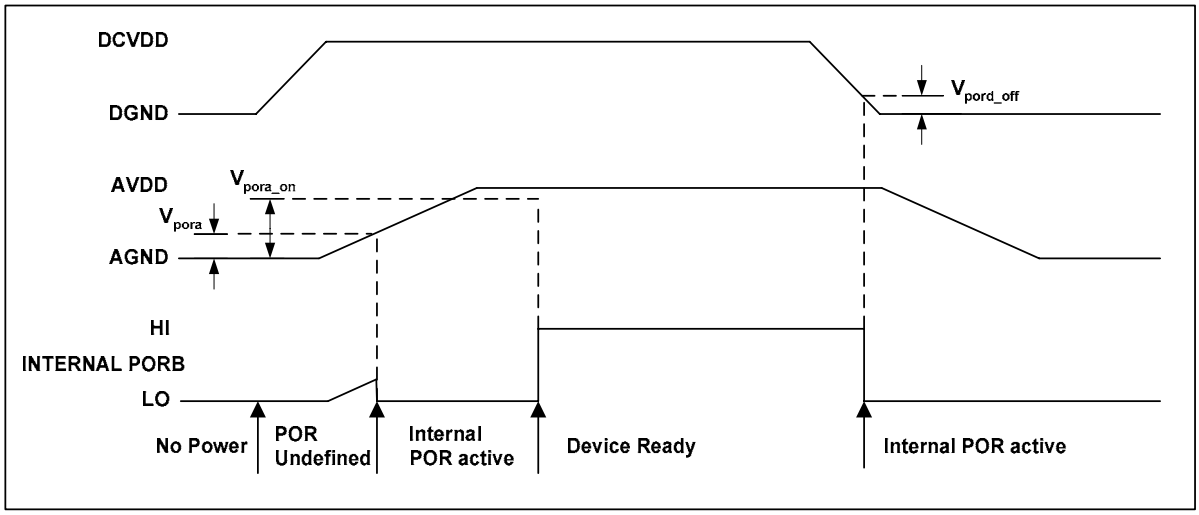


Figure 13 Typical Power up Sequence where DCVDD is Powered before AVDD

Figure 13 shows a typical power-up sequence where DCVDD comes up first. First it is assumed that DCVDD is already up to specified operating voltage. When AVDD goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When AVDD rises to V_{pora_on}, PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where DCVDD falls first, PORB is asserted low whenever DCVDD drops below the minimum threshold V_{pord_off}.

SYMBOL	MIN	TYP	MAX	UNIT
Vpora		0.6		V
Vpora_on		1.52		V
Vpora_off		1.5		V
Vpord_on		0.92		V
Vpord_off		0.9		V

Table 1 Typical POR Operation (typical values, not tested)

Notes:

1. If AVDD and DCVDD suffer a brown-out (i.e. drop below the minimum recommended operating level but do not go below V_{pora_off} or V_{pord_off}) then the chip will not reset and will resume normal operation when the voltage is back to the recommended level again.
2. The chip will enter reset at power down when AVDD or DCVDD falls below V_{pora_off} or V_{pord_off}. This may be important if the supply is turned on and off frequently by a power management system.
3. The minimum t_{por} period is maintained even if DCVDD and AVDD have zero rise time. This specification is guaranteed by design rather than test.

DEVICE DESCRIPTION

INTRODUCTION

The WM8953 is a low power, high quality audio ADC designed to interface with a wide range of processors and analogue components. A high level of mixed-signal integration in a very small 3.226x3.44mm footprint makes it ideal for portable applications such as mobile phones.

Eight highly flexible analogue inputs allow interfacing to up to four microphone inputs plus multiple stereo or mono line inputs (single-ended or differential).

The stereo ADCs are of hi-fi quality using a 24-bit, low-order oversampling architecture to deliver optimum performance. A flexible clocking arrangement supports a wide variety of clock inputs and sample rates; the integrated ultra-low power PLL provides additional flexibility. A high pass filter is available in the ADC path for removing DC offsets and suppressing low frequency noise such as mechanical vibration and wind noise.

The WM8953 has a highly flexible digital audio interface, supporting a number of protocols, including I^2S, DSP, MSB-first left/right justified, and can operate in master or slave modes. PCM operation is supported in the DSP mode. A-law and μ-law companding are also supported. Time division multiplexing (TDM) is available to allow multiple devices to stream data simultaneously on the same bus, saving space and power.

The SYSCLK (system clock) provides clocking for the ADCs, DSP core and the digital audio interface. SYSCLK can be derived directly from the MCLK pin or via an integrated PLL, providing flexibility to support a wide range of clocking schemes. All MCLK frequencies typically used in portable systems are supported for sample rates between 8kHz and 48kHz.

To allow full software control over all its features, the WM8953 uses a standard 2-wire or 3/4-wire control interface with readback of key registers supported. It is fully compatible and an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs. Unused circuitry can be disabled via software to save power, while low leakage currents extend standby and off time in portable battery-powered applications. The device address can be selected using the CSB/ADDR pin.

Versatile GPIO functionality is provided, with support for up to five button/accessory detect inputs with interrupt and status readback and flexible de-bouncing options, clock output, and logic '1' / logic '0' for control of additional external circuitry.