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WM8960

Stereo CODEC with 1W Stereo Class D Speaker Drivers and Headphone Drivers for Portable Audio Applications

DESCRIPTION

The WM8960 is a low power, high quality stereo CODEC designed for portable digital audio applications.

Stereo class D speaker drivers provide 1W per channel into 8Ω loads with a 5V supply. Low leakage, excellent PSRR and pop/click suppression mechanisms also allow direct battery connection to the speaker supply. Flexible speaker boost settings allow speaker output power to be maximised while minimising other analogue supply currents.

A highly flexible input configuration for up to three stereo sources is integrated, with a complete microphone interface. External component requirements are drastically reduced as no separate microphone, speaker or headphone amplifiers are required. Advanced on-chip digital signal processing performs automatic level control for the microphone or line input.

Stereo 24-bit sigma-delta ADCs and DACs are used with low power over-sampling digital interpolation and decimation filters and a flexible digital audio interface.

The master clock can be input directly or generated internally by an onboard PLL, supporting most commonly-used clocking schemes.

The WM8960 operates at analogue supply voltages down to 2.7V, although the digital supplies can operate at voltages down to 1.71V to save power. The speaker supply can operate at up to 5.5V, providing 1W per channel into 8Ω loads. Unused functions can be disabled using software control to save power.

The WM8960 is supplied in a very small and thin 5x5mm QFN package, ideal for use in hand-held and portable systems.

FEATURES

- DAC SNR 98dB ('A' weighted), THD -84dB at 48kHz, 3.3V
- ADC SNR 94dB ('A' weighted), THD -82dB at 48kHz, 3.3V
- Pop and click suppression
- 3D Enhancement
- Stereo Class D Speaker Driver
  - <0.1% THD with 1W per channel into 8Ω BTL speakers
  - 70dB PSRR @217Hz
  - 87% efficiency (1W output)
  - Flexible internal switching clock
- On-chip Headphone Driver
  - 40mW output power into 16Ω at 3.3V
  - Capless mode support
  - THD -75dB at 20mW, SNR 90dB with 16Ω load
- Microphone Interface
  - Pseudo differential for high noise immunity
  - Integrated low noise MICBIAS
  - Programmable ALC / Limiter and Noise Gate
- Low Power Consumption
- Low Supply Voltages
  - Analogue 2.7V to 3.6V (Speaker supply up to 5.5V)
  - Digital core and I/O: 1.71V to 3.6V
- On-chip PLL provides flexible clocking scheme
- Sample rates: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48
- 5x5x0.9mm QFN package

APPLICATIONS

- Games consoles
- Portable media / DVD players
- Mobile multimedia

TABLE OF CONTENTS

PIN CONFIGURATION

ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8960CGEFL/V	-40°C to +85°C	32-lead QFN (5x5x0.9mm) (Pb-free)	MSL3	260°C
WM8960CGEFL/RV	-40°C to +85°C	32-lead QFN (5x5x0.9mm) (Pb-free, Tape and reel)	MSL3	260°C
WM8960CGEFL/2RV	-40°C to +85°C	32-lead QFN (5x5x0.9mm) (Pb-free, Tape and reel)	MSL3	260°C

Note:

Reel quantity = 3500 (WM8960CGEFL/V and WM8960CGEFL/RV)

Reel quantity = 2200 (WM8960CGEFL/2RV)

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
1	MICBIAS	Analogue Output	Microphone bias
2	LINPUT3 / JD2	Analogue Input	Left channel line input / Left channel positive differential MIC input / Jack detect input pin
3	LINPUT2	Analogue Input	Left channel line input / Left channel positive differential MIC input
4	LINPUT1	Analogue Input	Left channel single-ended MIC input / Left channel negative differential MIC input
5	RINPUT1	Analogue Input	Right channel single-ended MIC input / Right channel negative differential MIC input
6	RINPUT2	Analogue Input	Right channel line input / Right channel positive differential MIC input
7	RINPUT3 / JD3	Analogue Input	Right channel line input / Right channel positive differential MIC input / Jack detect input pin
8	DCVDD	Supply	Digital core supply
9	DGND	Supply	Digital ground (Return path for both DCVDD and DBVDD)
10	DBVDD	Supply	Digital buffer (I/O) supply
11	MCLK	Digital Input	Master clock
12	BCLK	Digital Input / Output	Audio interface bit clock
13	DACLRC	Digital Input / Output	Audio interface DAC left / right clock
14	DACDAT	Digital Input	DAC digital audio data
15	ADCLRC / GPIO1	Digital Input / Output	Audio interface ADC left / right clock / GPIO1 pin
16	ADCDAT	Digital Output	ADC digital audio data
17	SCLK	Digital Input	Control interface clock input
18	SDIN	Digital Input/Output	Control interface data input / 2-wire acknowledge output
19	SPK_RN	Analogue Output	Right speaker negative output
20	SPKGND2	Supply	Ground for speaker drivers 2
21	SPKVDD2	Supply	Supply for speaker drivers 2
22	SPK_RP	Analogue Output	Right speaker positive output
23	SPK_LN	Analogue Output	Left speaker negative output
24	SPKGND1	Supply	Ground for speaker drivers 1
25	SPK_LP	Analogue Output	Left speaker positive output
26	SPKVDD1	Supply	Supply for speaker drivers 1
27	VMID	Analogue Output	Midrail voltage decoupling capacitor
28	AGND	Supply	Analogue ground (Return path for AVDD)
29	HP_R	Analogue Output	Right output (Line or headphone)
30	OUT3	Analogue Output	Mono, left, right or buffered midrail output for capless mode
31	HP_L	Analogue Output	Left output (Line or headphone)
32	AVDD	Supply	Analogue supply
33	GND_PADDLE		Die Paddle (Note 1)

Note:

1.   It is recommended that the QFN ground paddle should be connected to analogue ground on the application PCB.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (excluding SPKVDD1 and SPKVDD2)	-0.3V	+4.5V
SPKVDD1, SPKVDD2	-0.3V	+7V
Voltage range digital inputs	DGND -0.3V	DBVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Operating temperature range, T_A	-40°C	+85°C
Storage temperature after soldering	-65°C	+150°C

Notes:

1. Analogue, digital and speaker grounds must always be within 0.3V of each other.

2. All digital and analogue supplies are completely independent from each other (i.e. not internally connected).

3. DCVDD must be less than or equal to AVDD and DBVDD.

4. AVDD must be less than or equal to SPKVDD1 and SPKVDD2.

5. SPKVDD1 and SPKVDD2 must be high enough to support the peak output voltage when using DCGAIN and ACGAIN functions, to avoid output waveform clipping. Peak output voltage is AVDD*(DCGAIN+ACGAIN)/2.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD	1.71		3.6	V
Digital supply range (Buffer)	DBVDD	1.71		3.6	V
Analogue supplies range	AVDD	2.7		3.6	V
Speaker supply range	SPKVDD1, SPKVDD2	2.7		5.5	V
Ground	DGND, AGND, SPKGND1, SPKGND2		0		V

ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = SPKVDD1 = SPKVDD2 = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (LINPUT1, RINPUT1, LINPUT2, LINPUT3, RINPUT2, RINPUT3)						
Full-scale Input Signal Level – note this changes in proportion to AVDD	V_{INFS}	L/RINPUT1,2,3 Single-ended		1.0 0		Vrms dBV
		L/RINPUT1,2,3 Differential MIC		0.5 -6		Vrms dBV
Mic PGA equivalent input noise		0 to 20kHz, +30dB gain		150		uV
Input resistance (Note that input boost and bypass path resistances will be seen in parallel with PGA input resistance when these paths are enabled)	L/R$_{INPUT1}$	+30dB PGA gain Differential or single-ended MIC configuration		3		kΩ
	L/R$_{INPUT1}$	0dB PGA gain Differential or single-ended MIC configuration		49		kΩ
	L/R$_{INPUT1}$	-17.25dB PGA gain Differential or single-ended MIC configuration		87		kΩ
	L/R$_{INPUT2,}$ L/R$_{INPUT3}$	(Constant for all gains) Differential MIC configuration		85		kΩ
	L/R$_{INPUT2,}$ L/R$_{INPUT3}$	Max boost gain L/RINPUT2/3 to boost		7.5		kΩ
	L/R$_{INPUT2,}$ L/R$_{INPUT3}$	0dB boost gain L/RINPUT2/3 to boost		13		kΩ
	L/R$_{INPUT2,}$ L/R$_{INPUT3}$	Min boost gain L/RINPUT2/3 to boost		37		kΩ
	L/R$_{INPUT3}$	Max bypass gain L/RINPUT3 to bypass		17		kΩ
	L/R$_{INPUT3}$	Min bypass gain L/RINPUT3 to bypass		70		kΩ
Input capacitance				10		pF
MIC Programmable Gain Amplifier (PGA)						
Programmable Gain Min				-17.25		dB
Programmable Gain Max				30		dB
Programmable Gain Step Size		Guaranteed monotonic		0.75		dB
Mute Attenuation		LMIC2B = 0 and RMIC2B = 0		85		dB
Selectable Input Gain Boost						
Gain Boost Steps		Input from PGA		0, 13, 20, 29, MUTE		dB
		Input from L/RINPUT2 or L/RINPUT3		-12, -9, -6, -3, 0, 3, 6, MUTE		dB
Analogue Inputs (LINPUT1/2 Differential, RINPUT1/2 Differential) to ADC out via MIC PGA						
Signal to Noise Ratio (A-weighted)	SNR	AVDD = 3.3V		94		dB
		AVDD = 2.7V		93		
Total Harmonic Distortion Plus Noise	THD+N	-3dBFs input, AVDD = 3.3V		-86 0.005		dB %
		-3dBFs input, AVDD = 2.7V		-80 0.01		

Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = SPKVDD1 = SPKVDD2 = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Total Harmonic Distortion	THD	-3dBFs input, AVDD = 3.3V		-89 0.004		dB %
		-3dBFs input, AVDD = 2.7V		-81 0.009		
Analogue Inputs (LINPUT2, RINPUT2) to ADC out						
Signal to Noise Ratio (A-weighted)	SNR	AVDD = 3.3V	84	94		dB
		AVDD = 2.7V		93		
Total Harmonic Distortion Plus Noise	THD+N	-3dBFs input, AVDD = 3.3V		-86 0.005	-80	dB %
		-3dBFs input, AVDD = 2.7V		-80 0.01		
Total Harmonic Distortion	THD	-3dBFs input, AVDD = 3.3V		-89 0.004	-80	dB %
		-3dBFs input, AVDD = 2.7V		-81 0.009		
Analogue Inputs (LINPUT3, RINPUT3) to ADC out						
Signal to Noise Ratio (A-weighted)	SNR	AVDD = 3.3V		94		dB
		AVDD = 2.7V		93		
Total Harmonic Distortion Plus Noise	THD+N	-3dBFs input, AVDD = 3.3V		-86 0.005		dB %
		-3dBFs input, AVDD = 2.7V		-80 0.01		
Total Harmonic Distortion	THD	-3dBFs input, AVDD = 3.3V		-89 0.004		dB %
		-3dBFs input, AVDD = 2.7V		-81 0.009		
Analogue Inputs (LINPUT1, RINPUT1, LINPUT2, RINPUT2, LINPUT3, RINPUT3) to ADC out						
ADC Channel Separation		1kHz full scale signal into ADC via L/RINPUT1, MIC amp (single-ended) and boost		95		dB
		1kHz full scale signal into ADC via L/RINPUT1/2, MIC amp (pseudo-differential) and boost		85		dB
		1kHz full scale signal into ADC via L/RINPUT2 and boost		85		dB
		1kHz full scale signal into ADC via L/RINPUT3 and boost		92		dB
Line Input / MIC Separation (Quiescent input to ADC via boost; Output on ADC; 1kHz on L/RINPUT3 to HP out via bypass path)		Single-ended MIC input on L/RINPUT1		98		dB
		Differential MIC input using L/RINPUT2		90		dB
Boost / Bypass Separation (Quiescent L/RINPUT3 to HP outputs via bypass)		1kHz on LINPUT2 to ADC via boost only		96		dB
		1kHz on LINPUT1 to ADC via single-ended MIC PGA & boost		116		dB
Channel Matching		1kHz signal		0.2		dB

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Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = SPKVDD1 = SPKVDD2 = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Headphone Outputs (HP_L, HP_R)						
0dB Full scale output voltage				AVDD/3.3		Vrms
Mute attenuation		1kHz, full scale signal		86		dB
Channel Separation		L/RINPUT3 to headphone outputs via bypass		110		dB
DAC to Line-Out (HP_L or HP_R with 10kΩ / 50pF load)						
Signal to Noise Ratio (A-weighted)	SNR	AVDD=3.3V	90	99		dB
		AVDD=2.7V		98		
Total Harmonic Distortion Plus Noise	THD+N	AVDD=3.3V		-85	-80	dB
		AVDD=2.7V		-90		
Total Harmonic Distortion	THD	AVDD=3.3V		-87	-80	dB
		AVDD=2.7V		-92		
Channel Separation		1kHz full scale signal		110		dB
DAC to Line-Out (OUT3 with 10kΩ / 50pF load)						
Signal to Noise Ratio (A-weighted)	SNR	AVDD=3.3V		99		dB
		AVDD=2.7V		98		
Total Harmonic Distortion Plus Noise	THD+N	AVDD=3.3V		-85		dB
		AVDD=2.7V		-90		
Total Harmonic Distortion	THD	AVDD=3.3V		-87		dB
		AVDD=2.7V		-92		
Channel Separation		1kHz full scale signal		110		dB
Headphone Output (HP_L, HP_R, using capacitors unless otherwise specified)						
Output Power per channel	P_O	Output power is very closely correlated with THD; see below.				
Total Harmonic Distortion Plus Noise	THD+N	AVDD=2.7V, R_L=32Ω P_O=5mW		-78 0.013		dB %
		AVDD=2.7V, R_L=16Ω P_O=5mW		-75 0.018		
		AVDD=3.3V, R_L=32Ω, P_O=20mW		-72 0.025		
		AVDD=3.3V, R_L=16Ω, P_O=20mW		-70 0.032		
Signal to Noise Ratio (A-weighted)	SNR	AVDD = 3.3V	92	99		dB
		AVDD = 2.7V		98		
Speaker Outputs (DAC to SPK_LP, SPK_LN, SPK_RP, SPK_RN with 8Ω bridge tied load)						
Output Power	P_O	Output power is very closely correlated with THD; see below				
Total Harmonic Distortion Plus Noise (DAC to speaker outputs)	THD+N	P_O =200mW, R_L = 8Ω, SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V		-78 0.013		dB %
		P_O =320mW, R_L = 8Ω, SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V		-72 0.025		dB %
		P_O =500mW, R_L = 8Ω, SPKVDD1=SPKVDD2 =5V; AVDD=3.3V		-75 0.018		dB %
		P_O =1W, R_L = 8Ω, SPKVDD1=SPKVDD2 =5V; AVDD=3.3V		-70 0.032		dB %

Test Conditions

DCVDD = 1.8V, DBVDD = 3.3V, AVDD = SPKVDD1 = SPKVDD2 = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Total Harmonic Distortion Plus Noise (LINPUT3 and RINPUT3 to speaker outputs)	THD+N	P_O =200mW, R_L = 8Ω, SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V		-78 0.013		dB %
		P_O =320mW, R_L = 8Ω, SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V		-72 0.025		dB %
		P_O =500mW, R_L = 8Ω, SPKVDD1=SPKVDD2 =5V; AVDD=3.3V		-75 0.018		dB %
		P_O =1W, R_L = 8Ω, SPKVDD1=SPKVDD2 =5V; AVDD=3.3V		-70 0.032		dB %
Signal to Noise Ratio (A-weighted) (DAC to speaker outputs)	SNR	SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V; R_L = 8Ω, ref=2.0Vrms		90		dB
		SPKVDD1=SPKVDD2 =5V; AVDD=3.3V; R_L = 8Ω, ref=2.8Vrms		92		dB
Signal to Noise Ratio (A-weighted) (LINNPUT3 and RINPUT3 to speaker outputs)	SNR	SPKVDD1=SPKVDD2 =3.3V; AVDD=3.3V; R_L = 8Ω, ref=2.0Vrms		90		dB
		SPKVDD1=SPKVDD2 =5V; AVDD=3.3V; R_L = 8Ω, ref=2.8Vrms		92		dB
Speaker Supply Leakage current	I_{SPKVDD}	SPKVDD1=SPKVDD2 =5V; All other supplies disconnected		1		uA
		SPKVDD1=SPKVDD2 =5V; All other supplies 0V		1		uA
Power Supply Rejection Ratio (100mV ripple on SPKVDD1/SPKVDD2 @217Hz)	PSRR	DAC to speaker playback		80		dB
		L/RINPUT3 to speaker playback		80		dB
Analogue Reference Levels						
Midrail Reference Voltage	VMID		–3%	AVDD/2	+3%	V
Microphone Bias						
Bias Voltage	$V_{MICBIAS}$	3mA load current MBSEL=1	–5%	0.9×AVDD	+ 5%	V
		3mA load current MBSEL=0	–5%	0.65×AVDD	+ 5%	V
Bias Current Source	$I_{MICBIAS}$				3	mA
Output Noise Voltage	Vn	1K to 20kHz		15		nV/√Hz
Digital Input / Output						
Input HIGH Level	V_{IH}		0.7×DBVDD			V
Input LOW Level	V_{IL}				0.3×DBVDD	V
Output HIGH Level	V_{OH}	I_{OL}=1mA	0.9×DBVDD			V
Output LOW Level	V_{OL}	I_{OH}=-1mA			0.1×DBVDD	V
Input capacitance				10		pF
Input leakage			-0.9		0.9	uA
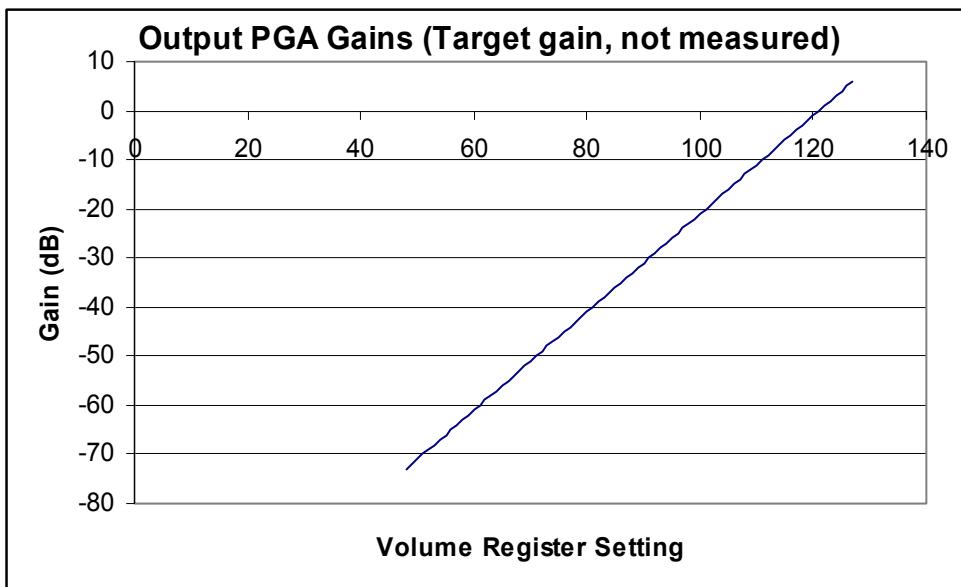
OUTPUT PGA GAIN

Figure 1 Output PGA Gains (LOUT1VOL, ROUT1VOL, SPKLVOL, SPKRVOL)

TYPICAL POWER CONSUMPTION

OFF, SLEEP MODE								
	DCVDD (V)	DBVDD (V)	SPKVDD (V)	AVDD (V)	DCVDD (mA)	DBVDD (mA)	SPKVDD (mA)	AVDD (mA)	Total Power (mW)
Off - Default state at power up	1.71	1.71	2.7	2.7	0.00	0.00	0.00	0.03	0.08
	1.8	1.8	3	3	0.00	0.00	0.00	0.03	0.10
	1.8	3.3	3.3	3.3	0.00	0.00	0.00	0.03	0.11
	3.6	3.6	5.5	3.6	0.00	0.00	0.00	0.03	0.13
Off - Thermal sensor disabled, no clocks	1.71	1.71	2.7	2.7	0.00	0.00	0.00	0.01	0.02
	1.8	1.8	3	3	0.00	0.00	0.00	0.01	0.03
	1.8	3.3	3.3	3.3	0.00	0.00	0.00	0.01	0.03
	3.6	3.6	5.5	3.6	0.00	0.00	0.00	0.01	0.04
Sleep - Thermal sensors enabled, VMID enabled using 250k VMID resistors	1.71	1.71	2.7	2.7	0.00	0.00	0.00	0.03	0.09
	1.8	1.8	3	3	0.00	0.00	0.00	0.04	0.11
	1.8	3.3	3.3	3.3	0.00	0.00	0.00	0.04	0.12
	3.6	3.6	5.5	3.6	0.00	0.00	0.00	0.04	0.13

PLAYBACK MODE								
	DCVDD (V)	DBVDD (V)	SPKVDD (V)	AVDD (V)	DCVDD (mA)	DBVDD (mA)	SPKVDD (mA)	AVDD (mA)	Total Power (mW)
Playback Mode - Playback to 8Ohm speakers, slave mode (no signal)	1.71	1.71	2.7	2.7	3.15	0.00	1.45	4.89	22.5
	1.8	1.8	3	3	3.34	0.00	1.63	5.53	27.5
	1.8	3.3	3.3	3.3	3.33	0.01	1.81	6.18	32.4
	3.6	3.6	5.5	3.6	7.53	0.00	3.23	6.85	69.5
Playback Mode - Playback to 8Ohm speakers, slave mode (0dB FS 1kHz signal)	1.71	1.71	2.7	2.7	3.27	0.00	267	4.93	738.5
	1.8	1.8	3	3	3.47	0.00	293	5.58	902.4
	1.8	3.3	3.3	3.3	3.47	0.01	321	6.23	1085.6
	3.6	3.6	5.5	3.6	8.76	0.01	511	6.54	2868.2
Playback Mode - Playback to 8Ohm speakers, master mode, PLL enabled (no signal)	1.71	1.71	2.7	2.7	2.99	0.47	1.47	5.82	25.6
	1.8	1.8	3	3	3.16	0.49	1.65	6.57	31.2
	1.8	3.3	3.3	3.3	3.16	0.92	1.84	7.34	39.0
	3.6	3.6	5.5	3.6	7.95	1.00	3.29	8.12	79.6
Playback Mode - Playback to 16Ohm HP, slave mode. No Signal	1.71	1.71	2.7	2.7	3.15	0.00	0.00	3.75	15.5
	1.8	1.8	3	3	3.33	0.00	0.00	4.24	18.7
	1.8	3.3	3.3	3.3	3.33	0.01	0.00	4.74	21.7
	3.6	3.6	5.5	3.6	8.25	0.00	0.00	5.25	48.6
Playback Mode - Playback to 16Ohm HP, slave mode (0dB FS 1kHz signal)	1.71	1.71	2.7	2.7	3.26	0.00	0.00	38.68	110.0
	1.8	1.8	3	3	3.46	0.00	0.00	43.53	136.8
	1.8	3.3	3.3	3.3	3.46	0.01	0.00	48.32	165.7
	3.6	3.6	5.5	3.6	8.52	0.00	0.00	53.06	221.7
Playback Mode - Playback to 16Ohm HP, slave mode (5mW/channel output)	1.71	1.71	2.7	2.7	3.26	0.00	0.00	17.44	52.7
	1.8	1.8	3	3	3.44	0.00	0.00	17.91	59.9
	1.8	3.3	3.3	3.3	3.45	0.01	0.00	18.37	66.9
	3.6	3.6	5.5	3.6	8.51	0.00	0.00	18.84	98.5
Playback Mode - Playback to 16Ohm HP, slave mode. (0.1mW/channel output)	1.71	1.71	2.7	2.7	3.25	0.00	0.00	5.47	20.3
	1.8	1.8	3	3	3.45	0.00	0.00	5.92	24.0
	1.8	3.3	3.3	3.3	3.45	0.01	0.00	6.37	27.2
	3.6	3.6	5.5	3.6	8.49	0.00	0.00	6.83	55.2
Playback Mode - Playback to 16Ohm HP, master mode, PLL enabled (no signal)	1.71	1.71	2.7	2.7	2.97	0.47	0.00	4.69	18.5
	1.8	1.8	3	3	3.14	0.49	0.00	5.29	22.4
	1.8	3.3	3.3	3.3	3.14	0.92	0.00	5.91	28.2
	3.6	3.6	5.5	3.6	7.91	1.01	0.00	6.55	55.7
Playback Mode - Playback to 10kOhm HP, slave mode (0dB FS 1kHz signal)	1.71	1.71	2.7	2.7	3.26	0.00	0.00	3.81	15.9
	1.8	1.8	3	3	3.46	0.00	0.00	4.30	19.1
	1.8	3.3	3.3	3.3	3.45	0.01	0.00	4.80	22.1
	3.6	3.6	5.5	3.6	8.51	0.00	0.00	5.31	49.8
Bypass Mode - Stereo playback bypassing ADC and DAC to Class D 8Ohm speaker (no signal)	1.71	1.71	2.7	2.7	0.28	0.00	1.47	3.07	12.7
	1.8	1.8	3	3	0.30	0.00	1.64	3.48	15.9
	1.8	3.3	3.3	3.3	0.30	0.01	1.82	3.91	19.5
	3.6	3.6	5.5	3.6	0.76	0.00	3.27	4.35	36.4
Bypass Mode - Stereo playback bypassing ADC and DAC to 16Ohm HP (no signal)	1.71	1.71	2.7	2.7	0.00	0.00	0.00	1.84	5.0
	1.8	1.8	3	3	0.00	0.00	0.00	2.09	6.3
	1.8	3.3	3.3	3.3	0.00	0.00	0.00	2.36	7.8
	3.6	3.6	5.5	3.6	0.00	0.00	0.00	2.62	9.5

RECORD MODE								
	DCVDD (V)	DBVDD (V)	SPKVDD (V)	AVDD (V)	DCVDD (mA)	DBVDD (mA)	SPKVDD (mA)	AVDD (mA)	Total Power (mW)
Record Mode - Stereo I/P into ADC sampling at 16kHz (no signal)	1.71	1.71	2.7	2.7	1.10	0.01	0.00	5.84	17.7
	1.8	1.8	3	3	1.17	0.01	0.00	6.24	20.8
	1.8	3.3	3.3	3.3	1.17	0.01	0.00	6.64	24.1
	3.6	3.6	5.5	3.6	2.92	0.01	0.00	7.05	35.9
Record Mode - Stereo I/P into ADC sampling at 44.1kHz (no signal)	1.71	1.71	2.7	2.7	2.99	0.01	0.00	5.99	21.3
	1.8	1.8	3	3	3.19	0.01	0.00	6.41	25.0
	1.8	3.3	3.3	3.3	3.19	0.03	0.00	6.83	28.4
	3.6	3.6	5.5	3.6	7.94	0.02	0.00	7.26	54.8
Record Mode - Stereo I/P into ADC sampling at 48kHz (no signal)	1.71	1.71	2.7	2.7	3.27	0.02	0.00	6.01	21.9
	1.8	1.8	3	3	3.47	0.02	0.00	6.44	25.6
	1.8	3.3	3.3	3.3	3.47	0.03	0.00	6.86	29.0
	3.6	3.6	5.5	3.6	8.63	0.03	0.00	7.29	57.4
Record Mode - Stereo I/P into ADC sampling at 44.1kHz with ALC enabled (no signal)	1.71	1.71	2.7	2.7	3.01	0.01	0.00	5.99	21.4
	1.8	1.8	3	3	3.20	0.02	0.00	6.41	25.0
	1.8	3.3	3.3	3.3	3.20	0.03	0.00	6.84	28.4
	3.6	3.6	5.5	3.6	7.97	0.03	0.00	7.27	54.9

Note:

1. Power in the load is included.

## SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING
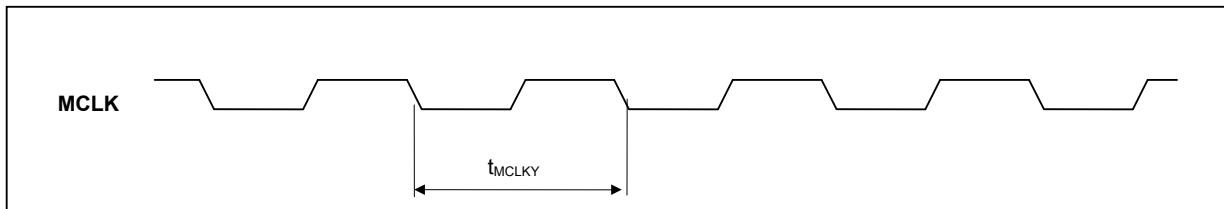
Figure 2 System Clock Timing Requirements

Test Conditions
DCVDD=1.8V, DBVDD=AVDD=SPKVDD1=SPKVDD2=3.3V, DGND=AGND=SPKGND1=SPKGND2=0V, T_A = +25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK cycle time	T_{MCLKY}		33.33			ns
MCLK duty cycle	T_{MCLKDS}		60:40		40:60	

AUDIO INTERFACE TIMING – MASTER MODE
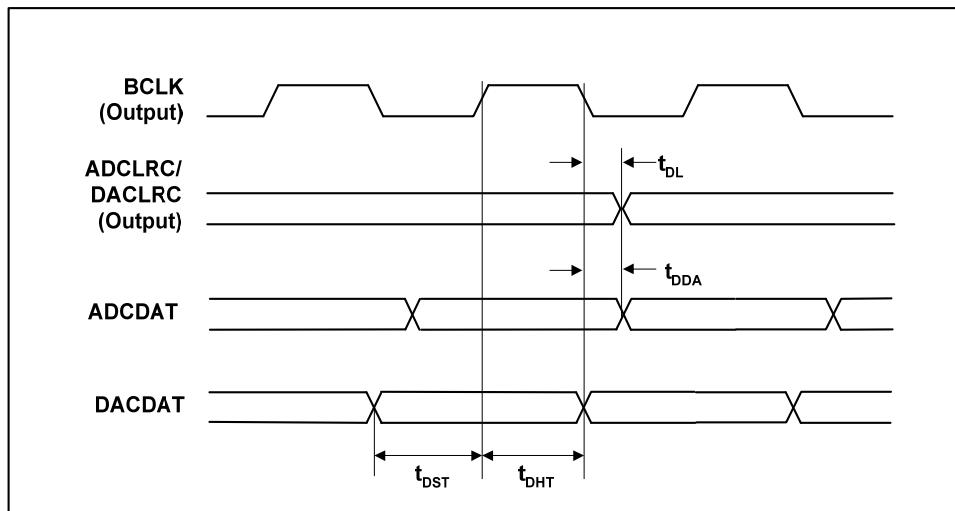
Figure 2 Digital Audio Data Timing – Master Mode (see Control Interface)

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD1=SPKVDD2=3.3V, DGND=AGND=SPKGND1=SPKGND2=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
ADCLRC/DACLRC propagation delay from BCLK falling edge	t_{DL}			10	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			10	ns
DACDAT setup time to BCLK rising edge	t_{DST}	10			ns
DACDAT hold time from BCLK rising edge	t_{DHT}	10			ns
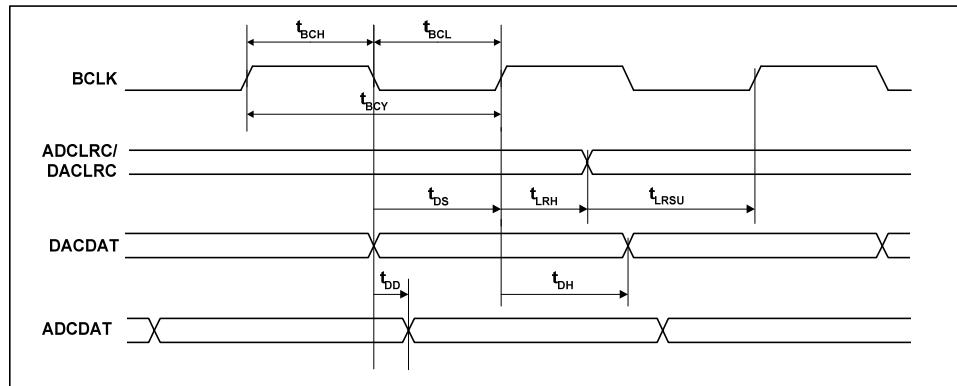
AUDIO INTERFACE TIMING – SLAVE MODE

Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD1=SPKVDD2=3.3V, DGND=AGND=SPKGND1=SPKGND2=0V, T_A=+25°C, Slave Mode, fs=48kHz,
MCLK= 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t_{BCY}	50			ns
BCLK pulse width high	t_{BCH}	20			ns
BCLK pulse width low	t_{BCL}	20			ns
ADCLRC/DACLRC set-up time to BCLK rising edge	t_{LRSU}	10			ns
ADCLRC/DACLRC hold time from BCLK rising edge	t_{LRH}	10			ns
DACDAT hold time from BCLK rising edge	t_{DH}	10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			10	ns
DACDAT set-up time to BCLK rising edge	t_{DS}	10			ns

Note:

BCLK period should always be greater than or equal to MCLK period.

## CONTROL INTERFACE TIMING – 2-WIRE MODE
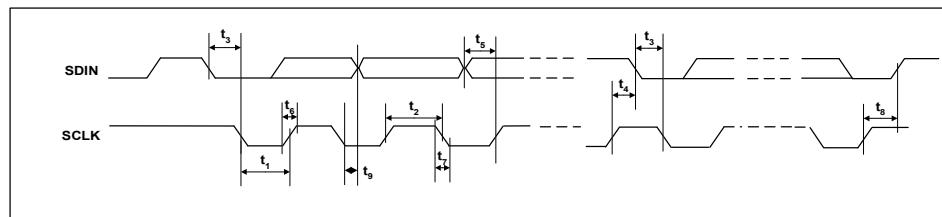
Figure 4 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD1=SPKVDD2=3.3V, DGND=AGND=SPKGND1=SPKGND2=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

| PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency				526	kHz
SCLK Low Pulse-Width	t_1	1.3			us
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDIN, SCLK Rise Time	t_6			300	ns
SDIN, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

INTERNAL POWER ON RESET CIRCUIT
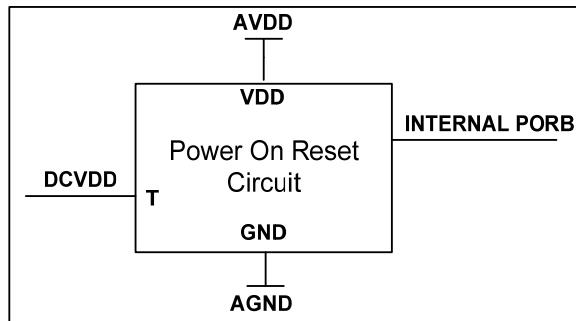
Figure 5 Internal Power on Reset Circuit Schematic

The WM8960 includes an internal Power-On-Reset Circuit, as shown in Figure 5, which is used to reset the digital logic into a default state after power up. The POR circuit is powered from AVDD and monitors DCVDD. It asserts PORB low if AVDD or DCVDD is below a minimum threshold.
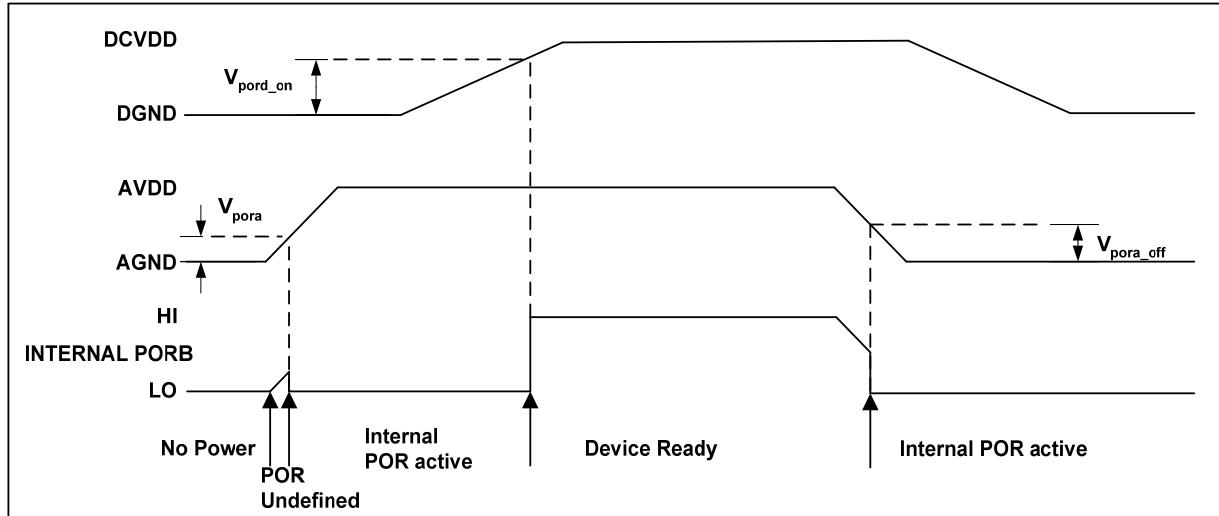

Figure 6 Typical Power up Sequence where AVDD is Powered before DCVDD

Figure 6 shows a typical power-up sequence where AVDD comes up first. When AVDD goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. Now AVDD is at full supply level. Next DCVDD rises to V_{pord_on} and PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where AVDD falls first, PORB is asserted low whenever AVDD drops below the minimum threshold V_{pora_off}.
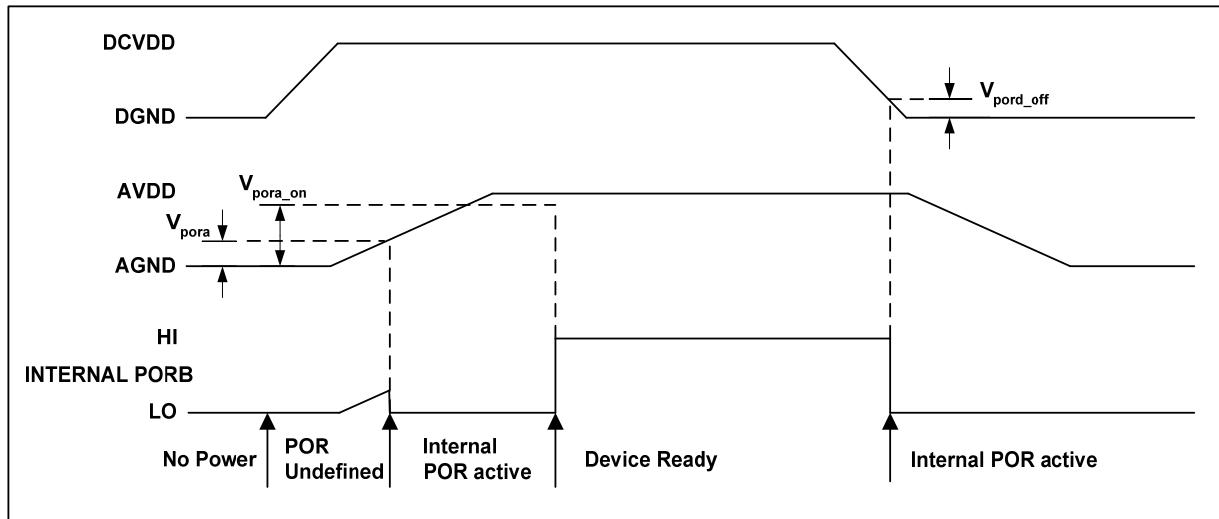
Figure 7 Typical Power up Sequence where DCVDD is Powered before AVDD

Figure 7 shows a typical power-up sequence where DCVDD comes up first. First it is assumed that DCVDD is already up to specified operating voltage. When AVDD goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When AVDD rises to V_{pora_on}, PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where DCVDD falls first, PORB is asserted low whenever DCVDD drops below the minimum threshold V_{pord_off}.

SYMBOL	MIN	TYP	MAX	UNIT
V_{pora}	0.4	0.6	0.8	V
V_{pora_on}	0.9	1.2	1.6	V
V_{pora_off}	0.4	0.6	0.8	V
V_{pord_on}	0.5	0.7	0.9	V
V_{pord_off}	0.4	0.6	0.8	V

Table 1 Typical POR Operation (typical values, not tested)

Notes:

1. If AVDD and DCVDD suffer a brown-out (i.e. drop below the minimum recommended operating level but do not go below V_{pora_off} or V_{pord_off}) then the chip will not reset and will resume normal operation when the voltage is back to the recommended level again.

2. The chip will enter reset at power down when AVDD or DCVDD falls below V_{pora_off} or V_{pord_off}. This may be important if the supply is turned on and off frequently by a power management system.

3. The minimum t_{por} period is maintained even if DCVDD and AVDD have zero rise time. This specification is guaranteed by design rather than test.

DEVICE DESCRIPTION

INTRODUCTION

The WM8960 is a low power audio CODEC offering a combination of high quality audio, advanced features, low power and small size. These characteristics make it ideal for portable digital audio applications with stereo speaker and headphone outputs such as games consoles, portable media players and multimedia phones.

Stereo class D speaker drivers can provide >1W per channel into 8Ω loads. BTL configuration provides high power output and excellent PSRR. Low leakage and pop/click suppression mechanisms allow direct battery connection, reducing component count and power consumption in portable battery-powered applications. Highly flexible speaker boost settings provide fully internal level-shifting of analogue output signals, allowing speaker output power to be maximised while minimising other analogue supply currents, and requiring no additional components.

A flexible input configuration includes support for two stereo microphone interfaces (single-ended or pseudo-differential) and additional stereo line inputs. Up to three stereo analogue input sources are available, removing the need for external analogue switches in many applications. Boost amplifiers are available for additional gain on the microphone inputs and a programmable gain amplifier with a mixed signal automatic level control (ALC) keeps the recording volume constant.

The stereo ADC and DAC are of hi-fi quality using a 24-bit, low-order oversampling architecture to deliver optimum performance. A flexible clocking arrangement supports mixed ADC and DAC sample rates.

The DAC output signal can be mixed with analogue input signals from the line inputs or bypass paths. This mix is available on speaker and headphone/line outputs.

The WM8960 has a configurable digital audio interface where ADC data can be read and digital audio playback data fed to the DAC. It supports a number of audio data formats including I^{2}S, DSP Mode (a burst mode in which frame sync plus two data packed words are transmitted), MSB-First, left justified and MSB-First, right justified, and can operate in master or slave modes. In PCM mode A-law and μ-law companding is supported.

The SYSCLK (system clock) provides clocking for the ADCs, DACs, DSP core, class D outputs and the digital audio interface. SYSCLK can be derived directly from the MCLK pin or via an integrated PLL, providing flexibility to support a wide range of clocking schemes. All MCLK frequencies typically used in portable systems are supported for sample rates between 8kHz and 48kHz. A flexible switching clock for the class D speaker drivers (synchronous with the audio DSP clocks for best performance) is also derived from SYSCLK.

To allow full software control over all its features, the WM8960 uses a 2 wire control interface. It is fully compatible and an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs. Unused circuitry can be disabled via software to save power, while low leakage currents extend standby and off time in portable battery-powered applications.

INPUT SIGNAL PATH

The WM8960 has three flexible stereo analogue input channels which can be configured as line inputs, differential microphone inputs or single-ended microphone inputs. Line inputs and microphone PGA outputs can be routed to the hi-fi ADCs or directly to the output mixers via a bypass path.

MICROPHONE INPUTS
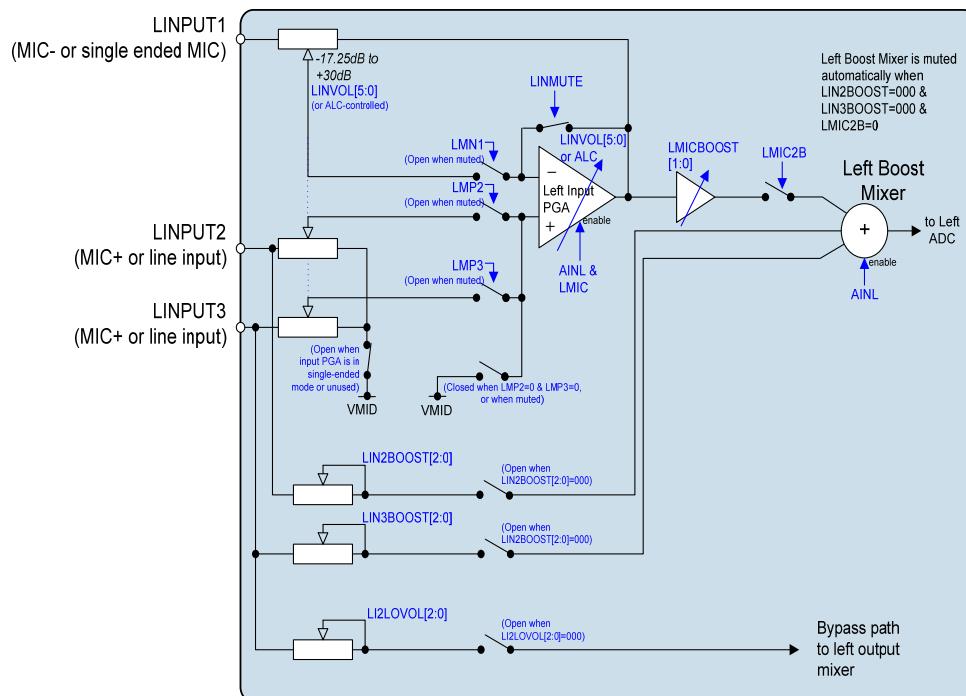
Differential microphones can be connected between LINPUT1 and LINPUT2 or LINPUT3, and between RINPUT1 and RINPUT2 or RINPUT3. Alternatively single-ended microphones can be connected to LINPUT1 or RINPUT1.

In single-ended microphone input configuration the microphone signal should be input to LINPUT1 or RINPUT1 and the internal non-inverting input of the input PGA should be switched to VMID.

In differential mode the larger signal should be input to LINPUT2 or LINPUT3 on the left channel, or RINPUT2 or RINPUT3 on the right channel. The smaller (e.g. noisy ground connection) should be input to LINPUT1 or RINPUT1.

The gain of the microphone PGAs can be controlled directly via software, or using the ALC / Limiter.

The inputs LINPUT2, RINPUT2, LINPUT3 and RINPUT3 should not be connected to the boost mixer or bypass path while operating as the non-inverting input in differential microphone configuration.
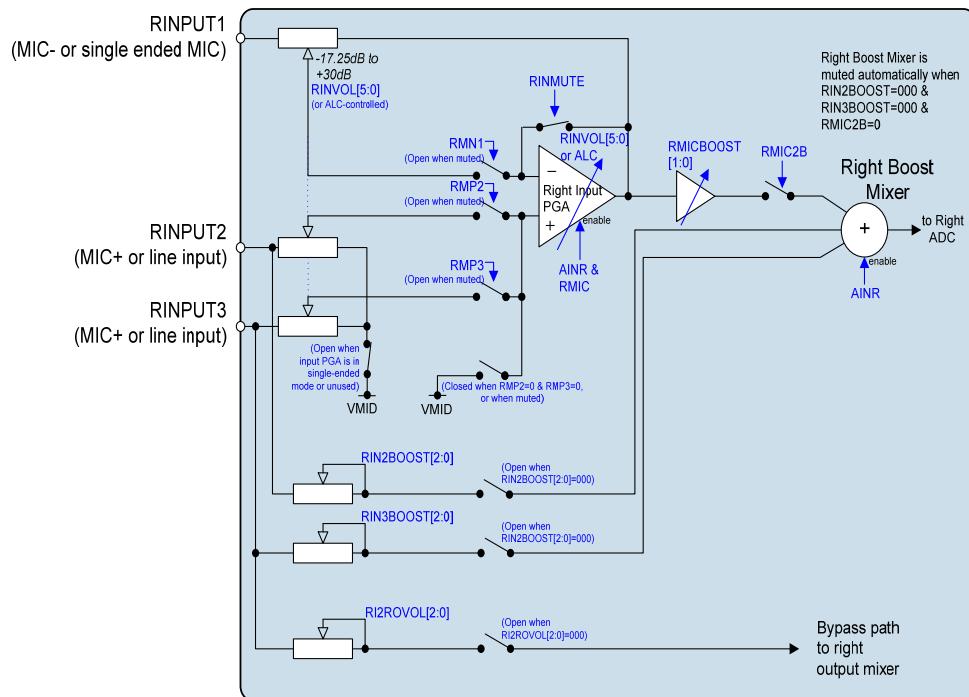
Figure 8 Microphone Input PGA Circuit

The input PGAs and boost mixers are enabled by the AINL and AINR register bits. The microphone PGAs can be also be disabled independently of the boost mixer to save power, using LMIC and RMIC register bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Power Management (1)	5	AINL	0	Left channel input PGA and boost stage enable 0 = PGA disabled, boost disabled 1 = PGA enabled (if LMIC = 1), boost enabled
	4	AINR	0	Right channel input PGA and boost stage enable 0 = PGA disabled, boost disabled 1 = PGA enabled (if LMIC = 1), boost enabled
R47 (2Fh) Power Management (3)	5	LMIC	0	Left channel input PGA enable 0 = PGA disabled 1 = PGA enabled (if AINL = 1)
	4	RMIC	0	Right channel input PGA enable 0 = PGA disabled 1 = PGA enabled (if AINR = 1)

Table 2 Input PGA and Boost Enable Register Settings

The input PGAs can be configured as differential inputs, using LINPUT1/LINPUT2 or LINPUT1/LINPUT3, and RINPUT1/RINPUT2 or RINPUT1/RINPUT3. The input impedance to these non-inverting inputs is constant in this configuration. Differential configuration is controlled by LMP2, LMP3, RMP2 and RMP3 as shown in Table 3.

When single-ended configuration is selected, the non-inverting input of the PGA is connected to VMID.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (20h) ADCL Input Signal Path	3	LMIC2B	0	Connect Left Input PGA to Left Input Boost mixer 0 = Not connected 1 = Connected
	6	LMP2	0	Connect LINPUT2 to non-inverting input of Left Input PGA 0 = LINPUT2 not connected to PGA 1 = LINPUT2 connected to PGA (Constant input impedance)
	7	LMP3	0	Connect LINPUT3 to non-inverting input of Left Input PGA 0 = LINPUT3 not connected to PGA 1 = LINPUT3 connected to PGA (Constant input impedance)
	8	LMN1	1	Connect LINPUT1 to inverting input of Left Input PGA 0 = LINPUT1 not connected to PGA 1 = LINPUT1 connected to PGA
R33 (21h) ADCR Input Signal Path	3	RMIC2B	0	Connect Right Input PGA to Right Input Boost mixer 0 = Not connected 1 = Connected
	6	RMP2	0	Connect RINPUT2 to non-inverting input of Right Input PGA 0 = RINPUT2 not connected to PGA 1 = RINPUT2 connected to PGA (Constant input impedance)
	7	RMP3	0	Connect RINPUT3 to non-inverting input of Right Input PGA 0 = RINPUT3 not connected to PGA 1 = RINPUT3 connected to PGA (Constant input impedance)
	8	RMN1	1	Connect RINPUT1 to inverting input of Right Input PGA 0 = RINPUT1 not connected to PGA 1 = RINPUT1 connected to PGA

Table 3 Input PGA Control

INPUT PGA VOLUME CONTROLS

The input PGAs have a gain range from -17.25dB to +30dB in 0.75dB steps. The gains from the inverting inputs (LINPUT1 and RINPUT1) to the PGA outputs and from the non-inverting inputs (LINPUT2/RINPUT2 and LINPUT3/RINPUT3) to the PGA output are always common in differential configuration and controlled by the register bits LINVOL[5:0] and RINVOL[5:0].

When the Automatic Level Control (ALC) is enabled the input PGA gains are controlled automatically and the LINVOL and RINVOL bits should not be used.

The left and right input PGAs can be independently muted using the LINMUTE and RINMUTE register bits.

To allow simultaneous volume updates of left and right channels, PGA gains are not altered until a 1 is written to the IPVU bit.

To prevent "zipper noise", a zero-cross function is provided, so that when enabled, volume updates will not take place until a zero-crossing is detected. In the event of a long period without zero-crossings, a timeout function is available. When this function is enabled (using the TOEN register bit), the volume will update automatically after a timeout. The timeout period is set by TOCLKSEL. Note that SYSCLK must be running to use this function.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (00h) Left Channel PGA	8	IPVU	N/A	Input PGA Volume Update Writing a 1 to this bit will cause left and right input PGA volumes to be updated (LINVOL and RINVOL)
	7	LINMUTE	1	Left Input PGA Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: IPVU must be set to un-mute.
	6	LIZC	0	Left Input PGA Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately
	5:0	LINVOL [5:0]	010111 (0dB)	Left Input PGA Volume Control 111111 = +30dB 111110 = +29.25dB . . 0.75dB steps down to 000000 = -17.25dB
R1 (01h) Right Channel PGA	8	IPVU	N/A	Input PGA Volume Update Writing a 1 to this bit will cause left and right input PGA volumes to be updated (LINVOL and RINVOL)
	7	RINMUTE	1	Right Input PGA Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: IPVU must be set to un-mute.
	6	RIZC	0	Right Input PGA Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately
	5:0	RINVOL [5:0]	010111 (0dB)	Right Input PGA Volume Control 111111 = +30dB 111110 = +29.25dB . . 0.75dB steps down to 000000 = -17.25dB
R23 (17h) Additional Control (1)	0	TOEN	0	Timeout Enable (Also enables jack detect debounce clock) 0 = Timeout disabled 1 = Timeout enabled
	1	TOCLKSEL	0	Slow Clock Selection (Used for volume update timeouts and for jack detect debounce) 0 = SYSCLK / 2^{21} (Slower Response) 1 = SYSCLK / 2^{19} (Faster Response)

Table 4 Input PGA Volume Control

See "Volume Updates" for more information on volume update bits, zero cross and timeout operation.

LINE INPUTS

Two pairs of stereo line inputs (LINPUT2 / RINPUT2 and LINPUT3 / RINPUT3) are available as analogue inputs into the ADC path. LINPUT3 and RINPUT3 can also be input directly to the output mixers via the bypass paths.

See "Output Signal Path" for more information on the bypass paths.

INPUT BOOST

The input path to the ADCs is via a boost stage, which can mix signals from the microphone PGAs and the line inputs.

The boost stage can provide up to +29dB additional gain from the microphone PGA output to the ADC input, providing a total maximum available analogue gain of +59dB from microphone to ADC. The microphone PGA path to the boost mixer is muted using LINMUTE and RINMUTE as shown in Table 4. Microphone PGA to boost gain settings are shown in Table 5.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (20h) ADCL Signal path	5:4	LMICBOOST [1:0]	00	Left Channel Input PGA Boost Gain 00 = +0dB 01 = +13dB 10 = +20dB 11 = +29dB
R33 (21h) ADCR Signal path	5:4	RMICBOOST [1:0]	00	Right Channel Input PGA Boost Gain 00 = +0dB 01 = +13dB 10 = +20dB 11 = +29dB

Table 5 Microphone PGA Boost Control

For line inputs, -12dB to +6dB gain is available on the boost mixer, with mute control, as shown in Table 6.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R43 (2Bh) Input Boost Mixer 1	6:4	LIN3BOOST [2:0]	000	LINPUT3 to Boost Mixer gain 000 = Mute 001 = -12dB ...3dB steps up to 111 = +6dB
	3:1	LIN2BOOST [2:0]	000	LINPUT2 to Boost Mixer gain 000 = Mute 001 = -12dB ...3dB steps up to 111 = +6dB
R44 (2Ch) Input Boost Mixer 2	6:4	RIN3BOOST [2:0]	000	RINPUT3 to Boost Mixer gain 000 = Mute 001 = -12dB ...3dB steps up to 111 = +6dB
	3:1	RIN2BOOST [2:0]	000	RINPUT2 to Boost Mixer gain 000 = Mute 001 = -12dB ...3dB steps up to 111 = +6dB

Table 6 Line Input Boost Control

When all three input paths to the boost mixer are disabled, the boost mixer will automatically be muted.

MICROPHONE BIASING CIRCUIT

The MICBIAS output provides a low noise reference voltage suitable for biasing electret type microphones and the associated external resistor biasing network. Refer to the Applications Information section for recommended external components. The MICBIAS voltage can be altered via the MBSEL register bit. When MBSEL=0, MICBIAS=0.9*AVDD and when MBSEL=1, MICBIAS=0.65*AVDD. The output can be enabled or disabled using the MICB control bit.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R25 (19h) Power management (1)	1	MICB	0	Microphone Bias Enable 0 = OFF (high impedance output) 1 = ON
R48 (30h) Additional Control (4)	0	MBSEL	0	Microphone Bias Voltage Control 0 = 0.9 * AVDD 1 = 0.65 * AVDD

Table 7 Microphone Bias Control

The internal MICBIAS circuitry is shown in Figure 9. The maximum source current capability for MICBIAS is 3mA. The external biasing resistors therefore must be large enough to limit the MICBIAS current to 3mA.
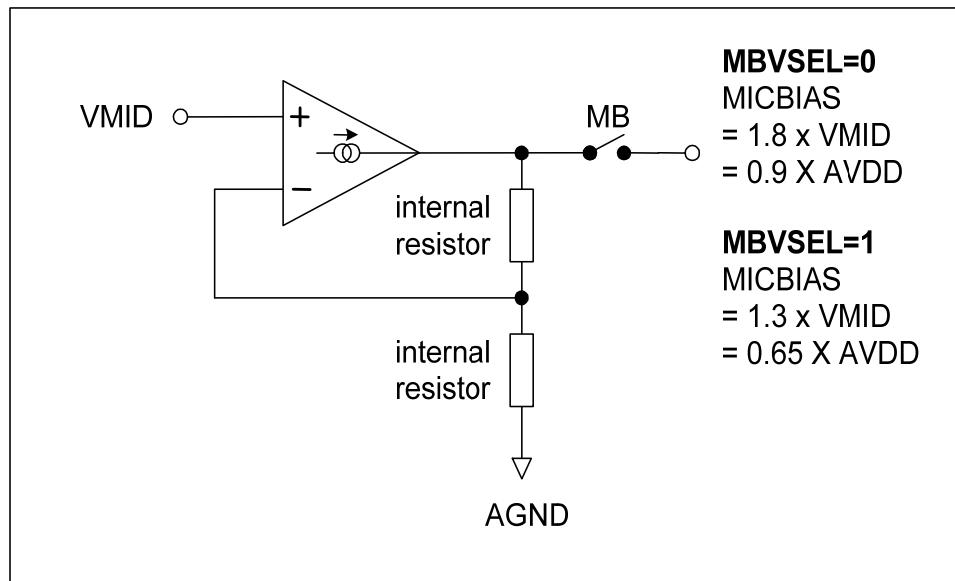

Figure 9 Microphone Bias Schematic

EXAMPLE INPUT CONFIGURATIONS

Some example input configurations are shown below.
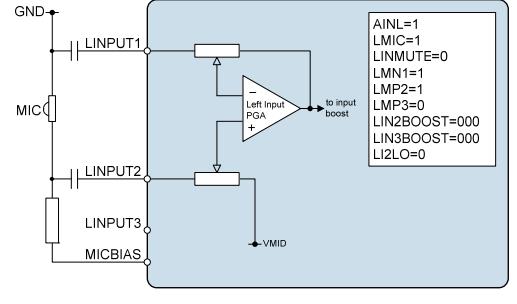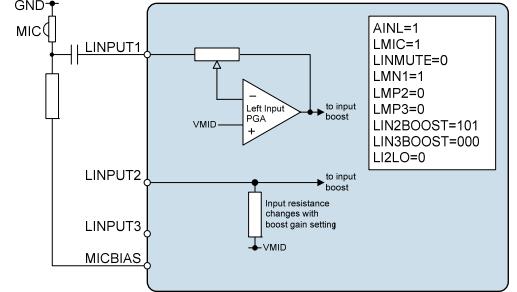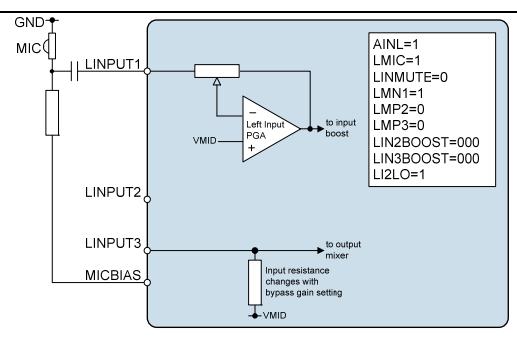
AINL=1 LMIC=1 LINMUTE=0 LMN1=1 LMP2=0 LMP3=0 LIN2BOOST=000 LIN3BOOST=000 LI2LO=0	Single-ended MIC configuration on left channel. LINPUT2 and LINPUT3 unused
AINL=1 LMIC=1 LINMUTE=0 LMN1=1 LMP2=1 LMP3=0 LIN2BOOST=000 LIN3BOOST=000 LI2LO=0	Pseudo-differential MIC configuration on left channel using LINPUT1 as ground connection and LINPUT2 as signal input. LINPUT3 unused.
AINL=1 LMIC=1 LINMUTE=0 LMN1=1 LMP2=0 LMP3=0 LIN2BOOST=101 LIN3BOOST=000 LI2LO=0	Single-ended MIC configuration on left channel. LINPUT2 used as additional input to boost stage. LINPUT3 unused.
AINL=1 LMIC=1 LINMUTE=0 LMN1=1 LMP2=0 LMP3=0 LIN2BOOST=000 LIN3BOOST=000 LI2LO=1	Single-ended MIC configuration on left channel. LINPUT3 used as input to bypass path. LINPUT2 unused.

Figure 10 Example Microphone Input Configurations (See also "Recommended External Components")