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WM8962

Ultra-Low Power Stereo CODEC with Audio Enhancement DSP, 1W Stereo Class D Speaker Drivers and Ground Referenced Headphone Drivers

DESCRIPTION

The WM8962 is a low power, high performance stereo CODEC designed for portable digital audio applications.

An integrated charge pump provides a ground referenced output which removes the need for DC-blocking capacitors on the headphone outputs, and uses the Wolfson 'Class-W' amplifier techniques - incorporating an innovative dual-mode charge pump architecture - to optimise efficiency and power consumption during playback. A DC Servo is used to reduce DC ground offsets. This improves power consumption and minimises pops and clicks.

Stereo class D speaker drivers provide 1W per channel into 8Ω loads, or 2W mono into a 4Ω load, with a 5V supply. Low leakage, excellent PSRR and pop/click suppression mechanisms also allow direct battery connection to the speaker supply. Flexible speaker boost settings allow speaker output power to be maximised while minimising other analogue supply currents.

Control sequences for audio path setup can be pre-loaded and executed by an integrated sequencer to reduce software driver development and eliminate pops and clicks via SilentSwitch™ technology.

Flexible input configuration: four stereo inputs or eight mono inputs on Left or Right ADC, with a complete analogue (four single-ended stereo inputs) and digital microphone interface. External component requirements are drastically reduced as no separate microphone, speaker or headphone amplifiers are required. Advanced on-chip digital signal processing performs automatic level control for the microphone or line input.

Stereo 24-bit sigma-delta ADCs and DACs are used with low power over-sampling digital interpolation and decimation filters and a flexible digital audio interface.

A programmable audio enhancement DSP is included with multiple preset algorithms. Virtual Surround Sound widens the stereo speaker audio image, HD Bass enhances low frequencies, and ReTune™ flattens the frequency response of the speaker or microphone path. A configurable DSP includes additional functions such as 3D widening for recording, a 5-band parametric EQ and Dynamic Range Controller.

Two high performance PLLs and one Frequency Locked Loop (FLL) are integrated to enable the user to clock a full audio system.

The WM8962 operates at analogue supply voltages down to 1.7V, although the digital supplies can operate at voltages down to 1.62V to save power. The speaker supply can operate at up to 5.5V. Unused functions can be disabled using software control to save power.

The WM8962 is supplied in a very small W-CSP package, ideal for use in hand-held and portable systems.

FEATURES

- DAC SNR 98dB ('A' weighted), THD -84dB at 48kHz, 1.8V
- ADC SNR 94dB ('A' weighted), THD -85dB at 48kHz, 1.8V
- Stereo Class D Speaker Driver
  - 1W per channel into 8Ω BTL speakers
  - 2W mono into 4Ω BTL speakers
  - Flexible internal switching clock
- Wolfson 'Class-W' ultra-low power headphone driver
  - Up to 31mW per channel output power at 1% THD+N into 16Ω at 1.8V
  - Ground Referenced
  - Low offset (+/- 1.2mV)
  - Pop and click suppression
  - Control sequencer for pop-minimised power-up/down
  - Single register write for default start-up sequence
- Microphone Interface
  - Single ended four stereo analogue input
  - Integrated low noise MICBIAS
  - Digital microphone interface
  - Programmable ALC / Limiter and Noise Gate
- Programmable Audio Enhancement DSP with Presets
  - Virtual Surround Sound
  - HD Bass
  - ReTune™
- Fixed Audio Processing DSP
  - 3D stereo widening
  - 5-band Parametric EQ
  - Dynamic range controller
  - Beep generator
- Two integrated PLLs enable clocking of full audio system
- Low Power Consumption
  - 7.7mW headphone playback
  - 8.3mW analogue record mode
- Low Supply Voltages
  - Analogue 1.7V to 2.0V (Speaker supply up to 5.5V)
  - Charge pump 1.7V to 2.0V
  - MIC bias amp supply 1.7V to 3.6V
  - Digital 1.62V to 2.0V
- 2-wire I2C and 3- or 4-wire SPI serial control interface
- Standard sample rates from 8kHz to 96kHz
- W-CSP, 3.6x3.9mm 49-pin

APPLICATIONS

- Portable gaming, Voice recorders
- Mobile multimedia
- Stereo DSC-Camcorder

BLOCK DIAGRAM

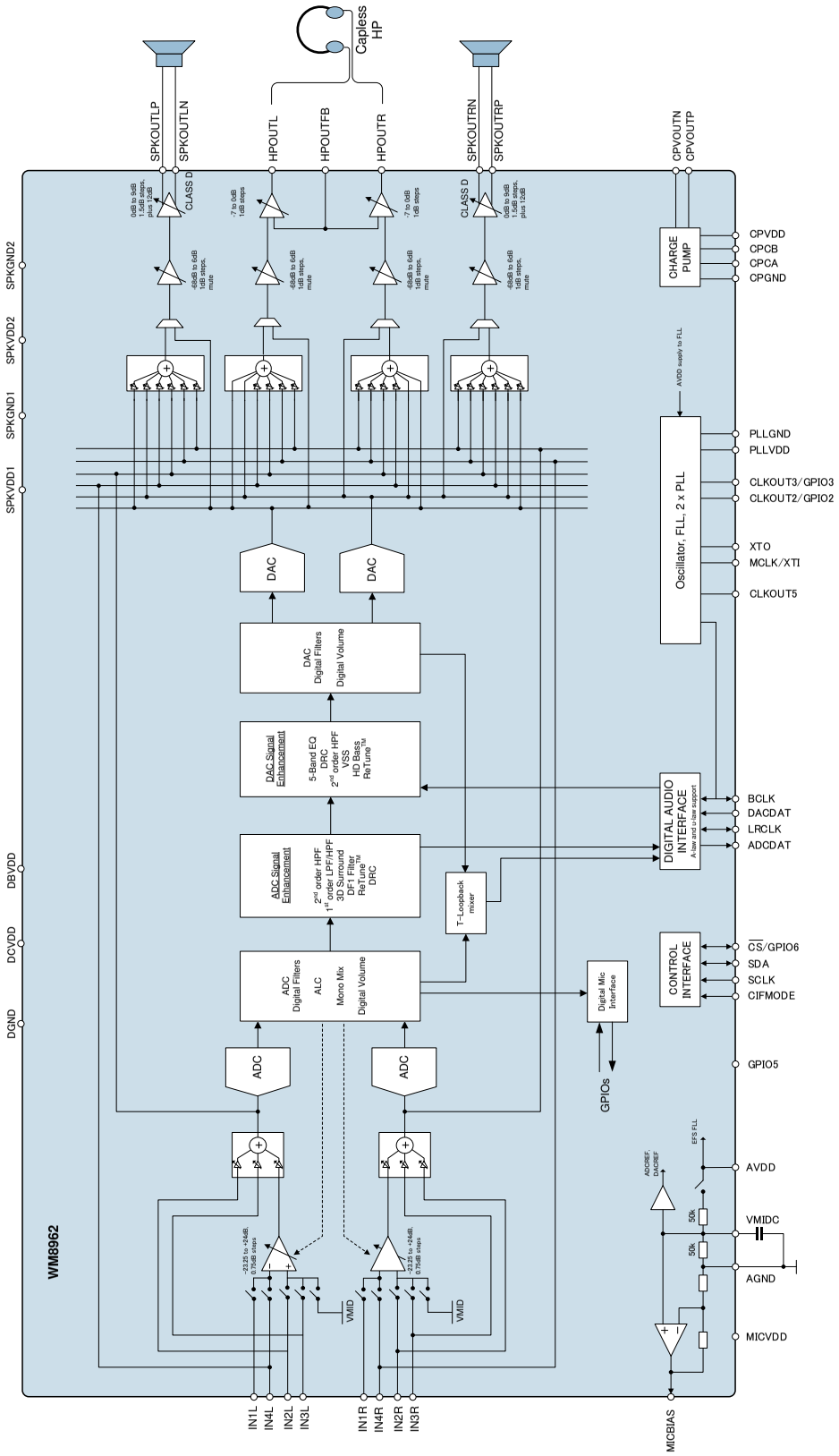
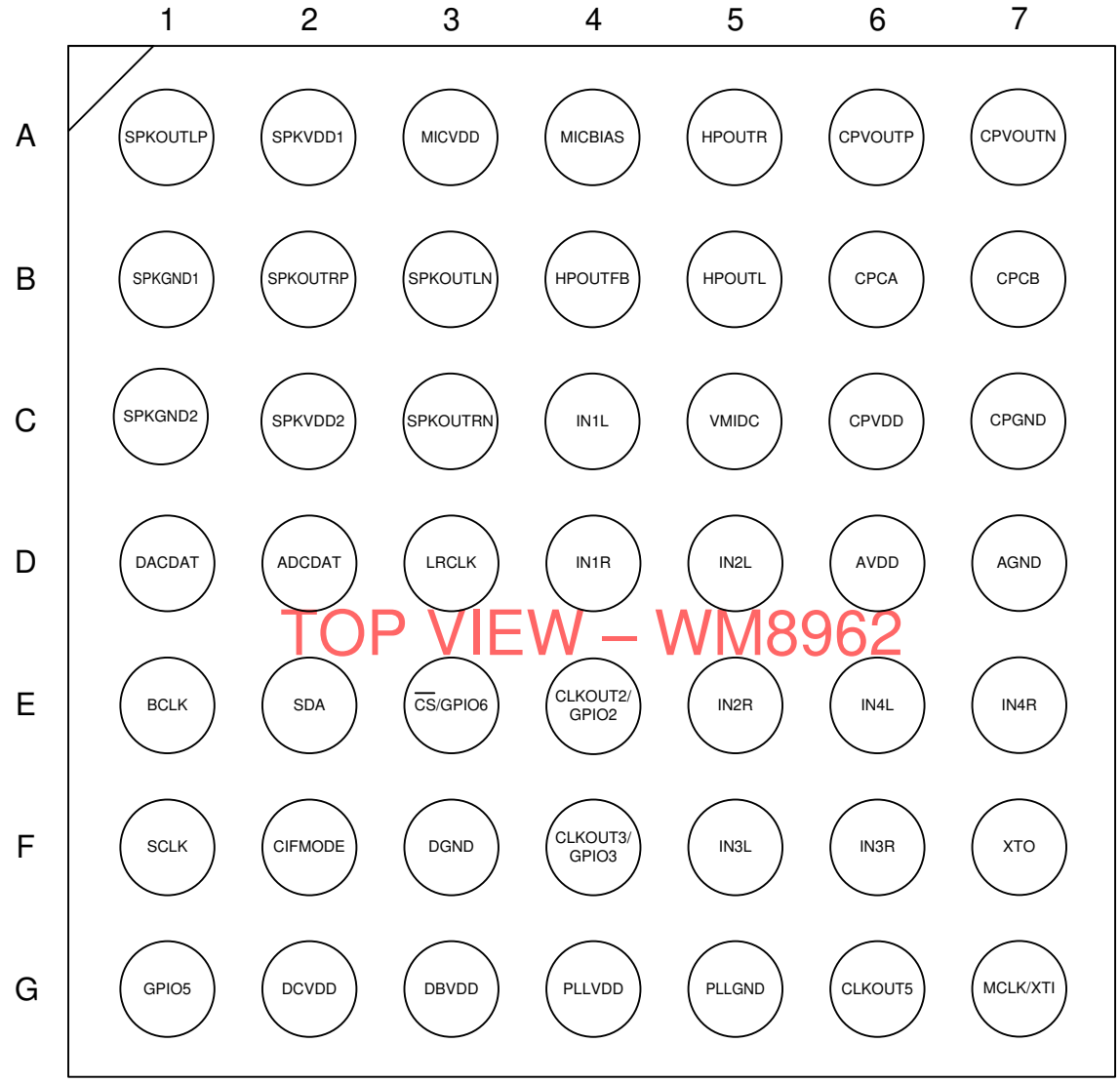


TABLE OF CONTENTS

PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8962ECS/R (see note 1)	-40°C to +85°C	49-ball CSP (3.6x3.9mm) (Pb-free, Tape and reel)	MSL1	260°C
WM8962ECSN/R (see note 2)	-40°C to +85°C	49-ball CSP (3.6x3.9mm) (Pb-free, Tape and reel)	MSL1	260°C

Note:

1. Reel quantity = 5,000
2. Reel quantity = 3,500

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
A1	SPKOUTLP	Analogue Output	Left speaker positive output
A2	SPKVDD1	Supply	Supply for left speaker drivers
A3	MICVDD	Supply	Microphone bias amp supply
A4	MICBIAS	Reference	Microphone bias
A5	HPOUTR	Analogue Output	Right output (Line or headphone)
A6	CPVOUTP	Supply	Charge pump positive supply (powers HPOUTL, HPOUTR)
A7	CPVOUTN	Supply	Charge pump negative supply (powers HPOUTL, HPOUTR)
B1	SPKGND1	Supply	Ground for left speaker drivers
B2	SPKOUTRP	Analogue Output	Right speaker positive output
B3	SPKOUTLN	Analogue Output	Left speaker negative output
B4	HPOUTFB	Analogue Input	HPOUTL/R ground loop noise rejection feedback
B5	HPOUTL	Analogue Output	Left output (Line or headphone)
B6	CPCA	Analogue Input	Charge pump fly-back capacitor pin
B7	CPCB	Analogue Input	Charge pump fly-back capacitor pin
C1	SPKGND2	Supply	Ground for right speaker drivers
C2	SPKVDD2	Supply	Supply for right speaker drivers
C3	SPKOUTRN	Analogue Output	Right speaker negative output
C4	IN1L	Analogue Input	Left channel single-ended input 1
C5	VMIDC	Reference	Mid-rail voltage (AVDD/2) - (requires decoupling capacitor)
C6	CPVDD	Supply	Charge pump power supply
C7	CPGND	Supply	Charge pump ground (return path for CPVDD)
D1	DACDAT	Digital Input	DAC digital audio data
D2	ADCDAT	Digital Output	ADC digital audio data
D3	LRCLK	Digital Input / Output	Audio interface left / right clock
D4	IN1R	Analogue Input	Right channel single-ended input 1
D5	IN2L	Analogue Input	Left channel single-ended input 2
D6	AVDD	Supply	Analogue supply
D7	AGND	Supply	Analogue ground (return path for AVDD and MICVDD)
E1	BCLK	Digital Input / Output	Audio interface bit clock
E2	SDA	Digital Input / Output	Control interface data input / 2-wire acknowledge output
E3	CS/GPIO6	Digital Input / Output	CS input / Digital Microphone input / General purpose input / output
E4	CLKOUT2/GPIO2	Digital Output	PLL2 Clock output / General purpose input / output
E5	IN2R	Analogue Input	Right channel single-ended input 2
E6	IN4L	Analogue Input	Left channel single-ended input 4
E7	IN4R	Analogue Input	Right channel single-ended input 4
F1	SCLK	Digital Input	Control interface clock input
F2	CIFMODE	Digital Input	Selects 2-wire or 3 / 4-wire control wire interface
F3	DGND	Supply	Digital ground
F4	CLKOUT3/GPIO3	Digital Output	PLL3 / FLL Clock output / GPIO
F5	IN3L	Analogue Input	Left channel single-ended input 3
F6	IN3R	Analogue Input	Right channel single-ended input 3
F7	XTO	Analogue Output	xtal output
G1	GPIO5	Digital Input / Output	Digital Microphone Input / General purpose input / output Important: See page 175 for start-up requirements.
G2	DCVDD	Supply	Digital Core Supply
G3	DBVDD	Supply	Digital Buffer Supply
G4	PLLVDD	Supply	PLL Supply
G5	PLLGND	Supply	PLL Ground
G6	CLKOUT5	Analogue Output	FLL / Oscillator Clock output
G7	MCLK / XTI	Digital Input	Master clock input / xtal input

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
DCVDD, AVDD, PLLVDD	-0.3V	+2.5V
MICVDD and DBVDD	-0.3V	+4.5V
SPKVDD1, SPKVDD2	-0.3V	+7.0V
CPVDD	-0.3V	+2.2V
Voltage range digital inputs	DGND -0.3V	DBVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Voltage range analogue outputs (HPOUTL, HPOUTR)	-CPVDD-0.3V	+CPVDD+0.3V
Temperature Range, T_A	-40°C	+85°C
Junction Temperature, T_{JMAX}	-40°C	+150°C
Storage temperature after soldering	-65°C	+150°C

Notes:

1. Analogue, digital and speaker grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other (i.e. not internally connected).
3. AVDD must be less than or equal to MICVDD.
4. AVDD must be less than or equal to SPKVDD1 and SPKVDD2.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital core supply range	DCVDD	1.62	1.8	2.0	V
Digital buffer supply range	DBVDD	1.62	1.8	3.6	V
Microphone bias supply range	MICVDD	1.7	2.5	3.6	V
Analogue supplies range	AVDD	1.7	1.8	2.0	V
PLL supply range	PLLVDD	1.7	1.8	2.0	V
Charge pump supply range (1.8V supply operation)	CPVDD	1.7	1.8	2.0	V
Speaker supply range	SPKVDD1, SPKVDD2	1.7	5.0	5.5	V
Ground	DGND, AGND, CPGND, SPKGND1, SPKGND2, PLLGND		0		V

Notes:

1. SPKVDD1 and SPKVDD2 must be high enough to support the peak output voltage when using CLASSD_VOL function, to avoid output waveform clipping. Peak output voltage is AVDD*CLASSD_VOL.
2. The AGND and PLLGND pins must be tied together as close as possible to the WM8962.
3. The WM8962 can operate with PLLVDD tied to 0V; device power consumption may be reduced, but the crystal oscillator, PLLs and CLKOUT functions will not be supported.

ELECTRICAL CHARACTERISTICS

Test Conditions

MICVDD = DCVDD = DBVDD = CPVDD = AVDD = PLLVDD = 1.8V, SPKVDD1 = SPKVDD2 = 5V.

T_A = +25ºC, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (IN1L, IN1R, IN4L, IN4R) to Input PGA						
Full-scale Input Signal Level – note this changes in proportion to AVDD	V_{INFS}	Single-ended PGA input		500 -6.02		mVrms dBV
Input resistance		+24dB PGA gain		3.6		kΩ
		0dB PGA gain		30.0		
		-23.25dB PGA gain		56.5		
Input capacitance	Cin			65		pF
Analogue Inputs (IN2L, IN2R, IN3L, IN3R) to Input PGA						
Full-scale Input Signal Level – note this changes in proportion to AVDD	V_{INFS}	Single-ended PGA input		500 -6.02		mVrms dBV
Input resistance		All gain settings		60		kΩ
Input Programmable Gain Amplifier (PGA)						
Minimum programmable gain				-23.25		dB
Maximum programmable gain				24		dB
Programmable Gain Step Size		Guaranteed monotonic		0.75		dB
PGA Noise (referred to input) (A-weighted)		IN1 and IN4		-113		dBV
PGA Noise (referred to input) (A-weighted)		IN2 and IN3		-113		dBV
Mute Attenuation				100		dB
Selectable Input Gain Boost (From Input PGA)						
Gain Boost Steps		Input from PGA		0, 6, 13, 18, 20, 24, 27, 29		dB
Mute Attenuation				95		dB
Selectable Input Gain to ADC Mixer (From IN2, IN3)						
Gain Boost Steps		Input from IN2 / IN3		-12,-9, -6, -3, 0, 3, 6		dB
Mute Attenuation				95		dB

Test Conditions

MICVDD = DCVDD = DBVDD = CPVDD = AVDD = PLLVDD = 1.8V, SPKVDD1 = SPKVDD2 = 5V.

T_A = +25ºC, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (IN1L, IN1R) to ADC out via Input PGA and Input Gain Boost						
Signal to Noise Ratio (A-weighted)	SNR	ADC_HP=0 MIXIN_BIAS=100 INPGA_BIAS=100 'Option 1' (low power) bias settings - see Note 2.		91		dB
Total Harmonic Distortion Plus Noise (-1dBFS input)	THD+N			-70		dB
Signal to Noise Ratio (A-weighted)	SNR	ADC_HP=0 MIXIN_BIAS=011 INPGA_BIAS=100 'Option 2' bias settings - see Note 2.		91		dB
Total Harmonic Distortion Plus Noise (-1dBFS input)	THD+N			-75		dB
Signal to Noise Ratio (A-weighted)	SNR	ADC_HP=0 MIXIN_BIAS=000 INPGA_BIAS=100 'Option 3' bias settings - see Note 2.	81	91		dB
Total Harmonic Distortion Plus Noise (-1dBFS input)	THD+N			-82	-72	dB
Signal to Noise Ratio (A-weighted)	SNR	ADC_HP=1 MIXIN_BIAS=000 INPGA_BIAS=000 'Option 4' (high performance) bias settings - see Note 2.		93		dB
Total Harmonic Distortion Plus Noise (-1dBFS input)	THD+N			-82		dB
ADC Channel Separation		1kHz		95		dB
		10kHz		97		
PSRR (AVDD)		100mV(peak-peak) 1kHz		60		dB
		100mV(peak-peak) 20kHz		40		
Channel Matching		1kHz signal		+/-0.5		dB

Test Conditions

MICVDD = DCVDD = DBVDD = CPVDD = AVDD = PLLVDD = 1.8V, SPKVDD1 = SPKVDD2 = 5V.

T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (IN2L, IN2R) to ADC out via Input Gain (Input PGA Bypassed)						
Signal to Noise Ratio (A-weighted)	SNR	ADC_HP=0 MIXIN_BIAS=100 INPGA_BIAS=100 'Option 1' (low power) bias settings - see Note 2.		91		dB
Total Harmonic Distortion Plus Noise (-1dBFS input)	THD+N			-70		dB
Signal to Noise Ratio (A-weighted)	SNR	ADC_HP=0 MIXIN_BIAS=011 INPGA_BIAS=100 'Option 2' bias settings - see Note 2.		91		dB
Total Harmonic Distortion Plus Noise (-1dBFS input)	THD+N			-75		dB
Signal to Noise Ratio (A-weighted)	SNR	ADC_HP=0 MIXIN_BIAS=000 INPGA_BIAS=100 'Option 3' bias settings - see Note 2.		91		dB
Total Harmonic Distortion Plus Noise (-1dBFS input)	THD+N			-85		dB
Signal to Noise Ratio (A-weighted)	SNR	ADC_HP=1 MIXIN_BIAS=000 INPGA_BIAS=000 'Option 4' (high performance) bias settings - see Note 2.		94		dB
Total Harmonic Distortion Plus Noise (-1dBFS input)	THD+N			-85		dB
ADC Channel Separation		1kHz		95		dB
		10kHz		87		
PSRR (AVDD)		100mV(peak-peak) 1kHz		60		dB
		100mV(peak-peak) 20kHz		40		
Analogue Inputs (IN4L, IN4R) to HPOUTL/R (used as Line output) with 10kΩ / 50pF load: Low Power headphone playback mode (Note 3)						
Input Resistance		+6dB PGA gain		10		kΩ
		0dB PGA gain		17		
		-15dB PGA gain		80		
Signal to Noise Ratio (A-weighted)	SNR			97		dB
Total Harmonic Distortion Plus Noise	THD+N	10kΩ, 50pF load		-80		dB

Test Conditions

MICVDD = DCVDD = DBVDD = CPVDD = AVDD = PLLVDD = 1.8V, SPKVDD1 = SPKVDD2 = 5V.

T_A = +25ºC, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Input Path Crosstalk						
IN1 / IN4 ADC input path crosstalk		1kHz		-98		dB
		10kHz		-79		
IN2 / IN3 ADC input path crosstalk		1kHz		-85		dB
		10kHz		-65		
IN2 / IN4 ADC input path crosstalk		1kHz		-90		dB
		10kHz		-69		
IN3 / IN4 ADC input path crosstalk		1kHz		-75		dB
		10kHz		-55		
The ADC path is enabled from one input pin; -6dBV test signal applied to the other input; crosstalk measured at ADC output. The test is repeated with the two input pins swapped; the crosstalk figure is the worst case of the two measurements.						

Test Conditions

MICVDD = DCVDD = DBVDD = CPVDD = AVDD = PLLVDD = 1.8V, SPKVDD1 = SPKVDD2 = 5V.

T_A = +25ºC, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
HPOUTL/R_VOL						
Minimum programmable gain				-68		dB
Maximum programmable gain				6		dB
Volume Gain Step Size		Guaranteed monotonic		1		dB
Mute Attenuation				94		dB
HP1L/R_VOL						
Minimum programmable gain				-7		dB
Maximum programmable gain				0		dB
Volume Gain Step Size		Guaranteed monotonic		1		dB
DAC to HPOUTL/R (used as Line output) with 10kΩ / 50pF load: Low Power headphone playback mode (Note 3)						
Full scale output voltage		HPOUTL/R_VOL = 0dB		0.96		Vrms
Signal to Noise Ratio (A-weighted)	SNR		87	97		dB
Total Harmonic Distortion Plus Noise	THD+N	10kΩ load		-84	-74	dB
Channel Separation		1kHz full scale signal		93		dB
		10kHz full scale signal		86		
PSRR (AVDD)		100mV(peak-peak) 1kHz		70		dB
		100mV(peak-peak) 20kHz		65		
DC offset		DC servo is enabled	0		+/-1.2	mV
DAC to HPOUTL/R (used as Line output) with 10kΩ / 50pF load: High Performance headphone playback mode (Note 3)						
Signal to Noise Ratio (A-weighted)	SNR		87	98		dB
Total Harmonic Distortion Plus Noise	THD+N	10kΩ load		-84	-74	dB

Test Conditions

MICVDD = DCVDD = DBVDD = CPVDD = AVDD = PLLVDD = 1.8V, SPKVDD1 = SPKVDD2 = 5V.

T_A = +25ºC, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to HPOUTL/R with headphone load: Low Power headphone playback mode (Note 3)						
Output Power at 1% THD+N	P_O	R_L=32Ω		26		mW
		R_L=16Ω		31		
Total Harmonic Distortion Plus Noise	THD+N	R_L=32Ω, P_O=2mW		-79 0.011		dB %
		R_L=32Ω, P_O=3.5mW		-79 0.011		
		R_L=32Ω, P_O=12mW		-78 0.013		
		R_L=16Ω, P_O=2mW		-81 0.0089		
		R_L=16Ω, P_O=22mW		-80 0.010		
Output Noise Level				-97	-87	dBV
DC offset		DC servo is enabled	0		+/-1.2	mV
Channel Separation		1kHz test signal, R_L =16Ω, P_O =22mW		95		dB
		10kHz test signal, R_L =16Ω, P_O =22mW		84		
DAC to HPOUTL/R with headphone load: High Performance playback mode (Note 3)						
Total Harmonic Distortion Plus Noise	THD+N	R_L =32Ω, P_O =12mW		-84 0.0063		dB %
		R_L =16Ω, P_O =22mW		-81 0.0089		
Output Noise Level				-98	-87	dBV

Test Conditions

MICVDD = DCVDD = DBVDD = CPVDD = AVDD = PLLVDD = 1.8V, SPKVDD1 = SPKVDD2 = 5V.

T_A = +25ºC, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SPKOUTL/R_VOL						
Minimum programmable gain				-68		dB
Maximum programmable gain				6		dB
Volume Gain Step Size		Guaranteed monotonic		1		dB
Mute Attenuation				92		dB
DAC to Stereo Speaker Outputs (DAC to SPKOUTLP, SPKOUTLN, SPKOUTRP, SPKOUTRN with 8Ω + 22µH bridge tied load)						
Output Power	P_O	1% THD+N, R_L = 8Ω, SPKVDD1=SPKVDD2=5.5V		1.26		W
		1% THD+N, R_L = 8Ω, SPKVDD1=SPKVDD2=1.7V		0.08		
Total Harmonic Distortion Plus Noise	THD+N	P_O =200mW, R_L = 8Ω, SPKVDD1=SPKVDD2=3.3V		-68 0.040		dB %
		P_O =320mW, R_L = 8Ω, SPKVDD1=SPKVDD2=3.3V		-72 0.025		
		P_O =320mW, R_L = 8Ω, SPKVDD1=SPKVDD2=5V		-67 0.045	-55	
		P_O =1W, R_L = 8Ω, SPKVDD1=SPKVDD2=5V, CLASSD_VOL=110 DACL/R_VOL=C1h		-61 0.089		
Signal to Noise Ratio (A-weighted) (DAC to speaker outputs)	SNR	SPKVDD1=SPKVDD2=3.3V, R_L = 8Ω, Output signal =2.0Vrms		90		dB
		SPKVDD1=SPKVDD2=5V, R_L = 8Ω, Output signal=2.8Vrms	83	93		
PSRR (SPKVDD1/SPKVDD2)	PSRR	100mV(peak-peak) 217Hz		78		dB
		100mV(peak-peak) 1kHz		78		

Test Conditions

MICVDD = DCVDD = DBVDD = CPVDD = AVDD = PLLVDD = 1.8V, SPKVDD1 = SPKVDD2 = 5V.

T_A = +25ºC, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Mono Speaker Output (DAC to SPKOUTLP/RP, SPKOUTLN/RN with 4Ω + 22µH bridge tied load)						
Output Power	P_O	1% THD+N, R_L = 4Ω, SPKVDD1=SPKVDD2=5.5V		2.45		W
		1% THD+N, R_L = 4Ω, SPKVDD1=SPKVDD2=1.7V		0.15		
Total Harmonic Distortion Plus Noise	THD+N	P_O =400mW, R_L = 4Ω, SPKVDD1=SPKVDD2=3.3V		-64 0.063		dB %
		P_O =640mW, R_L = 4Ω, SPKVDD1=SPKVDD2=3.3V,		-63 0.071		
		P_O =640mW, R_L = 4Ω, SPKVDD1=SPKVDD2=5V		-67 0.044		
		P_O =2W, R_L = 4Ω, SPKVDD1=SPKVDD2=5V, CLASSD_VOL=110 DACL/R_VOL=C1h		-61 0.089		
Signal to Noise Ratio (A-weighted) (DAC to speaker outputs)	SNR	SPKVDD1=SPKVDD2=3.3V, R_L = 4Ω, Output signal=2.0Vrms		90		dB
		SPKVDD1=SPKVDD2=5V, R_L = 4Ω, Output signal=2.8Vrms		93		

Test Conditions

MICVDD = DCVDD = DBVDD = CPVDD = AVDD = PLLVDD = 1.8V, SPKVDD1 = SPKVDD2 = 5V.

T_A = +25°C, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Reference Levels						
Mid-rail Reference Voltage	VMIDC		–3%	AVDD/2	+3%	V
Microphone Bias						
Bias Voltage (Note that MICVDD must be at least 300mV higher than $V_{MICBIAS}$)	$V_{MICBIAS}$	MICVDD=2.5V 2mA load current MICBIAS_LVL=1	-4%	1.156 × AVDD	+4%	V
		MICVDD=2.5V 2mA load current MICBIAS_LVL=0	-4%	0.828 × AVDD	+4%	
PSRR (MICVDD)	PSRR	100mV (peak-peak) 1kHz, MICBIAS_LVL=1		74		dB
PSRR (AVDD)	PSRR	100mV (peak-peak) 1kHz, MICBIAS_LVL=1		52		dB
Maximum Bias Current Source	$I_{MICBIAS}$			2		mA
Output Noise spectral density @1kHz	Vst	MICBIAS_LVL=1		85		nV/√Hz
MICBIAS Current Detect Function (see Note 1)						
Current Detect Threshold		MICDET_THR = 000	38	64	90	µA
		MICDET_THR = 001	-25%	166	+25%	
		MICDET_THR = 010	-20%	375	+20%	
		MICDET_THR = 011	-20%	475	+20%	
		MICDET_THR = 100	-20%	575	+20%	
		MICDET_THR = 101	-20%	680	+20%	
		MICDET_THR = 110	-20%	885	+20%	
		MICDET_THR = 111	-20%	990	+20%	
Delay Time for Current Detect Interrupt	t_{DET}			1.6		ms
MICBIAS Short Circuit (Hook Switch) Detect Function (see Note 1)						
Short Circuit Detect Threshold		MICSHORT_THR = 00	-18%	515	+18%	µA
		MICSHORT_THR = 01	-15%	680	+15%	
		MICSHORT_THR = 10	-15%	1050	+15%	
		MICSHORT_THR = 11	-15%	1215	+15%	
Delay Time for Short Circuit Detect Interrupt	t_{SHORT}			47		ms
Charge Pump						
Maximum Charge Pump switching frequency	CP_{FREQ}			1		MHz
Flyback capacitor (between CPCA and CPCB pins)	C_{FB}	at 2V	1			µF
VPOS capacitor		at 2V	2			µF
VNEG capacitor		at 2V	2			µF
Charge pump start-up time				190		µs

Test Conditions

MICVDD = DCVDD = DBVDD = CPVDD = AVDD = PLLVDD = 1.8V, SPKVDD1 = SPKVDD2 = 5V.

T_A = +25ºC, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Crystal Oscillator						
External crystal frequency				24		MHz
Oscillator load capacitance		XTI and XTO Pins		10.5		pF
Start-up time		measured from time when: PLLVDD ≥ 1.7V, AVDD ≥ 1.7V and DVDD ≥ 1.62V, until crystal output is stable and in specification.		1.5		ms
Phase Locked Loops (PLLs)						
Output frequency	F_{OUT}		22.5		50	MHz
Output duty cycle			40	50	60	%
Start-up time (including Crystal Oscillator start-up time)		measured from time when: PLLVDD ≥ 1.7V, AVDD ≥ 1.7V and DVDD ≥ 1.62V, until PLL outputs are stable and in specification.		1.5		ms
Frequency synthesis error				0		ppm
Absolute clock period jitter (peak)		Input Clock = 24MHz, 5pF load		500		ps
Short term jitter (peak, cycle to cycle)		N=1, 1000 samples, Input Clock = 24MHz, 5pF load. (see Note 4)		150		ps
Long term jitter (peak)		N=1000, 1000 samples, Input Clock = 24MHz, 5pF load. (see Note 4)		500		ps
MCLK / XTI input frequency range			14		40	MHz
Frequency Locked Loop (FLL)						
Input frequency	F_{REF}	FLL_REFCLK_DIV = 00	0.032		13.5	MHz
		FLL_REFCLK_DIV = 01	0.064		27	
		FLL_REFCLK_DIV = 10	0.128		36.864	
Output frequency	F_{OUT}		1.875		50	MHz
Start-Up time		VMID enabled; measured from FLL_ENA=1 to clock signal present on CLKOUTn.		220		µs
Frequency synthesis error				0		ppm
Start-Up time (free-running mode)		VMID enabled; measured from FLL_ENA=1 to clock signal present on CLKOUTn.		0.75		µs
Frequency accuracy (free-running mode)		Reference clock supplied initially		+/-10		%
		No reference clock provided		+/-30		%
Digital Input / Output						
Input HIGH Level	V_{IH}		0.7×DBVDD			V
Input LOW Level	V_{IL}				0.3×DBVDD	V
Output HIGH Level	V_{OH}	I_{OH}=1mA	0.9×DBVDD			V
Output LOW Level	V_{OL}	I_{OL}=-1mA			0.1×DBVDD	V
Input capacitance				15		pF
Input leakage			-0.9		0.9	µA
CLKOUTn output impedance				160		Ω

Test Conditions

MICVDD = DCVDD = DBVDD = CPVDD = AVDD = PLLVDD = 1.8V, SPKVDD1 = SPKVDD2 = 5V.

T_A = +25ºC, 1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Consumption						
AVDD	I_{AVDD}	OFF: power applied, all clocks stopped, thermal shut-down enabled		40	75	µA
DCVDD	I_{DCVDD}			3	25	µA
DBVDD	I_{DBVDD}			0	10	µA
CPVDD	I_{CPVDD}			0.5	10	µA
SPKVDD1	$I_{SPKVDD1}$			1	5	µA
SPKVDD2	$I_{SPKVDD2}$			1	5	µA
MICVDD	I_{MICVDD}			0.2	5	µA
PLLVDD	$I_{PLLVDD1}$			7	30	µA
MICVDD	I_{MICVDD}	SPKVDD1=SPKVDD2=5V, MICVDD=2.5V, All other supplies disconnected		0.2	5	µA
SPKVDD1	$I_{SPKVDD1}$			0.2	5	µA
SPKVDD2	$I_{SPKVDD2}$			0.2	5	µA
MICVDD	I_{MICVDD}	SPKVDD1=SPKVDD2=5V, MICVDD=2.5V, All other supplies 0V		0.2	5	µA
SPKVDD1	$I_{SPKVDD1}$			0.2	5	µA
SPKVDD2	$I_{SPKVDD2}$			0.2	5	µA

Note:

1. If AVDD ≠ 1.8, current threshold values should be multiplied by (AVDD/1.8)
2. Four different bias configurations are supported for ADC input paths; these are defined in the “Reference Voltages and Bias Control” section.
3. Two different bias configurations are supported for the DAC / Headphone output paths; these are defined in the “Reference Voltages and Bias Control” section.
4. N = number of clock periods in one sample.

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum full scale output signal and the output with no input signal applied.
2. Total Harmonic Distortion (dB) – THD is the level of the rms value of the sum of harmonic distortion products relative to the amplitude of the measured output signal.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the level of the rms value of the sum of harmonic distortion products plus noise in the specified bandwidth relative to the amplitude of the measured output signal.
4. Channel Separation (L/R) (dB) – left-to-right and right-to-left channel separation is the measured signal level in the idle channel at the test signal frequency relative to the signal level at the output of the active channel. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
5. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.
6. All performance measurements carried out with 20kHz low pass filter, and where noted an A-weighted filter. Failure to use such a filter will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.

TYPICAL PERFORMANCE

TYPICAL POWER CONSUMPTION

Analogue Input (IN1L, IN1R) to ADC out via Input PGA and Input Gain boost
Quiescent input, default register conditions unless otherwise stated.
MCLK = 12.288MHz, fs = 48kHz, MCLK rate = 256fs, 24-bit I2S, Slave mode,
INL_ENA = 1, INR_ENA = 1,
INPGAL_MUTE = 0, INPGAR_MUTE = 0,
ADCL_ENA = 1, ADCR_ENA = 1
VMID_SEL = 01, BIAS_ENA = 1
See "Reference Voltages and Bias Control" for details of the bias configuration registers.

	DCVDD 1.8V	DBVDD 1.8V	MICVDD 2.5V	AVDD 1.8V	PLLVDD 1.8V	CPVDD 1.8V	SPKVDD 5.0V	TOTAL
Quiescent input, Option 1 bias settings	2.4mA	0.0mA	0.0mA	2.5mA	0.0mA	0.0mA	0.0mA	8.8mW
Quiescent input, Option 2 bias settings	2.4mA	0.0mA	0.0mA	2.7mA	0.0mA	0.0mA	0.0mA	9.2mW
Quiescent input, Option 3 bias settings (default)	2.4mA	0.0mA	0.0mA	3.3mA	0.0mA	0.0mA	0.0mA	10.3mW
Quiescent input, Option 4 bias settings	2.6mA	0.0mA	0.0mA	5.4mA	0.0mA	0.0mA	0.0mA	14.4mW
-1dBFS ADC output	2.4mA	0.0mA	0.0mA	3.3mA	0.0mA	0.0mA	0.0mA	10.4mW
MICBIAS enabled	2.4mA	0.0mA	0.4mA	3.3mA	0.0mA	0.0mA	0.0mA	11.3mW
Quiescent input, fs = 8kHz, MCLK = 2.048MHz	0.3mA	0.0mA	0.0mA	3.0mA	0.0mA	0.0mA	0.0mA	6.0mW
Quiescent input, fs = 96kHz, MCLK = 24.576MHz	4.1mA	0.0mA	0.0mA	3.3mA	0.0mA	0.0mA	0.0mA	13.3mW
Quiescent input, fs = 48kHz, MCLK = 24.576MHz, MCLK = 512fs, DSP Sound Enhancement enabled	14.5mA	0.2mA	0.0mA	3.2mA	0.0mA	0.0mA	0.0mA	32.4mW

Analogue Input (IN2L, IN2R) to ADC out via Input PGA and Input Gain boost
Quiescent input, default register conditions unless otherwise stated.
MCLK = 12.288MHz, fs = 48kHz, MCLK rate = 256fs, 24-bit I2S, Slave mode,
MIXINL_ENA = 1, MIXINR_ENA = 1, IN2L_TO_MIXINL = 1, IN2R_TO_MIXINR = 1,
ADCL_ENA = 1, ADCR_ENA = 1,
VMID_SEL = 01, BIAS_ENA = 1.
See "Reference Voltages and Bias Control" for details of the bias configuration registers.

	DCVDD 1.8V	DBVDD 1.8V	MICVDD 2.5V	AVDD 1.8V	PLLVDD 1.8V	CPVDD 1.8V	SPKVDD 5.0V	TOTAL
Quiescent input, Option 1 bias settings	2.4mA	0.0mA	0.0mA	2.2mA	0.0mA	0.0mA	0.0mA	8.3mW
Quiescent input, Option 2 bias settings	2.4mA	0.0mA	0.0mA	2.4mA	0.0mA	0.0mA	0.0mA	8.7mW
Quiescent input, Option 3 bias settings (default)	2.4mA	0.0mA	0.0mA	3.0mA	0.0mA	0.0mA	0.0mA	9.8mW
Quiescent input, Option 4 bias settings	2.6mA	0.0mA	0.0mA	4.5mA	0.0mA	0.0mA	0.0mA	12.9mW
-1dBFS ADC output	2.4mA	0.0mA	0.0mA	3.0mA	0.0mA	0.0mA	0.0mA	9.9mW
MICBIAS enabled	2.4mA	0.0mA	0.4mA	3.0mA	0.0mA	0.0mA	0.0mA	10.7mW
Quiescent input, fs = 8kHz, MCLK = 2.048MHz	0.3mA	0.0mA	0.0mA	2.7mA	0.0mA	0.0mA	0.0mA	5.4mW
Quiescent input, fs = 96kHz, MCLK = 24.576MHz	4.1mA	0.0mA	0.0mA	3.0mA	0.0mA	0.0mA	0.0mA	12.8mW
Quiescent input, fs = 48kHz, MCLK = 24.576MHz, MCLK = 512fs, DSP Sound Enhancement enabled	14.5mA	0.2mA	0.0mA	3.0mA	0.0mA	0.0mA	0.0mA	32.0mW

Stereo DAC Playback to Headphone (HPOUTL, HPOUTR) - Low Power headphone playback mode, 16Ω load.
Default register conditions unless otherwise stated.
Default DAC to Headphone Power Up sequence completed.
CP_DYN_PWR = 1
MCLK = 12.288MHz, fs = 48kHz, MCLK rate = 256fs, 24-bit I2S, Slave mode,
Input signal level = 0dBFS, HP1x_VOL = 111b (0dB),
Note that Low Power headphone playback mode is selected by default.

	DCVDD 1.8V	DBVDD 1.8V	MICVDD 2.5V	AVDD 1.8V	PLLVDD 1.8V	CPVDD 1.8V	SPKVDD 5.0V	TOTAL
Quiescent output	2.0mA	0.0mA	0.0mA	1.7mA	0.0mA	0.5mA	0.0mA	7.7mW
0.1mW/channel output HPOUTx_VOL = 5Dh (-28dB)	1.9mA	0.0mA	0.0mA	1.7mA	0.0mA	2.7mA	0.0mA	11.4mW
2mW/channel output HPOUTx_VOL = 69h (-15dB)	2.0mA	0.0mA	0.0mA	1.7mA	0.0mA	10.1mA	0.0mA	25.0mW
16mW/channel output HPOUTx_VOL = 73h (-6dB)	2.0mA	0.0mA	0.0mA	1.7mA	0.0mA	53.7mA	0.0mA	103.4mW
Quiescent output, fs = 48kHz, MCLK = 24.576MHz, MCLK = 512fs, DSP Sound Enhancement enabled CP_DYN_PWR = 0	14.3mA	0.0mA	0.0mA	1.8mA	0.0mA	1.8mA	0.0mA	32.2mW

Stereo DAC Playback to Headphone (HPOUTL, HPOUTR) - High Performance headphone playback mode, 16Ω load.
Default register conditions unless otherwise stated.
Default DAC to Headphone Power Up sequence completed.
DAC_HP = 1, HP_PGAS_BIAS = 000, HP_BIAS_BOOST = 000. (These must be set after running the DAC power-up sequence.)
CP_DYN_PWR = 1
MCLK = 12.288MHz, fs = 48kHz, MCLK rate = 256fs, 24-bit I2S, Slave mode,
Input signal level = 0dBFS, HP1x_VOL = 000b (-7dB),
See "Reference Voltages and Bias Control" for details of the High Performance headphone playback mode.

	DCVDD 1.8V	DBVDD 1.8V	MICVDD 2.5V	AVDD 1.8V	PLLVDD 1.8V	CPVDD 1.8V	SPKVDD 5.0V	TOTAL
Quiescent output	2.0mA	0.0mA	0.0mA	2.5mA	0.0mA	0.5mA	0.0mA	8.9mW
0.1mW/channel output HPOUTx_VOL = 65h (-20dB)	2.1mA	0.0mA	0.0mA	2.5mA	0.0mA	2.9mA	0.0mA	13.3mW
2mW/channel output HPOUTx_VOL = 72h (-7dB)	2.1mA	0.0mA	0.0mA	2.5mA	0.0mA	22.5mA	0.0mA	48.7mW
16mW/channel output HPOUTx_VOL = 79h (-0dB) HP1x_VOL = 2h (-5dB)	2.1mA	0.0mA	0.0mA	2.5mA	0.0mA	59.6mA	0.0mA	115.6mW
Quiescent output, fs = 48kHz, MCLK = 24.576MHz, MCLK = 512fs, DSP Sound Enhancement enabled CP_DYN_PWR = 0	14.4mA	0.0mA	0.0mA	2.5mA	0.0mA	1.8mA	0.0mA	33.8mW

Stereo DAC Playback to Speaker (SPKOUTLP, SPKOUTLN, SPKOUTRP, SPKOUTRN) - 8.2Ω, 2.2µH load.
Default register conditions unless otherwise stated.
Default DAC to Headphone Power Up sequence completed.
DAC_MUTE = 0, DACL_ENA = 1, DACR_ENA = 1,
SPKOUTL_ENA = 1, SPKOUTL_PGA_ENA = 1, SPKOUTL_PGA_MUTE = 1,
SPKOUTR_ENA = 1, SPKOUTR_PGA_ENA = 1, SPKOUTR_PGA_MUTE = 1,
CLASSD_VOL = 111 (+12dB),
VMID_SEL = 01, BIAS_ENA = 1,
MCLK = 12.288MHz, fs = 48kHz, MCLK rate = 256fs, 24-bit I2S, Slave mode,

	DCVDD 1.8V	DBVDD 1.8V	MICVDD 2.5V	AVDD 1.8V	PLLVDD 1.8V	CPVDD 1.8V	SPKVDD 5.0V	TOTAL
Quiescent output	2.4mA	0.0mA	0.0mA	2.7mA	0.0mA	0.0mA	7.3mA	45.7mW
200mW/channel output	2.4mA	0.0mA	0.0mA	2.7mA	0.0mA	0.0mA	91.8mA	468.2mW
1W/channel output	2.3mA	0.0mA	0.0mA	2.6mA	0.0mA	0.0mA	532.7mA	2672.3mW
Quiescent output, fs = 48kHz, MCLK = 24.576MHz, MCLK = 512fs, DSP Sound Enhancement enabled	14.3mA	0.0mA	0.0mA	2.9mA	0.0mA	0.0mA	7.1mA	66.6mW

Clocking Configurations Default register conditions unless otherwise stated.								
	DCVDD 1.8V	**DBVDD 1.8V**	**MICVDD 2.5V**	**AVDD 1.8V**	**PLLVDD 1.8V**	**CPVDD 1.8V**	**SPKVDD 5.0V**	**TOTAL**
PLL3 enabled, 24MHz crystal oscillator reference, PLL3 output = 24.576MHz, MCLK = 12.288MHz.	0.680mA	0.160mA	0.0mA	0.056mA	2.278mA	0.0mA	0.001mA	5.718mW
FLL enabled, 24MHz crystal oscillator reference, FLL output = 12.288MHz, MCLK = 12.288MHz.	1.756mA	0.086mA	0.0mA	0.451mA	1.691mA	0.0mA	0.001mA	7.175mW

Notes:

1. SPKVDD = SPKVDD1 = SPKVDD2.
2. $I_{SPKVDD} = I_{SPKVDD1} + I_{SPKVDD2}$.
3. Speaker load inductance will affect the power consumption; reduced inductance will increase power consumption.

SIGNAL TIMING REQUIREMENTS

MASTER CLOCK

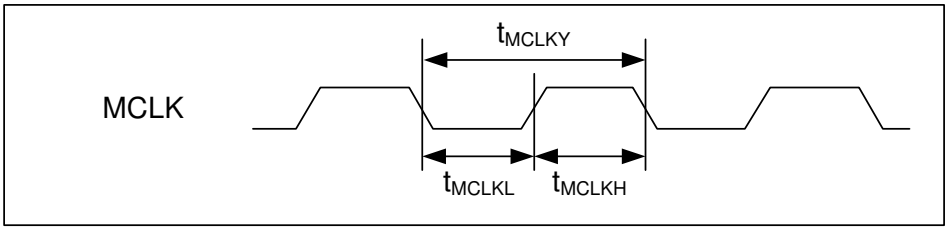


Figure 1 Master Clock Timing

Test Conditions
MICVDD=2.5V, DCVDD = CPVDD=AVDD =1.8V SPKVDD1 = SPKVDD2 = 5V,
DGND=AGND=CPGND=SPKGND1=SPKGND2=0V, T_A = +25ºC

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Master Clock Timing						
MCLK cycle time	T_{MCLKY}		20.345			ns
MCLK duty cycle	T_{MCLKH} : T_{MCLKL}		60:40		40:60	