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WM8976

Stereo CODEC with Speaker Driver

DESCRIPTION

The WM8976 is a low power, high quality CODEC designed for portable applications such as multimedia phone, digital still camera or digital camcorder.

The device integrates a preamp for differential microphone, and includes drivers for speakers, headphone and differential or stereo line output. External component requirements are reduced as no separate microphone or headphone amplifiers are required.

Advanced on-chip digital signal processing includes a 5-band equaliser, a mixed signal Automatic Level Control for the microphone or line input through the ADC as well as a purely digital limiter function for record or playback. Additional digital filtering options are available in the ADC path, to cater for application filtering such as 'wind noise reduction'.

The WM8976 digital audio interface can operate as a master or a slave. An internal PLL can generate all required audio clocks for the CODEC from common reference clock frequencies, such as 12MHz and 13MHz.

The WM8976 operates at analogue supply voltages from 2.5V to 3.3V, although the digital core can operate at voltages down to 1.71V to save power. The speaker outputs and OUT3/4 line outputs can run from a 5V supply if increased output power is required. Individual sections of the chip can also be powered down under software control.

FEATURES

Stereo CODEC:

- DAC SNR 98dB, THD -84dB ('A' weighted @ 48kHz)
- ADC SNR 95dB, THD -84dB ('A' weighted @ 48kHz)
- On-chip Headphone Driver with 'capless' option
  - 40mW per channel into 16Ω / 3.3V SPKVDD
- 1W output power into 8Ω BTL speaker / 5V SPKVDD
  - Capable of driving piezo speakers
  - Stereo speaker drive configuration

Mic Preamps:

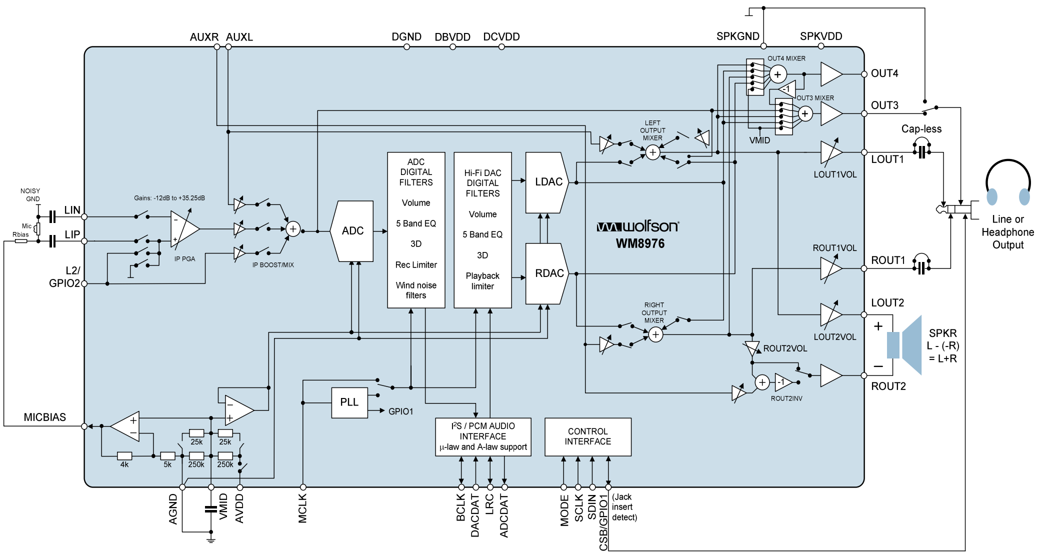
- Differential or single-ended microphone interfaces
  - Programmable preamp gain
  - Pseudo differential input with common mode rejection
  - Programmable ALC / Noise Gate in ADC path
- Low-noise bias supplied for electret microphone

Other Features:

- Enhanced 3-D function for improved stereo separation
- Digital playback limiter
- 5-band Equaliser (record or playback)
- Programmable ADC High Pass Filter (wind noise reduction)
- Programmable ADC Notch Filter
- Aux inputs for stereo analogue input signals or 'beep'
- On-chip PLL supporting 12, 13, 19.2MHz and other clocks
- Support for 8, 11.025, 12, 16, 22.05, 24, 32, 44.1 and 48kHz sample rates
- Low power, low voltage
  - 2.5V to 3.6V (digital: 1.71V to 3.6V)
- 5x5mm 32-lead QFN package

APPLICATIONS

- Stereo Camcorder or DSC
- Multimedia Phone



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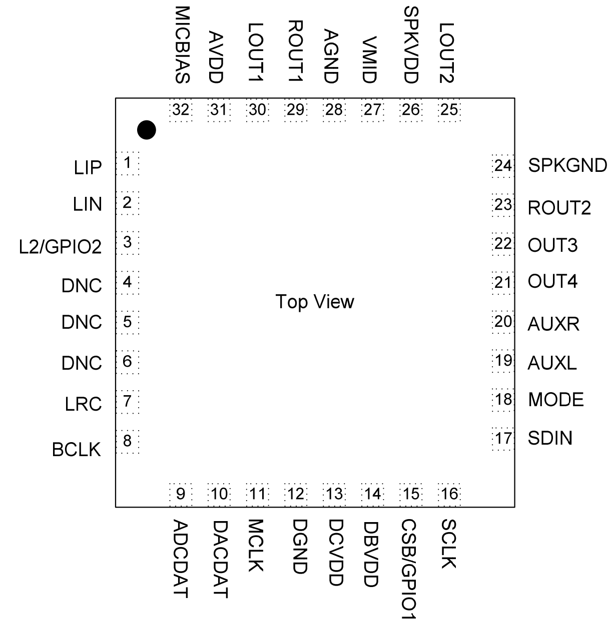
PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8976CGEFL/V	-25°C to +85°C	32-lead QFN (5 x 5 mm) (Pb-free)	MSL3	260°C
WM8976CGEFL/RV	-25°C to +85°C	32-lead QFN (5 x 5 mm) (Pb-free, tape and reel)	MSL3	260°C

Note:

Reel quantity = 3,500

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	LIP	Analogue input	Mic Pre-amp positive input
2	LIN	Analogue input	Mic Pre-amp negative input
3	L2/GPIO2	Analogue input	Line input/secondary mic pre-amp positive input/GPIO2 pin
4	DNC	Do not connect	Leave this pin floating
5	DNC	Do not connect	Leave this pin floating
6	DNC	Do not connect	Leave this pin floating
7	LRC	Digital Input / Output	DAC and ADC Sample Rate Clock
8	BCLK	Digital Input / Output	Digital Audio Port Clock
9	ADCDAT	Digital Output	ADC Digital Audio Data Output
10	DACDAT	Digital Input	DAC Digital Audio Data Input
11	MCLK	Digital Input	Master Clock Input
12	DGND	Supply	Digital ground
13	DCVDD	Supply	Digital core logic supply
14	DBVDD	Supply	Digital buffer (I/O) supply
15	CSB/GPIO1	Digital Input / Output	3-Wire Control Interface Chip Select / GPIO1 pin
16	SCLK	Digital Input	3-Wire Control Interface Clock Input / 2-Wire Control Interface Clock Input
17	SDIN	Digital Input / Output	3-Wire Control Interface Data Input / 2-Wire Control Interface Data Input
18	MODE	Digital Input	Control Interface Selection
19	AUXL	Analogue input	Left Auxiliary input
20	AUXR	Analogue input	Right Auxiliary input
21	OUT4	Analogue Output	Buffered midrail Headphone pseudo-ground, or Right line output or MONO mix output
22	OUT3	Analogue Output	Buffered midrail Headphone pseudo-ground, or Left line output
23	ROUT2	Analogue Output	Second right output, or BTL speaker driver positive output
24	SPKGND	Supply	Speaker ground (feeds speaker amp and OUT3/OUT4)
25	LOUT2	Analogue Output	Second left output, or BTL speaker driver negative output
26	SPKVDD	Supply	Speaker supply (feed speaker amp only)
27	VMID	Reference	Decoupling for ADC and DAC reference voltage
28	AGND	Supply	Analogue ground (feeds ADC and DAC)
29	ROUT1	Analogue Output	Headphone or Line Output Right
30	LOUT1	Analogue Output	Headphone or Line Output Left
31	AVDD	Supply	Analogue supply (feeds ADC and DAC)
32	MICBIAS	Analogue Output	Microphone Bias

Note:
It is recommended that the QFN ground paddle should be connected to analogue ground on the application PCB. Refer to the application note WAN_0118 on “Guidelines on How to Use QFN Packages and Create Associated PCB Footprints”

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
DBVDD, DCVDD, AVDD supply voltages	-0.3V	+4.5V
SPKVDD supply voltage	-0.3V	+7V
Voltage range digital inputs	DGND -0.3V	DVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Operating temperature range, T_A	-25°C	+85°C
Storage temperature after soldering	-65°C	+150°C

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other, i.e. not internally connected.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD		1.71[1]		3.6	V
Digital supply range (Buffer)	DBVDD		1.71[2]		3.6	V
Analogue core supply range	AVDD		2.5		3.6	V
Analogue output supply range	SPKVDD		2.5		5.5	V
Ground	DGND, AGND, SPKGND			0		V

Notes:

1. When using the PLL, DCVDD must not be less than 1.9V.
2. DBVDD must be greater than or equal to DCVDD.
3. Analogue supplies have to be ≥ to digital supplies.
4. In non-boosted mode, SPKVDD should = AVDD, if boosted SPKVDD should be ≥ 1.5x AVDD.

ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD=1.8V, AVDD=DBVDD=SPKVDD= 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Preamp Inputs (LIP, LIN)						
Full-scale Input Signal Level – note this changes in proportion to AVDD (Note 1)	V_{INFS}	PGABOOST = 0dB INPPGAVOL = 0dB		1.0 0		Vrms dBV
Mic PGA equivalent input noise	At 35.25dB gain	0 to 20kHz		150		uV
Input resistance	R_{MICIN}	Gain set to 35.25dB		1.6		kΩ
	R_{MICIN}	Gain set to 0dB		47		kΩ
	R_{MICIN}	Gain set to -12dB		75		kΩ
	R_{MICIP}	LIP2INPPGA = 1		94		kΩ
	C_{MICIN}			10		pF
MIC Programmable Gain Amplifier (PGA)						
Maximum Programmable Gain				35.25		dB
Minimum Programmable Gain				-12		dB
Programmable Gain Step Size		Guaranteed monotonic		0.75		dB
Mute Attenuation				120		dB
Selectable Input Gain Boost (0/+20dB)						
Gain Boost on PGA input		Boost disabled		0		dB
		Boost enabled		20		dB
Maximum Gain from AUXL or L2 input to boost/mixer				+6		dB
Minimum Gain from AUXL or L2 input to boost/mixer				-12		dB
Gain step size to boost/mixer		Guaranteed monotonic		3		dB
Auxiliary Analogue Inputs (AUXL, AUXR)						
Full-scale Input Signal Level (0dB) – note this changes in proportion to AVDD	V_{INFS}			AVDD/3.3 0		Vrms dBV
Input Capacitance	C_{MICIN}			10		pF
Automatic Level Control (ALC)						
Target Record Level			-22.5		-1.5	dB
Programmable gain			-12		35.25	dB
Gain Hold Time (Note 3,5)	t_{HOLD}	MCLK = 12.288MHz (Note 3)	0, 2.67, 5.33, 10.67, … , 43691 (time doubles with each step)			ms
Gain Ramp-Up (Decay) Time (Note 4,5)	t_{DCY}	ALCMODE=0 (ALC), MCLK=12.288MHz (Note 3)	3.3, 6.6, 13.1, … , 3360 (time doubles with each step)			ms
		ALCMODE=1 (limiter), MCLK=12.288MHz (Note 3)	0.73, 1.45, 2.91, … , 744 (time doubles with each step)			
Gain Ramp-Down (Attack) Time (Note 4,5)	t_{ATK}	ALCMODE=0 (ALC), MCLK=12.288MHz (Note 3)	0.83, 1.66, 3.33, … , 852 (time doubles with each step)			ms
		ALCMODE=1 (limiter), MCLK=12.288MHz (Note 3)	0.18, 0.36, 0.73, … , 186 (time doubles with each step)			
Mute Attenuation				120		dB

Test Conditions

DCVDD=1.8V, AVDD=DBVDD=SPKVDD= 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue to Digital Converter (ADC)						
Signal to Noise Ratio (Note 6)	SNR	A-weighted, 0dB gain	85	95		dB
Total Harmonic Distortion (Note 7)	THD	-3dBFS input		-84	-74	dB
Digital to Analogue Converter (DAC) to Line-Out (LOUT1, ROUT1 with 10kΩ / 50pF load)						
Full-scale output		PGA gains set to 0dB, OUT34BOOST=0		AVDD/3.3		Vrms
		PGA gains set to 0dB, OUT34BOOST=1		1.5x (AVDD/3.3)		
Signal to Noise Ratio (Note 6)	SNR	A-weighted	90	98		dB
Total Harmonic Distortion (Note 7)	THD	R_L = 10kΩ full-scale signal		-84	-76	dB
Channel Separation (Note 9)		1kHz signal		110		dB
Output Mixers (LMX1, RMX1)						
Maximum PGA gain into mixer				+6		dB
Minimum PGA gain into mixer				-15		dB
PGA gain step into mixer		Guaranteed monotonic		3		dB
Analogue Outputs (LOUT1, ROUT1, LOUT2, ROUT2)						
Maximum Programmable Gain				+6		dB
Minimum Programmable Gain				-57		dB
Programmable Gain step size		Guaranteed monotonic		1		dB
Mute attenuation		1kHz, full scale signal		85		dB
Headphone Output (LOUT1, ROUT1 with 32Ω load)						
0dB full scale output voltage				AVDD/3.3		Vrms
Signal to Noise Ratio	SNR	A-weighted		102		dB
Total Harmonic Distortion	THD	R_L = 16Ω, Po=20mW AVDD=3.3V		0.003 -92		% dB
		R_L = 32 Ω, Po=20mW AVDD=3.3V		0.008 - 82		% dB
Speaker Output (LOUT2, ROUT2 with 8Ω bridge tied load, INVROUT2=1)						
Full scale output voltage, 0dB gain. (Note 9)		SPKBOOST=0		SPKVDD/3.3		Vrms
		SPKBOOST=1		(SPKVDD/3.3)*1.5		
Output Power	P_O	Output power is very closely correlated with THD; see below				
Total Harmonic Distortion	THD	P_O =200mW, R_L = 8Ω, SPKVDD=3.3V		0.04 -68		% dB
		P_O =320mW, R_L = 8Ω, SPKVDD=3.3V		1.0 -40		% dB
		P_O =500mW, R_L = 8Ω, SPKVDD=5V		0.02 -74		% dB
		P_O =860mW, R_L = 8Ω, SPKVDD=5V		1.0 -40		% dB
Signal to Noise Ratio	SNR	SPKVDD=3.3V, R_L = 8Ω		90		dB
		SPKVDD=5V, R_L = 8Ω		90		dB
Power Supply Rejection Ratio (50Hz-22kHz)	PSRR	R_L = 8Ω BTL		80		dB
		R_L = 8Ω BTL SPKVDD=5V (boost)		69		dB

Test Conditions

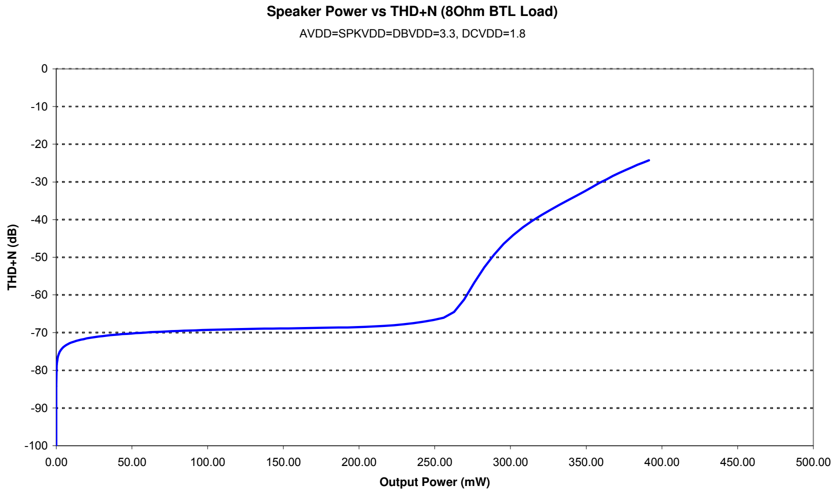
DCVDD=1.8V, AVDD=DBVDD=SPKVDD= 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

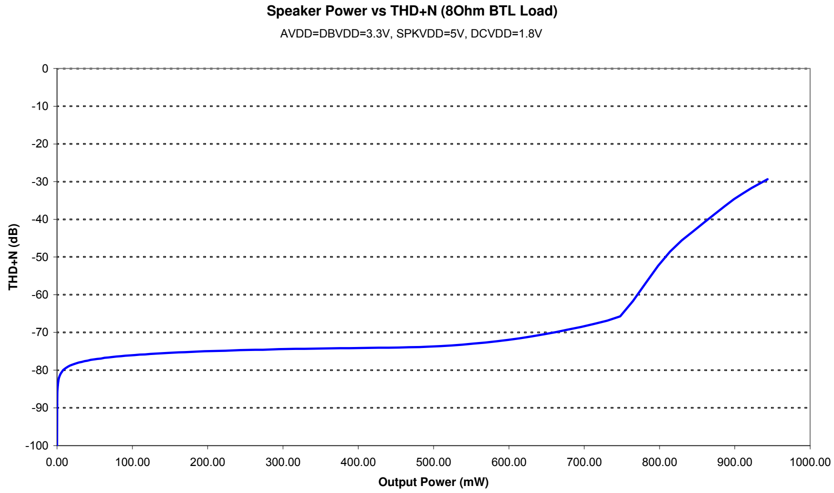
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUT3/OUT4 outputs (with 10kΩ / 50pF load)						
Full-scale output voltage, 0dB gain (Note 9)		OUT3BOOST=0/ OUT4BOOST=0		SPKVDD/3.3		Vrms
		OUT3BOOST=1 OUT4BOOST=1		(SPKVDD/3.3)*1.5		Vrms
Signal to Noise Ratio (Note 6)	SNR	A-weighted		98		dB
Total Harmonic Distortion (Note 7)	THD	R_L = 10 kΩ full-scale signal		-84		dB
Channel Separation (Note 8)		1kHz signal		100		dB
Power Supply Rejection Ratio (50Hz-22kHz)	PSRR	R_L = 10kΩ		52		dB
		R_L = 10kΩ SPKVDD=5V (boost)		56		dB
Microphone Bias						
Bias Voltage	$V_{MICBIAS}$	MBVSEL=0		0.9*AVDD		V
		MBVSEL=1		0.65*AVDD		V
Bias Current Source	$I_{MICBIAS}$				3	mA
Output Noise Voltage	Vn	1K to 20kHz		15		nV/√Hz
Digital Input / Output						
Input HIGH Level	V_{IH}		0.7×DBVDD			V
Input LOW Level	V_{IL}				0.3×DBVDD	V
Output HIGH Level	V_{OH}	I_{OL}=1mA	0.9×DBVDD			V
Output LOW Level	V_{OL}	I_{OH}-1mA			0.1xDBVDD	V
Input capacitance				10		pF
Input leakage				50		pA

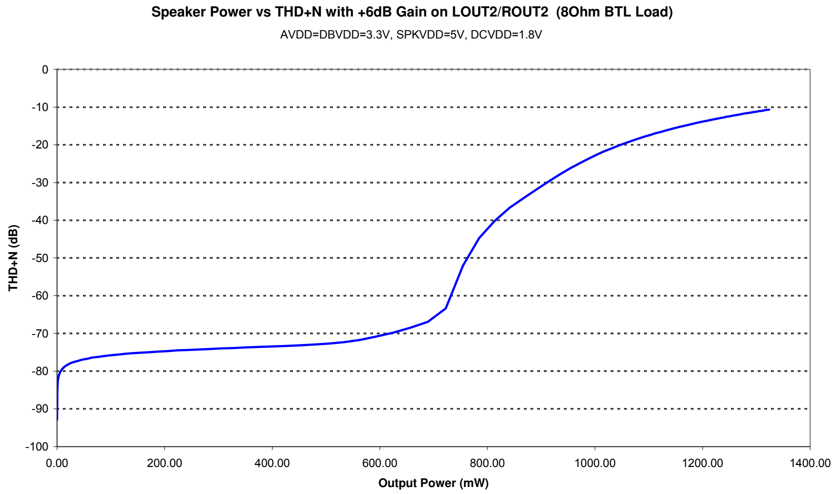
TERMINOLOGY

1. Input level to LIP is limited to a maximum of -3dB or THD+N performance will be reduced.
2. Note when BEEP path is not enabled then AUXL and AUXR have the same input impedances.
3. Hold Time is the length of time between a signal detected being too quiet and beginning to ramp up the gain. It does not apply to ramping down the gain when the signal is too loud, which happens without a delay.
4. Ramp-up and Ramp-Down times are defined as the time it takes for the PGA to sweep across 90% of its gain range.
5. All hold, ramp-up and ramp-down times scale proportionally with MCLK
6. Signal-to-noise ratio (dB) – SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
7. THD+N (dB) – THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
8. Channel Separation (dB) – Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Measured by applying a full scale signal to one channel input and measuring the level of signal apparent at the other channel output.
9. The maximum output voltage can be limited by the speaker power supply. If OUT3BOOST, OUT4BOOST or SPKBOOST is set then SPKVDD should be 1.5xAVDD to prevent clipping taking place in the output stage (when PGA gains are set to 0dB).

SPEAKER OUTPUT THD VERSUS POWER







POWER CONSUMPTION

Typical current consumption for various scenarios is shown below.

MODE	AVDD (3.0V) (mA)	DCVDD (1.8V) (mA)	DBVDD[1] (3.0V) (mA)	TOTAL POWER (mW)
Off	0.04[3]	0.0008	<0.0001	0.12
Sleep (VREF maintained, no clocks)	0.04	0.0008	<0.0001	0.12
MIC Record (8kHz)[2]	4.1	1.0	0.001	14.1
Stereo 16Ω HP Playback (48kHz, quiescent)[2]	3.3	6.2	0.004	21.1
Stereo 16Ω HP Playback (48kHz, white noise)[2]	5.4	7.3	0.004	29.4
Stereo 16Ω HP Playback (48kHz, sine wave)[2]	18	6.7	0.004	66.1

Notes:

1. DBVDD Current will increase with greater loading on digital I/O pins.
2. 5 Band EQ is enabled.
3. AVDD standby current will fall to nearer 15uA when thermal shutdown sensor is disabled.

Table 1 Power Consumption

ESTIMATING SUPPLY CURRENT

When either the DAC or ADC is enabled approximately 7mA will be drawn from DCVDD when DCVDD=1.8V and fs=48kHz. When the PLL is enabled approximately 1.5mA additional current will be drawn from DCVDD.

As a general rule, digital supply currents will scale in proportion to sample rates. Supply current for analogue and digital blocks will also be lower at lower supply voltages.

Power consumed by the output drivers will depend greatly on the signal characteristics. A quiet signal, or a signal with long periods of silence will consume less power than a signal which is continuously loud.

Estimated supply current for the analogue blocks is shown in Table 2. Note that power dissipated in the load is not shown.

REGISTER BIT	AVDD CURRENT (mA) AVDD=3.3V
BUFDCOPEN	0.1
OUT4MIXEN	0.2
OUT3MIXEN	0.2
PLLEN	1.2 (with clocks applied)
MICBEN	0.5
BIASEN	0.3
BUFIOEN	0.1
VMIDSEL	5KΩ = >0.3, less than 0.1 for 75KΩ 300KΩ settings
ROUT1EN	0.4
LOUT1EN	0.4
BOOSTENL	0.2
INPPGAENL	0.2
ADCENL	2.6 (x64, ADCOSR=0) 4.9 (x128, ADCOSR=1)
OUT4EN	0.2
OUT3EN	0.2
LOUT2EN	1mA from SPKVDD + 0.2mA from AVDD in 5V mode
ROUT2EN	1mA from SPKVDD + 0.2mA from AVDD in 5V mode
RMIXEN	0.2
LMIXEN	0.2
DACENR	1.8 (x64, DACOSR=0) 1.9 (x128, DACOSR=1)
DACENL	1.8 (x64, DACOSR=0) 1.9 (x128, DACOSR=1)

Table 2 AVDD Supply Current (AVDD=3.3V)

AUDIO PATHS OVERVIEW

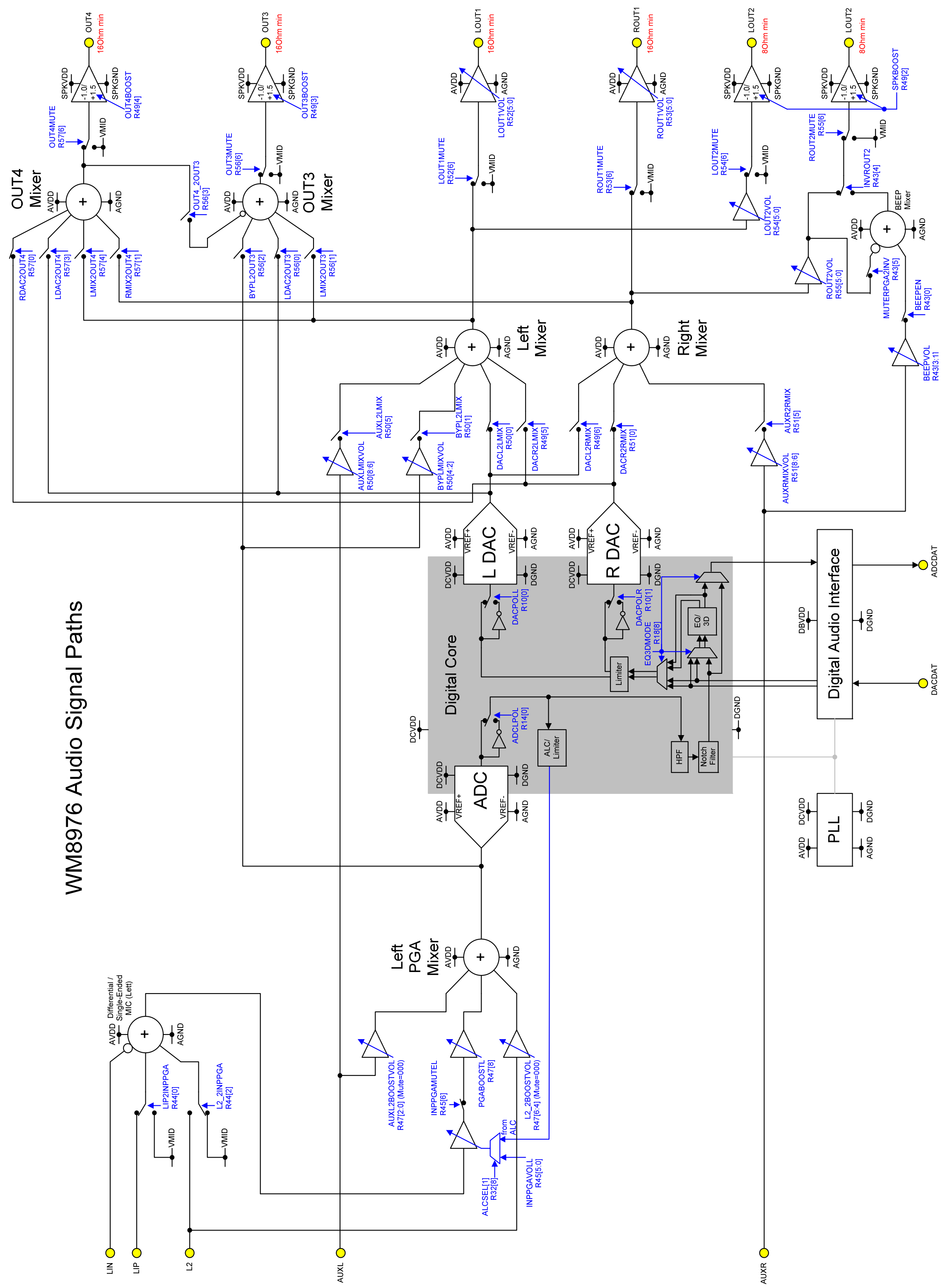


Figure 1 WM8976 Audio Signal Paths

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

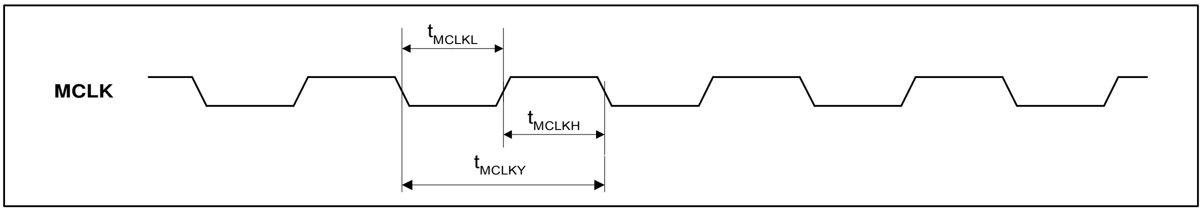


Figure 2 System Clock Timing Requirements

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD=3.3V, DGND=AGND=SPKGND=0V, T_A = +25°C

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK cycle time	T_{MCLKY}	MCLK=SYSCLK (=256fs)	81.38			ns
		MCLK input to PLL Note 1	20			ns
MCLK duty cycle	T_{MCLKDS}		60:40		40:60	

Note 1:

PLL pre-scaling and PLL N and K values should be set appropriately so that SYSCLK is no greater than 12.288MHz.

AUDIO INTERFACE TIMING – MASTER MODE

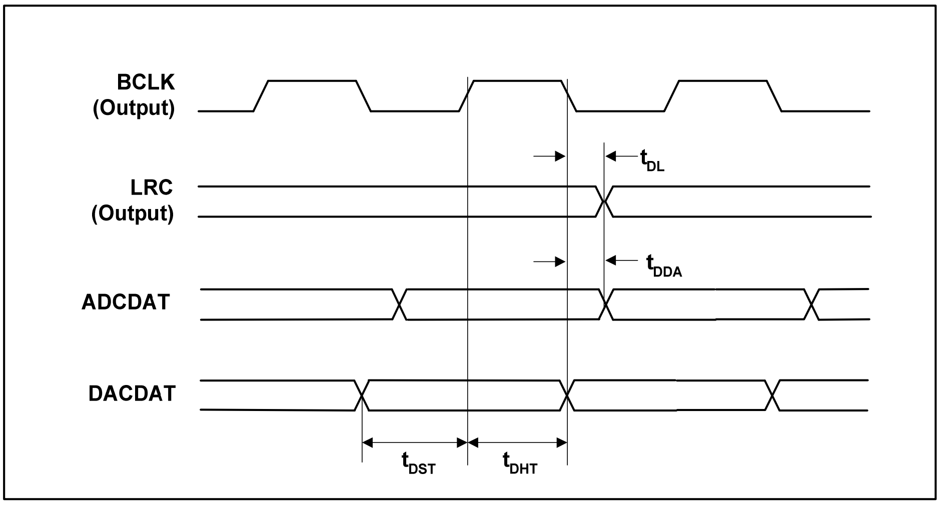


Figure 3 Digital Audio Data Timing – Master Mode (see Control Interface)

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD=3.3V, DGND=AGND=SPKGND=0V, T_A=+25°C, Master Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
LRC propagation delay from BCLK falling edge	t_{DL}			10	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			10	ns
DACDAT setup time to BCLK rising edge	t_{DST}	10			ns
DACDAT hold time from BCLK rising edge	t_{DHT}	10			ns

AUDIO INTERFACE TIMING – SLAVE MODE

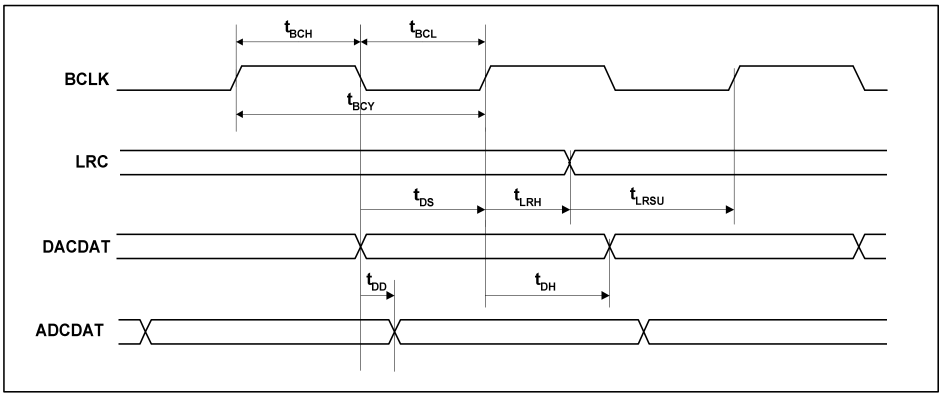


Figure 4 Digital Audio Data Timing – Slave Mode

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD=3.3V, DGND=AGND=SPKGND=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK= 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t_{BCY}	50			ns
BCLK pulse width high	t_{BCH}	20			ns
BCLK pulse width low	t_{BCL}	20			ns
LRC set-up time to BCLK rising edge	t_{LRSU}	10			ns
LRC hold time from BCLK rising edge	t_{LRH}	10			ns
DACDAT hold time from BCLK rising edge	t_{DH}	10			ns
DACDAT setup time to BCLK rising edge	t_{Ds}	10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			10	ns

Note:

BCLK period should always be greater than or equal to MCLK period.

CONTROL INTERFACE TIMING – 3-WIRE MODE

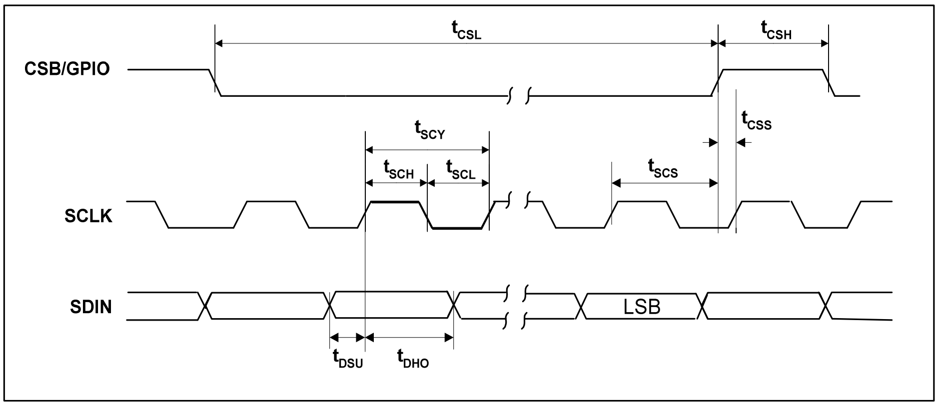


Figure 5 Control Interface Timing – 3-Wire Serial Control Mode

Test Conditions

DCVDD = 1.8V, DBVDD = AVDD = SPKVDD = 3.3V, DGND = AGND = SPKGND = 0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB rising edge	t_{SCS}	80			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDIN to SCLK set-up time	t_{DSU}	40			ns
SCLK to SDIN hold time	t_{DHO}	40			ns
CSB pulse width low	t_{CSL}	40			ns
CSB pulse width high	t_{CSH}	40			ns
CSB rising to SCLK rising	t_{CSS}	40			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

CONTROL INTERFACE TIMING – 2-WIRE MODE

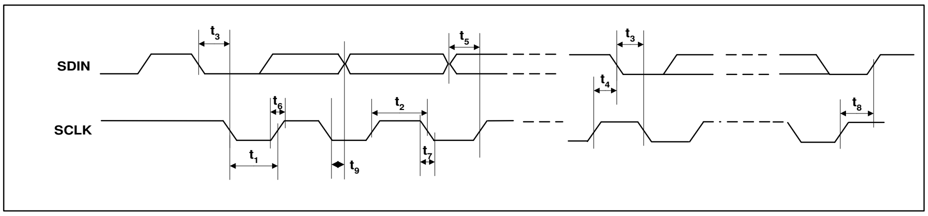


Figure 6 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DCVDD=1.8V, DBVDD=AVDD=SPKVDD=3.3V, DGND=AGND=SPKGND=0V, T_A=+25°C, Slave Mode, fs=48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency		0		526	kHz
SCLK Low Pulse-Width	t_1	1.3			us
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDIN, SCLK Rise Time	t_6			300	ns
SDIN, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

INTERNAL POWER ON RESET CIRCUIT

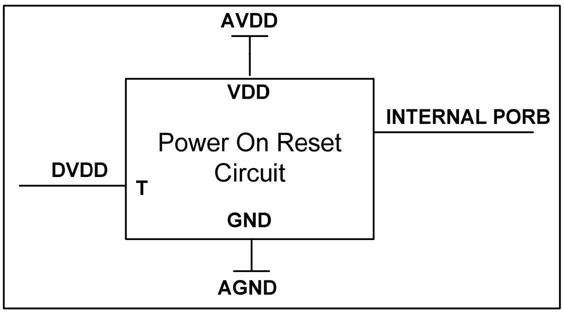


Figure 7 Internal Power on Reset Circuit Schematic

The WM8980 includes an internal Power-On-Reset Circuit, as shown in Figure 7, which is used reset the digital logic into a default state after power up. The POR circuit is powered from AVDD and monitors DVDD. It asserts PORB low if AVDD or DVDD is below a minimum threshold.

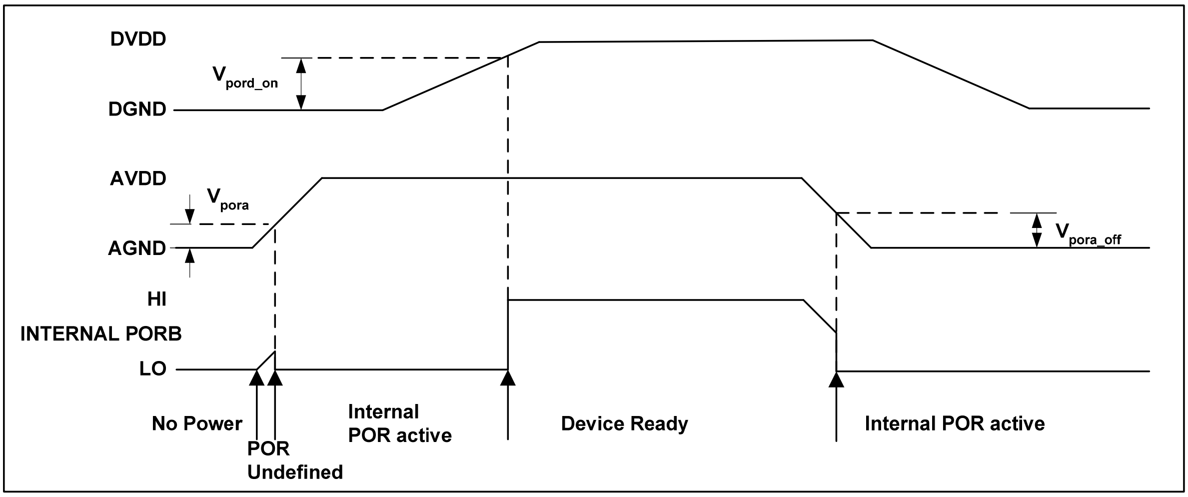


Figure 8 Typical Power up Sequence where AVDD is Powered before DVDD

Figure 8 shows a typical power-up sequence where AVDD comes up first. When AVDD goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. Now AVDD is at full supply level. Next DVDD rises to V_{pord_on} and PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where AVDD falls first, PORB is asserted low whenever AVDD drops below the minimum threshold V_{pora_off}.

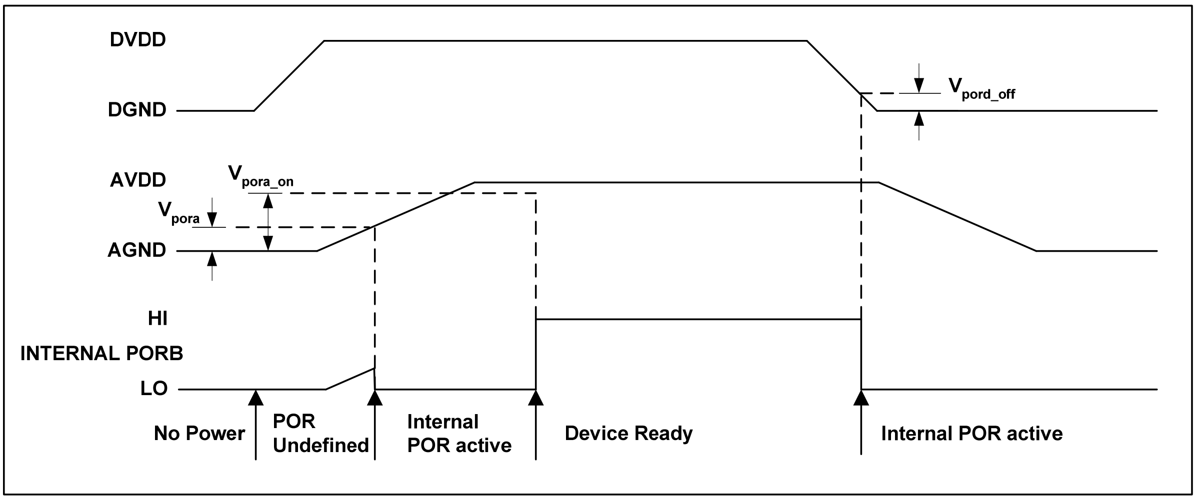


Figure 9 Typical Power up Sequence where DVDD is Powered before AVDD

Figure 9 shows a typical power-up sequence where DVDD comes up first. First it is assumed that DVDD is already up to specified operating voltage. When AVDD goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When AVDD rises to V_{pora_on}, PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where DVDD falls first, PORB is asserted low whenever DVDD drops below the minimum threshold V_{pord_off}.

SYMBOL	MIN	TYP	MAX	UNIT
V_{pora}	0.4	0.6	0.8	V
V_{pora_on}	0.9	1.2	1.6	V
V_{pora_off}	0.4	0.6	0.8	V
V_{pord_on}	0.5	0.7	0.9	V
V_{pord_off}	0.4	0.6	0.8	V

Table 3 Typical POR Operation (typical values, not tested)

Notes:

1. If AVDD and DVDD suffer a brown-out (i.e. drop below the minimum recommended operating level but do not go below V_{pora_off} or V_{pord_off}) then the chip will not reset and will resume normal operation when the voltage is back to the recommended level again.

2. The chip will enter reset at power down when AVDD or DVDD falls below V_{pora_off} or V_{pord_off}. This may be important if the supply is turned on and off frequently by a power management system.

3. The minimum t_{por} period is maintained even if DVDD and AVDD have zero rise time. This specification is guaranteed by design rather than test.

DEVICE DESCRIPTION

INTRODUCTION

The WM8976 is a low power audio CODEC combining a high quality stereo audio DAC and mono ADC, with flexible line and microphone input and output processing. Applications for this device include multimedia phones, digital camcorders, and digital still cameras with record and playback capability.

FEATURES

The chip offers great flexibility in use, and so can support many different modes of operation as follows:

MICROPHONE INPUT

A microphone input is provided, allowing a microphone to be pseudo-differentially connected, with user defined gain using internal resistors. The provision of the common mode input pin allows for rejection of common mode noise on the microphone input (level depends on gain setting chosen). A microphone bias is output from the chip which can be used to bias the microphone. The signal routing can be configured to allow manual adjustment of mic level, or to allow the ALC loop to control the level of mic signal that is transmitted.

Total gain through the microphone path of up to +55.25dB can be selected.

PGA AND ALC OPERATION

A programmable gain amplifier is provided in the input path to the ADC. This may be used manually or in conjunction with a mixed analogue/digital automatic level control (ALC) which keeps the recording volume constant.

LINE INPUTS (AUXL, AUXR)

The inputs, AUXL and AUXR, can be used as a stereo line input or as an input for warning tones (or ‘beeps’) etc. The left input can be summed into the record path, along with the microphone preamp output, so allowing for mixing of audio with ‘backing music’ etc as required.

ADC

The ADC uses a 24-bit delta sigma oversampling architecture to deliver optimum performance with low power consumption.

HI-FI DAC

The hi-fi DAC provides high quality audio playback suitable for all portable audio hi-fi type applications, including MP3 players and portable disc players of all types.

OUTPUT MIXERS

Flexible mixing is provided on the outputs of the device. A stereo mixer is provided for the stereo headphone or line outputs, LOUT1/ROUT1, and additional summers on the OUT3/OUT4 outputs allow for an optional differential or stereo line output on these pins. Gain adjustment PGAs are provided for the LOUT1/ROUT1 and LOUT2/ROUT2 outputs, and signal switching is provided to allow for all possible signal combinations. The output buffers can be configured in several ways, allowing support of up to three sets of external transducers; ie stereo headphone, BTL speaker, and BTL earpiece may be connected simultaneously. Thermal implications should be considered before simultaneous full power operation of all outputs is attempted.

Alternatively, if a speaker output is not required, the LOUT2 and ROUT2 pins might be used as a stereo headphone driver, (disable output invert buffer on ROUT2). In that case two sets of headphones might be driven, or the LOUT2 and ROUT2 pins used as a line output driver.

OUT3 and OUT4 can be configured to provide an additional stereo lineout from the output of the DACs, the mixers or the input microphone boost stages. Alternatively OUT4 can be configured as a mono mix of left and right DACs or mixers, or simply a buffered version of the chip midrail reference voltage. OUT3 can also be configured as a buffered VMID output. This voltage may then be used as a headphone 'pseudo ground' allowing removal of the large AC coupling capacitors often used in the output path.

AUDIO INTERFACES

The WM8976 has a standard audio interface, to support the transmission of data to and from the chip. This interface is a 3 wire standard audio interface which supports a number of audio data formats including I2S, DSP/PCM Mode (a burst mode in which LRC sync plus 2 data packed words are transmitted), MSB-First, left justified and MSB-First, right justified, and can operate in master or slave modes.

CONTROL INTERFACES

To allow full software control over all features, the WM8976 offers a choice of 2 or 3 wire control interface. It is fully compatible and an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs.

Selection between the modes is via the MODE pin. In 2 wire mode the address of the device is fixed as 0011010.

CLOCKING SCHEMES

WM8976 offers the normal audio DAC clocking scheme operation, where 256fs MCLK is provided to the DAC and ADC.
A PLL is included which may be used to generate these clocks in the event that they are not available from the system controller. This PLL uses an input clock, typically the 12MHz USB or ilink clock, to generate high quality audio clocks. If this PLL is not required for generation of these clocks, it can be reconfigured to generate alternative clocks which may then be output on the GPIO pins and used elsewhere in the system.

POWER CONTROL

The design of the WM8976 has given much attention to power consumption without compromising performance. It operates at very low voltages, and includes the ability to power off any unused parts of the circuitry under software control, and includes standby and power off modes.

OPERATION SCENARIOS

Flexibility in the design of the WM8976 allows for a wide range of operational scenarios, some of which are proposed below:

Multimedia phone; High quality playback to a stereo headset, a mono ear speaker or a loudspeaker is supported, allowing hi-fi playback to be mixed with voice and other analogue inputs while simultaneously transmitting a differential output from the microphone amplifier. A 5-band EQ enables hi-fi playback to be customised to suit the user's preferences and the music style, while programmable filtering allows fixed-frequency noise (e.g. 217Hz) to be reduced in the digital domain.

Camcorder; the provision of a microphone preamplifier allows support for both internal and external microphones. All drivers for speaker, headphone and line output connections are integrated. The selectable 'application filters' after the ADC provide for features such as 'wind noise' reduction, or mechanical noise reducing filters.

Digital still camera recording; Support for digital recording is similar to the camcorder case. However, additionally if the DSC supports MP3 playback, and perhaps recording, the ability of the ADC to support full 48ks/s high quality recording increases device flexibility.

AUXILIARY ANALOGUE INPUTS

An analogue stereo FM tuner or other auxiliary analogue input can be connected to the AUX inputs of WM8976, and the stereo signal listened to via headphones.

INPUT SIGNAL PATH

The WM8976 has flexible analogue inputs. An input PGA stage is followed by a boost/mix stage which drives into the hi-fi ADC. The input path has three input pins which can be configured in a variety of ways to accommodate single-ended or differential microphones. There is an auxiliary input pin which can be fed into to the input boost/mix stage as well as driving into the output path. A bypass path exists from the output of the boost/mix stage into the output left/right mixers.

MICROPHONE INPUTS

The WM8976 can accommodate a variety of microphone configurations including single ended and differential inputs. The inputs to the differential input PGA are LIN, LIP and L2.

In single-ended microphone input configuration the microphone signal should be input to LIN and the internal NOR gate configured to clamp the non-inverting input of the input PGA to VMID.

In differential mode the larger signal should be input to LIP and the smaller (e.g. noisy ground connections) should be input to LIN.

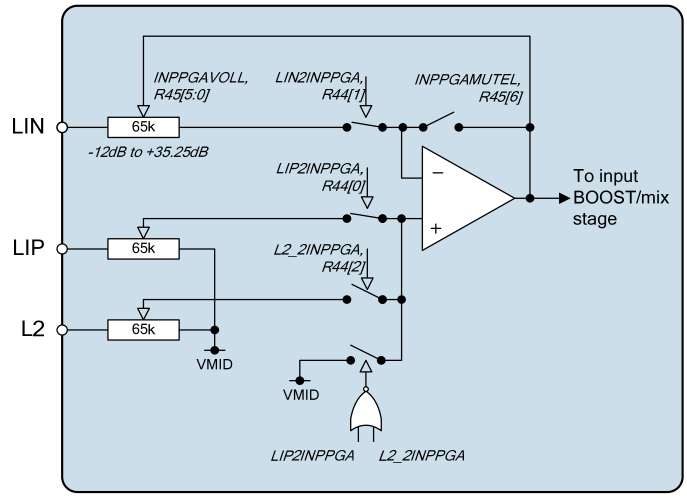


Figure 10 Microphone Input PGA Circuit

The input PGA is enabled by the IPPGAENL register bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R2 Power Management 2	2	INPPGAENL	0	Input PGA enable 0 = disabled 1 = enabled

Table 4 Input PGA Enable Register Settings

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R44 Input Control	0	LIP2INPPGA	1	Connect LIP pin to input PGA amplifier positive terminal. 0 = LIP not connected to input PGA 1 = input PGA amplifier positive terminal connected to LIP (constant input impedance)
	1	LIN2INPPGA	1	Connect LIN pin to input PGA negative terminal. 0=LIN not connected to input PGA 1=LIN connected to input PGA amplifier negative terminal.
	2	L2_2INPPGA	0	Connect L2 pin to input PGA positive terminal. 0=L2 not connected to input PGA 1=L2 connected to input PGA amplifier positive terminal (constant input impedance).

Table 5 Input PGA Control

INPUT PGA VOLUME CONTROL

The input microphone PGA has a gain range from -12dB to +35.25dB in 0.75dB steps. The gain from the LIN input to the PGA output and from the L2 amplifier to the PGA output is always common and controlled by the register bits INPPGAVOLL[5:0]. These register bits also affect the LIP pin when LIP2INPPGA=1, the L2 pin when L2_2INPPGA=1 and the L2 pin when L2_2INPPGA=1.

When the Automatic Level Control (ALC) is enabled the input PGA gains are controlled automatically and the INPPGAVOLL bits should not be used.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R45 Input PGA volume control	5:0	INPPGAVOLL	010000	Input PGA volume 000000 = -12dB 000001 = -11.25db . 010000 = 0dB . 111111 = 35.25dB
	6	INPPGAMUTEL	0	Mute control for input PGA: 0=Input PGA not muted, normal operation 1=Input PGA muted (and disconnected from the following input BOOST stage).
	7	INPPGAZCL	0	Input PGA zero cross enable: 0=Update gain when gain register changes 1=Update gain on 1st zero cross after gain register write.
	8	INPPGAUPDATE	Not latched	INPPGAVOLL volume does not update until a 1 is written to INPPGAUPDATE
R32 ALC control 1	8	ALCSEL	0	ALC function select: 0=ALC off 1=ALC on

Table 6 Input PGA Volume Control

VOLUME UPDATES

Volume settings will not be applied to the PGAs until a '1' is written to one of the INPPGAUPDATE bits. This is to allow left and right channels to be updated at the same time, as shown in Figure 11.

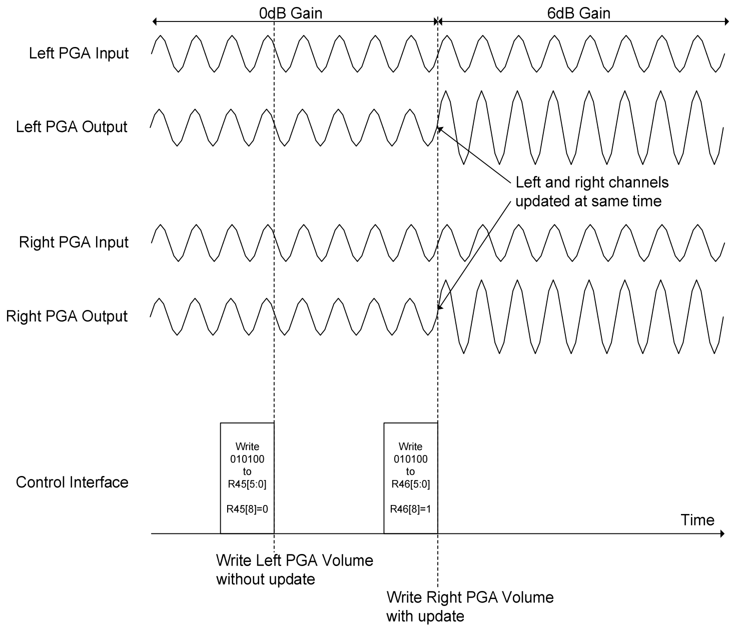


Figure 11 Simultaneous Left and Right Volume Updates

If the volume is adjusted while the signal is a non-zero value, an audible click can occur as shown in Figure 12.

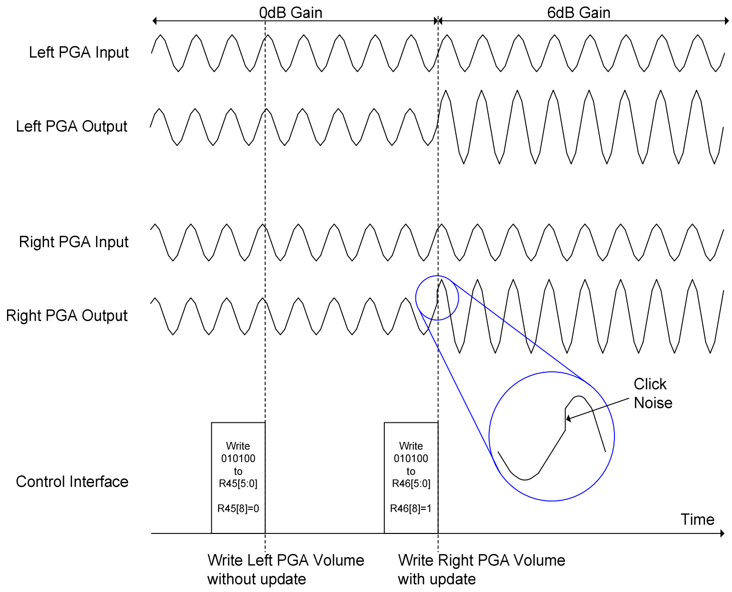


Figure 12 Click Noise During Volume Update

In order to prevent this click noise, a zero cross function is provided. When enabled, this will cause the PGA volume to update only when a zero crossing occurs, minimising click noise as shown in Figure 13.

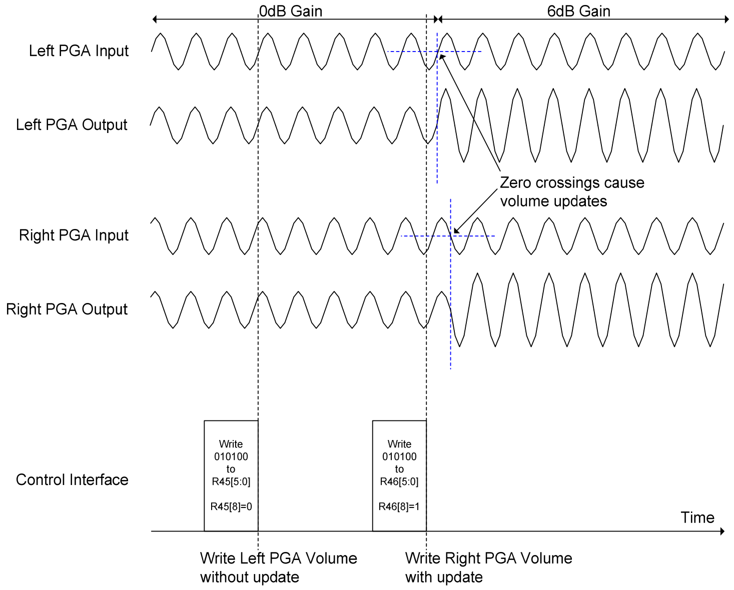


Figure 13 Volume Update Using Zero Cross Detection

If there is a long period where no zero-crossing occurs, a timeout circuit in the WM8980 will automatically update the volume. The volume updates will occur between one and two timeout periods, depending on when the INPPGAUPDATE bit is set as shown in Figure 14.

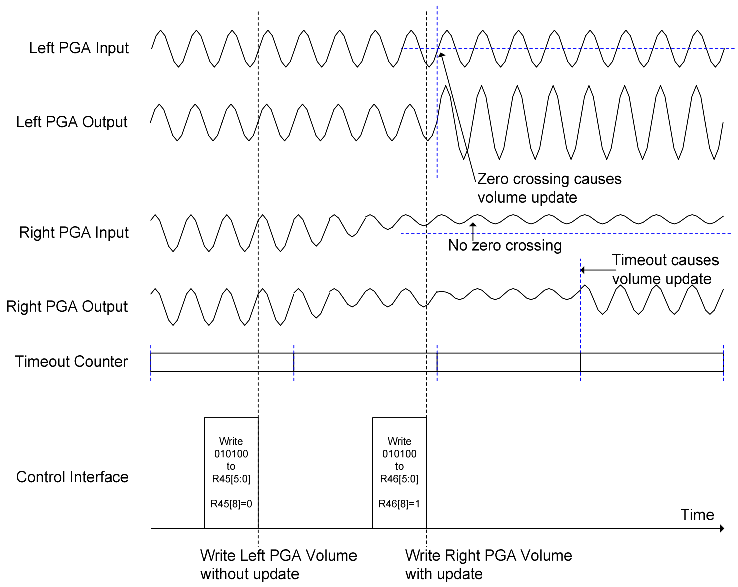


Figure 14 Volume Update after Timeout