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WM8983

Mobile Multimedia CODEC with 1W Speaker Driver

DESCRIPTION

The WM8983 is a low power, high quality stereo CODEC designed for portable multimedia applications. Highly flexible analogue mixing functions enable new application features, combining hi-fi quality audio with voice communication.

The device integrates preamps for stereo differential mics, and includes drivers for speaker, headphone and differential or stereo line output. External component requirements are reduced as no separate microphone or headphone amplifiers are required.

Advanced on-chip digital signal processing includes a 5-band equaliser, a mixed signal Automatic Level Control for the microphone or line input through the ADC as well as a purely digital limiter function for record or playback. A programmable high pass filter in the ADC path is provided for wind noise reduction and an IIR with programmable coefficients can be used as a notch filter to suppress fixed-frequency noise.

The WM8983 digital audio interface can operate in master or slave mode, while an integrated PLL supports flexible clocking schemes. A-law and μ-law companding are fully supported.

The WM8983 operates at analogue supply voltages from 2.5V to 3.3V, although the digital core can operate at voltages down to 1.71V to save power. Speaker supplies can operate up to 5V for increased speaker output power. Additional power management control enables individual sections of the chip to be powered down under software control.

FEATURES

Stereo CODEC:

- DAC SNR 98dB, THD -84dB ('A' weighted @ 48kHz)
- ADC SNR 95dB, THD -84dB ('A' weighted @ 48kHz)
- Speaker driver (1W into 8Ω BTL with 5V supply)
  - SNR 90dB
  - PSRR 80dB
- Headphone driver with 'capless' option
  - 40mW/channel output power into 16Ω / 3.3V AVDD2
- Pop and click suppression

Mic Preamps:

- Stereo Differential or mono microphone Interfaces
- Programmable preamp gain
- Pseudo differential inputs with common mode rejection
- Programmable ALC / Noise Gate in ADC path
- Low-noise bias supplied for electret microphones

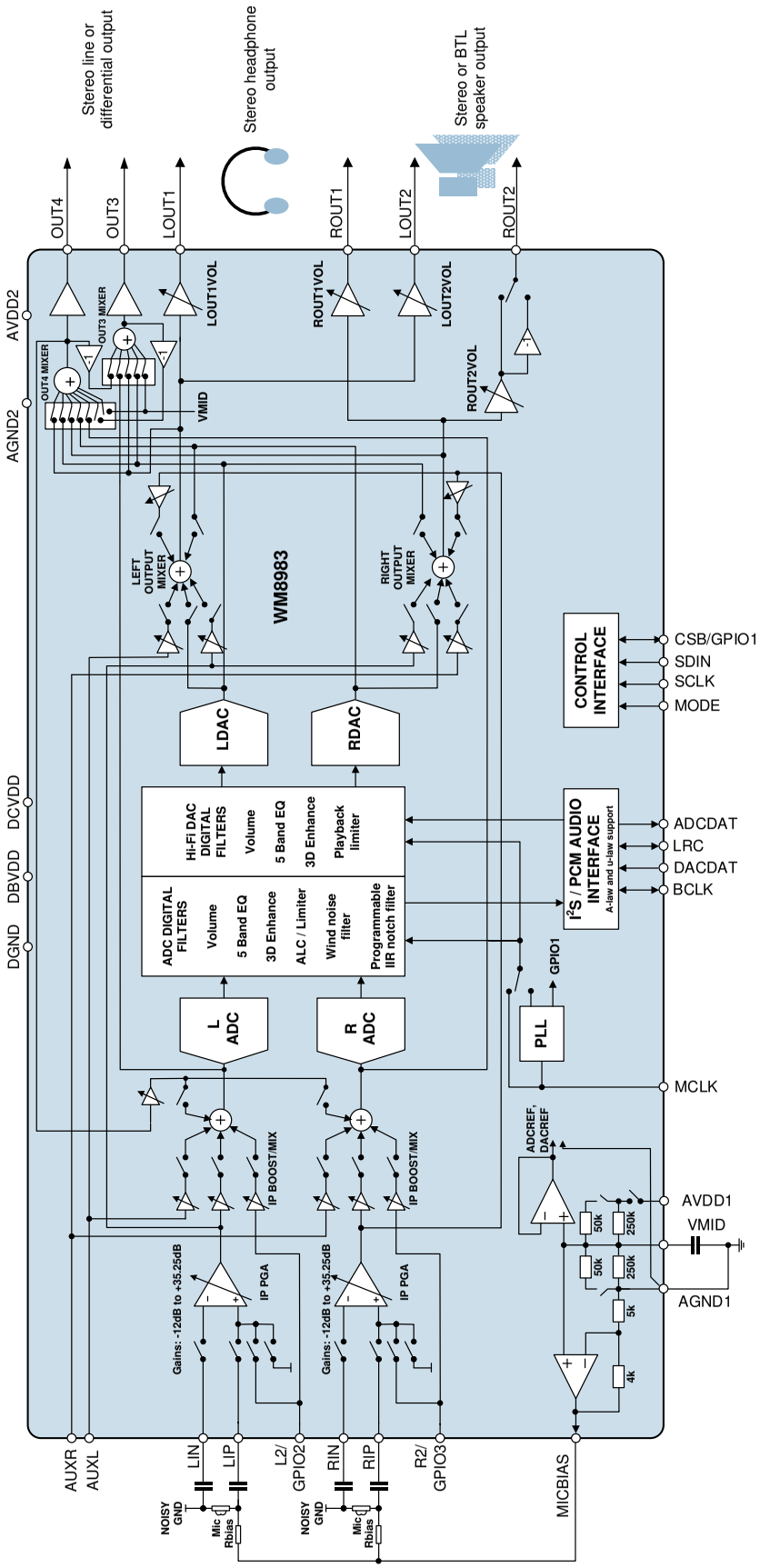
Other Features:

- Enhanced 3-D function for improved stereo separation
- Highly flexible mixing functions
- 5-band equaliser (ADC or DAC path)
- ADC Programmable high pass filter (wind noise reduction)
- ADC Programmable IIR notch filter
- Aux inputs for stereo analog input signals or 'beep'
- PLL supporting various clocks between 8MHz-50MHz
- Sample rates supported (kHz): 8, 11.025, 16, 12, 16, 22.05, 24, 32, 44.1, 48
- 2.5V to 3.6V analogue supplies
- 1.71V to 3.6V digital supplies
- 2.5V to 5.5V speaker supplies
- 5x5mm 32-lead QFN package

APPLICATIONS

- Multimedia mobile phones

BLOCK DIAGRAM



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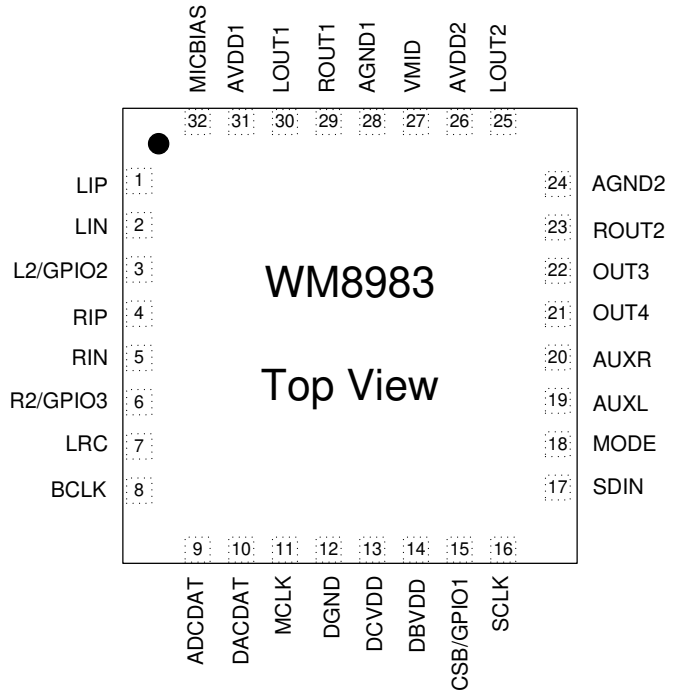
PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8983GEFL/V	-25°C to +85°C	32-lead QFN (5 x 5 mm) (pb-free)	MSL3	260ºC
WM8983GEFL/RV	-25°C to +85°C	32-lead QFN (5 x 5 mm) (pb-free, tape and reel)	MSL3	260ºC

Note:

Reel quantity = 3,500

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	LIP	Analogue input	Left MIC pre-amp positive input
2	LIN	Analogue input	Left MIC pre-amp negative input
3	L2/GPIO2	Analogue input	Left channel line input/secondary mic pre-amp positive input/GPIO2 pin
4	RIP	Analogue input	Right MIC pre-amp positive input
5	RIN	Analogue input	Right MIC pre-amp negative input
6	R2/GPIO3	Analogue input	Right channel line input/secondary mic pre-amp positive input/GPIO3 pin
7	LRC	Digital Input / Output	DAC and ADC sample rate clock
8	BCLK	Digital Input / Output	Digital audio bit clock
9	ADCDAT	Digital Output	ADC digital audio data output
10	DACDAT	Digital Input	DAC digital audio data input
11	MCLK	Digital Input	Master clock input
12	DGND	Supply	Digital ground
13	DCVDD	Supply	Digital core logic supply
14	DBVDD	Supply	Digital buffer (I/O) supply
15	CSB/GPIO1	Digital Input / Output	3-Wire control interface chip Select / GPIO1 pin
16	SCLK	Digital Input	3-Wire control interface clock input / 2-wire control interface clock input
17	SDIN	Digital Input / Output	3-Wire control interface data input / 2-Wire control interface data input
18	MODE	Digital Input	Control interface selection
19	AUXL	Analogue input	Left auxiliary input
20	AUXR	Analogue input	Right auxiliary input
21	OUT4	Analogue Output	right line output or mono mix output
22	OUT3	Analogue Output	mono or left line output
23	ROUT2	Analogue Output	Headphone or line output right 2
24	AGND2	Supply	Analogue ground (feeds ROUT2/LOUT2 and OUT3/OUT4)
25	LOUT2	Analogue Output	Headphone or line output left 2
26	AVDD2	Supply	Analogue supply (feeds output amplifiers ROUT2/LOUT2 and OUT3/OUT4)
27	VMID	Reference	Decoupling for ADC and DAC reference voltage
28	AGND1	Supply	Analogue ground (feeds all input amplifiers, PLL, ADC and DAC, internal bias circuits, output amplifiers LOUT1, ROUT1)
29	ROUT1	Analogue Output	Headphone or line output right 1
30	LOUT1	Analogue Output	Headphone or line output left 1
31	AVDD1	Supply	Analogue supply (feeds all input amplifiers, PLL, ADC and DAC, internal bias circuits, output amplifiers LOUT1, LOUT2))
32	MICBIAS	Analogue Output	Microphone bias

Note:

It is recommended that the QFN ground paddle should be connected to analogue ground on the application PCB.
Refer to the application note WAN_0118 on “Guidelines on How to Use QFN Packages and Create Associated PCB Footprints”

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
DBVDD, DCVDD, AVDD1 supply voltages	-0.3V	+4.5V
AVDD2 supply voltage	-0.3V	+7V
Voltage range digital inputs	DGND - 0.3V	DVDD + 0.3V
Voltage range analogue inputs	AGND1 - 0.3V AGND2 - 0.3V	AVDD1 + 0.3V AVDD2 + 0.3V
Storage temperature prior to soldering	30°C max / 85% RH max	
Storage temperature after soldering	-65°C	+150°C

Notes:

1. Analogue and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other.
3. Analogue supply voltages should not be less than digital supply voltages.
4. In non-boosted mode AVDD2 should be ≥ AVDD1. In boost mode, AVDD2 should be ≥ 1.5 x AVDD1.
5. DBVDD must be greater than or equal to DCVDD.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD		1.71		3.6	V
Digital supply range (Buffer)	DBVDD		1.71[2]		3.6	V
Analogue supply range	AVDD1		2.5		3.6	V
Speaker supply range	AVDD2		2.5		5.5	V
Ground	DGND, AGND1, AGND2			0		V

Notes:

1. Analogue supply voltages should not be less than digital supply voltages.
2. DBVDD should be ≥ 1.9V when using the PLL.

ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD=1.8V, AVDD1=AVDD2=DBVDD=3.3V, T_A = +25ºC, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Input PGA Inputs (LIP, LIN, RIP, RIN, L2, R2) **INPPGAVOLL, INPPGAVOLR, PGABOOSTL and PGABOOSTR = 0dB**						
Full-scale Input Signal Level – Single-ended input via LIN/RIN [1]				AVDD/3.3		V_{rms}
Full-scale Input Signal Level – Pseudo-differential input [1,2]				AVDD*0.7/ 3.3		V_{rms}
Input PGA equivalent input noise		INPPGAVOLL/R = +35.25dB No input signal 22Hz to 20kHz		150		µV
LIN, RIN input resistance		INPPGAVOLL and INPPGAVOLR = +35.25dB		1.7		kΩ
LIN, RIN input resistance		INPPGAVOLL and INPPGAVOLR = 0dB		47		kΩ
LIN, RIN input resistance		INPPGAVOLL and INPPGAVOLR = -12dB		76		kΩ
LIP, RIP input resistance		All gain settings		95		kΩ
L2, R2 input resistance		L2_2INPPGA and R2_2INPPGA = 1 L2_2BOOSTVOL and R2_2BOOSTVOL = 000		90		kΩ
L2, R2 input resistance		L2_2INPPGA and R2_2INPPGA = 0 L2_2BOOSTVOL and R2_2BOOSTVOL = +6dB		11		kΩ
L2, R2 input resistance		L2_2INPPGA and R2_2INPPGA = 0 L2_2BOOSTVOL and R2_2BOOSTVOL = 0dB		22		kΩ
L2, R2 input resistance		L2_2INPPGA and R2_2INPPGA = 0 L2_2BOOSTVOL and R2_2BOOSTVOL = -12dB		60		kΩ
Input Capacitance		All analogue input pins		10		pF
Input PGA Programmable Gain		Gain adjusted by INPPGAVOLL and INPPGAVOLL	-12		+35.25	dB
Programmable Gain Step Size		Guaranteed monotonic		0.75		dB
Input PGA Mute Attenuation		INPPGAMUTEL and INPPGAMUTER = 1		100		dB
Input Gain Boost		PGABOOSTL and PGABOOSTR = 0		0		dB
Input Gain Boost		PGABOOSTL and PGABOOSTR = 1		+20		dB

Test Conditions

DCVDD=1.8V, AVDD1=AVDD2=DBVDD=3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Auxiliary Analogue Inputs (AUXL, AUXR)						
Full-scale Input Signal Level [2]				AVDD/3.3		V_{rms}
Input Resistance		Left Input boost and mixer enabled, at +6dB		4.3		kΩ
		Left Input boost and mixer enabled, at 0dB gain		8.6		kΩ
		Left Input boost and mixer enabled, at -12dB gain		39.1		kΩ
		Right Input boost, mixer enabled, at +6dB gain		3		kΩ
		Right Input boost, mixer enabled, at 0dB gain		6		kΩ
		Right Input boost, mixer enabled, at -12dB gain		29		kΩ
Input Capacitance		All analogue Inputs		10		pF
Gain range from AUXL and AUXR input to left and right input PGA mixers		Gain adjusted by AUXL2BOOSTVOL and AUXR2BOOSTVOL	-12		+6	dB
AUXLBOOSTVOL and AUXRBOOSTVOL step size				3		dB
L2, R2 Line Input Programmable Gain						
Gain range from L2/R2 input to left and right input PGA mixers		Gain adjusted by L2_2BOOSTVOL and R2_2BOOSTVOL	-12		+6	dB
L2/R2_2BOOSTVOL step size				3		dB
L2/R2_2BOOSTVOL mute attenuation				100		dB
OUT4 to left or right input boost record path						
Gain range into left and right input PGA mixers		Gain adjusted by OUT4_2ADCVOL	-6		+12	dB
OUT4_2ADCVOL gain step size				3		dB
OUT4_2ADCVOL mute attenuation				100		dB
Analogue to Digital Converter (ADC) - Input from LIN/P and RIN/P in differential configuration to input PGA INPPGAVOLL, INPPGAVOLR, PGABOOSTL, PGABOOSTR, ADCLVOL and ADCRVOL = 0dB						
Signal to Noise Ratio [3]	SNR	A-weighted AVDD1=AVDD2=3.3V		93		dB
		A-weighted AVDD1=AVDD2=2.5V		91.5		dB
Total Harmonic Distortion [4]	THD	-12dBV Input AVDD1=AVDD2=3.3V		-78		dBFS
		-12dBV Input AVDD1=AVDD2=2.5V		-75		dBFS
Total Harmonic Distortion + Noise [5]	THD+N	-12dBV Input AVDD1=AVDD2=3.3V		-75		dBFS
		-12dBV Input AVDD1=AVDD2=2.5V		-72		dBFS
Channel Separation [6]		1kHz full scale input signal		100		dBFS

Test Conditions

DCVDD=1.8V, AVDD1=AVDD2=DBVDD=3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue to Digital Converter (ADC) - Input from L2, R2 into right PGA mixer. L2_2INPPGA and R2_2INPPGA = 0. INPPGAVOLL, INPPGAVOLR, L2_2BOOSTVOL, R2_2BOOSTVOL, ADCLVOL and ADCRVOL = 0dB						
Signal to Noise Ratio [3]	SNR	A-weighted AVDD1=AVDD2=3.3V		95		dB
		A-weighted AVDD1=AVDD2=2.5V		93		dB
Total Harmonic Distortion [4]	THD	-3dBV Input AVDD1=AVDD2=3.3V		-86		dBFS
		-3dBV Input AVDD1=AVDD2=2.5V		-78		dBFS
Total Harmonic Distortion + Noise [5]	THD+N	-3dBV Input AVDD1=AVDD2=3.3V		-80		dBFS
		-3dBV Input AVDD1=AVDD2=2.5V		-76		dBFS
Channel Separation [6]		1kHz input signal		100		dBFS
DAC to left and right mixers into 10kΩ / 50pF load on LOUT1 and ROUT1 LOUT1VOL, ROUT1VOL, DACLVOL and DACRVOL = 0dB						
Full-scale output [1]		LOUT1VOL and ROUTVOL = 0dB		AVDD1/3.3		V_{rms}
Signal to Noise Ratio [3]	SNR	A-weighted AVDD1=AVDD2=3.3V		100		dB
		A-weighted AVDD1=AVDD2=2.5V		99		dB
Total Harmonic Distortion [4]	THD	0dBFS input AVDD1=AVDD2=3.3V		-84		dBFS
		0dBFS input AVDD1=AVDD2=2.5V		-86		dBFS
Total Harmonic Distortion + Noise [5]	THD+N	0dBFS input AVDD1=AVDD2=3.3V		-83		dBFS
		0dBFS input AVDD1=AVDD2=2.5V		-84		dBFS
Channel Separation [6]		1kHz signal		100		dB
DAC to L/R mixer into 10kΩ / 50pF load on L/ROUT2 LOUT2VOL, ROUT2VOL, DACLVOL and DACRVOL = 0dB						
Full-scale output [1]				AVDD1/3.3		V_{rms}
Signal to Noise Ratio 3	SNR	A-weighted AVDD1=AVDD2=3.3V		100		dB
		A-weighted AVDD1=AVDD2=2.5V		96		dB
Total Harmonic Distortion [4]	THD	0dBFS input AVDD1=AVDD2=3.3V		-84		dBFS
		0dBFS input AVDD1=AVDD2=2.5V		-82		dBFS
Total Harmonic Distortion + Noise [5]	THD+N	0dBFS input AVDD1=AVDD2=3.3V		-82		dBFS
		0dBFS input AVDD1=AVDD2=2.5V		-80		dBFS
Channel Separation [6]		1kHz input signal		100		dB

Test Conditions

DCVDD=1.8V, AVDD1=AVDD2=DBVDD=3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to OUT3 and OUT4 mixers to OUT3/OUT4 outputs into 10kΩ / 50pF load. DACLVOL and DACRVOL = 0dB						
Full-scale output voltage				AVDD2/3.3		V_{rms}
Signal to Noise Ratio [3]	SNR	A-weighted AVDD1=AVDD2=3.3V		101.5		dB
Total Harmonic Distortion [4]	THD	full-scale signal AVDD1=AVDD2=3.3V		-80		dBFS
		full-scale signal AVDD1=AVDD2=2.5V		-87		dBFS
Total Harmonic Distortion + Noise [5]	THD+N	full-scale signal AVDD1=AVDD2=3.3V		-77		dBFS
		full-scale signal AVDD1=AVDD2=2.5V		-85		dBFS
Channel Separation [6]		1kHz signal		100		dBFS
DAC to left and right mixer into headphone (16Ω load) on LOUT2 and ROUT2 LOUT2VOL, ROUT2VOL, DACLVOL and DACRVOL = 0dB						
Full-scale output				AVDD1/3.3		V_{rms}
Signal to Noise Ratio [3]	SNR	A-weighted AVDD1=AVDD2=3.3V		98		dB
Total Harmonic Distortion [4]	THD	P_o = 20mW, RL=16Ω		-76		dBFS
Total Harmonic Distortion + Noise [5]	THD+N	Po = 20mW, RL=16Ω		-72		dBFS
Channel Separation [6]		1kHz signal		100		dB
Bypass paths to left and right output mixers. BYPL2LMIX = 1 and BYPR2RMIX = 1						
PGA gain range into mixer		Gain adjusted by BYPLMIXVOL and BYPRMIXVOL	-15	0	+6	dB
BYPLMIXVOL and BYPRMIXVOL gain step into mixer				3		dB
Mute attenuation		BYPL2LMIX = 0 BYPR2RMIX = 0		100		dB
Analogue outputs (LOUT1, ROUT1, LOUT2, ROUT2)						
Programmable Gain range		Gain adjusted by L/ROUT1VOL and L/ROUT2VOL	-57	0	+6	dB
Programmable Gain step size		Guaranteed monotonic		1		dB
Mute attenuation		1kHz, full scale signal L/ROUT1MUTE = 1 L/ROUT2MUTE = 1		85		dB

Test Conditions

DCVDD=1.8V, AVDD1=AVDD2=DBVDD=3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LIN and RIN input PGA to input boost stage into 10kΩ / 50pF load on OUT3/OUT4 outputs INPPGAVOLL, INPPGAVOLR, PGABOOSTL and PGABOOSTR = 0dB						
Full-scale output voltage, 0dB gain				AVDD2/3.3		V_{rms}
Signal to Noise Ratio 3	SNR	A-weighted AVDD1=AVDD2=3.3V	90	98		dB
		A-weighted AVDD1=AVDD2=2.5V		96		dB
		22Hz to 22kHz AVDD1=AVDD2=3.3V		95.5		dBFS
		22Hz to 22kHz AVDD1=AVDD2=2.5V		93.5		dBFS
Total Harmonic Distortion [4]	THD	full-scale signal AVDD1=AVDD2=3.3V		-84		dBFS
		full-scale signal AVDD1=AVDD2=2.5V		-82		dBFS
Total Harmonic Distortion + Noise [5]	THD+N	full-scale signal AVDD1=AVDD2=3.3V		-82		dBFS
		full-scale signal AVDD1=AVDD2=2.5V		-80		dBFS
Channel Separation [6]				100		dB
LIN and RIN into input PGA Bypass to LOUT1 and ROUT1 into 10kΩ / 50pF loads BYPLMIXVOL, BYPRMIXVOL, LOUT1VOL and ROUT1VOL = 0dB						
Full-scale output voltage, 0dB gain				AVDD1/3.3		V_{rms}
SIGNAL TO NOISE RATIO [3]	SNR	A-weighted AVDD1=AVDD2=3.3V	90	100		dB
		A-weighted AVDD1=AVDD2=2.5V		96		dB
		22Hz to 22kHz AVDD1=AVDD2=3.3V		95.5		dB
		22Hz to 22kHz AVDD1=AVDD2=2.5V		93.5		dB
Total Harmonic Distortion [4]	THD	full-scale signal AVDD1=AVDD2=3.3V		-87	-75	dBFS
		full-scale signal AVDD1=AVDD2=2.5V		-69		dBFS
Total Harmonic Distortion + Noise [5]	THD+N	full-scale signal AVDD1=AVDD2=3.3V		-85	-73	dBFS
		full-scale signal AVDD1=AVDD2=2.5V		-68		dBFS
Channel separation [6]		1kHz full scale signal		100		dB

Test Conditions

DCVDD=1.8V, AVDD1=AVDD2=DBVDD=3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Speaker Output (LOUT2, ROUT2 with 8Ω bridge tied load, INVROUT2=1)						
Full scale output voltage, 0dB gain. [7]		SPKBOOST=0		AVDD2/ 3.3		Vrms
		SPKBOOST=1		(AVDD2/ 3.3)*1.5		
Output Power	P_O	Output power is very closely correlated with THD; see below				
Total Harmonic Distortion	THD	P_O =200mW, R_L = 8Ω, AVDD2=3.3V		0.04 -68		% dB
		P_O =320mW, R_L = 8Ω, AVDD2=3.3V		1.0 -40		% dB
		P_O =500mW, R_L = 8Ω, AVDD2=5V		0.02 -74		% dB
		P_O =860mW, R_L = 8Ω, AVDD2=5V		1.0 -40		% dB
Signal to Noise Ratio	SNR	AVDD2=3.3V, R_L = 8Ω		90		dB
		AVDD2=5V, R_L = 8Ω		90		dB
Power Supply Rejection Ratio (50Hz-22kHz)	PSRR	R_L = 8Ω BTL		80		dB
		R_L = 8Ω BTL AVDD2=5V (boost)		69		dB
Microphone Bias						
Bias Voltage		MBVSEL=0		0.9 x AVDD1		V
		MBVSEL=1		0.65 x AVDD1		V
Bias Current Source		for $V_{MICBIAS}$ within +/-3%			3	mA
Output Noise Voltage		1kHz to 20kHz		15		nV/√Hz
Digital Input / Output						
Input HIGH Level	V_{IH}		0.7 × DBVDD			V
Input LOW Level	V_{IL}				0.3 × DBVDD	V
Output HIGH Level	V_{OH}	I_{OL}=1mA	0.9 × DBVDD			V
Output LOW Level	V_{OL}	I_{OH}=1mA			0.1 x DBVDD	V
Input Capacitance		All digital pins		10		pF

TERMINOLOGY

1. Full-scale input and output levels scale in relation to AVDD or AVDD2 depending upon the input or output used. For example, when AVDD = 3.3V, 0dBFS = $1V_{rms}$ (0dBV). When AVDD < 3.3V the absolute level of 0dBFS will decrease with a linear relationship to AVDD.
2. Input level to RIP and LIP in differential configurations is limited to a maximum of -3dB or performance will be reduced.
3. Signal-to-noise ratio (dBFS) – SNR is the difference in level between a reference full scale output signal and the device output with no signal applied. This ratio is also called idle channel noise. (No Auto-zero or Automute function is employed in achieving these results).
4. Total Harmonic Distortion (dBFS) – THD is the difference in level between a reference full scale output signal and the first seven odd harmonics of the output signal. To calculate the ratio, the fundamental frequency of the output signal is notched out and an RMS value of the next seven harmonics is calculated.
5. Total Harmonic Distortion plus Noise (dBFS) – THD+N is the difference in level between a reference full scale output signal and the sum of the harmonics, wide-band noise and interference on the output signal. To calculate the ratio, the fundamental frequency of the output signal is notched out and an RMS value of the total harmonics, wide-band noise and interference is calculated.
6. Channel Separation (dB) – Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
7. The maximum output voltage can be limited by the speaker power supply. If SPKBOOST is set, then AVDD2 should be 1.5xAVDD to prevent clipping taking place in the output stage (when PGA gains are set to 0dB).

TYPICAL PERFORMANCE

SPEAKER OUTPUT THD VERSUS POWER

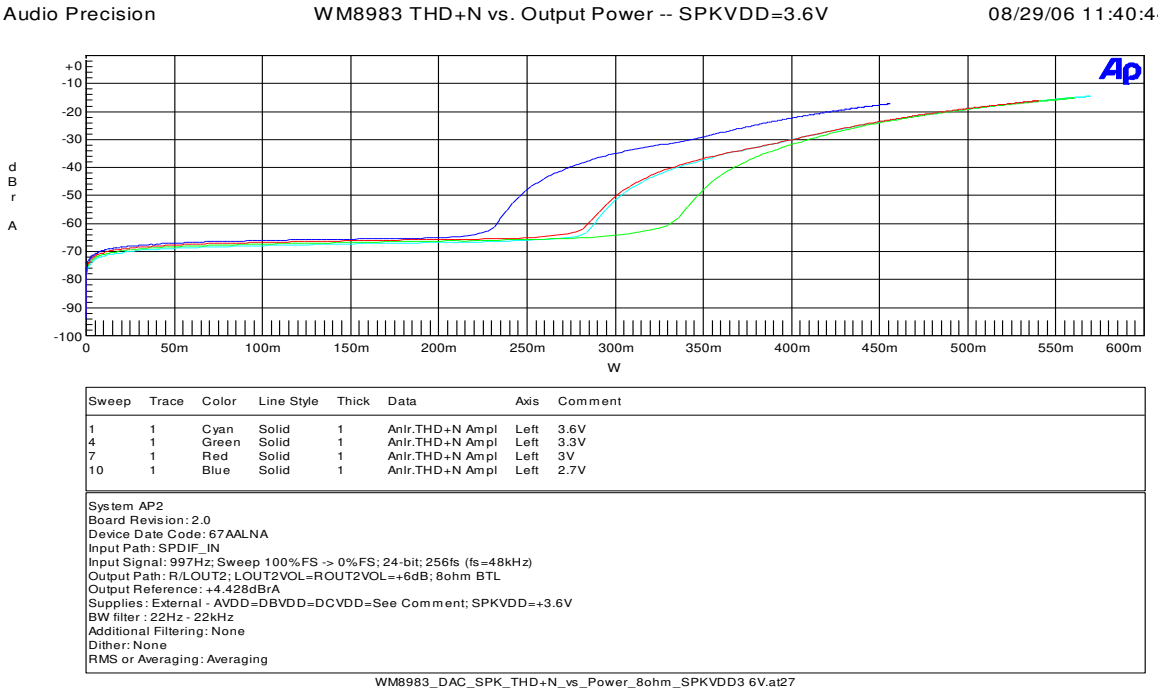


Figure 1 Speaker THD+N vs Output Power (Boost Disabled: SPKVDD=3.6V; SPKBOOST=0; AVDD Range =3.6-2.7V)

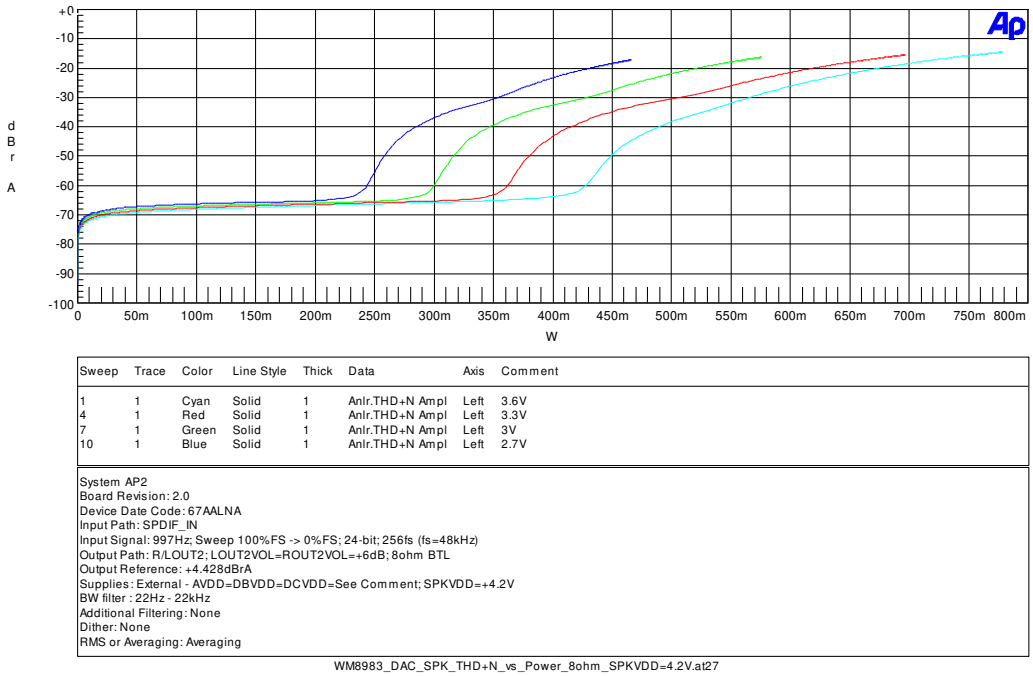
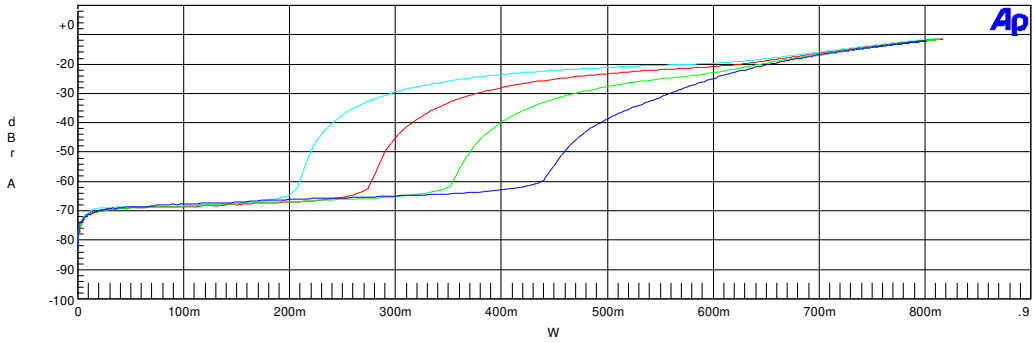


Figure 2 Speaker THD+N vs Output Power (Boost Disabled: SPKVDD=4.2V; SPKBOOST=0; AVDD Range =3.6-2.7V)

Audio Precision WM8983 THD+N vs. Output Power -- Boost enabled; SPKVDD=4.2V 08/29/06 12:58:55



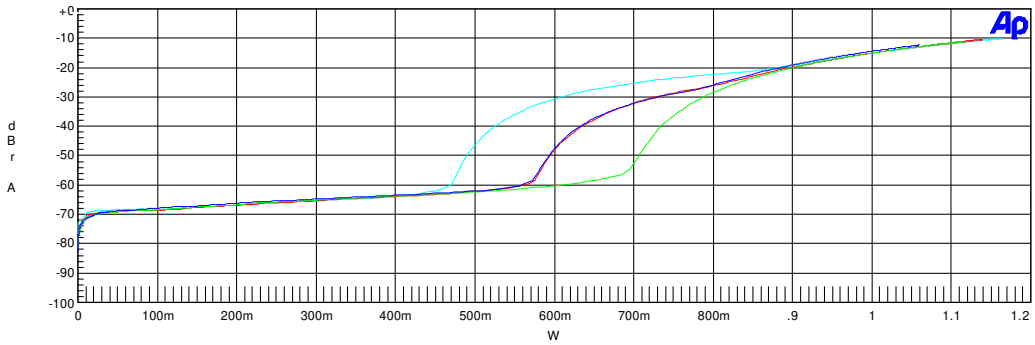
Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	1	Anlr.THD+N Ampl	Left	3.6V
4	1	Red	Solid	1	Anlr.THD+N Ampl	Left	3.3V
7	1	Green	Solid	1	Anlr.THD+N Ampl	Left	3V
10	1	Blue	Solid	1	Anlr.THD+N Ampl	Left	2.7V

System AP2
Board Revision: 2.0
Device Date Code: 67AALNA
Input Path: SPDIF_IN
Input Signal: 997Hz; Sweep 100%FS -> 0%FS; 24-bit; 256fs (fs=48kHz)
Output Path: R/LOUT2; LOUT2VOL=ROUT2VOL=+6dB; 8ohm BTL
Output Reference: +4.428dBrA
Supplies: External - AVDD=DBVDD=DCVDD=See Comment; SPKVDD=4.2V
BW filter : 22Hz - 22kHz
Additional Filtering: None
Dither: None
RMS or Averaging: Averaging

WM8983_DAC_SPK_THD+N_vs_Power_8ohm_Boost_SPKVDD=4.2V.at27

Figure 3 Speaker THD+N vs Output Power (Boost Mode: SPKVDD=4.2V; SPKBOOST=1; AVDD Range =3.6-2.7V)

Audio Precision WM8983 THD+N vs. Output Power -- Boost enabled; SPKVDD=5V 08/29/06 12:48:45



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Cyan	Solid	1	Anlr.THD+N Ampl	Left	3.6V
4	1	Red	Solid	1	Anlr.THD+N Ampl	Left	3.3V
7	1	Green	Solid	1	Anlr.THD+N Ampl	Left	3V
10	1	Blue	Solid	1	Anlr.THD+N Ampl	Left	2.7V

System AP2
Board Revision: 2.0
Device Date Code: 67AALNA
Input Path: SPDIF_IN
Input Signal: 997Hz; Sweep 100%FS -> 0%FS; 24-bit; 256fs (fs=48kHz)
Output Path: R/LOUT2; LOUT2VOL=ROUT2VOL=+6dB; 8ohm BTL
Output Reference: +4.428dBrA
Supplies: External - AVDD=DBVDD=DCVDD=See Comment; SPKVDD=5V
BW filter : 22Hz - 22kHz
Additional Filtering: None
Dither: None
RMS or Averaging: Averaging

WM8983_DAC_SPK_THD+N_vs_Power_8ohm_Boost_SPKVDD=5V.at27

Figure 4 Speaker THD+N vs Output Power (Boost Mode: SPKVDD=5V; SPKBOOST=1; AVDD Range =3.6-2.7V)

TYPICAL POWER CONSUMPTION

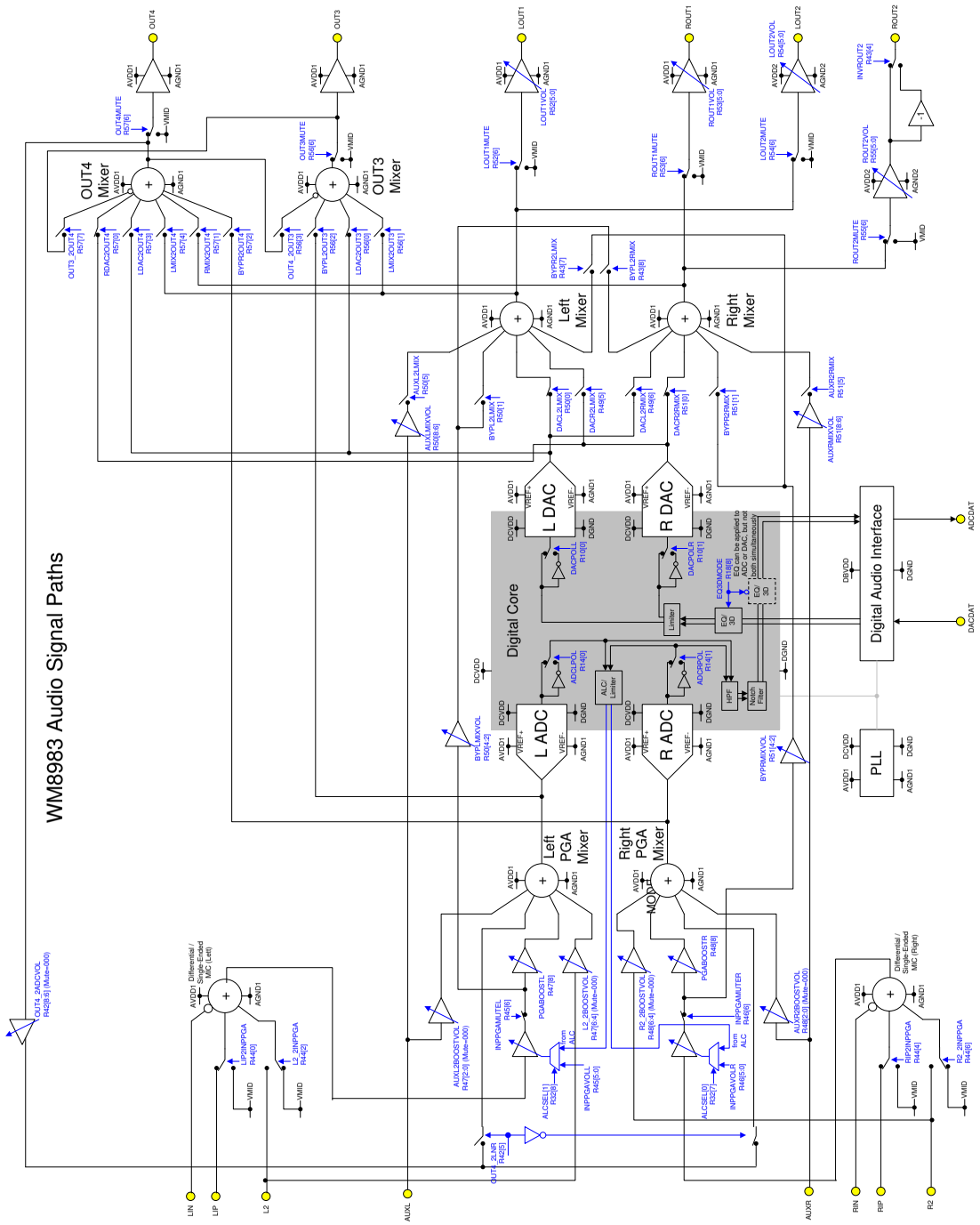
Estimated current consumption for typical scenarios are shown below.

Power delivered to the load is not included.

MODE	I_{AVDD1} mA (3.3V)	I_{AVDD2} mA (3.3V)	I_{DCVDD} mA (1.8V)	I_{DBVDD} mA (1.8V)	TOTAL mW
Off (No clocks, temperature sensor disabled)	0.010	0.010	0.001	0.002	0.071
Sleep (VREF maintained)	0.100	0.001	0.012	0.003	0.360
Mono Record from Differential MIC (8kHz, PLL enabled)	4.000	0.001	0.400	0.030	13.97
Stereo HP Playback (44.1kHz, PLL enabled)	3.700	0.950	2.100	0.100	19.31

Table 1 Power Consumption

AUDIO PATHS OVERVIEW



SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

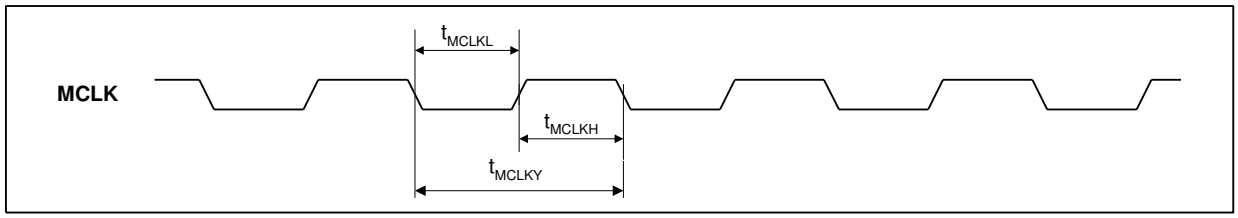


Figure 5 System Clock Timing Requirements

Test Conditions

DCVDD=1.8V, DBVDD=AVDD1=AVDD2=3.3V, DGND=AGND1=AGND2=0V, T_A = +25ºC, Slave Mode

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
MCLK cycle time	T_{MCLKY}	MCLK=SYSCLK (=256fs)	81.38			ns
		MCLK input to PLL Note 1	20			ns
MCLK duty cycle	T_{MCLKDS}		60:40		40:60	

Note:

1. PLL pre-scaling and PLL N and K values should be set appropriately so that SYSCLK is no greater than 12.288MHz.

AUDIO INTERFACE TIMING – MASTER MODE

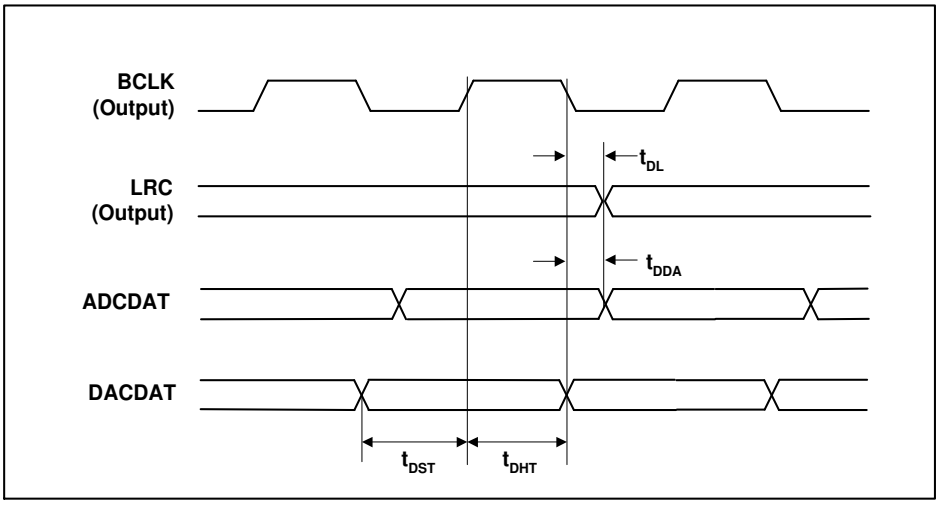


Figure 6 Digital Audio Data Timing – Master Mode (see Control Interface)

Test Conditions

DCVDD=1.8V, DBVDD=AVDD1=AVDD2=3.3V, DGND=AGND1=AGND2=0V, T_A=+25ºC, Master Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
LRC propagation delay from BCLK falling edge	t_{DL}			10	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			25	ns
DACDAT setup time to BCLK rising edge	t_{DST}	10			ns
DACDAT hold time from BCLK rising edge	t_{DHT}	10			ns

AUDIO INTERFACE TIMING – SLAVE MODE

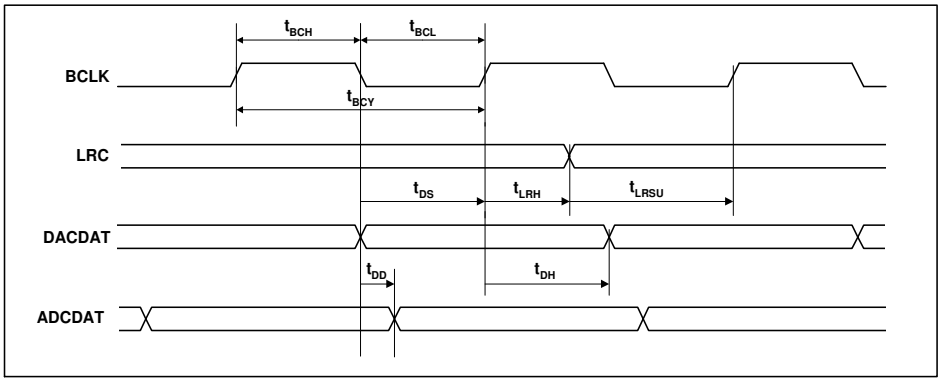


Figure 7 Digital Audio Data Timing – Slave Mode

Test Conditions

DCVDD=1.8V, DBVDD=AVDD1=AVDD2=3.3V, DGND=AGND1=AGND2=0V, T_A=+25ºC, Slave Mode, fs=48kHz, MCLK= 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t_{BCY}	50			ns
BCLK pulse width high	t_{BCH}	20			ns
BCLK pulse width low	t_{BCL}	20			ns
LRC set-up time to BCLK rising edge	t_{LRSU}	10			ns
LRC hold time from BCLK rising edge	t_{LRH}	10			ns
DACDAT hold time from BCLK rising edge	t_{DH}	10			ns
DACDAT set-up time to BCLK rising edge	t_{DS}	10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			25	ns

Note:

BCLK period should always be greater than or equal to MCLK period.

CONTROL INTERFACE TIMING – 3-WIRE MODE

3-wire mode is selected by connecting the MODE pin high.

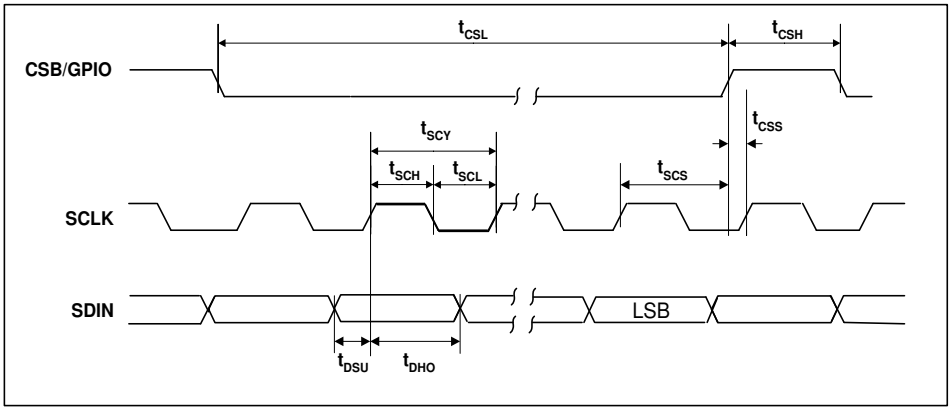


Figure 8 Control Interface Timing – 3-Wire Serial Control Mode

Test Conditions

DCVDD=1.8V, DBVDD=AVDD1=AVDD2=3.3V, DGND=AGND1=AGND2=0V, T_A=+25ºC, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB rising edge	t_{SCS}	80			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDIN to SCLK set-up time	t_{DSU}	40			ns
SCLK to SDIN hold time	t_{DHO}	40			ns
CSB pulse width low	t_{CSL}	40			ns
CSB pulse width high	t_{CSH}	40			ns
CSB rising to SCLK rising	t_{CSS}	40			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

CONTROL INTERFACE TIMING – 2-WIRE MODE

2-wire mode is selected by connecting the MODE pin low.

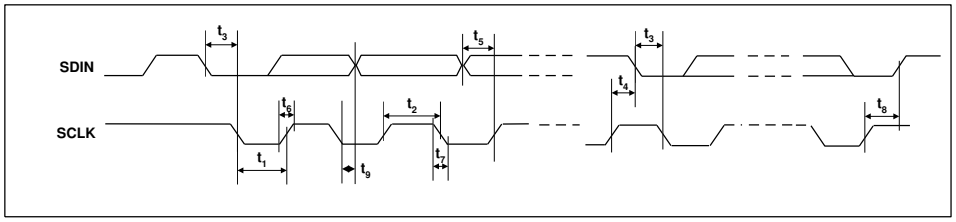


Figure 9 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DCVDD=1.8V, DBVDD=AVDD1=AVDD2=3.3V, DGND=AGND1=AGND2=0V, T_A=+25ºC, Slave Mode, fs=48kHz, MCLK=256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency		0		526	kHz
SCLK Low Pulse-Width	t_1	1.3			us
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDIN, SCLK Rise Time	t_6			300	ns
SDIN, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

INTERNAL POWER ON RESET CIRCUIT

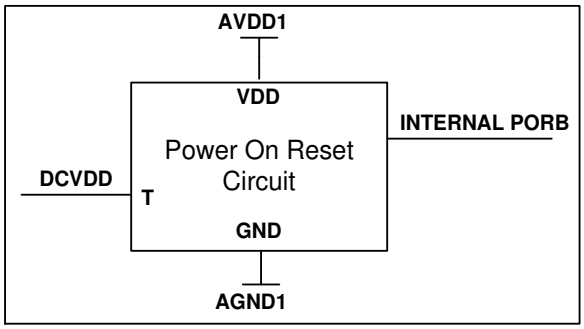


Figure 10 Internal Power on Reset Circuit Schematic

The WM8983 includes an internal Power-On-Reset Circuit, as shown in Figure 10, which is used reset the digital logic into a default state after power up. The POR circuit is powered from AVDD1 and monitors DCVDD. It asserts PORB low if AVDD1 or DCVDD is below a minimum threshold.

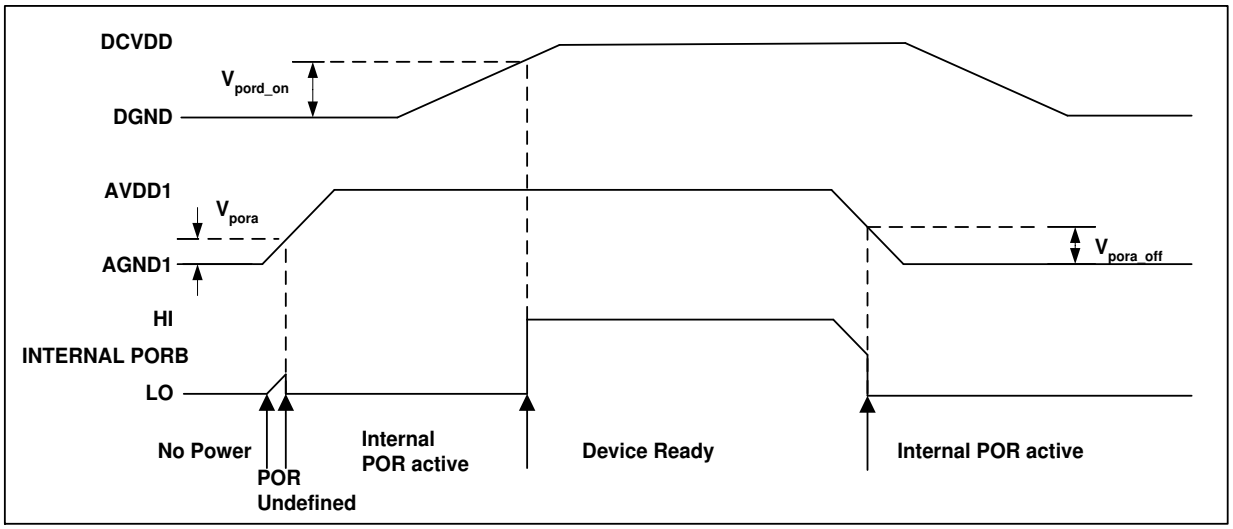


Figure 11 Typical Power up Sequence where AVDD1 is powered before DCVDD

Figure 11 shows a typical power-up sequence where AVDD1 comes up first. When AVDD1 goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. Now AVDD1 is at full supply level. Next DCVDD rises to V_{pord_on} and PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where AVDD1 falls first, PORB is asserted low whenever AVDD1 drops below the minimum threshold V_{pora_off}.

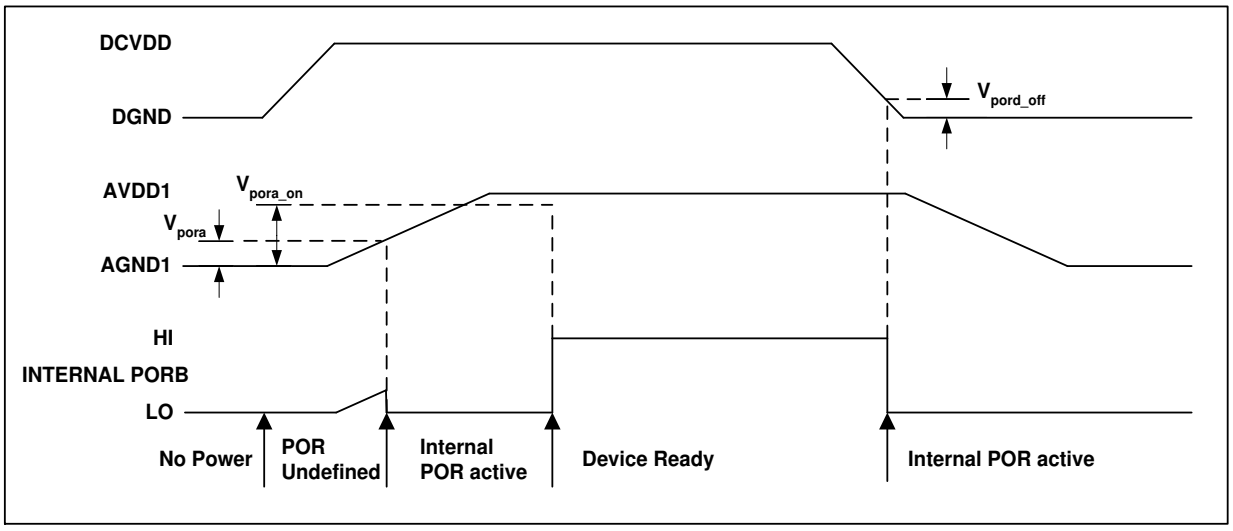


Figure 12 Typical Power up Sequence where DCVDD is Powered before AVDD1

Figure 12 shows a typical power-up sequence where DCVDD comes up first. First it is assumed that DCVDD is already up to specified operating voltage. When AVDD1 goes above the minimum threshold, V_{pora}, there is enough voltage for the circuit to guarantee PORB is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When AVDD1 rises to V_{pora_on}, PORB is released high and all registers are in their default state and writes to the control interface may take place.

On power down, where DCVDD falls first, PORB is asserted low whenever DCVDD drops below the minimum threshold V_{pord_off}.

SYMBOL	MIN	TYP	MAX	UNIT
V_{pora}	0.4	0.6	0.8	V
V_{pora_on}	0.9	1.2	1.6	V
V_{pora_off}	0.4	0.6	0.8	V
V_{pord_on}	0.5	0.7	0.9	V
V_{pord_off}	0.4	0.6	0.8	V

Table 2 Typical POR Operation (Typical Simulated Values)

Notes:

1. If AVDD1 and DCVDD suffer a brown-out (i.e. drop below the minimum recommended operating level but do not go below V_{pora_off} or V_{pord_off}), then the chip will not reset and will resume normal operation when the voltage is back to the recommended level again.
2. The chip will enter reset at power down when AVDD1 or DCVDD falls below V_{pora_off} or V_{pord_off}. This may be important if the supply is turned on and off frequently by a power management system.
3. The minimum t_{por} period is maintained even if DCVDD and AVDD1 have zero rise time. This specification is guaranteed by design rather than test.

RECOMMENDED CONTROL SEQUENCES

POWER UP/DOWN SEQUENCE

In order to minimise output pop and click noise, it is recommended that the WM8983 device is powered up and down under control using the following sequences:

Power Up:

- Turn on external power supplies. Wait for supply voltage to settle.
- Set low bias mode, BIASCUT = 1.
- Mute all Outputs and set PGAs to minimum gain, R52 to R57 = 0x140h.
- Enable VMID independent current bias, POBCTRL = 1, DELEN = 1.
- Enable required outputs, DACs and mixers.
- Enable analogue bias, BIASEN, and VMID with required charge time e.g. VMIDSEL=01 = 100kΩ.
- Setup digital interface, input amplifiers, PLL, ADCs and DACs for desired operation.
- Unmute L/ROUT1 and set desired volume, e.g. for 0dB R52 and R53 = 0x139h.
- Unmute L/ROUT2 and set desired volume, e.g. for 0dB R54 and R55 = 0x139h.
- Disable VMID independent current bias, POBCTRL = 0, DELEN = 0.

Power Down:

- Disable Thermal shutdown
- Disable VMIDSEL=00 and BIASEN=0
- Wait for VMID to discharge
- Power off registers R1, R2, R3 = 0x000h
- Remove external power supplies

Note:

Charging time constant is determined by impedance selected by VMIDSEL and the value of decoupling capacitor connected to VMID pin.