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CIRRUS LOGIC®

WM8988

Stereo CODEC for Portable Audio Applications

DESCRIPTION

The WM8988 is a low power, high quality stereo CODEC designed for portable digital audio applications.

The device integrates complete interfaces to 2 stereo headphone or line out ports. External component requirements are drastically reduced as no separate headphone amplifiers are required. Advanced on-chip digital signal processing performs graphic equaliser, 3-D sound enhancement and automatic level control for the microphone or line input.

The WM8988 can operate as a master or a slave, with various master clock frequencies including 12 or 24MHz for USB devices, or standard 256fs rates like 12.288MHz and 24.576MHz. Different audio sample rates such as 96kHz, 48kHz, 44.1kHz are generated directly from the master clock without the need for an external PLL.

The WM8988 operates at supply voltages down to 1.8V, although the digital core can operate at voltages down to 1.42V to save power, and the maximum for all supplies is 3.6 Volts. Different sections of the chip can also be powered down under software control.

The WM8988 is supplied in a very small and thin 4x4mm COL package, ideal for use in hand-held and portable systems.

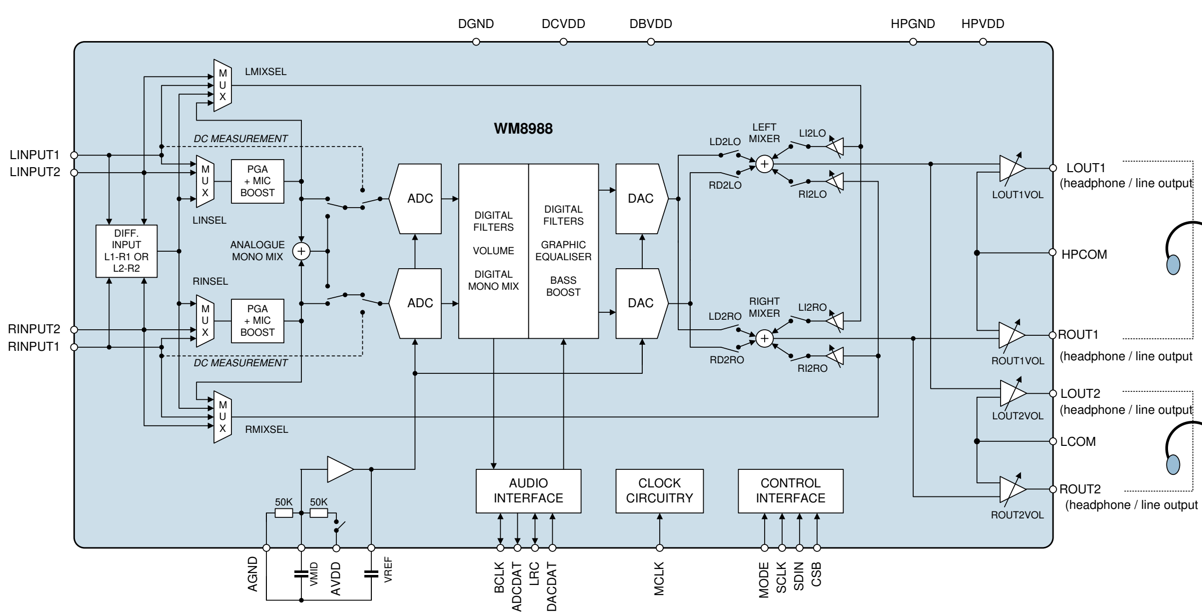
FEATURES

- DAC SNR 100dB (‘A’ weighted), THD –90dB at 48kHz, 3.3V
- ADC SNR 93dB (‘A’ weighted), THD -81dB at 48kHz, 3.3V
- Programmable ALC / Noise Gate
- 2x On-chip Headphone Drivers
  - >40mW output power on 16Ω / 3.3V
  - THD –80dB at 20mW, SNR 90dB with 16Ω load
- Digital Graphic Equaliser
- Low Power
  - 7mW stereo playback (1.8V / 1.5V supplies)
  - 14mW record and playback (1.8V / 1.5V supplies)
- Low Supply Voltages
  - Analogue 1.8V to 3.6V
  - Digital core: 1.42V to 3.6V
  - Digital I/O: 1.8V to 3.6V
- 256fs / 384fs or USB master clock rates: 12MHz, 24MHz
- Audio sample rates: 8, 11.025, 16, 22.05, 24, 32, 44.1, 48, 88.2, 96kHz generated internally from master clock
- 4x4mm COL package

APPLICATIONS

- Portable Multimedia players
- Multimedia handsets
- Handheld gaming

BLOCK DIAGRAM



Rev 4.2
DEC ‘16

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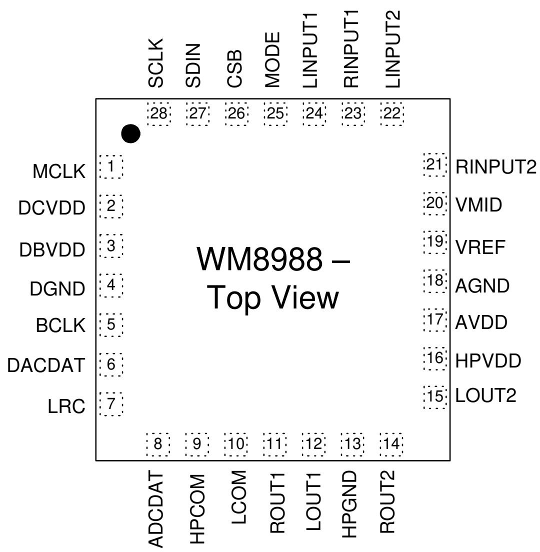
PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8988LGECN/V	-25°C to +85°C	28-lead COL QFN (4x4x0.55mm, lead-free)	MSL3	260°C
WM8988LGECN/RV	-25°C to +85°C	28-lead COL QFN (4x4x0.55mm, lead-free) Tape and reel	MSL3	260°C

Note:
Reel quantity = 3,500

PIN DESCRIPTION

PIN NO	NAME	TYPE	DESCRIPTION
1	MCLK	Digital Input	Master Clock
2	DCVDD	Supply	Digital Core Supply
3	DBVDD	Supply	Digital Buffer (I/O) Supply
4	DGND	Supply	Digital Ground (return path for both DCVDD and DBVDD)
5	BCLK	Digital Input / Output	Audio Interface Bit Clock
6	DACDAT	Digital Input	DAC Digital Audio Data
7	LRC	Digital Input / Output	Audio Interface Left / Right Clock
8	ADCDAT	Digital Output	ADC Digital Audio Data
9	HPCOM	Analogue Input	LOUT1 and ROUT1 common mode feedback
10	LCOM	Analogue Input	LOUT2 and ROUT2 common mode feedback
11	ROUT1	Analogue Output	Right Output 1 (Line or Headphone)
12	LOUT1	Analogue Output	Left Output 1 (Line or Headphone)
13	HPGND	Supply	Supply for Analogue Output Drivers (LOUT1/2, ROUT1/2)
14	ROUT2	Analogue Output	Right Output 1 (Line or Headphone)
15	LOUT2	Analogue Output	Left Output 1 (Line or Headphone)
16	HPVDD	Supply	Supply for Analogue Output Drivers (LOUT1/2, ROUT1/2, MONOUT)
17	AVDD	Supply	Analogue Supply
18	AGND	Supply	Analogue Ground (return path for AVDD)
19	VREF	Analogue Output	Reference Voltage Decoupling Capacitor
20	VMID	Analogue Output	Midrail Voltage Decoupling Capacitor
21	RINPUT2	Analogue Input	Right Channel Input 2
22	LINPUT2	Analogue Input	Left Channel Input 2
23	RINPUT1	Analogue Input	Right Channel Input 1
24	LINPUT1	Analogue Input	Left Channel Input 1
25	MODE	Digital Input	Control Interface Selection
26	CSB	Digital Input	Chip Select / Device Address Selection
27	SDIN	Digital Input/Output	Control Interface Data Input / 2-wire Acknowledge output
28	SCLK	Digital Input	Control Interface Clock Input

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus Logic tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages	-0.3V	+4.5V
Voltage range digital inputs	DGND -0.3V	DBVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Operating temperature range, T_A	-25°C	+85°C
Storage temperature after soldering	-65°C	+150°C

Notes

1. Analogue and digital grounds must always be within 0.3V of each other.
2. All digital and analogue supplies are completely independent from each other.
3. DCVDD must be less than or equal to AVDD and DBVDD.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core)	DCVDD	1.42		3.6	V
Digital supply range (Buffer)	DBVDD	1.7		3.6	V
Analogue supplies range	AVDD, HPVDD	1.8		3.6	V
Ground	DGND,AGND, HPGND		0		V

ELECTRICAL CHARACTERISTICS

Test Conditions

DCVDD = 1.5V, DBVDD = 2.4V, AVDD = HPVDD =2.4V, T_A = +25°C,
1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Inputs (LINPUT1, RINPUT1, LINPUT2, RINPUT2) to ADC out						
Full Scale Input Signal Level (for ADC 0dB Input at 0dB Gain)	V_{INFS}	AVDD = 3.3V	0.95	1.0	1.05	Vrms
		AVDD = 2.4V	0.690	0.727	0.763	
		AVDD = 1.8V	0.480	0.545	0.610	
Input Resistance	R_{IN}	L/RINPUT1 to ADC, PGA gain = 0dB	16	22		kΩ
		L/RINPUT1 to ADC, PGA gain = +30dB	1.5	2.8		
		L/RINPUT2 to ADC PGA gain = 0dB	16	22		
		L/RINPUT2 to ADC PGA gain = 30dB	1.5	2.8		
Input Capacitance				10		pF
Signal to Noise Ratio (A-weighted)	SNR	AVDD = 3.3V	80	93		dB
		AVDD = 2.4V	80	88		
		AVDD = 1.8V	78	87		
Total Harmonic Distortion	THD	-1dBFs input, AVDD = 3.3V		-81	-68	dB
		-1dBFS input, AVDD = 2.4V		-80	-68	
		-1dBFs input, AVDD = 1.8V		-76	-65	
Total Harmonic Distortion + Noise	THD+N	-1dBFs input, AVDD = 3.3V		-75	-65	dB
		-1dBFS input, AVDD = 2.4V		-70	-65	
		-1dBFs input, AVDD = 1.8V		-70	-60	
ADC Channel Separation		1kHz signal		85		dB
		10kHz signal		85		
Channel Matching		1kHz signal	-0.5	0.2	+0.5	dB
Analogue Outputs (LOUT1/2, ROUT1/2)						
0dB Full scale output voltage	V_{OUTFS}	AVDD = 3.3V	0.95	1.0	1.05	Vrms
		AVDD = 2.4V	0.690	0.727	0.763	
		AVDD = 1.8V	0.507	0.545	0.583	
Mute attenuation		1kHz, full scale signal		90		dB
Channel Separation		1kHz signal		85		dB
		10kHz signal		85		
PGA Gain range		guaranteed monotonic	+6		-67	dB
PGA step size			0.25	1	1.25	dB

Test Conditions

DCVDD = 1.5V, DBVDD = 2.4V, AVDD = HPVDD =2.4V, T_A = +25°C,
1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
DAC to Line-Out (L/ROUT1 or L/ROUT2 with 10kΩ / 50pF load)							
Signal to Noise Ratio (A-weighted)	SNR	AVDD=3.3V	DACMIXBIAS=0	88	100		dB
		HPCOM= LCOM=0	DACMIXBIAS=1		99		
		AVDD = 2.4V	DACMIXBIAS=0		97		
		HPCOM= LCOM=1	DACMIXBIAS=1	88	96		
		AVDD=1.8V	DACMIXBIAS=0		96		
		HPCOM= LCOM=0	DACMIXBIAS=1	85	95		
Total Harmonic Distortion	THD	AVDD=3.3V	DACMIXBIAS=0		-90	-75	dB
		HPCOM= LCOM=0	DACMIXBIAS=1		-89		
		AVDD = 2.4V	DACMIXBIAS=0		-83		
		HPCOM= LCOM=1	DACMIXBIAS=1		-82	-75	
		AVDD=1.8V	DACMIXBIAS=0		-80		
		HPCOM= LCOM=0	DACMIXBIAS=1		-79	-65	
Total Harmonic Distortion + Noise	THD+N	AVDD=3.3V	DACMIXBIAS=0		-88	-70	dB
		HPCOM= LCOM=0	DACMIXBIAS=1		-87		
		AVDD = 2.4V	DACMIXBIAS=0		-75		
		HPCOM= LCOM=1	DACMIXBIAS=1		-74	-70	
		AVDD=1.8V	DACMIXBIAS=0		-75		
		HPCOM= LCOM=0	DACMIXBIAS=1		-74	-65	
Channel Separation		1kHz signal			100		dB
		10kHz signal			85		
Ground noise rejection		10mV, 20kHz noise on LCOM/HPCOM, LCOM/HPCOM enabled			40		dB

Test Conditions

DCVDD = 1.5V, DBVDD = 2.4V, AVDD = HPVDD =2.4V, T_A = +25ºC,
1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Headphone Output (LOUT1/ROUT1, LOUT2/ROUT2 AC coupled to load)						
Output Power per channel	P_O	Output power is very closely correlated with THD; see below.				
Total Harmonic Distortion	THD	HPVDD=1.8V, R_L=32Ω P_O=5mW HPCOM=LCOM=0 DACMIXBIAS=1		0.013 -78		% dB
		HPVDD=1.8V, R_L=16Ω P_O=5mW HPCOM=LCOM=0 DACMIXBIAS=1		0.010 -80		% dB
		HPVDD=2.4V, R_L=32Ω, P_O=5mW HPCOM=LCOM=1 DACMIXBIAS=1		0.010 -80		% dB
		HPVDD=2.4V, R_L=16Ω, P_O=5mW HPCOM=LCOM=1 DACMIXBIAS=1		0.013 -78	0.032 -70	% dB
		HPVDD=3.3V, R_L=32Ω, P_O=20mW HPCOM=LCOM=0 DACMIXBIAS=0		0.010 -82		% dB
		HPVDD=3.3V, R_L=16Ω, P_O=20mW HPCOM=LCOM=0 DACMIXBIAS=0		0.010 -80		% dB
Total Harmonic Distortion + Noise	THD+N	HPVDD=1.8V, R_L=32Ω P_O=5mW HPCOM=LCOM=0 DACMIXBIAS=1		-80		dB
		HPVDD=1.8V, R_L=16Ω P_O=5mW HPCOM=LCOM=0 DACMIXBIAS=1		-78		dB
		HPVDD=2.4V, R_L=32Ω, P_O=5mW HPCOM=LCOM=1 DACMIXBIAS=1		-79		dB
		HPVDD=2.4V, R_L=16Ω, P_O=5mW HPCOM=LCOM=1 DACMIXBIAS=1		-77	-65	dB
		HPVDD=3.3V, R_L=32Ω, P_O=20mW HPCOM=LCOM=0 DACMIXBIAS=0		-80		dB
		HPVDD=3.3V, R_L=16Ω, P_O=20mW HPCOM=LCOM=0 DACMIXBIAS=0		-78		dB

Test Conditions

DCVDD = 1.5V, DBVDD = 2.4V, AVDD = HPVDD =2.4V, T_A = +25°C,
1kHz signal, fs = 48kHz, PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal to Noise Ratio (A-weighted)	SNR	HPVDD = 3.3V HPCOM=LCOM=0 DACMIXBIAS=1		100		dB
		HPVDD = 2.4V HPCOM=LCOM=1 DACMIXBIAS=1	90	96		dB
		HPVDD = 1.8V HPCOM=LCOM=0 DACMIXBIAS=0		96		dB
Headphone Output Ground noise rejection		10mV, 20kHz noise on HPCOM, HPCOM enabled		40		dB
Line Output Ground Noise Rejection		10mV, 20kHz noise on LCOM, LCOM enabled		40		dB
Analogue Reference Levels						
Midrail Reference Voltage	VMID		–3%	AVDD/2	+3%	V
Buffered Reference Voltage	VREF		–3%	AVDD/2	+3%	V
Digital Input / Output						
Input HIGH Level	V_{IH}		0.7×DBVDD			V
Input LOW Level	V_{IL}				0.3×DBVDD	V
Output HIGH Level	V_{OH}	I_{OH} = +1mA	0.9×DBVDD			V
Output LOW Level	V_{OL}	I_{OL} = -1mA			0.1×DBVDD	V

POWER CONSUMPTION

The power consumption of the WM8988 depends on the following factors.

- Supply voltages: Reducing the supply voltages also reduces supply currents, and therefore results in significant power savings, especially in the digital sections of the WM8988.
- Operating mode: Significant power savings can be achieved by always disabling parts of the WM8988 that are not used (e.g. mic pre-amps, unused outputs, DAC, ADC, etc.)

SCENARIO	DETAIL	AVDD POWER (MW)	HPVDD POWER (MW)	DCVDD POWER (MW)	DBVDD POWER (MW)	TOTAL POWER (MW)
OFF	Clocks Stopped	0.001	0.000	0.012	0.000	0.01
Playback to Lineout	0dB 1kHz Sinusoid	4.9	1.2	4.8	0.4	11.3
Playback to Headphone 32ohm Quiescent	No Signal	4.7	1.0	4.7	0.4	10.3
Playback to Headphone 32ohm -50dB (near silence)	1kHz Sinusoid	4.6	1.1	4.8	0.4	10.9
Playback to Headphone 32ohm -21dB (0.1mW/channel)	1kHz Sinusoid	4.6	4.9	4.8	0.4	14.7
Playback to Headphone 32ohm -9dB (2mW/channel)	1kHz Sinusoid	4.6	17.7	4.8	0.4	27.5

Table 1 Power Consumption for 2.4v / 1.8v Supplies

SCENARIO	DETAIL	AVDD POWER (MW)	HPVDD POWER (MW)	DCVDD POWER (MW)	DBVDD POWER (MW)	TOTAL POWER (MW)
OFF	Clocks Stopped	0.001	0.000	0.013	0.000	0.01
Playback to Lineout	0dB 1kHz Sinusoid	7.6	2.0	4.9	0.4	14.9
Playback to Headphone 32ohm Quiescent	No Signal	7.6	1.8	4.9	0.4	14.7
Playback to Headphone 32ohm -50dB (near silence)	1kHz Sinusoid	7.6	1.8	4.8	0.4	14.6
Playback to Headphone 32ohm -24dB (0.1mW/channel)	1kHz Sinusoid	7.6	5.9	4.8	0.4	18.7
Playback to Headphone 32ohm -11dB (2mW/channel)	1kHz Sinusoid	7.6	22.3	4.8	0.4	35.1

Table 2 Power Consumption for 3.0v / 1.8v Supplies

Notes:

1. All figures are at T_A = +25ºC, Slave Mode, fs = 48kHz, MCLK = 12.288 MHz (256fs),
2. The power dissipated in the headphone is not included in the above table.

SIGNAL TIMING REQUIREMENTS

SYSTEM CLOCK TIMING

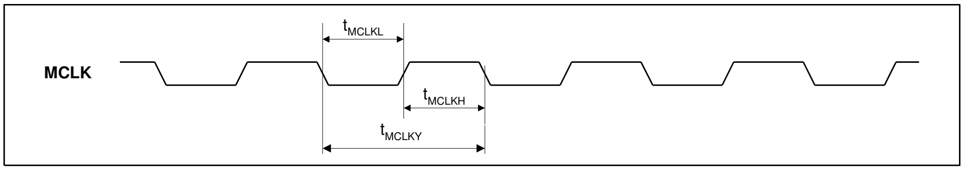


Figure 1 System Clock Timing Requirements

Test Conditions

CLKDIV2=0, DCVDD = 1.42V, DBVDD = 3.3V, DGND = 0V, T_A = +25ºC,
Slave Mode fs = 48kHz, MCLK = 384fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
System Clock Timing Information					
MCLK System clock pulse width high	T_{MCLKL}	21			ns
MCLK System clock pulse width low	T_{MCLKH}	21			ns
MCLK System clock cycle time	T_{MCLKY}	54			ns
MCLK duty cycle	T_{MCLKDS}	60:40		40:60	

Test Conditions

CLKDIV2=1, DCVDD = 1.42V, DBVDD = 3.3V, DGND = 0V, T_A = +25ºC,
Slave Mode fs = 48kHz, MCLK = 384fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
System Clock Timing Information					
MCLK System clock pulse width high	T_{MCLKL}	10			ns
MCLK System clock pulse width low	T_{MCLKH}	10			ns
MCLK System clock cycle time	T_{MCLKY}	27			ns

AUDIO INTERFACE TIMING – MASTER MODE

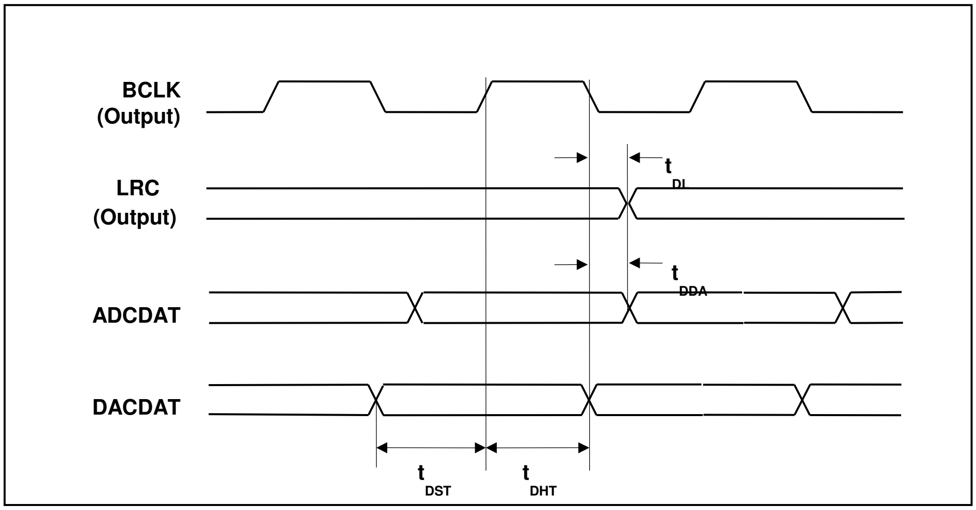


Figure 2 Digital Audio Data Timing – Master Mode

Test Conditions

DCVDD = 1.42V, DBVDD = 3.3V, DGND = 0V, T_A = +25ºC,

Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Bit Clock Timing Information					
BCLK rise time (10pF load)	t_{BCLKR}			3	ns
BCLK fall time (10pF load)	t_{BCLKF}			3	ns
BCLK duty cycle (normal mode, BCLK = MCLK/n)	t_{BCLKDS}		50:50		
BCLK duty cycle (USB mode, BCLK = MCLK)	t_{BCLKDS}		T_{MCLKDS}		
Audio Data Input Timing Information					
DACLRC propagation delay from BCLK falling edge	t_{DL}			10	ns
ADCDAT propagation delay from BCLK falling edge	t_{DDA}			10	ns
DACDAT setup time to BCLK rising edge	t_{DST}	10			ns
DACDAT hold time from BCLK rising edge	t_{DHT}	10			ns

AUDIO INTERFACE TIMING – SLAVE MODE

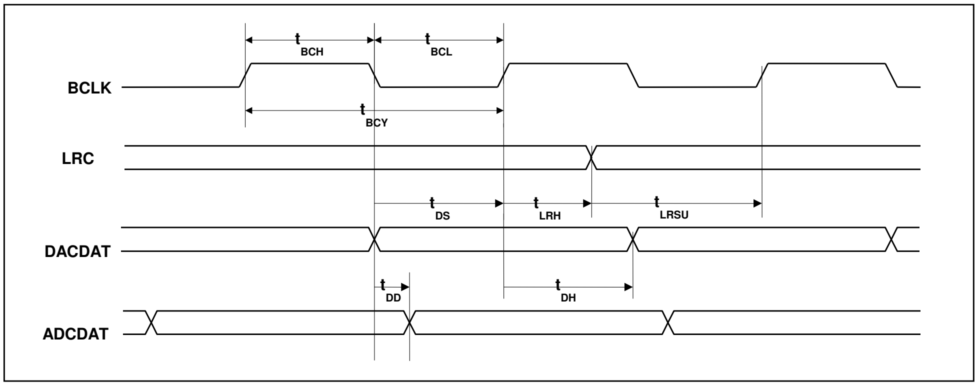


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

DCVDD = 1.42V, DBVDD = 3.3V, DGND = 0V, T_A = +25ºC,

Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
BCLK cycle time	t_{BCY}	50			ns
BCLK pulse width high	t_{BCH}	20			ns
BCLK pulse width low	t_{BCL}	20			ns
DACLRC set-up time to BCLK rising edge	t_{LRSU}	10			ns
DACLRC hold time from BCLK rising edge	t_{LRH}	10			ns
DACDAT hold time from BCLK rising edge	t_{DH}	10			ns
ADCDAT propagation delay from BCLK falling edge	t_{DD}			10	ns

Note:

BCLK period should always be greater than or equal to MCLK period.

CONTROL INTERFACE TIMING – 3-WIRE MODE

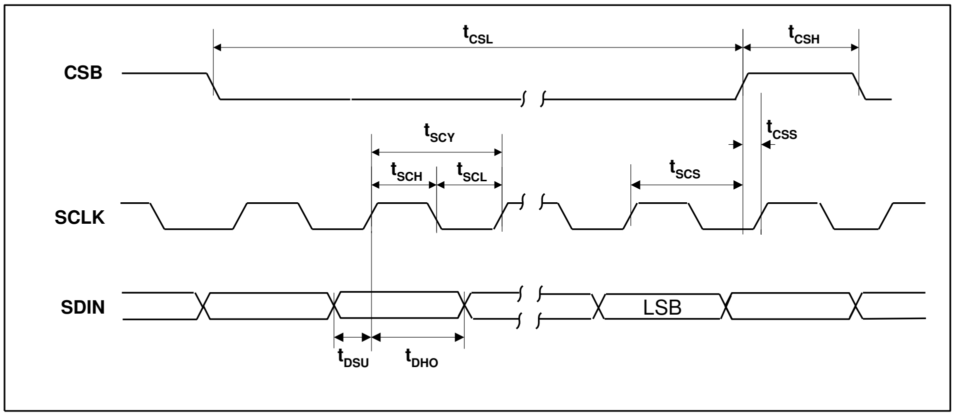


Figure 4 Control Interface Timing – 3-Wire Serial Control Mode

Test Conditions

DCVDD = 1.42V, DBVDD = 3.3V, DGND = 0V, T_A = +25ºC,

Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK rising edge to CSB rising edge	t_{SCS}	80			ns
SCLK pulse cycle time	t_{SCY}	200			ns
SCLK pulse width low	t_{SCL}	80			ns
SCLK pulse width high	t_{SCH}	80			ns
SDIN to SCLK set-up time	t_{DSU}	40			ns
SCLK to SDIN hold time	t_{DHO}	40			ns
CSB pulse width low	t_{CSL}	40			ns
CSB pulse width high	t_{CSH}	40			ns
CSB rising to SCLK rising	t_{CSS}	40			ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

CONTROL INTERFACE TIMING – 2-WIRE MODE

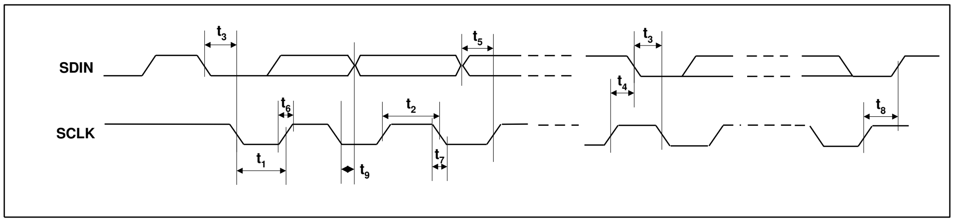


Figure 5 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

DCVDD = 1.42V, DBVDD = 3.3V, DGND = 0V, T_A = +25°C,
Slave Mode, fs = 48kHz, MCLK = 256fs, 24-bit data, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency		0		526	kHz
SCLK Low Pulse-Width	t_1	1.3			us
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDIN, SCLK Rise Time	t_6			300	ns
SDIN, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

INTERNAL POWER ON RESET CIRCUIT

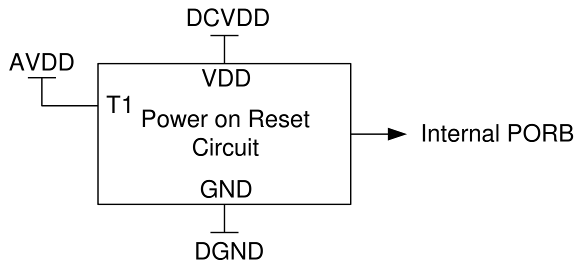


Figure 6 Internal Power on Reset Circuit Schematic

The WM8988 includes an internal Power-On-Reset Circuit, as shown in Figure 6, which is used to reset the digital logic into a default state after power up. The power on reset circuit is powered from DCVDD and monitors DCVDD and AVDD. It asserts PORB low if DCVDD or AVDD are below a minimum threshold.

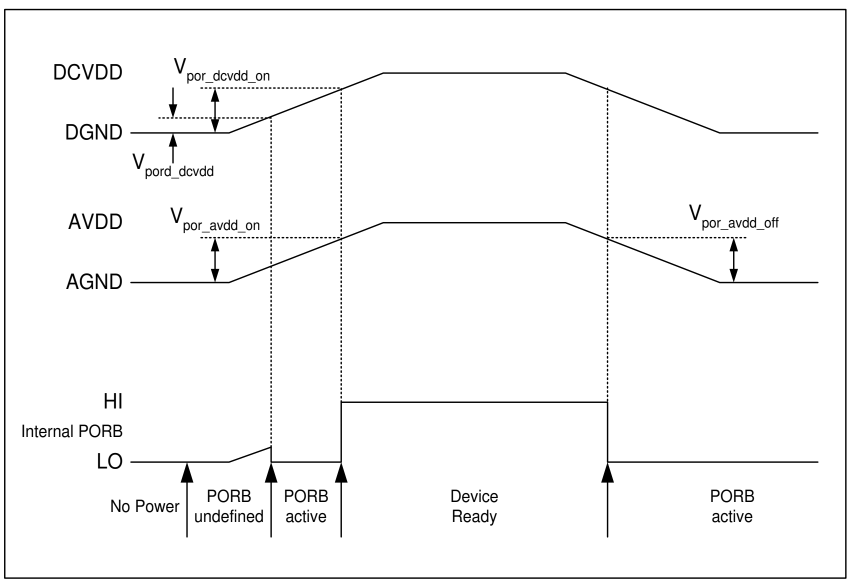


Figure 7 Typical Power-Up Sequence

Figure 7 shows a typical power-up sequence. When DCVDD and AVDD rise above the minimum thresholds, Vpord_dcvdd and Vpord_avdd, there is enough voltage for the circuit to guarantee the Power on Reset is asserted low and the chip is held in reset. In this condition, all writes to the control interface are ignored. When DCVDD rises to Vpor_dcvdd_on and AVDD rises to Vpor_avdd_on, PORB is released high and all registers are in their default state and writes to the control interface may take place. If DCVDD and AVDD rise at different rates then PORB will only be released when DCVDD and AVDD have both exceeded the Vpor_dcvdd_on and Vpor_avdd_on thresholds.

On power down, PORB is asserted low whenever DCVDD drops below the minimum threshold Vpor_dcvdd_off or AVDD drops below the minimum threshold Vpor_avdd_off.

SYMBOL	MIN	TYP	MAX	UNIT
V_{pord_dcvdd}	0.4	0.6	0.8	V
$V_{por\_dcvdd\_on}$	0.9	1.26	1.6	V
$V_{por\_avdd\_on}$	0.5	0.7	0.9	V
$V_{por\_avdd\_off}$	0.4	0.6	0.8	V

Table 3 Typical POR Operation (typical values, not tested)

DEVICE DESCRIPTION

INTRODUCTION

The WM8988 is a low power audio CODEC offering a combination of high quality audio, advanced features, low power and small size. These characteristics make it ideal for portable digital audio applications such as MP3 and minidisk player / recorders. Stereo 24-bit multi-bit delta sigma ADCs and DACs are used with oversampling digital interpolation and decimation filters.

The device includes three stereo analogue inputs that can be switched internally. Each can be used as either a line level input or microphone input and LINPUT1/RINPUT1 and LINPUT2/RINPUT2 can be configured as mono differential inputs. A programmable gain amplifier with automatic level control (ALC) keeps the recording volume constant. The on-chip stereo ADC and DAC are of a high quality using a multi-bit, low-order oversampling architecture to deliver optimum performance with low power consumption.

The DAC output signal first enters an analogue mixer where an analogue input and/or the post-ALC signal can be added to it. This mix is available on line and headphone outputs.

The WM8988 has a configurable digital audio interface where ADC data can be read and digital audio playback data fed to the DAC. It supports a number of audio data formats including I^2S, DSP Mode (a burst mode in which frame sync plus 2 data packed words are transmitted), MSB-First, left justified and can operate in master or slave modes.

The WM8988 uses a unique clocking scheme that can generate many commonly used audio sample rates from either a 12.00MHz USB clock or an industry standard 256/384 fs clock. This feature eliminates the common requirement for an external phase-locked loop (PLL) in applications where the master clock is not an integer multiple of the sample rate. Sample rates of 8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz, 88.2kHz and 96kHz can be generated. The digital filters used for recording and playback are optimised for each sampling rate used.

To allow full software control over all its features, the WM8988 offers a choice of 2 or 3 wire MPU control interface. It is fully compatible and an ideal partner for a wide range of industry standard microprocessors, controllers and DSPs.

The design of the WM8988 has given much attention to power consumption without compromising performance. It operates at very low voltages, and includes the ability to power off parts of the circuitry under software control, including standby and power off modes.

INPUT SIGNAL PATH

The input signal path for each channel consists of a switch to select between three analogue inputs, followed by a PGA (programmable gain amplifier) and an optional microphone gain boost. A differential input of either (LINPUT1 – RINPUT1) or (LINPUT2 – RINPUT2) may also be selected. The gain of the PGA can be controlled either by the user or by the on-chip ALC function (see Automatic Level Control).

The signal then enters an ADC where it is digitised. Alternatively, the two channels can also be mixed in the analogue domain and digitised in one ADC while the other ADC is switched off. The mono-mix signal appears on both digital output channels.

SIGNAL INPUTS

The WM8988 has two sets of high impedance, low capacitance AC coupled analogue inputs, LINPUT1/RINPUT1 and LINPUT2/RINPUT2. Inputs can be configured as microphone or line level by enabling or disabling the microphone gain boost.

LINSEL and RINSEL control bits (see Table 4) are used to select independently between external inputs and internally generated differential products (LINPUT1-RINPUT1 or LINPUT2-RINPUT2). The choice of differential signal, LINPUT1-RINPUT1 or LINPUT2-RINPUT2 is made using DS (refer to Table 6).

As an example, the WM8988 can be set up to convert one differential and one single ended mono signal by applying the differential signal to LINPUT1/RINPUT1 and the single ended signal to

RINPUT2. By setting LINSEL to L-R Differential (see Table 4), DS to LINPUT1 – RINPUT1 (see Table 6) and RINSEL to RINPUT2, each mono signal can then be routed to a separate ADC or Bypass path.

The signal inputs are biased internally to the reference voltage VREF. Whenever the line inputs are muted or the device placed into standby mode, the inputs are kept biased to VREF using special anti-thump circuitry. This reduces any audible clicks that may otherwise be heard when changing inputs.

DC MEASUREMENT

For DC measurements (for example, battery voltage monitoring), the input signal at the LINPUT1 and/or RINPUT1 pins can be taken directly into the respective ADC, bypassing both PGA and microphone boost. The ADC output then becomes unsigned relative to AVDD, instead of being a signed (two's complement) number relative to VREF. Setting L/RDCM will override L/RINSEL. The input range for dc measurement is AGND to AVDD.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R32 (20h) ADC Signal Path Control (Left)	7:6	LINSEL	00	Left Channel Input Select 00 = LINPUT1 01 = LINPUT2 10 = Reserved 11 = L-R Differential (either LINPUT1-RINPUT1 or LINPUT2-RINPUT2, selected by DS)
	5:4	LMICBOOST	00	Left Channel Microphone Gain Boost 00 = Boost off (bypassed) 01 = 13dB boost 10 = 20dB boost 11 = 29dB boost
R33 (21h) ADC Signal Path Control (Right)	7:6	RINSEL	00	Right Channel Input Select 00 = RINPUT1 01 = RINPUT2 10 = Reserved 11 = L-R Differential (either LINPUT1-RINPUT1 or LINPUT2-RINPUT2, selected by DS)
	5:4	RMICBOOST	00	Right Channel Microphone Gain Boost 00 = Boost off (bypassed) 01 = 13dB boost 10 = 20dB boost 11 = 29dB boost

Table 4 Input Software Control

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R31 (1Fh) ADC input Mode	5	RDCM	0	Right Channel DC Measurement 0 = Normal Operation, PGA Enabled 1 = Measure DC level on RINPUT1
	4	LDCM	0	Left Channel DC Measurement 0 = Normal Operation, PGA Enabled 1 = Measure DC level on LINPUT1

Table 5 DC Measurement Select

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R31 (1Fh) ADC Input Mode	8	DS	0	Differential input select 0: LINPUT1 – RINPUT1 1: LINPUT2 – RINPUT2

Table 6 Differential Input Select

MONO MIXING

The stereo ADC can operate as a stereo or mono device, or the two channels can be mixed to mono, either in the analogue domain (i.e. before the ADC) or in the digital domain (after the ADC). MONOMIX selects the mode of operation. For analogue mono mix either the left or right channel ADC can be used, allowing the unused ADC to be powered off or used for a dc measurement conversion. The user also has the flexibility to select the data output from the audio interface using DATSEL. The default is for left and right channel ADC data to be output, but the interface may also be configured so that e.g. left channel ADC data is output as both left and right data for when an analogue mono mix is selected.

Note: If DC measurement is selected this overrides the MONOMIX selection.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R31 (1Fh) ADC input Mode	7:6	MONOMIX [1:0]	00	00: Stereo 01: Analogue Mono Mix (using left ADC) 10: Analogue Mono Mix (using right ADC) 11: Digital Mono Mix

Table 7 Mono Mixing

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R23 (17h) Additional Control (1)	3:2	DATSEL [1:0]	00	00: left data=left ADC; right data =right ADC 01: left data =left ADC; right data = left ADC 10: left data = right ADC; right data =right ADC 11: left data = right ADC; right data = left ADC

Table 8 ADC Data Output Configuration

PGA CONTROL

The PGA matches the input signal level to the ADC input range. The PGA gain is logarithmically adjustable from +30dB to –17.25dB in 0.75dB steps. Each PGA can be controlled either by the user or by the ALC function (see Automatic Level Control). When ALC is enabled for one or both channels, then writing to the corresponding PGA control register has no effect.

The gain is independently adjustable on both Right and Left Line Inputs. Additionally, by controlling the register bits LIVU and RIVU, the left and right gain settings can be simultaneously updated. Setting the LZCEN and RZCEN bits enables a zero-cross detector which ensures that PGA gain changes only occur when the signal is at zero, eliminating any zipper noise. If zero cross is enabled a timeout is also available to update the gain if a zero cross does not occur. This function may be enabled by setting TOEN in register R23 (17h).

The inputs can also be muted in the analogue domain under software control. The software control registers are shown in Table 9. If zero crossing is enabled, it is necessary to enable zero cross timeout to un-mute the input PGAs. This is because their outputs will not cross zero when muted. Alternatively, zero cross can be disabled before sending the un-mute command.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 (00h) Left Channel PGA	8	LIVU	0	Left Volume Update 0 = Store LINVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LINVOL, right = intermediate latch)
	7	LINMUTE	1	Left Channel Input Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: LIVU must be set to un-mute.
	6	LZCEN	0	Left Channel Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately
	5:0	LINVOL [5:0]	010111 (0dB)	Left Channel Input Volume Control 111111 = +30dB 111110 = +29.25dB . . 0.75dB steps down to 000000 = -17.25dB
R1 (01h) Right Channel PGA	8	RIVU	0	Right Volume Update 0 = Store RINVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (right = RINVOL, left = intermediate latch)
	7	RINMUTE	1	Right Channel Input Analogue Mute 1 = Enable Mute 0 = Disable Mute Note: RIVU must be set to un-mute.
	6	RZCEN	0	Right Channel Zero Cross Detector 1 = Change gain on zero cross only 0 = Change gain immediately
	5:0	RINVOL [5:0]	010111 (0dB)	Right Channel Input Volume Control 111111 = +30dB 111110 = +29.25dB . . 0.75dB steps down to 000000 = -17.25dB
R23 (17h) Additional Control (1)	0	TOEN	0	Timeout Enable 0 : Timeout Disabled 1 : Timeout Enabled

Table 9 Input PGA Software Control

ANALOGUE TO DIGITAL CONVERTER (ADC)

The WM8988 uses a multi-bit, oversampled sigma-delta ADC for each channel. The use of multi-bit feedback and high oversampling rates reduces the effects of jitter and high frequency noise. The ADC Full Scale input level is proportional to AVDD. With a 3.3V supply voltage, the full scale level is 1.0 Volts r.m.s. Any voltage greater than full scale may overload the ADC and cause distortion.

ADC DIGITAL FILTER

The ADC filters perform true 24-bit signal processing to convert the raw multi-bit oversampled data from the ADC to the correct sampling frequency to be output on the digital audio interface. The digital filter path is illustrated in Figure 8.

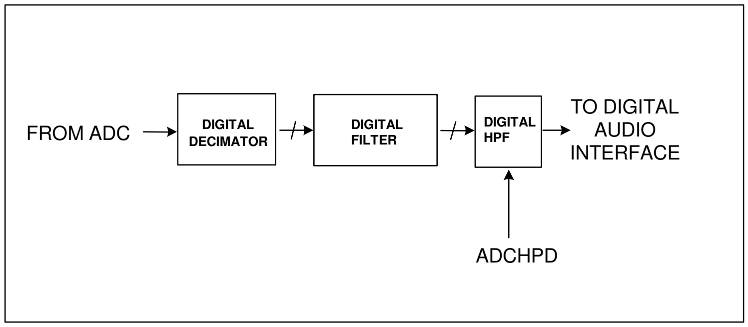


Figure 8 ADC Digital Filter

The ADC digital filters contain a digital high-pass filter, selectable via software control. The high-pass filter response is detailed in the Digital Filter Characteristics section. When the high-pass filter is enabled the DC offset is continuously calculated and subtracted from the input signal. By setting HPOR, the last calculated DC offset value is stored when the high-pass filter is disabled and will continue to be subtracted from the input signal. If the DC offset is changed, the stored and subtracted value will not change unless the high-pass filter is enabled. This feature can be used for calibration purposes. In addition the high-pass filter may be enabled separately on the left and right channels (see Table 11).

The output data format can be programmed by the user to accommodate stereo or monophonic recording on both inputs. The polarity of the output signal can also be changed under software control. The software control is shown in Table 10.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R5 (05h) ADC and DAC Control	6:5	ADCPOL [1:0]	00	00 = Polarity not inverted 01 = L polarity invert 10 = R polarity invert 11 = L and R polarity invert
	4	HPOR	0	Store dc offset when high-pass filter disabled 1 = store offset 0 = clear offset
	0	ADCHPD	0	ADCHPD and HPFLREN together determine high-pass filter behaviour (see Table 11)
R27 (1Bh)	5	HPFLREN	0	

Table 10 ADC Signal Path Control

HPFLREN	ADCHPD	LEFT CHANNEL	RIGHT CHANNEL
0	0	HPF ON	HPF ON
0	1	HPF OFF	HPF OFF
1	0	HPF ON	HPF OFF
1	1	HPF OFF	HPF ON

Table 11 ADC High Pass Filter Modes

DIGITAL ADC VOLUME CONTROL

The output of the ADCs can be digitally amplified or attenuated over a range from –97dB to +30dB in 0.5dB steps. The volume of each channel can be controlled separately. The gain for a given eight-bit code X is given by:

$0.5 \times (X\text{-}195)$ dB for $1 \leq X \leq 255$; MUTE for $X = 0$

The LAVU and RAVU control bits control the loading of digital volume control data. When LAVU or RAVU are set to 0, the LADCVOL or RADCVOL control data will be loaded into the respective control register, but will not actually change the digital gain setting. Both left and right gain settings are updated when either LAVU or RAVU are set to 1. This makes it possible to update the gain of both channels simultaneously.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R21 (15h) Left ADC Digital Volume	7:0	LADCVOL [7:0]	11000011 (0dB)	Left ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -97dB 0000 0010 = -96.5dB ... 0.5dB steps up to 1111 1111 = +30dB
	8	LAVU	0	Left ADC Volume Update 0 = Store LADCVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = LADCVOL, right = intermediate latch)
R22 (16h) Right ADC Digital Volume	7:0	RADCVOL [7:0]	11000011 (0dB)	Right ADC Digital Volume Control 0000 0000 = Digital Mute 0000 0001 = -97dB 0000 0010 = -96.5dB ... 0.5dB steps up to 1111 1111 = +30dB
	8	RAVU	0	Right ADC Volume Update 0 = Store RADCVOL in intermediate latch (no gain change) 1 = Update left and right channel gains (left = intermediate latch, right = RADCVOL)

Table 12 ADC Digital Volume Control

AUTOMATIC LEVEL CONTROL (ALC)

The WM8988 has an automatic level control that aims to keep a constant recording volume irrespective of the input signal level. This is achieved by continuously adjusting the PGA gain so that the signal level at the ADC input remains constant. A digital peak detector monitors the ADC output and changes the PGA gain if necessary. Note that when the ALC function is enabled, the settings of registers 0 and 1 (LINVOL, LIVU, LIZC, LINMUTE, RINVOL, RIVU, RIZC and RINMUTE) are ignored.

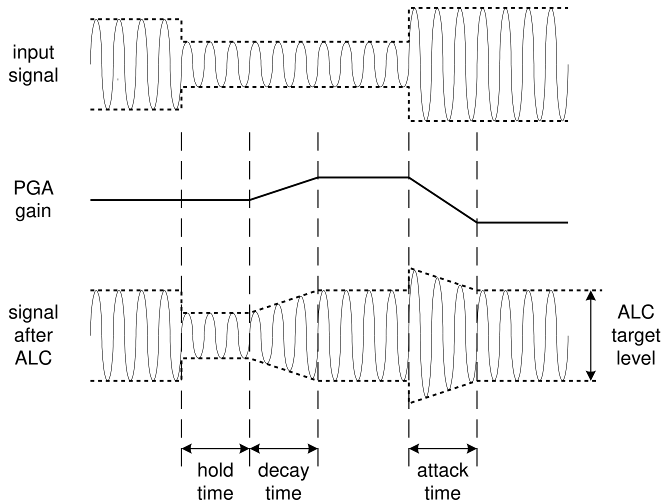


Figure 9 ALC Operation

The ALC function is enabled using the ALCSEL control bits. When enabled, the recording volume can be programmed between –6dB and –28.5dB (relative to ADC full scale) using the ALCL register bits. An upper limit for the PGA gain can be imposed by setting the MAXGAIN control bits.

HLD, DCY and ATK control the hold, decay and attack times, respectively:

Hold time is the time delay between the peak level detected being below target and the PGA gain beginning to ramp up. It can be programmed in power-of-two (2^n) steps, e.g. 2.67ms, 5.33ms, 10.67ms etc. up to 43.7s. Alternatively, the hold time can also be set to zero. The hold time only applies to gain ramp-up, there is no delay before ramping the gain down when the signal level is above target.

Decay (Gain Ramp-Up) Time is the time that it takes for the PGA gain to ramp up across 90% of its range (e.g. from –15B up to 27.75dB). The time it takes for the recording level to return to its target value therefore depends on both the decay time and on the gain adjustment required. If the gain adjustment is small, it will be shorter than the decay time. The decay time can be programmed in power-of-two (2^n) steps, from 24ms, 48ms, 96ms, etc. to 24.58s.

Attack (Gain Ramp-Down) Time is the time that it takes for the PGA gain to ramp down across 90% of its range (e.g. from 27.75dB down to -15B gain). The time it takes for the recording level to return to its target value therefore depends on both the attack time and on the gain adjustment required. If the gain adjustment is small, it will be shorter than the attack time. The attack time can be programmed in power-of-two (2^n) steps, from 6ms, 12ms, 24ms, etc. to 6.14s.

When operating in stereo, the peak detector takes the maximum of left and right channel peak values, and any new gain setting is applied to both left and right PGAs, so that the stereo image is preserved. However, the ALC function can also be enabled on one channel only. In this case, only one PGA is controlled by the ALC mechanism, while the other channel runs independently with its PGA gain set through the control register.

When one ADC channel is unused or used for DC measurement, the peak detector disregards that channel. The ALC function can also operate when the two ADC outputs are mixed to mono in the digital domain, but not if they are mixed to mono in the analogue domain, before entering the ADCs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R17 (11h) ALC Control 1	8:7	ALCSEL [1:0]	00 (OFF)	ALC function select 00 = ALC off (PGA gain set by register) 01 = Right channel only 10 = Left channel only 11 = Stereo (PGA registers unused) Note: ensure that LINVOL and RINVOL settings (reg. 0 and 1) are the same before entering this mode.
	6:4	MAXGAIN [2:0]	111 (+30dB)	Set Maximum Gain of PGA 111 : +30dB 110 : +24dB ….(-6dB steps) 001 : -6dB 000 : -12dB
	3:0	ALCL [3:0]	1011 (-12dB)	ALC target – sets signal level at ADC input 0000 = -28.5dB FS 0001 = -27.0dB FS … (1.5dB steps) 1110 = -7.5dB FS 1111 = -6dB FS
R18 (12h) ALC Control 2	7	ALCZC	0 (zero cross off)	ALC uses zero cross detection circuit.
	3:0	HLD [3:0]	0000 (0ms)	ALC hold time before gain is increased. 0000 = 0ms 0001 = 2.67ms 0010 = 5.33ms … (time doubles with every step) 1111 = 43.7s
R19 (13h) ALC Control 3	7:4	DCY [3:0]	0011 (192ms)	ALC decay (gain ramp-up) time 0000 = 24ms 0001 = 48ms 0010 = 96ms … (time doubles with every step) 1010 or higher = 24.58s
	3:0	ATK [3:0]	0010 (24ms)	ALC attack (gain ramp-down) time 0000 = 6ms 0001 = 12ms 0010 = 24ms … (time doubles with every step) 1010 or higher = 6.14s

Table 13 ALC Control

PEAK LIMITER

To prevent clipping when a large signal occurs just after a period of quiet, the ALC circuit includes a limiter function. If the ADC input signal exceeds 87.5% of full scale (–1.16dB), the PGA gain is ramped down at the maximum attack rate (as when ATK = 0000), until the signal level falls below 87.5% of full scale. This function is automatically enabled whenever the ALC is enabled.

Note:

If ATK = 0000, then the limiter makes no difference to the operation of the ALC. It is designed to prevent clipping when long attack times are used.

NOISE GATE

When the signal is very quiet and consists mainly of noise, the ALC function may cause "noise pumping", i.e. loud hissing noise during silence periods. The WM8988 has a noise gate function that prevents noise pumping by comparing the signal level at the LINPUT1/2 and/or RINPUT1/2 pins against a noise gate threshold, NGTH. The noise gate cuts in when:

- Signal level at ADC [dB] < NGTH [dB] + PGA gain [dB] + Mic Boost gain [dB]

This is equivalent to:

- Signal level at input pin [dB] < NGTH [dB]

The ADC output can then either be muted or alternatively, the PGA gain can be held constant (preventing it from ramping up as it normally would when the signal is quiet).

The table below summarises the noise gate control register. The NGTH control bits set the noise gate threshold with respect to the ADC full-scale range. The threshold is adjusted in 1.5dB steps. Levels at the extremes of the range may cause inappropriate operation, so care should be taken with set–up of the function. Note that the noise gate only works in conjunction with the ALC function, and always operates on the same channel(s) as the ALC (left, right, both, or none).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R20 (14h) Noise Gate Control	7:3	NGTH [4:0]	00000	Noise gate threshold 13 -76.5dBfs 13 -75dBfs … 1.5 dB steps 11110 -31.5dBfs 11111 -30dBfs
	2:1	NGG [1:0]	00	Noise gate type X0 = PGA gain held constant 01 = mute ADC output 11 = reserved (do not use this setting)
	0	NGAT	0	Noise gate function enable 1 = enable 0 = disable

Table 14 Noise Gate Control

Note:

The performance of the ADC may degrade at high input signal levels if the monitor bypass mux is selected with MIC boost and ALC enabled.