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WM8998

High Performance Audio Hub CODEC

DESCRIPTION

The WM8998 is a highly-integrated low-power audio hub CODEC for smartphones, tablets and other portable audio devices. It is optimised for use in multimedia devices where the audio processing requirements are implemented on the host applications processor.

The WM8998 digital core combines fixed-function signal processing blocks with a fully-flexible, all-digital audio mixing and routing engine, for extensive use-case flexibility. Signal processing blocks include filters, EQ, dynamics processors and sample rate converters.

A SLIMbus® interface supports multi-channel audio paths and host control register access. Multiple sample rates are supported concurrently via the SLIMbus interface. Three further digital audio interfaces are provided, each supporting a wide range of standard audio sample rates and serial interface formats. Automatic sample rate detection enables seamless wideband/narrowband voice call handover.

The stereo headphone driver provides ground-referenced outputs, with noise levels as low as $1\mu V_{RMS}$ for hi-fi quality line or headphone output. The CODEC also features a stereo line output, stereo 2W Class-D speaker outputs, a dedicated BTL earpiece output, PDM for external speaker amplifiers, and an IEC-60958-3 compatible S/PDIF transmitter. A signal generator for controlling haptics devices is included; vibe actuators can connect directly to the Class-D speaker output, or via an external driver on the PDM output interface. All inputs, outputs and system interfaces can function concurrently.

The WM8998 supports up to six analogue mic/line inputs, and up to three PDM digital inputs. The input multiplexers support up to three signal paths. Microphone activity detection with interrupt is available. A smart accessory interface supports most standard 3.5mm accessories. Impedance sensing and measurement is provided for external accessory and push-button detection.

The WM8998 power, clocking and output driver architectures are all designed to maximise battery life in voice, music and standby modes. Low-power 'Sleep' is supported, with configurable wake-up events. The WM8998 is powered from a 1.8V external supply. A separate supply is required for the Class D speaker drivers (typically direct connection to 4.2V battery).

Two integrated FLLs provide support for a wide range of system clock frequencies. The WM8998 is configured using the I2C or SLIMbus interfaces. The fully-differential internal analogue architecture, minimal analogue signal paths and on-chip RF noise filters ensure a very high degree of noise immunity.

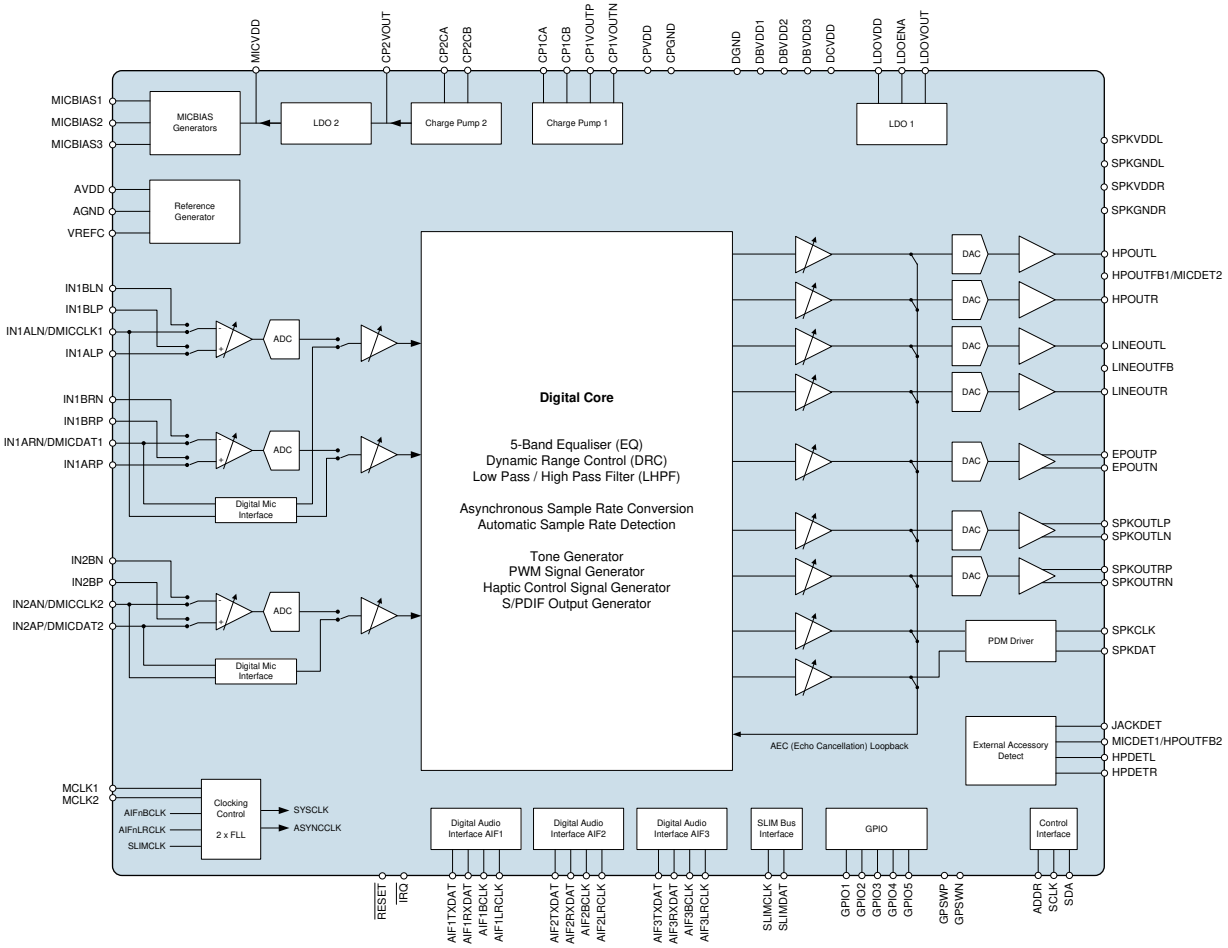
FEATURES

- Hi-Fi audio hub CODEC for mobile applications
- Digital audio processing core
  - Fully flexible digital signal routing and mixing
  - Wind noise, sidetone and other programmable filters
  - Dynamic Range Control (compressor, limiter)
  - Fully parametric EQs
  - Low-pass / High-pass filters
- Multi-channel asynchronous sample rate conversion
- Integrated multi-channel 24-bit hi-fi audio hub CODEC
  - 3 ADCs, 96dB SNR microphone input (48kHz)
  - 7 DACs, 122dB SNR headphone playback (48kHz)
- Audio inputs
  - Up to 6 analogue or 3 digital microphone inputs
  - Single-ended or differential mic/line inputs
- Stereo headphone output driver
  - 28mW into 32Ω load at 0.1% THD+N
  - 6.9mW typical headphone playback power consumption
  - Pop suppression functions
  - $1\mu V_{RMS}$ noise floor (A-weighted)
- Ground-referenced line output driver
  - Stereo single-ended or Mono differential configuration
- Mono BTL earpiece output driver
  - 100mW into 32Ω BTL load at 5% THD+N
- Stereo (2 x 2W) Class D speaker output drivers
  - Direct drive of external haptics vibe actuators
- Two-channel digital speaker (PDM) output interface
- IEC-60958-3 compatible S/PDIF transmitter
- SLIMbus audio and control interface
- 3 full digital audio interfaces
  - Standard sample rates from 8kHz up to 192kHz
  - TDM support on all AIFs
  - 6 channel input and output on AIF1 and AIF2
- Flexible clocking, derived from MCLKn, BCLKn or SLIMbus
- 2 low-power FLLs support reference clocks down to 32kHz
- Advanced accessory detection functions
  - Low-power standby mode and configurable wake-up
- Configurable functions on 5 GPIO pins
- Integrated LDO regulators and charge pumps
- Support for single 1.8V supply operation
- Small W-CSP package, 0.4mm pitch

APPLICATIONS

- Smartphones and Multimedia handsets
- Tablets and Mobile Internet Devices (MID)

BLOCK DIAGRAM



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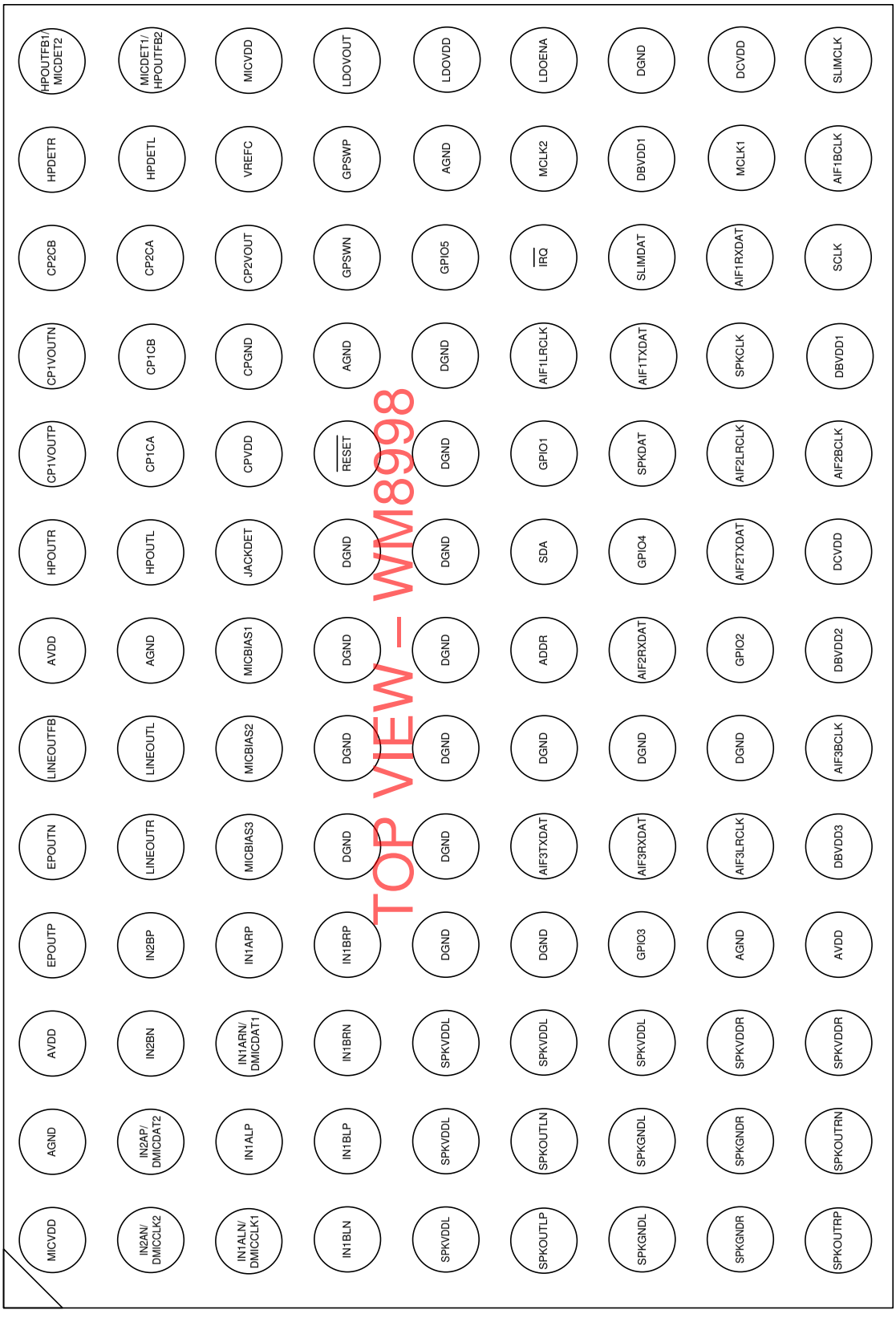
PIN CONFIGURATION



ORDERING INFORMATION

ORDER CODE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8998ECS/R	-40°C to +85°C	W-CSP (Pb-free, Tape and reel)	MSL1	260°C

Note:
Reel quantity = 7000

PIN DESCRIPTION

A description of each pin on the WM8998 is provided below.
Note that a table detailing the associated power domain for every digital input / digital output pin is provided on the following page.
Note that, where multiple pins share a common name, these pins should be tied together on the PCB.
All Digital Output pins are CMOS outputs, unless otherwise stated.

PIN NO	NAME	TYPE	DESCRIPTION
F7	ADDR	Digital Input	Control interface (I2C) address select
A2, B7, D10, E12, H4	AGND	Supply	Analogue ground (Return path for AVDD)
J12	AIF1BCLK	Digital Input / Output	Audio interface 1 bit clock
F10	AIF1LRCLK	Digital Input / Output	Audio interface 1 left / right clock
H11	AIF1RXDAT	Digital Input	Audio interface 1 RX digital audio data
G10	AIF1TXDAT	Digital Output	Audio interface 1 TX digital audio data
J9	AIF2BCLK	Digital Input / Output	Audio interface 2 bit clock
H9	AIF2LRCLK	Digital Input / Output	Audio interface 2 left / right clock
G7	AIF2RXDAT	Digital Input	Audio interface 2 RX digital audio data
H8	AIF2TXDAT	Digital Output	Audio interface 2 TX digital audio data
J6	AIF3BCLK	Digital Input / Output	Audio interface 3 bit clock
H5	AIF3LRCLK	Digital Input / Output	Audio interface 3 left / right clock
G5	AIF3RXDAT	Digital Input	Audio interface 3 RXdigital audio data
F5	AIF3TXDAT	Digital Output	Audio interface 3 TX digital audio data
A3, A7, J4	AVDD	Supply	Analogue supply
B9	CP1CA	Analogue Output	Charge pump 1 fly-back capacitor pin
B10	CP1CB	Analogue Output	Charge pump 1 fly-back capacitor pin
A10	CP1VOUTN	Analogue Output	Charge pump 1 negative output decoupling pin
A9	CP1VOUTP	Analogue Output	Charge pump 1 positive output decoupling pin
B11	CP2CA	Analogue Output	Charge pump 2 fly-back capacitor pin
A11	CP2CB	Analogue Output	Charge pump 2 fly-back capacitor pin
C11	CP2VOUT	Analogue Output	Charge pump 2 output decoupling pin / Supply for LDO2
C10	CPGND	Supply	Charge pump 1 & 2 ground (Return path for CPVDD)
C9	CPVDD	Supply	Supply for Charge Pump 1 & 2
G12, J10	DBVDD1	Supply	Digital buffer (I/O) supply (core functions and Audio Interface 1)
J7	DBVDD2	Supply	Digital buffer (I/O) supply (for Audio Interface 2, GPIO2, GPIO4)
J5	DBVDD3	Supply	Digital buffer (I/O) supply (for Audio Interface 3, GPIO3)
H13, J8	DCVDD	Supply	Digital core supply
D5, D6, D7, D8, E4, E5, E6, E7, E8, E9, E10, F4, F6, G6, G13, H6	DGND	Supply	Digital ground (Return path for DCVDD, DBVDD1, DBVDD2 and DBVDD3)
A5	EPOUTN	Analogue Output	Earpiece negative output
A4	EPOUTP	Analogue Output	Earpiece positive output

PIN NO	NAME	TYPE	DESCRIPTION
F9	GPIO1	Digital Input / Output	General Purpose pin GPIO1. The output configuration is selectable CMOS or Open Drain.
H7	GPIO2	Digital Input / Output	General Purpose pin GPIO2. The output configuration is selectable CMOS or Open Drain.
G4	GPIO3	Digital Input / Output	General Purpose pin GPIO3. The output configuration is selectable CMOS or Open Drain.
G8	GPIO4	Digital Input / Output	General Purpose pin GPIO4. The output configuration is selectable CMOS or Open Drain.
E11	GPIO5	Digital Input / Output	General Purpose pin GPIO5. The output configuration is selectable CMOS or Open Drain.
D11	GPSWN	Analogue Output	General Purpose analogue switch contact (negative)
D12	GPSWP	Analogue Input	General Purpose analogue switch contact (positive)
B12	HPDETL	Analogue Input	Headphone left (HPOUTL) sense input
A12	HPDETR	Analogue Input	Headphone right (HPOUTR) sense input
A13	HPOUTFB1/ MICDET2	Analogue Input	HPOUTL and HPOUTR ground feedback pin 1/ Microphone & accessory sense input 2
B8	HPOUTL	Analogue Output	Left headphone output
A8	HPOUTR	Analogue Output	Right headphone output
C1	IN1ALN/ DMICCLK1	Analogue Input / Digital Output	Left channel negative differential Mic/Line input / Digital MIC clock output 1
C2	IN1ALP	Analogue Input	Left channel single-ended Mic/Line input / Left channel positive differential Mic/Line input
C3	IN1ARN/ DMICDAT1	Analogue input / Digital Input	Right channel negative differential Mic/Line input / Digital MIC data input 1
C4	IN1ARP	Analogue Input	Right channel single-ended Mic/Line input / Right channel positive differential Mic/Line input
B1	IN2AN/ DMICCLK2	Analogue Input / Digital Output	Negative differential Mic/Line input / Digital MIC clock output 2
B2	IN2AP/ DMICDAT2	Analogue Input / Digital Input	Single-ended Mic/Line input / Positive differential Mic/Line input/ Digital MIC data input 2
D1	IN1BLN	Analogue Input	Left channel negative differential Mic/Line input
D2	IN1BLP	Analogue Input	Left channel single-ended Mic/Line input / Left channel positive differential Mic/Line input
D3	IN1BRN	Analogue input	Right channel negative differential Mic/Line input
D4	IN1BRP	Analogue Input	Right channel single-ended Mic/Line input / Right channel positive differential Mic/Line input
B3	IN2BN	Analogue Input	Negative differential Mic/Line input
B4	IN2BP	Analogue Input	Single-ended Mic/Line input / Positive differential Mic/Line input
F11	$\overline{\text{IRQ}}$	Digital Output	Interrupt Request ($\overline{\text{IRQ}}$) output (default is active low). The pin configuration is selectable CMOS or Open Drain.
C8	JACKDET	Analogue Input	Jack detect input
F13	LDOENA	Digital Input	Enable pin for LDO1 (generates DCVDD supply). Logic 1 input enables LDO1. If using external DCVDD supply, then LDO1 is not used, and LDOENA must be held at logic 0.
E13	LDOVDD	Supply	Supply for LDO1
D13	LDOVOUT	Analogue Output	LDO1 output. If using external DCVDD, then LDOVOUT must be left floating.
A6	LINEOUTFB	Analogue Input	LINEOUTL and LINEOUTR ground loop noise rejection feedback
B6	LINEOUTL	Analogue Output	Left line output
B5	LINEOUTR	Analogue Output	Right line output
H12	MCLK1	Digital Input	Master clock 1
F12	MCLK2	Digital Input	Master clock 2
C7	MICBIAS1	Analogue Output	Microphone bias 1

PIN NO	NAME	TYPE	DESCRIPTION
C6	MICBIAS2	Analogue Output	Microphone bias 2
C5	MICBIAS3	Analogue Output	Microphone bias 3
B13	MICDET1/ HPOUTFB2	Analogue Input	Microphone & accessory sense input 1/ HPOUTL and HPOUTR ground feedback pin 2
A1, C13	MICVDD	Analogue Output	LDO2 output decoupling pin (generated internally by WM8998). (Can also be used as reference/supply for external microphones.)
D9	RESET	Digital Input	Digital Reset input (active low)
J11	SCLK	Digital Input	Control interface (I2C) clock input
F8	SDA	Digital Input / Output	Control interface (I2C) data input and output The output function is implemented as an Open Drain circuit.
J13	SLIMCLK	Digital Input	SLIMBus Clock input
G11	SLIMDAT	Digital Input / Output	SLIMBus Data input / output
H10	SPKCLK	Digital Output	Digital speaker (PDM) clock output
G9	SPKDAT	Digital Output	Digital speaker (PDM) data output
G1, G2	SPKGNDL	Supply	Left speaker driver ground (Return path for SPKVDDL)
H1, H2	SPKGNDR	Supply	Right speaker driver ground (Return path for SPKVDDR)
F2	SPKOUTLN	Analogue Output	Left speaker negative output
F1	SPKOUTLP	Analogue Output	Left speaker positive output
J2	SPKOUTRN	Analogue Output	Right speaker negative output
J1	SPKOUTRP	Analogue Output	Right speaker positive output
E1, E2, E3, F3, G3	SPKVDDL	Supply	Left speaker driver supply
H3, J3	SPKVDDR	Supply	Right speaker driver supply
C12	VREFC	Analogue Output	Bandgap reference decoupling capacitor connection

The following table identifies the power domain and ground reference associated with each of the input / output pins.

PIN NO	NAME	POWER DOMAIN	GROUND DOMAIN
F7	ADDR	DBVDD1	DGND
J12	AIF1BCLK	DBVDD1	DGND
F10	AIF1LRCLK	DBVDD1	DGND
H11	AIF1RXDAT	DBVDD1	DGND
G10	AIF1TXDAT	DBVDD1	DGND
J9	AIF2BCLK	DBVDD2	DGND
H9	AIF2LRCLK	DBVDD2	DGND
G7	AIF2RXDAT	DBVDD2	DGND
H8	AIF2TXDAT	DBVDD2	DGND
J6	AIF3BCLK	DBVDD3	DGND
H5	AIF3LRCLK	DBVDD3	DGND
G5	AIF3RXDAT	DBVDD3	DGND
F5	AIF3TXDAT	DBVDD3	DGND
F9	GPIO1	DBVDD1	DGND
H7	GPIO2	DBVDD2	DGND
G4	GPIO3	DBVDD3	DGND
G8	GPIO4	DBVDD2	DGND
E11	GPIO5	DBVDD1	DGND
C1	IN1ALN/ DMICCLK1	(when DMICCLK1 function is selected): MICVDD, MICBIAS1, MICBIAS2 or MICBIAS3 The DMICCLK1 power domain is selectable using IN1_DMIC_SUP	AGND
C3	IN1ARN/ DMICDAT1	(when DMICDAT1 function is selected): MICVDD, MICBIAS1, MICBIAS2 or MICBIAS3 The DMICDAT1 power domain is selectable using IN1_DMIC_SUP	AGND
B1	IN2AN/ DMICCLK2	(when DMICCLK2 function is selected): MICVDD, MICBIAS1, MICBIAS2 or MICBIAS3 The DMICCLK2 power domain is selectable using IN2_DMIC_SUP	AGND
B2	IN2AP/ DMICDAT2	(when DMICDAT2 function is selected): MICVDD, MICBIAS1, MICBIAS2 or MICBIAS3 The DMICDAT2 power domain is selectable using IN2_DMIC_SUP	AGND
F11	$\overline{\text{IRQ}}$	DBVDD1	DGND
F13	LDOENA	DBVDD1	DGND
H12	MCLK1	DBVDD1	DGND
F12	MCLK2	DBVDD1	DGND
D9	$\overline{\text{RESET}}$	DBVDD1	DGND
J11	SCLK	DBVDD1	DGND
F8	SDA	DBVDD1	DGND
J13	SLIMCLK	DBVDD1	DGND
G11	SLIMDAT	DBVDD1	DGND
H10	SPKCLK	DBVDD1	DGND
G9	SPKDAT	DBVDD1	DGND

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus tests its package types according to IPC/JEDEC J-STD-020 for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Supply voltages (LDOVDD, AVDD, DCVDD, CPVDD)	-0.3V	+2.0V
Supply voltages (DBVDD1, DBVDD2, DBVDD3)	-0.3V	+4.0V
Supply voltages (SPKVDDL, SPKVDDR)	-0.3V	+6.0V
Voltage range digital inputs (DBVDD1 domain)	AGND - 0.3V	DBVDD1 + 0.3V
Voltage range digital inputs (DBVDD2 domain)	AGND - 0.3V	DBVDD2 + 0.3V
Voltage range digital inputs (DBVDD3 domain)	AGND - 0.3V	DBVDD3 + 0.3V
Voltage range digital inputs (DMICDATn)	AGND - 0.3V	MICVDD + 0.3V
Voltage range analogue inputs (IN1A*, IN1B*, IN2A*, MICDETn, HPOUTFBn, LINEOUTFB)	AGND - 0.3V	MICVDD + 0.3V
Voltage range analogue inputs (IN2B*)	AGND - 3.3V	MICVDD + 0.3V
Voltage range analogue inputs (JACKDET, HPDETL, HPDETR)	CP1VOUTN - 0.3V	AVDD + 0.3V
Voltage range analogue inputs (GPSWP, GPSWN)	AGND - 0.3V	MICVDD + 0.3V
Ground (DGND, CPGND, SPKGNDL, SPKGNDR)	AGND - 0.3V	AGND + 0.3V
Operating temperature range, T_A	-40ºC	+85ºC
Operating junction temperature, T_J	-40ºC	+125ºC
Storage temperature after soldering	-65ºC	+150ºC

Notes:

1. DCVDD must not be powered if AVDD is not present.
2. CP1VOUT2N is an internal supply, generated by the WM8998 Charge Pump (CP1). The CP1VOUT2N voltage may vary between AGND and -CPVDD.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Digital supply range (Core) See notes 2, 3, 4, 5	DCVDD (≤24.576MHz clocking)	1.14	1.2	1.9	V
	DCVDD (>24.576MHz clocking)	1.71	1.8	1.9	
Digital supply range (I/O)	DBVDD1	1.7		1.9	V
Digital supply range (I/O)	DBVDD2, DBVDD3	1.7		3.47	V
LDO supply range	LDOVDD	1.7	1.8	1.9	V
Charge Pump supply range	CPVDD	1.7	1.8	1.9	V
Speaker supply range	SPKVDDL, SPKVDDR	2.4		5.5	V
Analogue supply range See note 2	AVDD	1.7	1.8	1.9	V
Ground See note 1	DGND, AGND, CPGND, SPKGNDL, SPKGNDR		0		V
Power supply rise time See notes 7, 8, 9, 10	DCVDD	10		2000	µs
	All other supplies	1			
Operating temperature range	T_A	-40		85	°C

Notes:

3. The grounds must always be within 0.3V of AGND.
4. AVDD must be supplied before DCVDD. DCVDD must not be powered if AVDD is not present. There are no other power sequencing requirements.
5. An internal LDO (powered by LDOVDD) can be used to provide the DCVDD supply.
6. 'Sleep' mode is supported when DCVDD is below the limits noted, provided AVDD and DBVDD1 are present.
7. Under default conditions, digital core clocking rates above 24.576MHz are inhibited. The register-controlled clocking limit should only be raised when the applicable DCVDD voltage is present.
8. An internal Charge Pump and LDO (powered by CPVDD) provide the microphone bias supply; the MICVDD pin should not be connected to an external supply.
9. DCVDD minimum rise time does not apply when this is powered using the internal LDO.
10. If DCVDD is supplied externally, and the rise time exceeds 2ms, then $\overline{\text{RESET}}$ must be asserted (low) during the rise, and held asserted until after DCVDD is within the recommended operating limits.
11. The specified minimum power supply rise times assume a minimum decoupling capacitance of 100nF per pin. However, Cirrus strongly advises that the recommended decoupling capacitors are present on the PCB and that appropriate layout guidelines are observed.
12. The specified minimum power supply rise times also assume a maximum PCB inductance of 10nH between decoupling capacitor and pin.

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = 1.8V,

With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Input Signal Level (IN1AL, IN1AR, IN1BL, IN1BR, IN2A, IN2B)						
Full-scale input signal level (0dBFS output)	V_{INFS}	Single-ended PGA input, 6dB PGA gain		0.5 -6		V_{RMS} dBV
		Differential PGA input, 0dB PGA gain		1 0		V_{RMS} dBV

Notes:

1. The full-scale input signal level is also the maximum analogue input level, before clipping occurs.
2. The full-scale input signal level changes in proportion with AVDD. For differential input, it is calculated as AVDD / 1.8.
3. A $1.0V_{RMS}$ differential signal equates to $0.5V_{RMS}$/-6dBV per input.
4. A sinusoidal input signal is assumed.

Test Conditions

T_A = +25°C

With the exception of the condition(s) noted above, the following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Input Pin Characteristics (IN1AL, IN1AR, IN1BL, IN1BR, IN2A, IN2B)						
Input resistance	R_{IN}	Differential input, All PGA gain settings		24		kΩ
		Single-ended input, 0dB PGA gain		16		
Input capacitance	C_{IN}				5	pF

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Programmable Gain Amplifiers (PGAs)						
Minimum programmable gain				0		dB
Maximum programmable gain				31		dB
Programmable gain step size		Guaranteed monotonic		1		dB

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Microphone Input Signal Level (DMICDAT1, DMICDAT2)						
Full-scale input signal level (0dBFS signal to digital core)		0dB gain		-6		dBFS

Note:

The digital microphone input signal level is measured in dBFS, where 0dBFS is a signal level equal to the full-scale range (FSR) of the PDM input. The FSR is defined as the amplitude of a 1kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively - this is the largest 1kHz sine wave that will fit in the digital output range without clipping.

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Headphone Output Driver (HPOUTL, HPOUTR)						
Load resistance, Single-ended output mode		Charge Pump Normal mode (default)	15			Ω
		Charge Pump Low Impedance mode	6			
Load resistance, Differential (BTL) output mode		Charge Pump Normal mode (default)	30			Ω
		Charge Pump Low Impedance mode	15			
Load resistance		Device survival with load applied indefinitely	0.1			Ω
Load capacitance		Direct connection, Single-ended mode			500	pF
		Direct connection, Differential (BTL) mode			250	
		Connection via 16Ω series resistor			2	nF
DC offset at Load		Single-ended mode		0.1		mV
		Differential (BTL) mode		0.2		
Note - to support HPOUT loads less than 15Ω, (or less than 30Ω BTL), the Charge Pump (CP1) must be configured for low impedance operation, as described in the “Output Signal Path” section.						
Line Output Driver (LINEOUTL, LINEOUTR)						
Load resistance		Normal operation	600			Ω
		Device survival with load applied indefinitely	0.1			
Load capacitance		Direct connection, Single-ended mode			500	pF
		Direct connection, Differential (BTL) mode			250	
		Connection via 16Ω series resistor			2	nF
DC offset at Load		Single-ended mode		0.1		mV
		Differential (BTL) mode		0.2		
Earpiece Output Driver (EPOUTP+EPOUTN)						
Load resistance		Charge Pump Normal mode (default)	30			Ω
		Charge Pump Low Impedance mode	15			
		Device survival with load applied indefinitely	0.1			
Load capacitance		Direct connection (BTL)			250	pF
		Connection via 16Ω series resistor			2	nF
DC offset at Load				0.1		mV
Note - to support EPOUT loads less than 30Ω, the Charge Pump (CP1) must be configured for low impedance operation, as described in the “Output Signal Path” section.						

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Speaker Output Driver (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN)						
Load resistance		Normal operation	4			Ω
		Device survival with load applied indefinitely	0			
Load capacitance					200	pF
DC offset at Load				5		mV
SPKVDD leakage current				1		µA
Digital Speaker Output (SPKDAT)						
Full-scale output level (0dBFS digital core output)		0dB gain		-6		dBFS

Note:

The digital output signal level is measured in dBFS, where 0dBFS is a signal level equal to the full-scale range (FSR) of the PDM output. The FSR is defined as the amplitude of a 1kHz sine wave whose positive and negative peaks are represented by the maximum and minimum digital codes respectively - this is the largest 1kHz sine wave that will fit in the digital output range without clipping.

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Input Paths (IN1AL, IN1AR, IN1BL, IN1BR, IN2A, IN2B) to ADC (Differential Input Mode, INn_SRC = x0)						
Signal to Noise Ratio (A-weighted)	SNR	High performance mode (INn_OSR = 1)	87	96		dB
		Normal mode (INn_OSR = 0)		93		
Total Harmonic Distortion	THD	-1dBV input		-90		dB
Total Harmonic Distortion Plus Noise	THD+N	-1dBV input		-88	-79	dB
Channel separation (Left/Right)				100		dB
Input noise floor		A-weighted, PGA gain = +18dB		3.2		μV_{RMS}
Common mode rejection ratio	CMRR	PGA gain = +30dB		65		dB
		PGA gain = 0dB		70		
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		70		dB
		100mV(peak-peak) 10kHz		65		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		95		dB
		100mV(peak-peak) 10kHz		95		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Input Paths (IN1AL, IN1AR, IN1BL, IN1BR, IN2A, IN2B) to ADC (Single-Ended Input Mode, INn_SRC = x1) PGA Gain = +6dB unless otherwise stated.						
Signal to Noise Ratio (A-weighted)	SNR	High performance mode (INn_OSR = 1)	86	94		dB
		Normal mode (INn_OSR = 0)		92		
Total Harmonic Distortion	THD	-7dBV input		-82		dB
Total Harmonic Distortion Plus Noise	THD+N	-7dBV input		-81	-71	dB
Channel separation (Left/Right)				100		dB
Input noise floor		A-weighted, PGA gain = +18dB		4.6		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		70		dB
		100mV(peak-peak) 10kHz		50		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		85		dB
		100mV(peak-peak) 10kHz		70		
DAC to Headphone Output (HPOUTL, HPOUTR; R_L = 32Ω)						
Maximum output power	P_O	0.1% THD+N		28		mW
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1Vrms		122		dB
Total Harmonic Distortion	THD	P_O = 20mW		-86		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 20mW		-84		dB
Total Harmonic Distortion	THD	P_O = 5mW		-89		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 5mW		-85		dB
Channel separation (Left/Right)		P_O = 20mW		110		dB
Output noise floor		A-weighted		1		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		115		dB
		100mV (peak-peak) 10kHz		80		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		115		dB
		100mV(peak-peak) 10kHz		80		
DAC to Headphone Output (HPOUTL, HPOUTR; R_L = 16Ω)						
Maximum output power	P_O	0.1% THD+N		34		mW
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1Vrms	114	122		dB
Total Harmonic Distortion	THD	P_O = 20mW		-78		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 20mW		-76		dB
Total Harmonic Distortion	THD	P_O = 5mW		-78		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 5mW		-77	-67	dB
Channel separation (Left/Right)		P_O = 20mW		110		dB
Output noise floor		A-weighted		1	2	μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		115		dB
		100mV (peak-peak) 10kHz		80		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		115		dB
		100mV(peak-peak) 10kHz		80		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Line Output (HPOUTL, HPOUTR; Load = 10kΩ, 50pF)						
Full-scale output signal level	V_{OUT}	0dBFS input	1 0			Vrms dBV
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1Vrms	114	122		dB
Total Harmonic Distortion	THD	0dBFS input		-89		dB
Total Harmonic Distortion Plus Noise	THD+N	0dBFS input		-88	-73	dB
Channel separation (Left/Right)				110		dB
Output noise floor		A-weighted		1	2	μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		115		dB
		100mV (peak-peak) 10kHz		80		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		115		dB
		100mV(peak-peak) 10kHz		80		
DAC to Line Output (LINEOUTL, LINEOUTR; Load = 10kΩ, 50pF)						
Full-scale output signal level	V_{OUT}	0dBFS input	1 0			Vrms dBV
Signal to Noise Ratio	SNR	A-weighted, Output signal = 1Vrms	114	122		dB
Total Harmonic Distortion	THD	0dBFS input		-90		dB
Total Harmonic Distortion Plus Noise	THD+N	0dBFS input		-89	-73	dB
Channel separation (Left/Right)				110		dB
Output noise floor		A-weighted		1	2	μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		127		dB
		100mV (peak-peak) 10kHz		90		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		130		dB
		100mV(peak-peak) 10kHz		85		
DAC to Earpiece Output (EPOUTP+EPOUTN, R_L = 32Ω BTL)						
Maximum output power	P_O	0.1% THD+N		83		mW
		5% THD+N		100		
Signal to Noise Ratio	SNR	A-weighted, Output signal = 2Vrms	118	127		dB
Total Harmonic Distortion	THD	P_O = 50mW		-92		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 50mW		-90		dB
Total Harmonic Distortion	THD	P_O = 5mW		-85		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 5mW		-83	-73	dB
Output noise floor		A-weighted		1	2.5	μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		113		dB
		100mV (peak-peak) 10kHz		115		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		130		dB
		100mV(peak-peak) 10kHz		100		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Earpiece Output (EPOUTP+EPOUTN, R_L = 16Ω BTL)						
Maximum output power	P_O	0.1% THD+N		83		mW
		10% THD+N		110		
Signal to Noise Ratio	SNR	A-weighted, Output signal = 2Vrms		127		dB
Total Harmonic Distortion	THD	P_O = 50mW		-92		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 50mW		-90		dB
Total Harmonic Distortion	THD	P_O = 5mW		-90		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 5mW		-88		dB
Output noise floor		A-weighted		1		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		113		dB
		100mV (peak-peak) 10kHz		115		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		130		dB
		100mV(peak-peak) 10kHz		100		
DAC to Speaker Output (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN, Load = 8Ω, 22µH, BTL) High Performance mode (OUT4_OSR=1)						
Maximum output power	P_O	SPKVDD = 5.0V, 1% THD+N		1.37		W
		SPKVDD = 4.2V, 1% THD+N		0.97		
		SPKVDD = 3.6V, 1% THD+N		0.71		
Signal to Noise Ratio	SNR	A-weighted, Output signal = 3Vrms	90	100		dB
Total Harmonic Distortion	THD	P_O = 0.7W		-74		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 0.7W		-73		dB
Total Harmonic Distortion	THD	P_O = 0.5W		-74		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 0.5W		-73	-57	dB
Channel separation (Left/Right)		P_O = 0.5W		95		dB
Output noise floor		A-weighted		30	95	μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		80		dB
		100mV (peak-peak) 10kHz		70		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		70		dB
		100mV (peak-peak) 10kHz		70		

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Speaker Output (SPKOUTLP+SPKOUTLN, SPKOUTRP+SPKOUTRN, Load = 4Ω, 15µH, BTL) High Performance mode (OUT4_OSR=1)						
Maximum output power	P_O	SPKVDD = 5.0V, 1% THD+N		2.4		W
		SPKVDD = 4.2V, 1% THD+N		1.69		
		SPKVDD = 3.6V, 1% THD+N		1.24		
Signal to Noise Ratio	SNR	A-weighted, Output signal = 3Vrms		100		dB
Total Harmonic Distortion	THD	P_O = 1.0W		-61		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 1.0W		-60		dB
Total Harmonic Distortion	THD	P_O = 0.5W		-64		dB
Total Harmonic Distortion Plus Noise	THD+N	P_O = 0.5W		-63		dB
Channel separation (Left/Right)		P_O = 0.5W		85		dB
Output noise floor		A-weighted		30		μV_{RMS}
PSRR (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		80		dB
		100mV (peak-peak) 10kHz		70		
PSRR (SPKVDDL, SPKVDDR)	PSRR	100mV (peak-peak) 217Hz		70		dB
		100mV (peak-peak) 10kHz		70		

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Input / Output (except DMICDATn and DMICCLKn) **Digital I/O is referenced to DBVDD1, DBVDD2 or DBVDD3. See "Pin Description" for the domain applicable to each pin.** **See "Recommended Operating Conditions" for the valid operating voltage range of each DBVDDn domain.**						
Input HIGH Level	V_{IH}	V_{DBVDDn} =1.8V ±10%	0.65 × V_{DBVDDn}			V
		V_{DBVDDn} =3.3V ±10%	0.7 × V_{DBVDDn}			
Input LOW Level	V_{IL}	V_{DBVDDn} =1.8V ±10%			0.35 × V_{DBVDDn}	V
		V_{DBVDDn} =3.3V ±10%			0.3 × V_{DBVDDn}	
Note that digital input pins should not be left unconnected or floating.						
Output HIGH Level	V_{OH}	I_{OH} = 1mA	0.9 × V_{DBVDDn}			V
Output LOW Level	V_{OL}	I_{OL} = -1mA			0.1 × V_{DBVDDn}	V
Input capacitance				10		pF
Input leakage			-1		1	µA
Pull-up resistance (where applicable)			42	49	56	kΩ
Pull-down resistance (where applicable)			80	105	130	kΩ
Digital Microphone Input / Output (DMICDATn and DMICCLKn) **DMICDATn and DMICCLKn are each referenced to a selectable supply, V_{SUP}, according to the INn_DMIC_SUP registers**						
DMICDATn input HIGH Level	V_{IH}		0.65 × V_{SUP}			V
DMICDATn input LOW Level	V_{IL}				0.35 × V_{SUP}	V
DMICCLKn output HIGH Level	V_{OH}	I_{OH} = 1mA	0.8 × V_{SUP}			V
DMICCLKn output LOW Level	V_{OL}	I_{OL} = -1mA			0.2 × V_{SUP}	V
Input capacitance				10		pF
Input leakage			-1		1	µA
SLIMbus Digital Input / Output (SLIMCLK and SLIMDAT) **1.8V I/O Signalling (ie. 1.65V ≤ DBVDD1 ≤1.95V)**						
Input HIGH Level	V_{IH}		0.65 × V_{DBVDD1}			V
Input LOW Level	V_{IL}				0.35 × V_{DBVDD1}	V
Output HIGH Level	V_{OH}	I_{OH} = 1mA	0.9 × V_{DBVDD1}			V
Output LOW Level	V_{OL}	I_{OL} = -1mA			0.1 × V_{DBVDD1}	V
Pin capacitance					5	pF
General Purpose Input / Output (GPIOn)						
Clock output frequency		GPIO pin configured as OPCLK or FLL output			26.5	MHz
General Purpose Switch The GPSWP pin should be positive-biased with respect to GPSWN. The GPSWN pin voltage must not exceed GPSWP + 0.3V.						
Switch resistance	$R_{DS(ON)}$	Switch closed, I=1mA		40		Ω
Switch resistance	$R_{DS(OFF)}$	Switch open		100		MΩ

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Microphone Bias (MICBIAS1, MICBIAS2, MICBIAS3) Note - No capacitor on MICBIASn Note - In regulator mode, it is required that V_{MICVDD} - $V_{MICBIASn}$ > 200mV						
Minimum Bias Voltage	$V_{MICBIAS}$	Regulator mode (MICBn_BYPASS=0) Load current ≤ 1.0mA		1.5		V
Maximum Bias Voltage				2.8		V
Bias Voltage output step size				0.1		V
Bias Voltage accuracy			-5%		+5%	V
Bias Current		Regulator mode (MICBn_BYPASS=0), V_{MICVDD} - $V_{MICBIAS}$ >200mV			2.4	mA
		Bypass mode (MICBn_BYPASS=1)			5.0	
Output Noise Density		Regulator mode (MICBn_BYPASS=0), MICBn_LVL = 4h, Load current = 1mA, Measured at 1kHz		50		nV/√Hz
Integrated noise voltage		Regulator mode (MICBn_BYPASS=0), MICBn_LVL = 4h, Load current = 1mA, 100Hz to 7kHz, A-weighted		4		µVrms
Power Supply Rejection Ratio (DBVDDn, LDOVDD, CPVDD, AVDD)	PSRR	100mV (peak-peak) 217Hz		95		dB
		100mV (peak-peak) 10kHz		65		
Load capacitance		Regulator mode (MICBn_BYPASS=0), MICBn_EXT_CAP=0			50	pF
		Regulator mode (MICBn_BYPASS=0), MICBn_EXT_CAP=1	1.8	4.7		µF
Output discharge resistance		MICBn_ENA=0, MICBn_DISCH=1		5		kΩ

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
External Accessory Detect						
Load impedance detection range Detection via HPDETL pin (ACCDET_MODE=001) or HPDETR pin (ACCDET_MODE=010)		HP_IMPEDANCE_ RANGE=00	4		30	Ω
		HP_IMPEDANCE_ RANGE=01	8		100	
		HP_IMPEDANCE_ RANGE=10	100		1000	
		HP_IMPEDANCE_ RANGE=11	1000		10000	
Load impedance detection range Detection via the MICDET1 or MICDET2 pin (ACCDET_MODE=100)			400		6000	Ω
Load impedance detection accuracy (ACCDET_MODE=001, 010 or 100)			-30		+30	%
Load impedance detection range Detection via the MICDET1 or MICDET2 pin (ACCDET_MODE=000). 2.2kΩ (2%) MICBIAS resistor. Note these characteristics assume no other component is connected to MICDETn. See “Applications Information” for recommended external components when a typical microphone is present.		for MICD_LVL[0] = 1	0		3	Ω
		for MICD_LVL[1] = 1	17		21	
		for MICD_LVL[2] = 1	36		44	
		for MICD_LVL[3] = 1	62		88	
		for MICD_LVL[4] = 1	115		160	
		for MICD_LVL[5] = 1	207		381	
		for MICD_LVL[8] = 1	475		30000	
Jack Detection input threshold voltage (JACKDET)	$V_{JACKDET}$	Jack insertion		0.5 x AVDD		V
		Jack removal		0.85 x AVDD		
Jack Detect pull-up resistance			0.65	1	1.3	MΩ

Test Conditions

DBVDD1 = DBVDD2 = DBVDD3 = LDOVDD = CPVDD = AVDD = 1.8V,
DCVDD = 1.2V (powered from LDO1), MICVDD = 3.0V (powered from LDO2), SPKVDDL = SPKVDDR = 4.2V,
T_A = +25ºC, 1kHz sinusoid signal, fs = 48kHz, Input PGA gain = 0dB, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MICVDD Charge Pump and Regulator (CP2 and LDO2)						
Output voltage	V_{MICVDD}		1.7	2.7	3.3	V
Programmable output voltage step size				50		mV
Maximum output current				8		mA
Start-up time		4.7µF on MICVDD, $I_{MICBIASn}$ = 1mA		4.5		ms
Frequency Locked Loop (FLL1, FLL2)						
Output frequency		Normal operation, input reference supplied	13		50	MHz
		Free-running mode, no reference supplied		30		
Lock Time		F_{REF} = 32kHz, F_{OUT} = 24.576MHz		10		ms
		F_{REF} = 12MHz, F_{OUT} = 24.576MHz		1		
RESET pin Input						
RESET input pulse width (To trigger a Hardware Reset, the RESET input must be asserted for longer than this duration)			1			µs

Test Conditions

The following electrical characteristics are valid across the full range of recommended operating conditions.

Device Reset Thresholds						
AVDD Reset Threshold	V_{AVDD}	V_{AVDD} rising			0.96	V
		V_{AVDD} falling	0.54			
DCVDD Reset Threshold	V_{DCVDD}	V_{DCVDD} rising			1.03	V
		V_{DCVDD} falling	0.48			
DBVDD1 Reset Threshold	V_{DBVDD1}	V_{DBVDD1} rising			0.96	V
		V_{DBVDD1} falling	0.54			
Note that the reset thresholds are derived from simulations only, across all operational and process corners. Device performance is not assured outside the voltage ranges defined in the “Recommended Operating Conditions” section. Refer to this section for the WM8998 power-up sequencing requirements.						

TERMINOLOGY

1. Signal-to-Noise Ratio (dB) – SNR is a measure of the difference in level between the maximum full scale output signal and the output with no input signal applied. (Note that this is measured without any mute function enabled.)
2. Total Harmonic Distortion (dB) – THD is the ratio of the RMS sum of the harmonic distortion products in the specified bandwidth (see note below) relative to the RMS amplitude of the fundamental (ie. test frequency) output.
3. Total Harmonic Distortion plus Noise (dB) – THD+N is the ratio of the RMS sum of the harmonic distortion products plus noise in the specified bandwidth (see note below) relative to the RMS amplitude of the fundamental (ie. test frequency) output.
4. Power Supply Rejection Ratio (dB) - PSRR is the ratio of a specified power supply variation relative to the output signal that results from it. PSRR is measured under quiescent signal path conditions.
5. Common Mode Rejection Ratio (dB) – CMRR is the ratio of a specified input signal (applied to both sides of a differential input), relative to the output signal that results from it.
6. Channel Separation (L/R) (dB) – left-to-right and right-to-left channel separation is the difference in level between the active channel (driven to maximum full scale output) and the measured signal level in the idle channel at the test signal frequency. The active channel is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the associated idle channel.
7. Multi-Path Crosstalk (dB) – is the difference in level between the output of the active path and the measured signal level in the idle path at the test signal frequency. The active path is configured and supplied with an appropriate input signal to drive a full scale output, with signal measured at the output of the specified idle path.
8. Mute Attenuation – This is a measure of the difference in level between the full scale output signal and the output with mute applied.
9. All performance measurements are specified with a 20kHz low pass 'brick-wall' filter and, where noted, an A-weighted filter. Failure to use these filters will result in higher THD and lower SNR readings than are found in the Electrical Characteristics. The low pass filter removes out-of-band noise.