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AC'97 Audio and Touchpanel CODEC

DESCRIPTION

The WM9712L is a highly integrated input / output device designed for mobile computing and communications. The device can connect directly to a 4-wire or 5-wire touchpanel, mono or stereo microphones, stereo headphones and a mono speaker, reducing total component count in the system. Additionally, phone input and output pins are provided for seamless integration with wireless communication devices.

The WM9712L also offers up to four auxiliary ADC inputs for analogue measurements such as temperature or light, and five GPIO pins for interfacing to buttons or other digital devices. To monitor the battery voltage in portable systems, the WM9712L has two uncommitted comparator inputs.

All device functions are accessed and controlled through a single AC-Link interface compliant with the AC'97 standard. Additionally, the WM9712L can generate interrupts to indicate pen down, pen up, availability of touchpanel data, low battery, dead battery, and GPIO conditions.

The WM9712L operates at supply voltages from 1.8 to 3.6 Volts. Each section of the chip can be powered down under software control to save power. The device is available in a small leadless 7x7mm QFN package, ideal for use in handheld portable systems.

FEATURES

- AC'97 Rev 2.2 compatible stereo CODEC
 - DAC SNR 94dB, THD -87dB
 - ADC SNR 92dB, THD -87dB
 - Variable Rate Audio, supports all WinCE sample rates
 - Tone Control, Bass Boost and 3D Enhancement
- On-chip 45mW headphone driver
- On-chip 400mW mono speaker driver
- Stereo, mono or differential microphone input
 - Automatic Level Control (ALC)
- Auxiliary mono DAC (ring tone or DC level generation)
- Seamless interface to wireless chipset
- Resistive touchpanel interface
 - Supports 4-wire and 5-wire panels
 - 12-bit resolution, INL ± 2 LSBs (<0.5 pixels)
 - X, Y and touch-pressure (Z) measurement
 - Pen-down detection supported in Sleep Mode
- Up to 5 GPIO pins
- 2 comparator inputs for battery monitoring
- Up to 4 auxiliary ADC inputs
- 1.8V to 3.6V supplies
- 7x7mm QFN

APPLICATIONS

- Personal Digital Assistants (PDA)
- Smartphones
- Handheld and Tablet Computers

BLOCK DIAGRAM

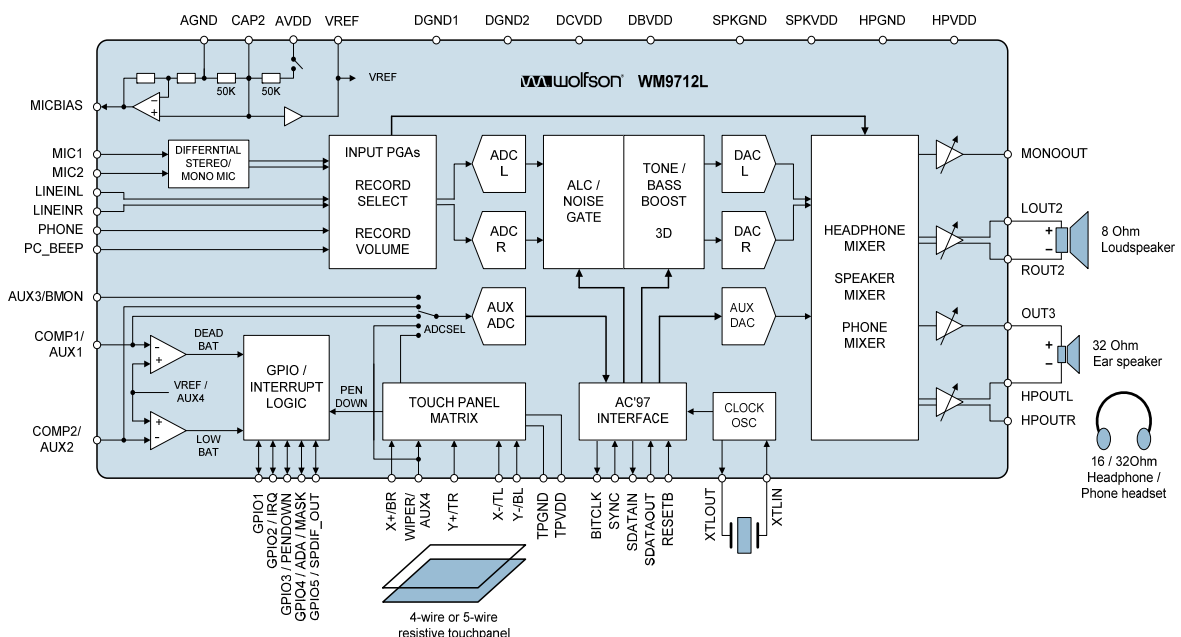
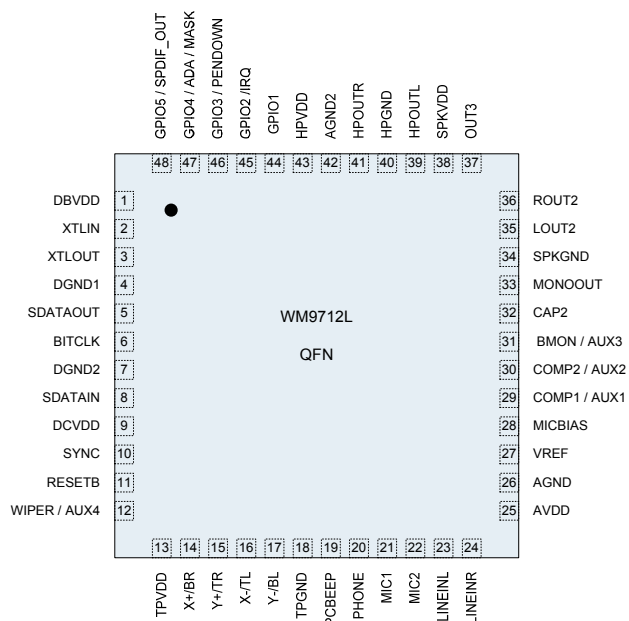


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PIN CONFIGURATION



ORDERING INFORMATION

| DEVICE | TEMP. RANGE | PACKAGE | MOISTURE LEVEL SENSITIVITY | PEAK SOLDERING TEMP |
|-----------------|--------------|--------------------------------------|----------------------------|---------------------|
| WM9712CLGEFL/V | -25 to +85°C | 48-lead QFN (Pb-free) | MSL3 | 260°C |
| WM9712CLGEFL/RV | -25 to +85°C | 48-lead QFN (pb-free, tape and reel) | MSL3 | 260°C |

Note:

Reel quantity = 2,200

PIN DESCRIPTION

| PIN | NAME | TYPE | DESCRIPTION |
|-----|--------------------|-------------------|---|
| 1 | DBVDD | Supply | Digital I/O Buffer Supply |
| 2 | XTLIN | Digital Input | Clock Crystal Connection 1 / External Clock Input |
| 3 | XTLOUT | Digital Output | Clock Crystal Connection 2 |
| 4 | DGND1 | Supply | Digital Ground (return path for both DCVDD and DBVDD) |
| 5 | SDATAOUT | Digital Input | Serial Data Output from Controller / Input to WM9712L |
| 6 | BITCLK | Digital Output | Serial Interface Clock Output to Controller |
| 7 | DGND2 | Supply | Digital Ground (return path for both DCVDD and DBVDD) |
| 8 | SDATAIN | Digital Output | Serial Data Input to Controller / Output from WM9712L |
| 9 | DCVDD | Supply | Digital Core Supply |
| 10 | SYNC | Digital Input | Serial Interface Synchronisation Pulse from Controller |
| 11 | RESETB | Digital Input | Reset (asynchronous, active Low, resets all registers to their default) |
| 12 | WIPER / AUX4 | Analogue Input | Top Sheet Connection for 5-wire Touchpanels / Auxiliary ADC Input |
| 13 | TPVDD | Supply | Touchpanel Driver Supply |
| 14 | X+/BR | Analogue Input | Touchpanel Connection: X+ (Right) for 4-wire / bottom right for 5-wire |
| 15 | Y+/TR | Analogue Input | Touchpanel Connection: Y+ (Top) for 4-wire / top right for 5-wire |
| 16 | X-/TL | Analogue Input | Touchpanel Connection: X- (Left) for 4-wire / top left for 5-wire |
| 17 | Y-/BL | Analogue Input | Touchpanel Connection: Y- (Bottom) for 4-wire / bottom left for 5-wire |
| 18 | TPGND | Supply | Touchpanel Driver Ground |
| 19 | PCBEEP | Analogue Input | Line Input to analogue audio mixers, typically used for beeps |
| 20 | PHONE | Analogue Input | Phone Input (RX) |
| 21 | MIC1 | Analogue Input | Left Microphone or Microphone 1 Input |
| 22 | MIC2 | Analogue Input | Right Microphone or Microphone 2 Input |
| 23 | LINEINL | Analogue Input | Left Line Input |
| 24 | LINEINR | Analogue Input | Right Line Input |
| 25 | AVDD | Supply | Analogue Supply (feeds audio DACs, ADCs, PGAs, mic boost, mixers) |
| 26 | AGND | Supply | Analogue Ground |
| 27 | VREF | Analogue Output | Internal Reference Voltage (buffered CAP2) |
| 28 | MICBIAS | Analogue Output | Bias Voltage for Microphones (buffered CAP2 × 1.8) |
| 29 | COMP1 / AUX1 | Analogue Input | Comparator 1 (dead battery alarm) / Auxiliary ADC Input 1 |
| 30 | COMP2 / AUX2 | Analogue Input | Comparator 2 (low battery alarm) / Auxiliary ADC Input 2 |
| 31 | BMON / AUX3 | Analogue Input | Battery Monitor Input / Auxiliary ADC Input 3 |
| 32 | CAP2 | Analogue In / Out | Internal Reference Voltage (normally AVDD/2, if not overdriven) |
| 33 | MONOOUT | Analogue Output | Mono Output, intended for Phone TX signal |
| 34 | SPKGND | Supply | Speaker Ground (feeds output buffers on pins 35 and 36) |
| 35 | LOUT2 | Analogue Output | Left Output 2 (Speaker, Line or Headphone) |
| 36 | ROUT2 | Analogue Output | Right Output 2 (Speaker, Line or Headphone) |
| 37 | OUT3 | Analogue Output | Analogue Output 3 (from AUXDAC or headphone pseudo-ground) |
| 38 | SPKVDD | Supply | Speaker Supply (feeds output buffers on pins 35 and 36) |
| 39 | HPOUTL | Analogue Output | Headphone Left Output |
| 40 | HPGND | Supply | Headphone Ground (feeds output buffers on pins 37, 39, 41) |
| 41 | HPOUTR | Analogue Output | Headphone Right Output |
| 42 | AGND2 | Supply | Analogue Ground, Chip Substrate |
| 43 | HPVDD | Supply | Headphone Supply (feeds output buffers on pins 37, 39, 41) |
| 44 | GPIO1 | Digital In / Out | GPIO Pin 1 |
| 45 | GPIO2 / IRQ | Digital In / Out | GPIO Pin 2 or IRQ (Interrupt Request) Output |
| 46 | GPIO3 / PENDOWN | Digital In / Out | GPIO Pin 3 or Pen Down Output |
| 47 | GPIO4 / ADA / MASK | Digital In / Out | GPIO Pin 4 or ADA (ADC Data Available) Output or Mask input (On reset, pin level configures device power up status. See Applications section for external components configuration) |
| 48 | GPIO5 / SPDIF_OUT | Digital In / Out | GPIO Pin 5 or SPDIF Digital Audio Output |

Note: It is recommended that the QFN ground paddle should be connected to analogue ground on the application PCB.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.



ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Wolfson tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.

MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

| CONDITION | MIN | MAX |
|---|------------|-------------|
| Digital supply voltages (DCVDD, DBVDD) | -0.3V | +3.63V |
| Analogue supply voltages (AVDD, HPVDD, SPKVDD, TPVDD) | -0.3V | +3.63V |
| Touchpanel supply voltage (TPVDD) | AVDD -0.3V | AVDD +0.3V |
| Voltage range digital inputs | DGND -0.3V | DBVDD +0.3V |
| Voltage range analogue inputs | AGND -0.3V | AVDD +0.3V |
| Voltage range touchpanel Inputs X+, X-, Y+ and Y- | | TPVDD +0.3V |
| Voltage range touchpanel Inputs X+, X-, Y+ and Y- | | AVDD +0.3V |
| Voltage range, BMON/AUX3 (pin31) | | +5V |
| Operating temperature range, T _A | -25°C | +85°C |

RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|----------------------------|-----------------|------|-----|-----------------|------|
| Digital input/output buffer supply range | DBVDD | Notes 1, 2 | 1.8 | | 3.6 or AVDD+0.3 | V |
| Digital core supply range | DCVDD | Notes 1, 2 | 1.8 | | 3.6 or AVDD+0.3 | V |
| Analogue supply range | AVDD, HPVDD, SPKVDD, TPVDD | | 1.8 | | 3.6 | V |
| Digital ground | DCGND, DBGND | | | 0 | | V |
| Analogue ground | AGND, HPGND, SPKGND, TPGND | | | 0 | | V |
| Difference AGND to DGND | | Note 3 | -0.3 | 0 | +0.3 | V |

Notes:

1. AVDD, DCVDD and DBVDD can all be different
2. Digital supplies (DCVDD, DBVDD) must not exceed analogue supplies (AVDD, HPVDD, SPKVDD, TPVDD) by more than 0.3V
3. AGND is normally the same as DGND

ELECTRICAL CHARACTERISTICS

AUDIO OUTPUTS

Test Conditions

DBVDD=3.3V, DCVDD = 3.3V, AVDD=HPVDD=SPKVDD =3.3V, T_A = +25°C, 1kHz signal, f_s = 48kHz, 18-bit audio data unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-------------------|--|-----|-------------|-----|---------|
| DAC to Line-Out (HPOUTL/R or MONOOUT with 10kΩ / 50pF load) | | | | | | |
| Full-scale output | | AVDD = 3.3V, PGA gains set to 0dB | | 1 | | V rms |
| Signal to Noise Ratio (A-weighted) | SNR | | 85 | 94 | | dB |
| Total Harmonic Distortion | THD | -3dB output | | -87 | -80 | dB |
| Power Supply Rejection | PSRR | 100mV, 20Hz to 20kHz signal on AVDD | | 50 | | dB |
| Speaker Output (LOUT2/ROUT2 with 8Ω bridge tied load, INV=1) | | | | | | |
| Output Power | P _O | Output power is very closely correlated with THD; see below. | | | | |
| Output Power at 1% THD | P _O | | | 400 | | mW |
| Abs. Max Output Power | P _{Omax} | | | 500 | | mW |
| Total Harmonic Distortion | THD | P _O =200mW | | -66 0.05 | | dB % |
| Signal to Noise Ratio (A-weighted) | SNR | | 90 | 100 | | dB |
| Headphone Output (HPOUTL/R, OUT3 or LOUT2/ROUT2 with 16Ω or 32Ω load) | | | | | | |
| Output Power per channel | P _O | Output power is very closely correlated with THD; see below. | | | | |
| Total Harmonic Distortion | THD | P _O =10mW, R _L =16Ω | | -76 | | dB |
| | | P _O =10mW, R _L =32Ω | | -73 | | |
| | | P _O =20mW, R _L =16Ω | | -75 | -70 | |
| | | P _O =20mW, R _L =32Ω | | -78 | | |
| Signal to Noise Ratio (A-weighted) | SNR | | 90 | 95 | | dB |

Note:

- All THD values are valid for the output power level quoted above – for example, at HPVDD=3.3V and R_L=16Ω, THD is -76dB when output power is 10mW. Higher output power is possible, but will result in a deterioration in THD.

AUDIO INPUTS**Test Conditions**

DBVDD=3.3V, DCVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 18-bit audio data unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-------------------|--------------------------------------|--------------------------------|-------|-----|-------|
| LINEINL/R, MICL/R and PHONE pins | | | | | | |
| Full Scale Input Signal Level (for ADC 0dB Input at 0dB Gain) | V _{INFS} | AVDD = 3.3V | | 1.0 | | V rms |
| | | AVDD = 1.8V | | 0.545 | | |
| | | differential input mode (MS = 01) | half of the value listed above | | | |
| Input Resistance | R _{IN} | 0dB PGA gain | | 34 | | kΩ |
| | | 12dB PGA gain | 10 | 16 | 22 | |
| Input Capacitance | | | | 5 | | pF |
| Line input to ADC (LINEINL, LINEINR, PHONE) | | | | | | |
| Signal to Noise Ratio (A-weighted) | SNR | | 85 | 92 | | dB |
| Total Harmonic Distortion | THD | -6dBFS | | -87 | -80 | dB |
| Power Supply Rejection | PSRR | 20Hz to 20kHz | | 50 | | dB |
| Microphone input to ADC (MIC1/2 pins) | | | | | | |
| Signal to Noise Ratio (A-weighted) | SNR | 20dB boost enabled | | 80 | | dB |
| Total Harmonic Distortion | THD | 20dB boost enabled | | -80 | | dB |
| Power Supply Rejection Ratio | PSRR | | | 50 | | dB |
| Common Mode Rejection Ratio | CMRR | Differential mic mode | | TBD | | dB |

AUXILIARY MONO DAC (AUXDAC)**Test Conditions**

AVDD = 3.3V, T_A = +25°C, unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------|--------|-----------------|-----|-----|-----|------|
| Resolution | | | | 12 | | bits |
| Full scale output voltage | | AVDD=3.3V | | 1 | | Vrms |
| Signal to Noise Ratio (A-weighted) | SNR | | 65 | 70 | | dB |
| Total Harmonic Distortion | THD | | | -62 | -50 | dB |

TOUCHPANEL AND AUXILIARY ADC**Test Conditions**DBVDD=3.3V, DCVDD = 3.3V, AVDD = TPVDD = 3.3V, T_A = +25°C, MCLK = 24.576 MHz, unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------|---|------|--------------------|------|------|
| Input Pins X+, X-, Y+, Y-, WIPER/AUX4, COMP1/AUX1, COMP2/AUX2 and BMON/AUX3 | | | | | | |
| Input Voltage | | | AGND | | AVDD | V |
| Input leakage current | | AUX pin not selected as AUX ADC input | | <10 | | nA |
| ADC Resolution | | | | 12 | | bits |
| Differential Non-Linearity Error | DNL | | | ±0.25 | ±1 | LSB |
| Integral Non-Linearity Error | INL | | | | ±2 | LSB |
| Offset Error | | | | | ±4 | LSB |
| Gain Error | | | | | ±6 | LSB |
| Power Supply Rejection | PSRR | | | 50 | | dB |
| Throughput Rate | | DEL = 1111 (zero settling time) | | | 48 | kHz |
| Settling Time (programmable) | | MCLK = 24.576MHz | 0 | | 6 | ms |
| Conversion Time | | Note: touch pressure measurements require two conversions | | 20.8 | | µs |
| Switch matrix resistance | | | | 12 | | Ω |
| Programmable Pull-up resistor | R _{PU} | RPU = 000001 | 55 | 63 | 70 | kΩ |
| Pen down detector threshold | | | | VDD/2 | | V |
| Pressure measurement current | I _P | PIL = 1 | | 400 | | µA |
| | | PIL = 0 | | 200 | | |
| BMON/AUX3 (pin 31 only) | | | | | | |
| Input Range | | AVDD = 3.3V | AGND | | 5 | V |
| | | AVDD = 1.8V | AGND | | 3.3 | V |
| Scaling | | | -3% | 1/3 | +3% | |
| Input Resistance (Note 1) | | during measurement | | 30 | | kΩ |
| | | average over time | | 30 / duty cycle | | |

Note:

- Current only flows into pin 31 during a measurement. At all other times, BMON/AUX3 is effectively an open circuit.

COMPARATORS**Test Conditions**AVDD = 3.3V, T_A = +25°C, unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--------|-----------------------------------|------|-----|------|------|
| COMP1/AUX1 and COMP2/AUX2 (pins 29, 30) | | | | | | |
| Input Voltage | | | AGND | | AVDD | V |
| Input leakage current | | pin not selected as AUX ADC input | | <10 | | nA |
| Comparator Input Offset (COMP1, COMP2 only) | | | -50 | | +50 | mV |
| COMP2 delay (COMP2 only) | | 24.576MHz crystal | 0 | | 10.9 | s |

REFERENCE VOLTAGES**Test Conditions**

DBVDD=3.3V, DCVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 18-bit audio data unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------|----------------------|-----------------|------|------|------|--------|
| Audio ADCs, DACs, Mixers | | | | | | |
| Reference Input/Output | CAP2 pin | | 1.6 | 1.65 | 1.7 | V |
| Buffered Reference Output | VREF pin | | 1.6 | 1.65 | 1.7 | V |
| Microphone Bias | | | | | | |
| Bias Voltage | V _{MICBIAS} | | 2.88 | 2.97 | 3.06 | V |
| Bias Current Source | I _{MICBIAS} | | | | 3 | mA |
| Output Noise Voltage | V _n | 1K to 20kHz | | 15 | | nV/√Hz |

DIGITAL INTERFACE CHARACTERISTICS**Test Conditions**

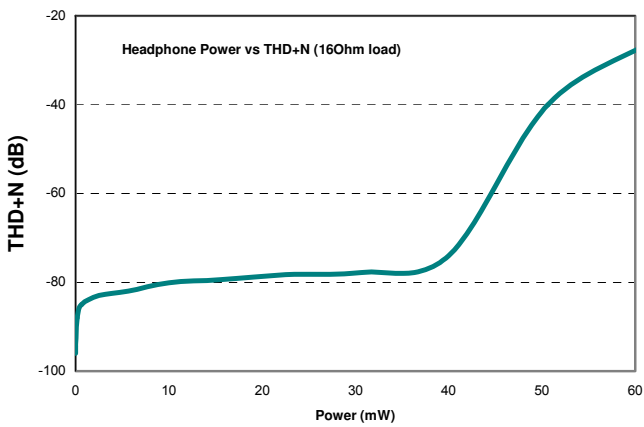
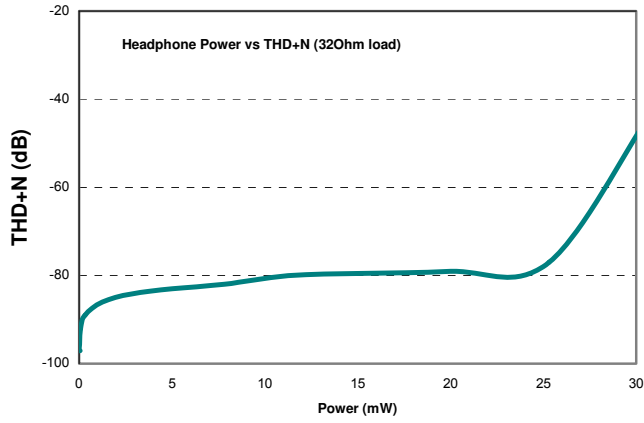
DBVDD = 3.3V, DCVDD = 3.3V, T_A = +25°C, unless otherwise stated.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|-----------------|----------------------|-----------|--------|-----------|------|
| Digital Logic Levels (all digital input or output pins) – CMOS Levels | | | | | | |
| Input HIGH level | V _{IH} | | DBVDD×0.7 | | | V |
| Input LOW level | V _{IL} | | | | DBVDD×0.3 | V |
| Output HIGH level | V _{OH} | source current = 2mA | DBVDD×0.9 | | | |
| Output LOW level | V _{OL} | sink current = 2mA | | | DBVDD×0.1 | |
| Clock Frequency | | | | | | |
| Master clock (XTLIN pin) | | | | 24.576 | | MHz |
| AC'97 bit clock (BIT_CLK pin) | | | | 12.288 | | MHz |
| AC'97 sync pulse (SYNC pin) | | | | 48 | | kHz |

Note:

- All audio and non-audio sample rates and other timing scales proportionately with the master clock.
- For signal timing on the AC-Link, please refer to the AC'97 specification (Revision 2.2)

HEADPHONE / SPEAKER OUTPUT THD VERSUS POWER



POWER CONSUMPTION

The power consumption of the WM9712L depends on the following factors.

- Supply voltages: Reducing the supply voltages also reduces digital supply currents, and therefore results in significant power savings especially in the digital sections of the WM9712L.
- Operating mode: Significant power savings can be achieved by always disabling parts of the WM9712L that are not used (e.g. audio ADC, DAC, touchpanel digitiser).

| Mode Description | 26h 14:8 | 24h 15:0 | Other Settings | AVDD | | DCVDD | | DBVDD | | Total Power (mW) |
|---|----------|--------------------|------------------------------------|-------------------|----------------------------|-------------------|-------------------------|-------------------|----------------------|-------------------------------|
| | | | | V | I (mA) | V | I (mA) | V | I (mA) | |
| OFF (lowest possible power) Clocks stopped | 11111111 | 011111111111111111 | 58h, SVD = 1 | 3.3 2.5 1.8 | 0.0005 0.0004 0.0003 | 3.3 2.5 1.8 | 0 0 0 | 3.3 2.5 1.8 | 0 0 0 | 0.00165 0.001 0.00054 |
| LPS (Low Power Standby) VREF maintained using 1MOhm string | 11111111 | 011111111111111111 | | 3.3 2.5 1.8 | 0.005 0.004 0.003 | 3.3 2.5 1.8 | 0 0 0 | 3.3 2.5 1.8 | 0 0 0 | 0.0165 0.01 0.0054 |
| Standby Mode (ready to playback) VREF maintained using 50kOhm string | 11101111 | 011111111111111111 | | 3.3 2.5 1.8 | 0.56 0.37 0.241 | 3.3 2.5 1.8 | 0 0 0 | 3.3 2.5 1.8 | 0 0 0 | 1.848 0.925 0.4338 |
| "Idle" Mode VREF maintained using 50kOhm string use LPS mode instead, if possible | 11001111 | 011111111111111111 | | 3.3 2.5 1.8 | 1.1 0.76 0.508 | 3.3 2.5 1.8 | 0 0 0 | 3.3 2.5 1.8 | 0 0 0 | 3.63 1.9 0.9144 |
| Touchpanel only (waiting for pen-down) AC-Link running | 11011111 | 011111111111111111 | 76h = 0C00h 78h = 0001h | 3.3 2.5 1.8 | 0.05 0.02 0.009 | 3.3 2.5 1.8 | 1.301 0.883 0.571 | 3.3 2.5 1.8 | 3.26 2.1 1.41 | 15.2163 7.5075 3.582 |
| Touchpanel only (continuous conversion) 93.75 points per second | 10011111 | 011111111111111111 | 76h = 0C00h 78h = C001h | 3.3 2.5 1.8 | 0.08 0.04 0.027 | 3.3 2.5 1.8 | 5.85 3.922 2.87 | 3.3 2.5 1.8 | 2.67 2.1 1.41 | 28.38 15.155 7.7526 |
| Phone Call - using headphone / ear speaker HPOUTL, HPOUTR and OUT3 active AC-Link stopped | 01100111 | 0111100010101100 | 0Eh, bit 7 = 1 (mic gain boost) | 3.3 2.5 1.8 | 2.36 1.838 1.218 | 3.3 2.5 1.8 | 0 0 0 | 3.3 2.5 1.8 | 0 0 0 | 7.788 4.595 2.1924 |
| Phone Call - using loudspeaker AC-Link stopped | 11100111 | 0111101100110100 | 0Eh, bit 7 = 1 (mic gain boost) | 3.3 2.5 1.8 | 2.385 1.837 1.218 | 3.3 2.5 1.8 | 0 0 0 | 3.3 2.5 1.8 | 0 0 0 | 7.8705 4.5925 2.1924 |
| Record from mono microphone with MICBIAS all analogue outputs disabled | 10001110 | 011010111111111111 | 0Eh, bit 7 = 1 (mic gain boost) | 3.3 2.5 1.8 | 3.27 2.66 1.838 | 3.3 2.5 1.8 | 11.21 7.78 5.21 | 3.3 2.5 1.8 | 2.6 2.13 1.41 | 56.364 31.425 15.2244 |
| Record phone call both sides mixed to mono call using headphone / ear speaker | 00000000 | 0000000010001000 | 0Eh, bit 7 = 1 (mic gain boost) | 3.3 2.5 1.8 | 9.461 7.46 5.318 | 3.3 2.5 1.8 | 12.22 8.552 5.799 | 3.3 2.5 1.8 | 2.62 2.1 1.48 | 80.1933 45.28 22.6746 |
| DAC Playback - using loudspeaker | 10000001 | 0001111101110111 | | 3.3 2.5 1.8 | 3.45 2.549 1.738 | 3.3 2.5 1.8 | 9.884 6.755 4.606 | 3.3 2.5 1.8 | 2.6 2.1 1.41 | 52.5822 28.51 13.9572 |
| DAC Playback - using headphone | 00000001 | 0001110011101111 | | 3.3 2.5 1.8 | 3.62 2.71 1.748 | 3.3 2.5 1.8 | 9.8 6.78 4.606 | 3.3 2.5 1.8 | 2.6 2.1 1.47 | 52.866 28.975 14.0832 |
| DAC Playback - to Line-out | 00000001 | 0001110011101111 | | 3.3 2.5 1.8 | 3.62 2.71 1.748 | 3.3 2.5 1.8 | 9.8 6.78 4.606 | 3.3 2.5 1.8 | 2.6 2.1 1.41 | 52.866 28.975 13.9752 |
| Maximum Power (everything on) | 00000000 | 0000000000000000 | 0Eh, bit 7 = 1 (mic gain boost) | 3.3 2.5 1.8 | 9.593 7.37 5.388 | 3.3 2.5 1.8 | 12.26 8.563 5.8 | 3.3 2.5 1.8 | 2.62 2.12 1.48 | 80.7609 45.1325 22.8024 |

Table 1 Supply Current Consumption

Notes:

1. All figures are at $T_A = +25^\circ\text{C}$, audio sample rate $f_s = 48\text{kHz}$, with zero signal (quiescent).
2. The power dissipated in the headphone, speaker and touchpanel is not included in the above table.

DEVICE DESCRIPTION

INTRODUCTION

The WM9712L is designed to meet the mixed-signal requirements of portable and wireless computer systems. It includes audio recording and playback, touchpanel digitisation, battery monitoring, auxiliary ADC and GPIO functions, all controlled through a single 5-wire AC-Link interface.

SOFTWARE SUPPORT

The basic audio features of the WM9712L are software compatible with standard AC'97 device drivers. However, to better support the touchpanel and other additional functions, Wolfson Microelectronics supplies custom device drivers for selected CPUs and operating systems. Please contact your local Wolfson Sales Office for more information.

AC'97 COMPATIBILITY

The WM9712L uses an AC'97 interface to communicate with a microprocessor or controller. The audio and GPIO functions are largely compliant with AC'97 Revision 2.2. The following **differences** from the AC'97 standard are noted:

- Pinout: The function of some pins has been changed to support device specific features. The PHONE and PCBEEP pins have been moved to different locations on the device package.
- Package: The package for the WM9712L is a 7×7mm leadless QFN package.
- Audio mixing: The WM9712L handles all the audio functions of a smartphone, including audio playback, voice recording, phone calls, phone call recording, ring tones, as well as simultaneous use of these features. The AC'97 mixer architecture does not fully support this. The WM9712L therefore uses a modified AC'97 mixer architecture with three separate mixers.
- Tone Control, Bass Boost and 3D Enhancement: These functions are implemented in the digital domain and therefore affect only signals being played through the audio DACs, not all output signals as stipulated in AC'97.

Some other functions are **additional** to AC'97:

- On-chip BTL loudspeaker driver
- On-chip BTL driver for ear speaker (phone receiver)
- Auxiliary mono DAC for ring tones, system alerts etc.
- Touchpanel controller
- Auxiliary ADC Inputs
- 2 Analogue Comparators for Battery Alarm
- Programmable Filter Characteristics for Tone Control and 3D Enhancement

AUDIO INPUTS

The following sections give an overview of the analogue audio input pins and their function. For more information on recommended external components, please refer to the “Applications Information” section.

LINE INPUT

The LINEINL and LINEINR inputs are designed to record line level signals, and/or to mix into one of the analogue outputs.

Both pins are directly connected to the record selector. The record PGA adjusts the recording volume, controlled by register 1Ch or by the ALC function.

For analogue mixing, the line input signals pass through a separate PGA, controlled by register 10h. The signals can be routed into all three output mixers (headphone, speaker and phone). Each LINEIN-to-mixer path has an independent mute bit. When the line inputs are not used, the line-in PGA can be switched off to save power (see “Power Management” section).

LINEINL and LINEINR are biased internally to the reference voltage VREF. Whenever the inputs are muted or the device placed into standby mode, the inputs remain biased to VREF using special anti-thump circuitry to suppress any audible clicks when changing inputs.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|------------------|------|-------------|-------------|---|
| 10h | 12:8 | LINEINL VOL | 01000 (0dB) | LINEINL input gain 00000: +12dB ... (1.5dB steps) 11111: -34.5dB |
| | 4:0 | LINEINR VOL | 01000 (0dB) | LINEINR input gain similar to LINEINLVOL |
| | 15 | L2H | 1 | Mute LINEIN path to headphone mixer 1: Mute, 0: No mute (ON) |
| | 14 | L2S | 1 | Mute LINEIN path to speaker mixer 1: Mute, 0: No mute (ON) |
| | 13 | L2P | 1 | Mute LINEIN path to phone mixer 1: Mute, 0: No mute (ON) |

Table 2 Line Input Control

MICROPHONE INPUT

The MIC1 and MIC2 inputs are designed for direct connection to single-ended mono, stereo or differential mono microphone. If the microphone is mono, the same signal appears on both left and right channels. In stereo mode, MIC1 is routed to the left and MIC2 to the right channel.

For voice recording, the microphone signal is directly connected to the record selector. The record PGA adjusts the recording volume, controlled by register 1Ch or by the ALC function.

For analogue mixing, the signal passes through a separate PGA, controlled by register 0Eh. The microphone signal can be routed into the phone mixer (for normal phone call operation) and/or the headphone mixer (using register 14h, see “Audio Mixers / Sidetone Control” section), but not into the speaker mixer (to prevent acoustic feedback from the speaker into the microphone). When the microphone inputs are not used, the microphone PGA can be switched off to save power (see “Power Management” section).

MIC1 and MIC2 are biased internally to the reference voltage VREF. Whenever the inputs are muted or the device placed into standby mode, the inputs remain biased to VREF using special anti-thump circuitry to suppress any audible clicks when changing inputs.

It is also possible to use the LINEINL and LINEINR pins as a second differential microphone input. This is achieved by setting the DS bit (register 5Ch, bit 11) to '1'. This disables the line-in audio paths and routes the signal from LINEINL and LINEINR through the differential mic path, as if it came from the MIC1 and MIC2 pins. Only one differential microphone be used at a time. The DS bit only has an effect when MS = 01 (differential mode).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | |
|--|--------|----------------|--|--|---|
| 0Eh Mic Volume | 14 | M12P | 1 | Mute MIC1 path to phone mixer 1: Mute, 0: No mute (ON) | |
| | 13 | M22P | 1 | Mute MIC2 path to phone mixer 1: Mute, 0: No mute (ON) | |
| | 12:8 | LMICVOL | 01000 (0dB) | Left microphone volume Only used when MS = 11 Similar to MICVOL | |
| | 7 | 20dB | 0 | Microphone gain boost (Note 1) 1: 20dB boost ON 0: No boost (0dB gain) | |
| | 6:5 | MS | 00 | Microphone mode select | |
| | | | | 00 | Single-ended mono (left) left = right = MIC1 (pin 21) Volume controlled by MICVOL |
| 01 | | | | Differential mono mode left = right = MIC1 – MIC2 Volume controlled by MICVOL | |
| 10 | | | | Single-ended mono (right) left = right = MIC2 (pin 22) Volume controlled by MICVOL | |
| | 11 | | Stereo mode MIC1 = left, MIC2 = right Left Volume controlled by LMICVOL Right volume controlled by MICVOL | | |
| 4:0 | MICVOL | 01000 (0dB) | Microphone volume to mixers 00000: +12dB ... (1.5dB steps) 11111: -34.5dB | | |
| 5Ch Additional Analogue Functions | 8 | DS | 0 | Differential Microphone Select 0 : Use MIC1 and MIC2 1: Use LINEL and LINER (Note 2) | |

Table 3 Microphone Input Control

Note:

1. The 20dB gain boost acts on the input to the phone mixer only. A separate microphone boost for recording can be enabled using the BOOST bit in register 1Ah.
2. When the LINEL and LINER are selected for differential microphone select then the MIC1 and MIC2 input pins become disabled, these signals can therefore not be routed internally to the device.

MICROPHONE BIAS

The MICBIAS output (pin 28) provides a low noise reference voltage suitable for biasing electret type microphones and the associated external resistor biasing network. The internal MICBIAS circuitry is shown below. Note that the maximum source current capability for MICBIAS is 3mA. The external biasing resistors and microphone cartridge therefore must limit the MICBIAS current to 3mA.

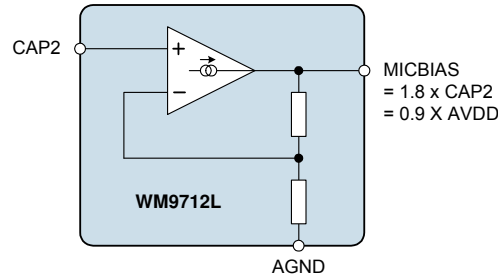


Figure 2 Microphone Bias Schematic

PHONE INPUT

Pin 20 (PHONE) is a mono, line level input designed to connect to the receive path of a telephony device.

The pin connects directly to the record selector for phone call recording (Note: to record both sides of a phone call, one ADC channel should record the PHONE signal while the other channel records the MIC signal). The RECVOL PGA adjusts the recording volume, controlled by register 1Ch or by the ALC function.

To listen to the PHONE signal, the signal passes through a separate PGA, controlled by register 0Ch. The signal can be routed into the headphone mixer (for normal phone call operation) and/or the speaker mixer (for speakerphone operation), but not into the phone mixer (to prevent forming a feedback loop). When the phone input is not used, the phone-in PGA can be switched off to save power (see “Power Management” section).

PHONE is biased internally to the reference voltage VREF. Whenever the input is muted or the device placed into standby mode, the input remains biased to VREF using special anti-thump circuitry to suppress any audible clicks when changing inputs.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|--------------------|-----|-----------|-------------|---|
| 0Ch Phone Input | 15 | P2H | 1 | Mute PHONE path to headphone mixer 1: Mute, 0: No mute (ON) |
| | 14 | P2S | 1 | Mute PHONE path to speaker mixer 1: Mute, 0: No mute (ON) |
| | 4:0 | PHONE VOL | 01000 (0dB) | PHONE input gain 00000: +12dB ... (1.5dB steps) 11111: -34.5dB |

Table 4 Phone Input Control

PCBEEP INPUT

Pin 19 (PCBEEP) is a mono, line level input intended for externally generated signal or warning tones. It is routed directly to the record selector and all three output mixers, without an input amplifier. The signal gain into each mixer can be independently controlled, with a separate mute bit for each signal path.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---------------------|-------|--------|--------------|--|
| 0Ah PCBEEP input | 15 | B2H | 1 | Mute PCBEEP path to headphone mixer 1: Mute, 0: No mute (ON) |
| | 14:12 | B2HVOL | 010 (0dB) | PCBEEP to headphone mixer gain 000: +6dB ... (3dB steps) 111: -15dB |
| | 11 | B2S | 1 | Mute PCBEEP path to speaker mixer 1: Mute, 0: No mute (ON) |
| | 10:8 | B2SVOL | 010 (0dB) | PCBEEP to speaker mixer gain 000: +6dB ... (3dB steps) 111: -15dB |
| | 7 | B2P | 1 | Mute PCBEEP path to phone mixer 1: Mute, 0: No mute (ON) |
| | 6:4 | B2PVOL | 010 (0dB) | PCBEEP to phone mixer gain 000: +6dB ... (3dB steps) 111: -15dB |

Table 5 PCBEEP Control

AUDIO ADC

The WM9712L has a stereo sigma-delta ADC to digitize audio signals. The ADC achieves high quality audio recording at low power consumption. The ADC sample rate can be controlled by writing to a control register (see "Variable Rate Audio"). It is independent of the DAC sample rate.

To save power, the left and right ADCs can be separately switched off using the PD11 and PD12 bits, whereas PR0 disables both ADCs (see "Power Management" section). If only one ADC is running, the same ADC data appears on both the left and right AC-Link slots.

HIGH PASS FILTER

The WM9712L audio ADC incorporates a digital high-pass filter that eliminates any DC bias from the ADC output data. The filter is enabled by default. For DC measurements, it can be disabled by writing a '1' to the HPF bit (register 5Ch, bit 3).

ADC SLOT MAPPING

By default, the output of the left audio ADC appears on slot 3 of the SDATAIN signal (pin 8), and the right ADC data appears on slot 4. However, the ADC output data can also be sent to other slots, by setting the ASS (ADC slot select) control bits as shown below.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|--|-----|-------|---------|---|
| 5Ch Additional Function Control | 1:0 | ASS | 00 | ADC to slot mapping 00: Left = Slot 3, Right = Slot 4 (default) 01: Left = Slot 7, Right = Slot 8 10: Left = Slot 6, Right = Slot 9 11: Left = Slot 10, Right = Slot 11 |
| | 3 | HPF | 0 | High-pass filter disable 0: Filter enabled (for audio) 1: Filter disabled (for DC measurements) |

Table 6 ADC Control

RECORD SELECTOR

The record selector determines which input signals are routed into the audio ADC. The left and right channels can be selected independently. This is useful for recording a phone call: one channel can be used for the RX signal and the other for the TX signal, so that both sides of the conversation are digitized.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|----------------------|-------|----------|---------|---|
| 1Ah Record Select | 14 | BOOST | 0 | 20dB Boost 1: Boost ADC input signal by 20dB 0 :No boost |
| | 13:12 | R2P | 11 | Record to phone path enable 00: Left ADC and Right ADC to phone mixer 01 : Left ADC to phone mixer 10: Right ADC to phone imixer 11 : Muted |
| | 11 | R2PBOOST | 0 | 20dB Boost for ADC to phone signal 1: Boost signal by 20dB 0 :No boost |
| | 10:8 | RECSL | 000 | Left ADC signal source 000: MIC* (pre-PGA) 001-010: Reserved (do not use this setting) 011: Speaker mix 100: LINEINL (pre-PGA) 101: Headphone Mix (left) 110: Phone Mix 111: PHONE (pre-PGA) |
| | 2:0 | RECSR | 000 | Right ADC signal source 000: MIC* (pre-PGA) 001-010: Reserved (do not use this setting) 011: Speaker mix 100: LINEINR (pre-PGA) 101: Headphone Mix (right) 110: Phone Mix 111: PHONE (pre-PGA) |

Table 7 Audio Record Selector

Note:

*In stereo mic mode, MIC1 is routed to the left ADC and MIC2 to the right ADC. In all mono mic modes, the same signal (MIC1, MIC2 or MIC1-MIC2) is routed to both the left and right ADCs. See "Microphone Input" section for details.

RECORD GAIN

The amplitude of the signal that enters the audio ADC is controlled by the Record PGA (Programmable Gain Amplifier). The PGA gain can be programmed either by writing to the Record Gain register, or by the Automatic Level Control (ALC) circuit (see next section). When the ALC is enabled, any writes to the Record Gain register have no effect.

Two different gain ranges can be implemented: the standard gain range defined in the AC'97 standard, or an extended gain range with smaller gain steps. The ALC circuit always uses the extended gain range, as this has been found to result in better sound quality.

The output of the Record PGA can also be mixed into the phone and/or headphone outputs (see "Audio Mixers"). This makes it possible to use the ALC function for the microphone signal in a smartphone application.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION | |
|--------------------|---------|---------|---|---|--|
| 1Ch Record Gain | 15 | RMU | 1 | Mute Audio ADC (both channels) 1: Mute (OFF) 0: No Mute (ON) | |
| | 14 | GRL | 0 | Gain range select (left) 0: Standard (0 to 22.5dB, 1.5dB step size) 1: Extended (-17.25 to +30dB, 0.75dB steps) | |
| | 13:8 | RECVOLL | 000000 | Record Volume (left) | |
| | | | | Standard (GRL=0) | Extended (GRL=1) |
| | | | | XX0000: 0dB XX0001: +1.5dB ... (1.5dB steps) XX1111: +22.5dB | 000000: -17.25dB 000001: -16.5dB ... (0.75dB steps) 111111: +30dB |
| | 7 | ZC | 0 | Zero Cross Enable 0: Record Gain changes immediately 1: Record Gain changes when signal is zero or after time-out | |
| | 6 | GRR | 0 | Gain range select (right) Similar to GRL | |
| 5:0 | RECVOLR | 000000 | Record Volume (right) Similar to RECVOLL | | |

Table 8 Record Gain Register

AUTOMATIC LEVEL CONTROL

The WM9712L has an automatic level control that aims to keep a constant recording volume irrespective of the input signal level. This is achieved by continuously adjusting the PGA gain so that the signal level at the ADC input remains constant. A digital peak detector monitors the ADC output and changes the PGA gain if necessary.

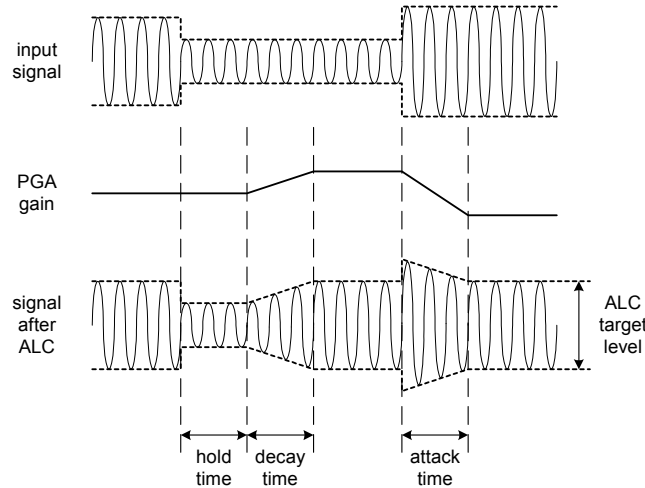


Figure 3 ALC Operation

The ALC function is enabled using the ALCSEL control bits. When enabled, the recording volume can be programmed between -6dB and -28.5dB (relative to ADC full scale) using the ALCL register bits.

HLD, DCY and ATK control the hold, decay and attack times, respectively:

Hold time is the time delay between the peak level detected being below target and the PGA gain beginning to ramp up. It can be programmed in power-of-two (2^n) steps, e.g. 2.67ms, 5.33ms, 10.67ms etc. up to 43.7s. Alternatively, the hold time can also be set to zero. The hold time only applies to gain ramp-up, there is no delay before ramping the gain down when the signal level is above target.

Decay (Gain Ramp-Up) Time is the time that it takes for the PGA gain to ramp up across 90% of its range (e.g. from -15dB up to 27.75dB). The time it takes for the recording level to return to its target value therefore depends on both the decay time and on the gain adjustment required. If the gain adjustment is small, it will be shorter than the decay time. The decay time can be programmed in power-of-two (2^n) steps, from 24ms, 48ms, 96ms, etc. to 24.58s.

Attack (Gain Ramp-Down) Time is the time that it takes for the PGA gain to ramp down across 90% of its range (e.g. from 27.75dB down to -15dB gain). The time it takes for the recording level to return to its target value therefore depends on both the attack time and on the gain adjustment required. If the gain adjustment is small, it will be shorter than the attack time. The attack time can be programmed in power-of-two (2^n) steps, from 6ms, 12ms, 24ms, etc. to 6.14s.

When operating in stereo, the peak detector takes the maximum of left and right channel peak values, and any new gain setting is applied to both left and right PGAs, so that the stereo image is preserved. However, the ALC function can also be enabled on one channel only. In this case, only one PGA is controlled by the ALC mechanism, while the other channel runs independently with its PGA gain set through the control register.

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---------------------------------|-------|------------|-----------------|---|
| 62h ALC / Noise Gate Control | 15:14 | ALCSEL | 00 (OFF) | ALC function select 00 = ALC off (PGA gain set by register) 01 = Right channel only 10 = Left channel only 11 = Stereo (PGA registers unused) Note: Ensure that RECVOLL and RECVOLR settings (reg. 1Ch) are the same before entering this mode |
| | 13:11 | MAXGAIN | 111 (+30dB) | PGA gain limit for ALC 111 = +30dB 110 = +24dB ... (6dB steps) 001 = -6dB 000 = -12dB |
| | 8 | ALCZC | 0 | ALC Zero Cross enable (overrides ZC bit in register 1Ch) 0: PGA Gain changes immediately 1: PGA Gain changes when signal is zero or after time-out |
| | 9:10 | ZC TIMEOUT | 11 | Programmable zero cross timeout 11 2^{17} x MCLK period 10 2^{16} x MCLK period 01 2^{15} x MCLK period 00 2^{14} x MCLK period |
| 60h ALC Control | 15:12 | ALCL | 1011 (-12dB) | ALC target – sets signal level at ADC input 0000 = -28.5dB FS 0001 = -27.0dB FS ... (1.5dB steps) 1110 = -7.5dB FS 1111 = -6dB FS |
| | 11:8 | HLD | 0000 (0ms) | ALC hold time before gain is increased. 0000 = 0ms 0001 = 2.67ms 0010 = 5.33ms ... (time doubles with every step) 1111 = 43.691s |
| | 7:4 | DCY | 0011 (192ms) | ALC decay (gain ramp-up) time 0000 = 24ms 0001 = 48ms 0010 = 96ms ... (time doubles with every step) 1010 or higher = 24.58s |
| | 3:0 | ATK | 0010 (24ms) | ALC attack (gain ramp-down) time 0000 = 6ms 0001 = 12ms 0010 = 24ms ... (time doubles with every step) 1010 or higher = 6.14s |

Table 9 ALC Control

MAXIMUM GAIN

The MAXGAIN register sets the maximum gain value that the PGA can be set to whilst under the control of the ALC. This has no effect on the PGA when ALC is not enabled.

PEAK LIMITER

To prevent clipping when a large signal occurs just after a period of quiet, the ALC circuit includes a limiter function. If the ADC input signal exceeds 87.5% of full scale (-1.16dB), the PGA gain is ramped down at the maximum attack rate (as when $\text{ATK} = 0000$), until the signal level falls below 87.5% of full scale. This function is automatically enabled whenever the ALC is enabled.

(Note: If $\text{ATK} = 0000$, then the limiter makes no difference to the operation of the ALC. It is designed to prevent clipping when long attack times are used).

NOISE GATE

When the signal is very quiet and consists mainly of noise, the ALC function may cause “noise pumping”, i.e. loud hissing noise during silence periods. The WM9712L has a noise gate function that prevents noise pumping by comparing the signal level at the input pins (i.e. before the record PGA) against a noise gate threshold, NGTH. Provided that the noise gate function is enabled ($\text{NGAT} = 1$), the noise gate cuts in when:

- Signal level at ADC [dB] < NGTH [dB] + PGA gain [dB] + Mic Boost gain [dB]

This is equivalent to:

- Signal level at input pin [dB] < NGTH [dB]

The PGA gain is then held constant (preventing it from ramping up as it normally would when the signal is quiet). If the NGG bit is set, the ADC output is also muted when the noise gate cuts in.

The table below summarises the noise gate control register. The NGTH control bits set the noise gate threshold with respect to the ADC full-scale range. The threshold is adjusted in 1.5dB steps. Levels at the extremes of the range may cause inappropriate operation, so care should be taken with set-up of the function. Note that the noise gate only works in conjunction with the ALC function, and always operates on the same channel(s) as the ALC (left, right, both, or none).

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---------------------------------|-----|-----------|---------|--|
| 62h ALC / Noise Gate Control | 7 | NGAT | 0 | Noise gate function enable 1 = enable 0 = disable |
| | 5 | NGG | 0 | Noise gate type 0 = PGA gain held constant 1 = mute ADC output |
| | 4:0 | NGTH(4:0) | 00000 | Noise gate threshold 00000: -76.5dBFS 00001: -75dBFS ... 1.5 dB steps 11110: -31.5dBFS 11111: -30dBFS |

Table 10 Noise Gate Control

AUDIO DACS

STEREO DAC

The WM9712L has a stereo sigma-delta DAC that achieves high quality audio playback at low power consumption. Digital tone control, adaptive bass boost and 3-D enhancement functions operate on the digital audio data before it is passed to the stereo DAC. (Contrary to the AC'97 specification, they have no effect on analogue input signals or signals played through the auxiliary DAC. Nevertheless, the ID2 and ID5 bits in the reset register, 00h, are set to '1' to indicate that the WM9712L supports tone control and bass boost.)

The DAC output has a PGA for volume control. The DAC sample rate can be controlled by writing to a control register (see "Variable Rate Audio"). It is independent of the ADC sample rate. The left and right DACs can be separately powered down using the PD13 and PD14 control bits, whereas the PR1 bit disables both DACs (see "Power Management" section).

STEREO DAC VOLUME

The volume of the DAC output signal is controlled by a PGA (Programmable Gain Amplifier). It can be mixed into the headphone, speaker and phone output paths (see "Audio Mixers").

| REGISTER ADDRESS | BIT | LABEL | DEFAULT | DESCRIPTION |
|---------------------------------------|------|-------------|----------------|--|
| 18h DAC Volume | 15 | D2H | 1 | Mute DAC path to headphone mixer 1: Mute, 0: No mute (ON) |
| | 14 | D2S | 1 | Mute DAC path to speaker mixer 1: Mute, 0: No mute (ON) |
| | 13 | D2P | 1 | Mute DAC path to phone mixer 1: Mute, 0: No mute (ON) |
| | 12:8 | DACL VOL | 01000 (0dB) | Left DAC Volume 00000: +12dB ... (1.5dB steps) 11111: -34.5dB |
| | 4:0 | DACR VOL | 01000 (0dB) | Right DAC Volume similar to DACLVOL |
| 5Ch Additional Functions (1) | 15 | AMUTE | 0 | Read-only bit to indicate auto-muting 1: DAC auto-muted 0: DAC not muted |
| | 7 | AMEN | 0 | DAC Auto-Mute Enable 1: Automatically mutes analogue output of stereo DAC if digital input is zero 0: Auto-mute OFF |

Table 11 Stereo DAC Volume Control