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WM9714L

AC'97 Audio Codec

DESCRIPTION

The WM9714L is a highly integrated input/output device designed for mobile computing and communications.

The chip is architected for dual CODEC operation, supporting hi-fi stereo CODEC functions via the AC link interface, and additionally supporting voice CODEC functions via a PCM type Synchronous Serial Port (SSP). A third, auxiliary DAC is provided which may be used to support generation of supervisory tones, or ring-tones at different sample rates to the main CODEC.

The device can connect directly to mono or stereo microphones, stereo headphones and a stereo speaker, reducing total component count in the system. Cap-less connections to the headphones, speakers, and earpiece may be used, saving cost and board area. Additionally, multiple analogue input and output pins are provided for seamless integration with analogue connected wireless communication devices.

All device functions are accessed and controlled through a single AC-Link interface compliant with the AC'97 standard. The 24.576 MHz master clock can be input directly or generated internally from a 13MHz (or other frequency) clock by an on-chip PLL. The PLL supports a wide range of input clock from 2.048MHz to 78.6MHz.

The WM9714L operates at supply voltages from 1.8V to 3.6V. Each section of the chip can be powered down under software control to save power. The device is available in a small leadless 7x7mm QFN package, ideal for use in hand-held portable systems.

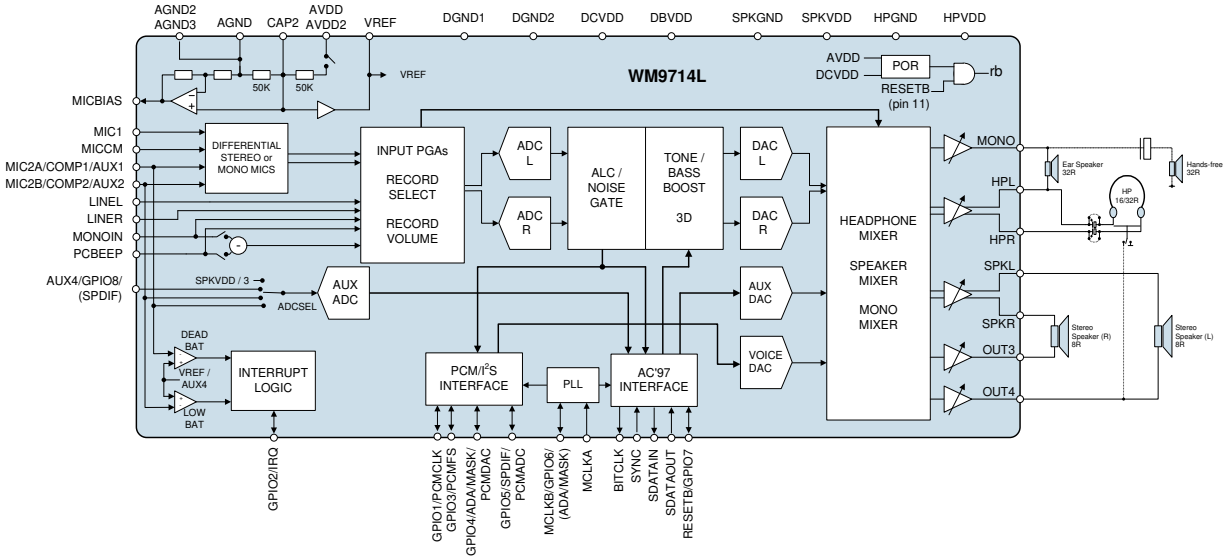
FEATURES

- AC'97 Rev 2.2 compatible stereo CODEC
  - DAC SNR 94dB, THD –85dB
  - ADC SNR 87dB, THD –86dB
  - Variable Rate Audio, supports all WinCE sample rates
  - Tone Control, Bass Boost and 3D Enhancement
- On-chip 45mW headphone driver
- On-chip 400mW mono or stereo speaker drivers
- Stereo, mono or differential microphone input
  - Automatic Level Control (ALC)
  - Mic insert and mic button press detection
- Auxiliary mono DAC (ring tone or DC level generation)
- Seamless interface to wireless chipset
- Additional PCM/I^{2}S interface to support voice CODEC
- PLL derived audio clocks.
- Supports input clock ranging from 2.048MHz to 78.6MHz
- 1.8V to 3.6V supplies (digital down to 1.62V, speaker up to 4.2V)
- 7x7mm 48-lead QFN package

APPLICATIONS

- Smartphones
- Personal Digital Assistants (PDA)
- Handheld and Tablet Computers

BLOCK DIAGRAM



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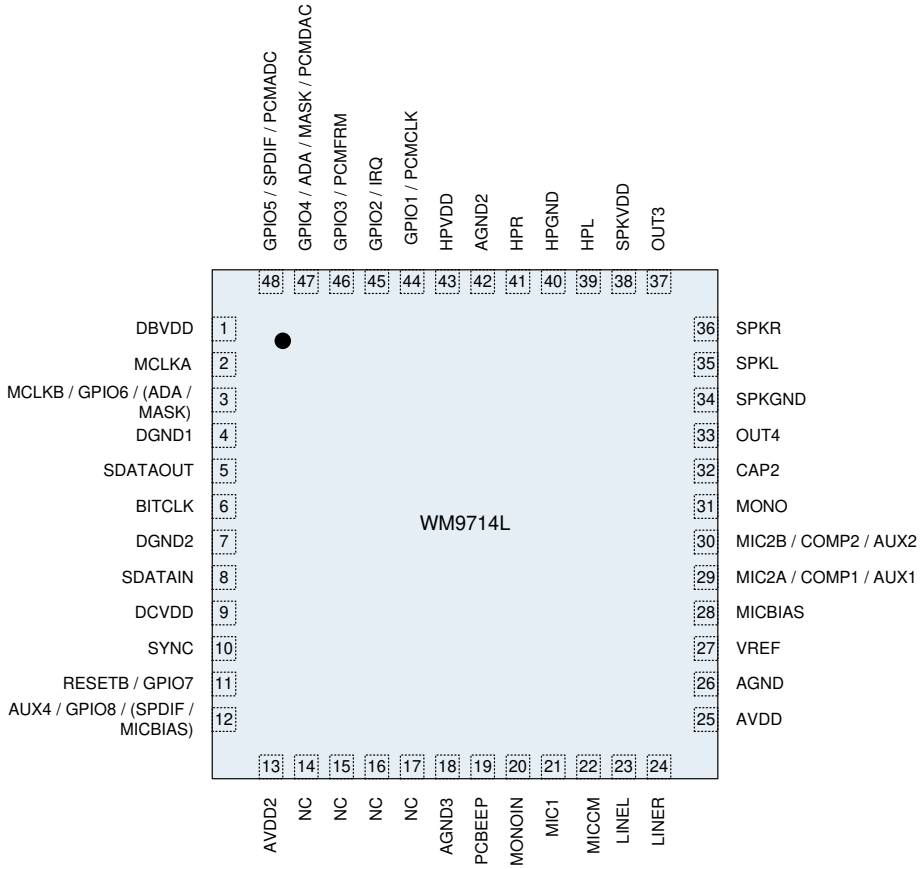
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM9714CLGEFL/V	-25 to +85ºC	48-lead QFN (Pb-free)	MSL3	260ºC
WM9714CLGEFL/RV	-25 to +85ºC	48-lead QFN (Pb-free, tape and reel)	MSL3	260ºC

Note:

Reel quantity = 2,200

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	DBVDD	Supply	Digital I/O Buffer Supply
2	MCLKA	Digital Input	Master Clock A Input
3	MCLKB / GPIO6 / (ADA / MASK)	Digital In/Out	Master Clock B Input / GPIO6 / (ADA output / MASK input)
4	DGND1	Supply	Digital Ground (return path for both DCVDD and DBVDD)
5	SDATAOUT	Digital Input	Serial Data Output from Controller / Input to WM9714L
6	BITCLK	Digital Output	Serial Interface Clock Output to Controller

PIN	NAME	TYPE	DESCRIPTION
7	DGND2	Supply	Digital Ground (return path for both DCVDD and DBVDD)
8	SDATAIN	Digital Output	Serial Data Input to Controller / Output from WM9714L
9	DCVDD	Supply	Digital Core Supply
10	SYNC	Digital Input	Serial Interface Synchronisation Pulse from Controller
11	RESETB / GPIO7	Digital In / Out	Reset (asynchronous, active Low, resets all registers to their default) / GPIO7
12	AUX4 / GPIO8 / (S/PDIF)	Analogue In / Out	Auxiliary ADC input / GPIO8 / (S/PDIF digital audio output)
13	AVDD2	Supply	Analogue Supply
14	NC	Analogue Input	Do not connect
15	NC	Analogue Input	Do not connect
16	NC	Analogue Input	Do not connect
17	NC	Analogue Input	Do not connect
18	AGND3	Supply	Analogue Ground
19	PCBEEP	Analogue Input	Line Input to analogue audio mixers, typically used for beeps
20	MONOIN	Analogue Input	Mono Input (RX)
21	MIC1	Analogue Input	Microphone preamp A input 1
22	MICCM	Analogue Input	Microphone common mode input
23	LINEL	Analogue Input	Left Line Input
24	LINER	Analogue Input	Right Line Input
25	AVDD	Supply	Analogue Supply (audio DACs, ADCs, PGAs, mic amps, mixers)
26	AGND	Supply	Analogue Ground
27	VREF	Analogue Output	Internal Reference Voltage (buffered CAP2)
28	MICBIAS	Analogue Output	Bias Voltage for Microphones (buffered CAP2 × 1.8)
29	MIC2A / COMP1 / AUX1	Analogue Input	Microphone preamp A input 2 / COMP1 input / Auxiliary ADC input
30	MIC2B / COMP2 / AUX2	Analogue Input	Microphone preamp B input / COMP2 input / Auxiliary ADC input
31	MONO	Analogue output	Mono output driver (line or headphone)
32	CAP2	Analogue In / Out	Internal Reference Voltage (normally AVDD/2, if not overdriven)
33	OUT4	Analogue Output	Auxiliary output driver (speaker, line or headphone)
34	SPKGND	Supply	Speaker ground (feeds output buffers on pins 33, 35, 36 and 37)
35	SPKL	Analogue Output	Left speaker driver (speaker, line or headphone)
36	SPKR	Analogue Output	Right speaker driver (speaker, line or headphone)
37	OUT3	Analogue Output	Auxiliary output driver (speaker, line or headphone)
38	SPKVDD	Supply	Speaker supply (feeds output buffers on pins 33, 35, 36 and 37)
39	HPL	Analogue Output	Headphone left driver (line or headphone)
40	HPGND	Supply	Headphone ground (feeds output buffers on pins 39 and 41)
41	HPR	Analogue Output	Headphone right driver (line or headphone)
42	AGND2	Supply	Analogue ground, chip substrate
43	HPVDD	Supply	Headphone supply (feeds output buffers on pins 39 and 41)
44	GPIO1 / PCMCLK	Digital In / Out	GPIO Pin 1 / PCM interface clock
45	GPIO2 / IRQ	Digital In / Out	GPIO Pin 2 / IRQ (Interrupt Request) output
46	GPIO3 / PCMFS	Digital In / Out	GPIO Pin 3 / PCM frame signal
47	GPIO4 / ADA / MASK / PCMDAC	Digital In / Out	GPIO Pin 4 / ADA (ADC data available) output or Mask input / PCM input (DAC) data
48	GPIO5 / S/PDIF / PCMADC	Digital In / Out	GPIO Pin 5 / S/PDIF digital audio output / PCM output (ADC) data
49	GND_PADDLE		Die Paddle (Note 1)

Notes:

1. It is recommended that the GND_PADDLE is connected to analogue ground. Refer to “Recommended External Components” and “Package Dimensions” for further information.

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

Cirrus Logic tests its package types according to IPC/JEDEC J-STD-020B for Moisture Sensitivity to determine acceptable storage conditions prior to surface mount assembly. These levels are:

MSL1 = unlimited floor life at <30°C / 85% Relative Humidity. Not normally stored in moisture barrier bag.
MSL2 = out of bag storage for 1 year at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.
MSL3 = out of bag storage for 168 hours at <30°C / 60% Relative Humidity. Supplied in moisture barrier bag.

The Moisture Sensitivity Level for each package type is specified in Ordering Information.

CONDITION	MIN	MAX
Digital supply voltages (DCVDD, DBVDD)	-0.3V	+3.63V
Analogue supply voltages (AVDD, AVDD2, HPVDD)	-0.3V	+3.63V
Speaker supply voltage (SPKVDD)	-0.3V	+4.2V
Voltage range digital inputs	DGND -0.3V	DBVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Operating temperature range, T_A	-25ºC	+85ºC

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital input/output buffer supply range	DBVDD		1.71	3.3	3.6	V
Digital core supply range	DCVDD		1.71	1.8	3.6	V
Analogue supply range	AVDD, AVDD2, HPVDD		1.8	3.3	3.6	V
Speaker supply range	SPKVDD		1.8	3.3	4.2	V
Digital ground	DGND1, DGND2			0		V
Analogue ground	AGND, AGND3, HPGND, SPKGND			0		V
Difference AGND to DGND		Note 1	-0.3	0	+0.3	V

Note:

1. AGND is normally the same as DGND1/DGND2
2. DCVDD <= DBVDD and DCVDD <= AVDD
3. DCVDD should be >=2V when using the PLL

ELECTRICAL CHARACTERISTICS

AUDIO OUTPUTS

Test Conditions

DBVDD=3.3V, DCVDD = 3.3V, AVDD=HPVDD=SPKVDD =3.3V, T_A = +25ºC, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC to Line-Out (HPL/R, SPKL/R or MONO with 10kΩ / 50pF load)						
Full-scale output (0dBFS)		AVDD = 3.3V, PGA gains set to 0dB		1		V rms
Signal to Noise Ratio (A-weighted)	SNR		85	94		dB
Total Harmonic Distortion	THD	-3dB output		-85	-74	dB
Power Supply Rejection	PSRR	100mV, 20Hz to 20kHz signal on AVDD		50		dB
Speaker Output (SPKL/SPKR with 8Ω bridge tied load, INV=1)						
Output Power at 1% THD	P_O	THD = 1%		400		mW (rms)
Abs. max output power	$P_O$max			500		mW (rms)
Total Harmonic Distortion	THD	P_O = 200mW		-66 0.05		dB %
Signal to Noise Ratio (A-weighted)	SNR			90		dB
Stereo Speaker Output (SPKL/OUT4 and SPKR/OUT3 with 8Ω bridge tied load, INV=1)						
Output Power at 1% THD	P_O	THD = 1%		400		mW (rms)
Abs. max output power	$P_O$max			500		mW (rms)
Total Harmonic Distortion	THD	P_O = 200mW		-66 0.05		dB %
Signal to Noise Ratio (A-weighted)	SNR			90		dB
Headphone Output (HPL/R, OUT3/4 or SPKL/SPKR with 16Ω or 32Ω load)						
Output Power per channel	P_O	Output power is very closely correlated with THD; see below.				
Total Harmonic Distortion	THD	P_O=10mW, R_L=16Ω		-80		dB
		P_O=10mW, R_L=32Ω		-80		
		P_O=20mW, R_L=16Ω		-78		
		P_O=20mW, R_L=32Ω		-79		
Signal to Noise Ratio (A-weighted)	SNR			90		dB

Note:

1. All THD values are valid for the output power level quoted above – for example, at HPVDD=3.3V and R_L=16Ω, THD is –80dB when output power is 10mW. Higher output power is possible, but will result in deterioration in THD.

AUDIO INPUTS

Test Conditions

DBVDD=3.3V, DCVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
LINEL/R, MIC1/2A/2B, MONOIN and PCBEEP pins						
Full Scale Input Signal Level (0dBFS)	V_{INFS}	AVDD = 3.3V		1.0		Vrms
		AVDD = 1.8V		0.545		
		differential input mode (MS = 01) AVDD = 3.3V		0.5		
		differential input mode (MS = 01) AVDD = 1.8V		0.273		
Input Resistance	R_{IN}	0dB PGA gain	25.6	32	38.4	kΩ
		12dB PGA gain	10.4	13	15.6	
Input Capacitance				5		pF
Line input to ADC (LINEL, LINER, MONOIN)						
Signal to Noise Ratio (A-weighted)	SNR		80	87		dB
Total Harmonic Distortion	THD	-3dBFS input		-86	-80	dB
Power Supply Rejection	PSRR	20Hz to 20kHz		50		dB
Microphone input to ADC (MIC1/2A/2B pins)						
Signal to Noise Ratio (A-weighted)	SNR	20dB boost enabled		80		dB
Total Harmonic Distortion	THD	20dB boost enabled		-80		dB

AUXILIARY MONO DAC (AUXDAC)

Test Conditions

DBVDD=3.3V, DCVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 8kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				12		bits
Full scale output voltage		AVDD=3.3V		1		Vrms
Signal to Noise Ratio (A-weighted)	SNR			TBD		dB
Total Harmonic Distortion	THD			TBD		dB

PCM VOICE DAC (VXDAC)

Test Conditions

DBVDD=3.3V, DCVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 8kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				16		bits
Sample rates				8	16	Ks/s
Full scale output voltage		AVDD=3.3V		1		Vrms
Signal to Noise Ratio (A-weighted)	SNR			80		dB
Total Harmonic Distortion	THD			74		dB

AUXILIARY ADC

Test Conditions

DBVDD = 3.3V, DCVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Pins AUX4, COMP1/AUX1, COMP2/AUX2						
Input Voltage			AGND		AVDD	V
Input leakage current		AUX pin not selected as AUX ADC input		<10		nA
ADC Resolution				12		bits
Differential Non-Linearity Error	DNL			±0.25	±1	LSB
Integral Non-Linearity Error	INL				±2	LSB
Offset Error					±4	LSB
Gain Error					±6	LSB
Power Supply Rejection	PSRR			50		dB
Channel-to-channel isolation				80		dB
Throughput Rate		DEL = 1111 (zero settling time)			48	kHz
Settling Time (programmable)		MCLK = 24.576MHz	0		6	ms

COMPARATORS

Test Conditions

DBVDD = 3.3V, DCVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMP1/AUX1 and COMP2/AUX2 (pins 29, 30 – when not used as mic inputs)						
Input Voltage			AGND		AVDD	V
Input leakage current		pin not selected as AUX ADC input		<10		nA
Comparator Input Offset (COMP1, COMP2 only)			-50		+50	mV
COMP2 delay (COMP2 only)		MCLK = 24.576MHz	0		10.9	s

REFERENCE VOLTAGES

Test Conditions

DBVDD=3.3V, DCVDD = 3.3V, AVDD = 3.3V, T_A = +25°C, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio ADCs, DACs, Mixers						
Reference Input/Output	CAP2 pin		1.63	1.65	1.66	V
Buffered Reference Output	VREF pin		1.64	1.65	1.67	V
Microphone Bias						
Bias Voltage	$V_{MICBIAS}$		2.92	2.97	3.00	V
Bias Current Source	$I_{MICBIAS}$				3	mA
Output Noise Voltage	Vn	1K to 20kHz		15		nV/√Hz

DIGITAL INTERFACE CHARACTERISTICS

Test Conditions

DBVDD = 3.3V, DCVDD = 3.3V, T_A = +25ºC, unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (all digital input or output pins) – CMOS Levels						
Input HIGH level	V_{IH}		DBVDD×0.7			V
Input LOW level	V_{IL}				DBVDD×0.3	V
Output HIGH level	V_{OH}	source current = 2mA	DBVDD×0.9			
Output LOW level	V_{OL}	sink current = 2mA			DBVDD×0.1	
Clock Frequency						
Master clock (MCLKA pin)				24.576		MHz
AC'97 bit clock (BIT_CLK pin)				12.288		MHz
AC'97 sync pulse (SYNC pin)				48		kHz

Note:

1. All audio and non-audio sample rates and other timing scales proportionately with the master clock.
2. For signal timing on the AC-Link, please refer to the AC'97 specification (Revision 2.2)

POWER CONSUMPTION

The power consumption of the WM9714L depends on the following factors:

- Supply voltages: Reducing the supply voltages also reduces digital supply currents, end therefore results in significant power savings especially in the digital sections of the WM9714L.
- Operating mode: Significant power savings can be achieved by always disabling parts of the WM9714L that are not used (e.g. audio ADC, DAC, AUXADC).
- Sample rates: Running at lower sample rates will reduce power consumption significantly. The figures below are for 48kHz (unless otherwise specified), but in many scenarios it is not necessary to run at this frequency, e.g. 8kHz PCM voice call scenario uses only 11.4mW (see below).

MODE DESCRIPTION	AVDD Supply Current V / mA		DCVDD Supply Current V / mA		DBVDD Supply Current V / mA		Total Power (mW)
Off (lowest possible power) Clocks stopped. This is the default configuration after power-up.	3.3	0.01	3.3	0	3.3	0.005	0.05
LPS (Low Power Standby) VREF maintained using 1MOhm string	3.3	0.014	3.3	0	3.3	0.005	0.06
PCM Voice call (fs=8kHz)	2.8	2.37	2.8	1.7	2.8	0.006	11.4
Record from mono microphone	3.3	3.644	3.3	10.973	3.3	2.974	58.05
Stereo DAC Playback (AC link to headphone)	3.3	3.733	3.3	9.720	3.3	2.789	53.60
Stereo DAC Playback (AC link to headphone) PLL running with 13MHz input to MCLKB	3.3	4.801	3.3	10.504	3.3	2.814	59.79
Maximum Power - everything on	3.3	13.656	3.3	15.472	3.3	2.938	105.82

Table 1 Supply Current Consumption

Notes:

1. Unless otherwise specified, all figures are at TA = +25C, audio sample rate fs = 48kHz, with zero signal (quiescent), and voltage references settled.
2. The power dissipated in headphones and speakers is not included in the above table.

SIGNAL TIMING REQUIREMENTS

AC97 INTERFACE TIMING

CLOCK SPECIFICATIONS

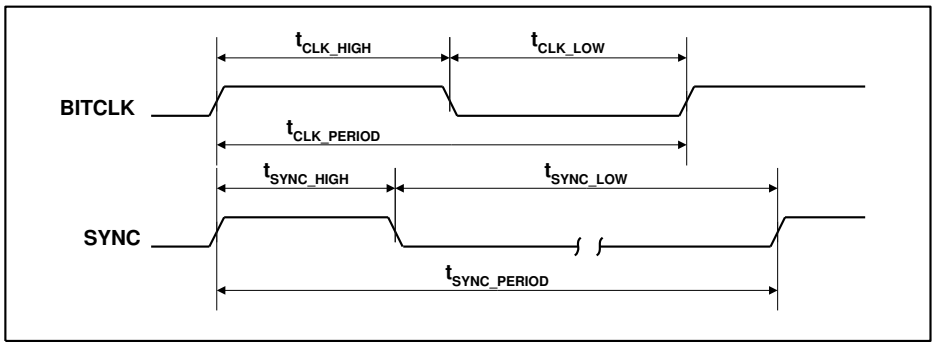


Figure 1 Clock Specifications (50pF External Load)

Test Conditions

DBVDD = 3.3V, DCVDD = 3.3V, DGND1 = DGND2 = 0V, T_A = -25°C to +85°C, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
BITCLK frequency			12.288		MHz
BITCLK period	t_{CLK_PERIOD}		81.4		ns
BITCLK output jitter				750	ps
BITCLK high pulse width (Note 1)	t_{CLK_HIGH}	36	40.7	45	ns
BITCLK low pulse width (Note 1)	t_{CLK_LOW}	36	40.7	45	ns
SYNC frequency			48		kHz
SYNC period	t_{SYNC_PERIOD}		20.8		µs
SYNC high pulse width	t_{SYNC_HIGH}		1.3		µs
SYNC low pulse width	t_{SYNC_LOW}		19.5		µs

Note:

1. Worst case duty cycle restricted to 45/55

DATA SETUP AND HOLD

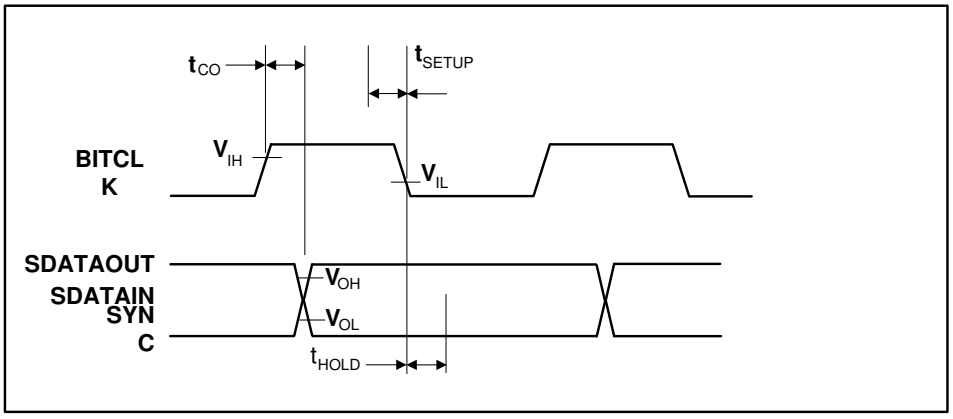


Figure 2 Data Setup and Hold (50pF External Load)

Note:

Setup and hold times for SDATAIN are with respect to the AC'97 controller, not the WM9713L.

Test Conditions

DBVDD = 3.3V, DCVDD = 3.3V, DGND1 = DGND2 = 0V, T_A = -25°C to +85°C, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Setup to falling edge of BITCLK	t_{SETUP}	10			ns
Hold from falling edge of BITCLK	t_{HOLD}	10			ns
Output valid delay from rising edge of BITCLK	t_{CO}			15	ns

SIGNAL RISE AND FALL TIMES

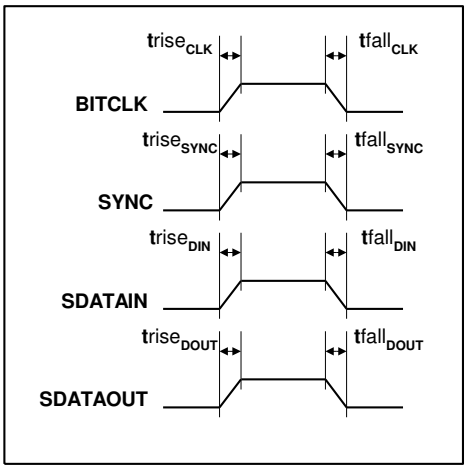


Figure 3 Signal Rise and Fall Times (50pF External Load)

Test Conditions

DBVDD = 3.3V, DCVDD = 3.3V, DGND1 = DGND2 = 0V, T_A = -25°C to +85°C, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
BITCLK rise time	trise$_{CLK}$	2		6	ns
BITCLK fall time	tfall$_{CLK}$	2		6	ns
SYNC rise time	trise$_{SYNC}$			6	ns
SYNC fall time	tfall$_{SYNC}$			6	ns
SDATAIN rise time	trise$_{DIN}$	2		6	ns
SDATAIN fall time	tfall$_{DIN}$	2		6	ns
SDATAOUT rise time	trise$_{DOUT}$			6	ns
SDATAOUT fall time	tfall$_{DOUT}$			6	ns

AC-LINK POWERDOWN

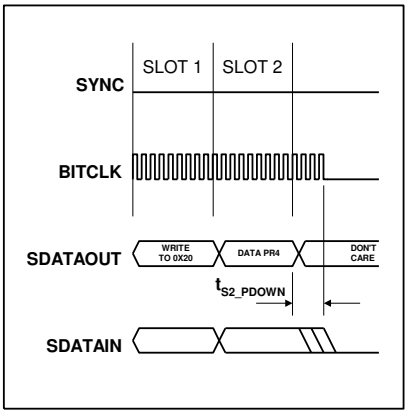


Figure 4 AC-Link Powerdown Timing

AC-Link powerdown occurs when PR4 (register 26h, bit 12) is set (see "Power Management").

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
End of Slot 2 to BITCLK and SDATAIN low	t_{S2_PDOWN}			1.0	µs

COLD RESET (ASYNCHRONOUS – RESETS REGISTER SETTINGS)

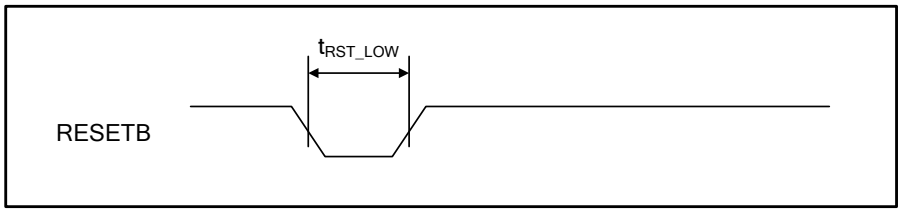


Figure 5 Cold Reset Timing

Note:

For correct operation SDATAOUT and SYNC must be held LOW for entire RESETB active low period otherwise the device may enter test mode. See AC'97 specification and Application Note WAN 0104 for further details.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
RESETB active low pulse width	t_{RST_LOW}	1.0			µs

WARM RESET (ASYNCHRONOUS – PRESERVES REGISTER SETTINGS)

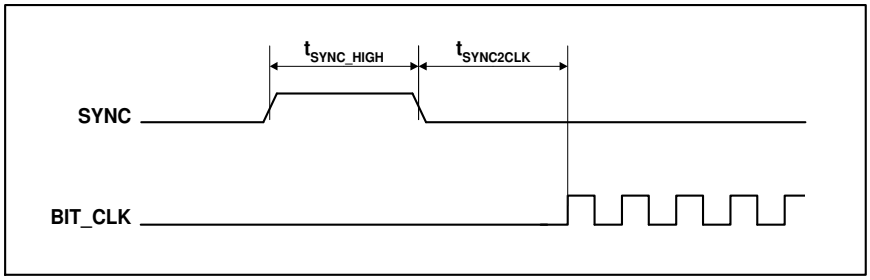


Figure 6 Warm Reset Timing

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SYNC active high pulse width	t_{SYNC_HIGH}		1.3		µs
SYNC inactive to BITCLK startup delay	$t_{RST2CLK}$	162.4			ns

PCM AUDIO INTERFACE TIMING – SLAVE MODE

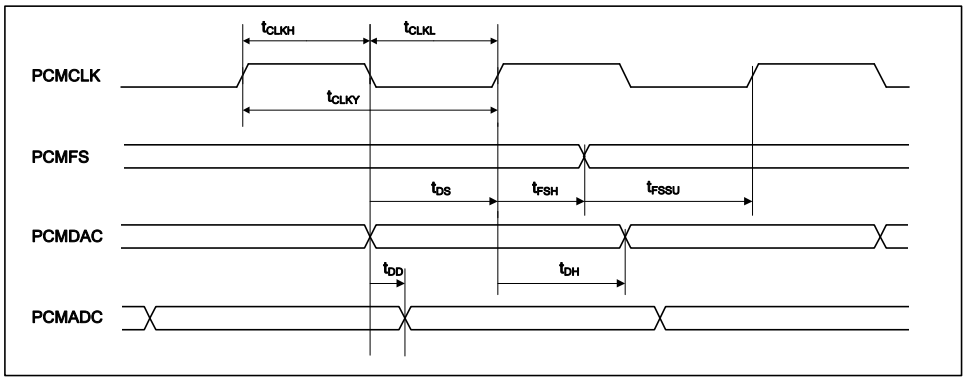


Figure 7 Digital Audio Data Timing – Slave Mode

Test Conditions

DBVDD = 3.3V, DCVDD = 3.3V, DGND1 = DGND2 = 0V, T_A = -25°C to +85°C, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
PCMCLK cycle time	t_{PCMY}	50			ns
PCMCLK pulse width high	t_{PCMH}	20			ns
PCMCLK pulse width low	t_{PCML}	20			ns
PCMFS set-up time to PCMCLK rising edge	t_{FSSU}	10			ns
PCMFS hold time from PCMCLK rising edge	t_{FSH}	10			ns
PCMDAC set-up time from PCMCLK rising edge	t_{DS}	10			ns
PCMDAC hold time from PCMCLK rising edge	t_{DH}	10			ns
PCMADC propagation delay from PCMCLK falling edge	t_{DD}			10	ns

Note:

1. PCMCLK period should always be greater than or equal to Voice CLK period.

PCM AUDIO INTERFACE TIMING – MASTER MODE

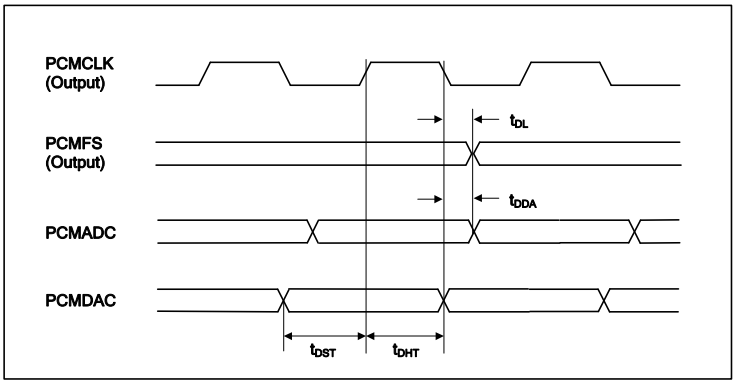


Figure 8 Digital Audio Data Timing – Master Mode (see Control Interface)

Test Conditions

DBVDD = 3.3V, DCVDD = 3.3V, DGND1 = DGND2 = 0V, T_A = -25°C to +85°C, unless otherwise stated.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information					
PCMFS propagation delay from PCMCLK falling edge	t_{DL}			10	ns
PCMADC propagation delay from PCMCLK falling edge	t_{DDA}			10	ns
PCMDAC setup time to PCMCLK rising edge	t_{DST}	10			ns
PCMDAC hold time from PCMCLK rising edge	t_{DHT}	10			ns

DEVICE DESCRIPTION

INTRODUCTION

The WM9714L is a largely pin-compatible upgrade to WM9712, with a PCM voice CODEC added. This CODEC is interfaced via a PCM type audio interface which makes use of GPIO pins for connection.

It is designed to meet the mixed-signal requirements of portable and wireless smartphone systems. It includes audio recording and playback, battery monitoring, auxiliary ADC and GPIO functions, all controlled through a single 5-wire AC-Link interface. Additionally, PCM voice CODEC functions are supported through provision of an additional voice DAC and a PCM audio serial interface.

A PLL is included to allow unrelated reference clocks to be used for generation of the AC link system clock. Typically 13MHz or 2.048MHz clock sources might be used as a reference.

SOFTWARE SUPPORT

The basic audio features of the WM9714L are software compatible with standard AC'97 device drivers. However, to better support additional functions, Cirrus Logic supplies custom device drivers for selected CPUs and operating systems. Please contact your local Cirrus Logic representative for more information.

AC'97 COMPATIBILITY

The WM9714L uses an AC'97 interface to communicate with a microprocessor or controller. The audio and GPIO functions are largely compliant with AC'97 Revision 2.2. The following **differences** from the AC'97 standard are noted:

- Pinout: The function of some pins has been changed to support device specific features. The PHONE and PCBEEP pins have been moved to different locations on the device package.
- Package: The default package for the WM9714L is a 7×7mm leadless QFN package.
- Audio mixing: The WM9714L handles all the audio functions of a smartphone, including audio playback, voice recording, phone calls, phone call recording, ring tones, as well as simultaneous use of these features. The AC'97 mixer architecture does not fully support this. The WM9714L therefore uses a modified AC'97 mixer architecture with three separate mixers.
- Tone Control, Bass Boost and 3D Enhancement: These functions are implemented in the digital domain and therefore affect only signals being played through the audio DACs, not all output signals as stipulated in AC'97.

Some other functions are **additional** to AC'97:

- On-chip BTL loudspeaker driver for mono or stereo speakers
- On-chip BTL driver for ear speaker (phone receiver)
- Auxiliary mono DAC for ring tones, system alerts etc.
- Auxiliary ADC Inputs
- 2 Analogue Comparators for Battery Alarm
- Programmable Filter Characteristics for Tone Control and 3D Enhancement
- PCM interface to additional Voice DAC and existing audio ADCs
- PLL to create AC'97 system clock from unrelated reference clock input

PCM CODEC

The PCM voice CODEC functions typically required by mobile telephony devices are provided by an extra voice DAC on the WM9714L, which is interfaced via a standard PCM type data interface, which is constructed through optional use of 4 of the GPIO pins on WM9714L. The audio output data from one or both of the audio ADCs can also be output over this PCM interface, allowing a full voice CODEC function to be implemented. This PCM interface supports sample rates from 8 to 48ks/s using the standard AC'97 master clock.

AUDIO PATHS OVERVIEW

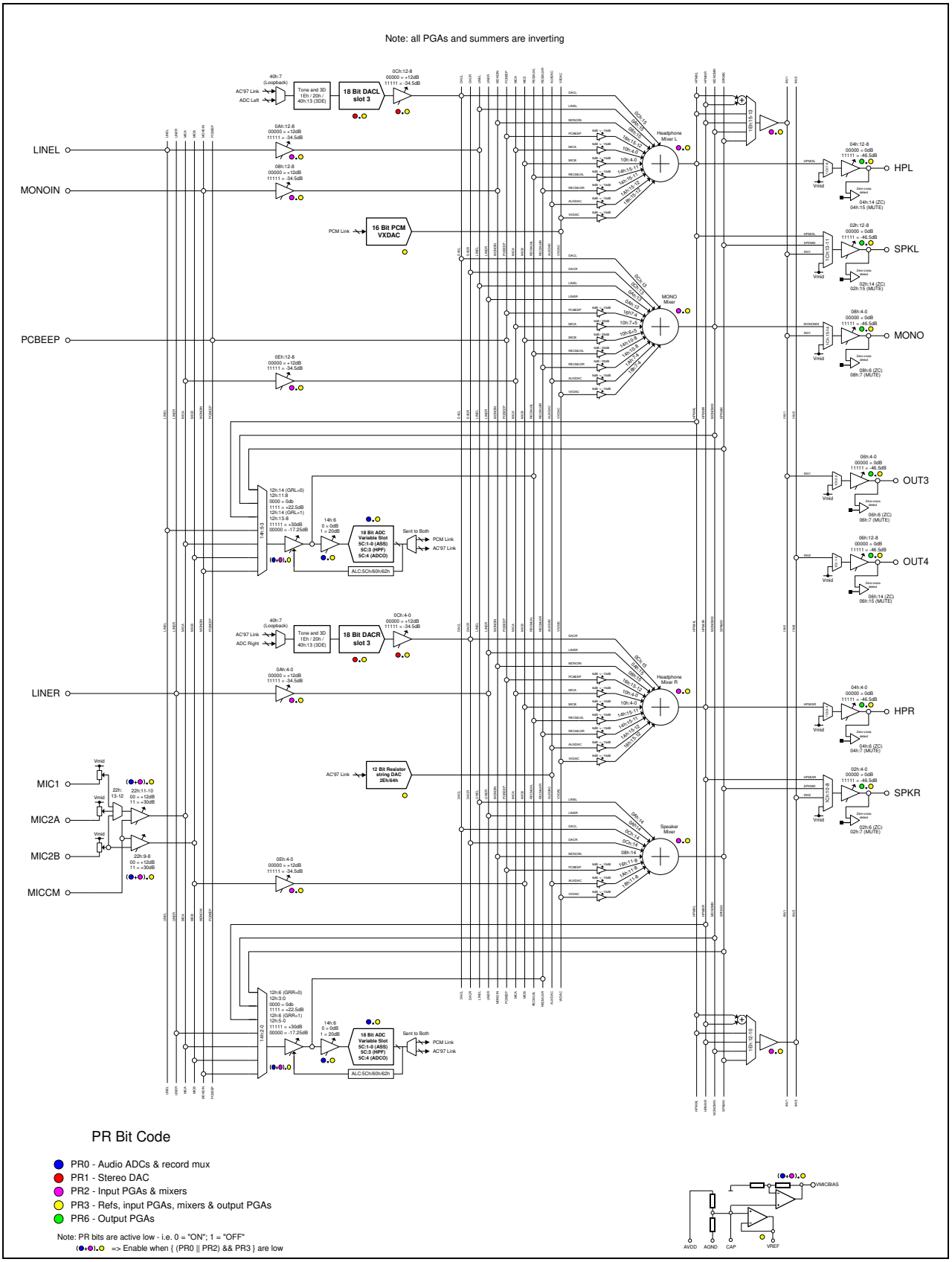


Figure 9 Audio Paths Overview

CLOCK GENERATION

WM9714L supports clocking from 2 separate sources, which can be selected via the AC'97 interface:

- External clock input MCLKA
- External clock input MCLKB

The source clock is divided to appropriate frequencies in order to run the AC'97 interface, PCM interface, voice DAC and Hi-fi DSP by means of a programmable divider block. Clock rates may be changed during operation via the AC'97 link in order to support alternative modes, for example low power mode when voice data is being transmitted only. A PLL is present to add flexibility in selection of input clock frequencies, typical choices being 2.048MHz, 4.096MHz or 13MHz.

INITIALISING THE AC'97 LINK

By default, the AC'97 link is disabled and therefore will not be running after power on or a COLD reset event. Before any register map configuration can begin, it is necessary to start the AC'97 link. This is achieved by sending a WARM reset to the CODEC as defined in Figure 6**.**

Default mode on power-up also assumes a clock will be present on MCLKA with the PLL powered down. After a WARM reset the CODEC will start the AC'97 link using MCLKA as a reference. This enables data to be clocked via the AC'97 link to define the desired clock divider mode and whether PLL needs to be activated.

Note: MCLKA can be any available frequency.

When muxing between MCLKA and MCLKB both clocks must be active for at least two clock cycles after the switching event.

CLOCK DIVISION MODES

Figure 10 shows the clocking strategy for WM9714L. Clocking is controlled by CLK_MUX, CLK_SRC and S[6:0].

- CLKAX2, CLKBX2 – clock doublers on inputs MCLKA and MCLKB.
- CLK_MUX - selects between MCLKA and MCLKB.
- CLK_SRC – selects between external or PLL derived clock reference.
- S[3:0] – sets the voice DAC clock rate and PCM interface clock when in master mode (division ratio 1 to 16 available).
- S[6:4] - sets the hi-fi clocking rate (division ratio 1 to 8 available).

The registers used to set these switches can be accessed from register address 44h (see Table 3).

If a mode change requires switching from an external clock to a PLL generated clock then it is recommended to set the clock division ratios required for the PLL clock scheme prior to switching between clocks. This option is accommodated by means of two sets of registers. S_{PLL}[6:0] is used to set the divide ratio of the clock when in PLL mode and S_{EXT}[6:0] is used to divide the clock when it is derived from an external source. If the PLL is selected (CLK_SRC = 0), S[6:0] = S_{PLL}[6:0]. S_{PLL}[6:0] is defined in register 46h (see Table 4) and is written to using the page address mode. More details on page address mode for controlling the PLL are found on page 24. Register 46h also contains a number of separate control bits relating to the PLL's function. If an external clock is selected (CLK_SRC = 1) S[6:0] = S_{EXT}[6:0]. S_{EXT}[6:0] is defined in register address 44h. Writing to registers 44h and 46h enables pre-programming of the required clock mode before the PLL output is selected.

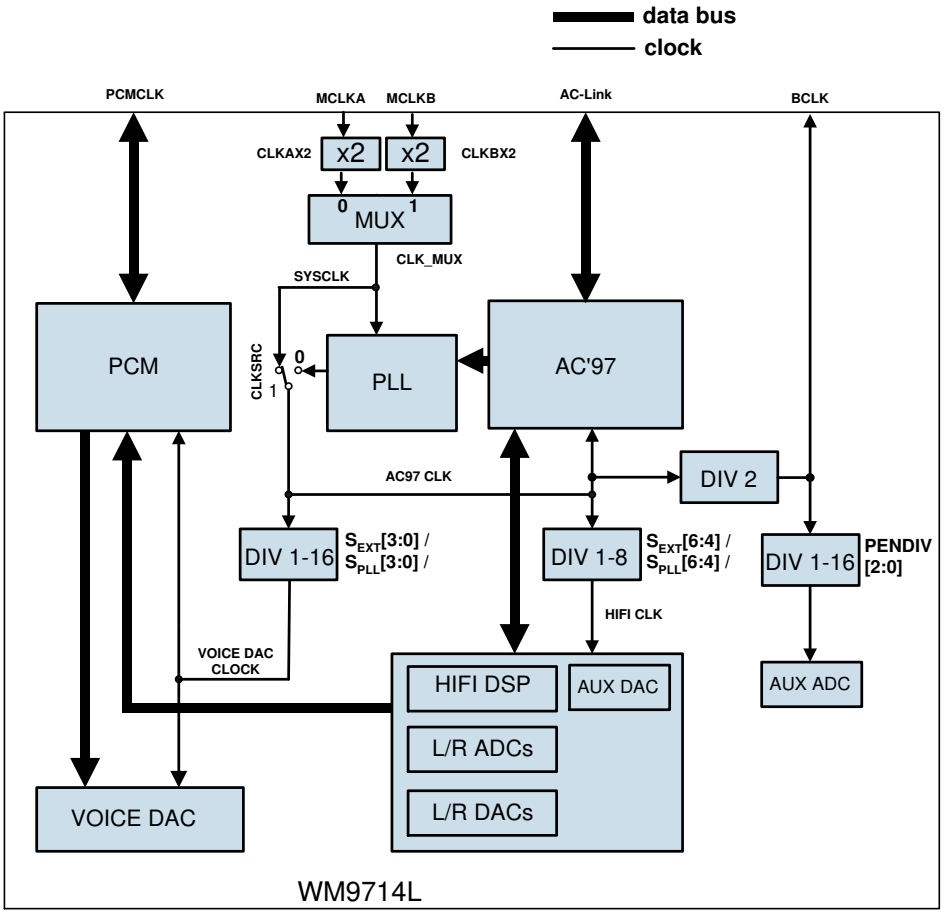


Figure 10 Clocking Architecture for WM9714L

INTERNAL CLOCK FREQUENCIES

The internal clock frequencies are defined as follows (refer to Figure 10):

- AC97 CLK – nominally 24.576MHz, used to generate AC97 BITCLK at 12.288MHz.
- HIFI CLK – for hi-fi playback at 48ks/s HIFI CLK = 24.576MHz. See Table 2 for voice only playback.
- Voice DAC CLK – see Table 2 for sample rate vs clock frequency.

SAMPLE RATE	VOICE DAC CLK FREQUENCY	HIFI CLK FREQUENCY
8ks/s voice and hi-fi	2.048MHz	24.576MHz
8ks/s voice only (power save)	2.048MHz	4.096MHz
16ks/s voice and hi-fi	4.096MHz	24.576MHz
16ks/s voice only (power save)	4.096MHz	8.192MHz
32ks/s voice and hi-fi	8.192MHz	24.576MHz
48ks/s voice and hi-fi	12.288MHz	24.576MHz

Table 2 Clock Division Mode Table

AUXADC

The clock for the AUXADC nominally runs at 768kHz and is derived from BITCLK. The divisor for the clock generator is set by PENDIV. This enables the AUXADC clock frequency to be set according to power consumption and conversion rate considerations.

Clock mode and division ratios are controlled by register 44h as shown in Table 3.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
44h	14:12	S_{EXT}[6:4]	000 (div 1)	Defines clock division ratio for Hi-fi: DSP, ADCs and DACs 000: f 001: f/2 ... 111: f/8
	11:8	S_{EXT}[3:0]	0000 (div 1)	Defines clock division ratio for PCM interface and voice DAC in external clock mode only: 0000: f 0001: f/2 … 1111: f/16
	7	CLKSRC	1 (ext clk)	Selects between PLL clock and External clock 0: PLL clock 1: external clock
	5:3	PENDIV	000 (div 16)	Sets AUXADC clock divisor 000: f/16 001: f/12 010: f/8 011: f/6 100: f/4 101: f/3 110: f/2 111: f
	2	CLKBX2	0 (Off)	Clock doubler for MCLKB
	1	CLKAX2	0 (Off)	Clock doubler for MCLKA
	0	CLKMUX	0 (MCLKA)	Selects between MCLKA and MCLKB (N.B. On power-up clock must be present on MCLKA and must be active for 2 clock cycles after switching to MCLKB) 0: SYSCLK=MCLKA 1: SYSCLK=MCLKB

Table 3 Clock Muxing and Division Control

PLL MODE

The PLL operation is controlled by register 46h (see Table 4) and has two modes of operation:

- Integer N
- Fractional N

The PLL has been optimized for nominal input clock (PLL_IN) frequencies in the range 8.192MHz – 19.661MHz (LF=0) and 2.048MHz – 4.9152MHz (LF=1). Through use of a clock divider (div by 2 / 4) on the input to the PLL frequencies up to 78.6MHz can be accommodated. The input clock divider is enabled by DIVSEL (0=Off) and the division ratio is set by DIVCTL (0=div2, 1=div4).

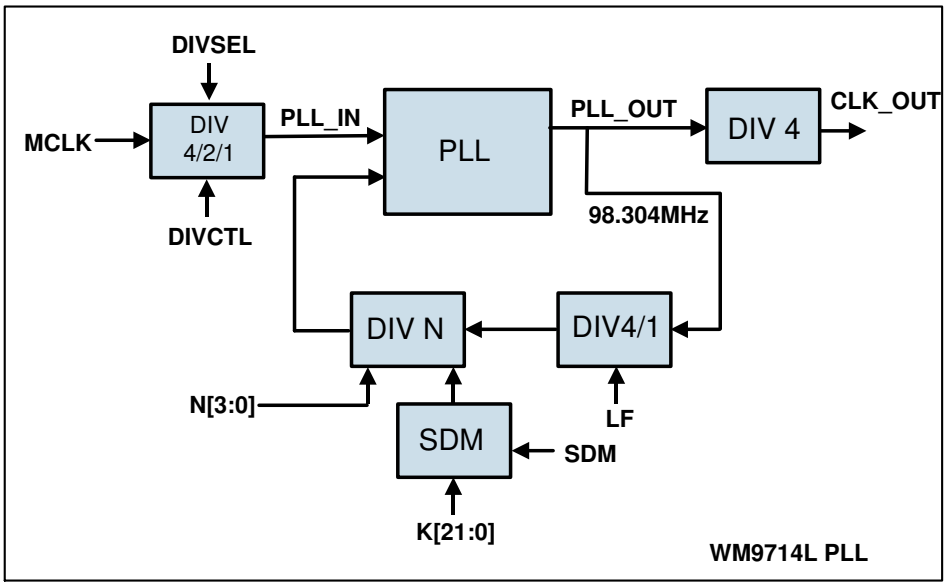


Figure 11 PLL Architecture

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
46h	15:12	N[3:0]	0000	**PLL N Divide Control** 0000 = Divide by 1 0001 = Divide by 1 0010 = Divide by 2 … 1111 = Divide by 15 **Note:** must be set between 05h and 0Ch for integer N mode
	11	LF	0 = off	**PLL Low Frequency Input Control** 1 = Low frequency mode (input clock < 8.192MHz) 0 = Normal mode
46h	10	SDM	0 = off	**PLL SDM Enable Control** 1 = Enable SDM (required for fractional N mode) 0 = Disable SDM
46h	9	DIVSEL	0 = off	**PLL Input Clock Division Control** 0 = Divide by 1 1 = Divide according to DIVCTL
	8	DIVCTL	0	**PLL Input Clock Division Value Control** 0 = Divide by 2 1 = Divide by 4
46h	6:4	PGADDR	000	**Pager Address** Pager address bits to access programming of K[21:0] and S_{PLL}[6:0]
46h	3:0	PGDATA	0000	**Pager Data** Pager data bits

Table 4 PLL Clock Control

INTEGER N MODE

The nominal output frequency of the PLL (PLL_OUT) is 98.304MHz which is divided by 4 to achieve a nominal system clock of 24.576MHz.

The integer division ratio (N) is determined by: F_{PLL_out} / F_{PLL_IN} , and is set by N[3:0] and must be in the range 5 to 12 for integer N operation (0101 = div by 5, 1100 = div by 12). Note that setting LF=1 enables a further division by 4 required for input frequencies in the range 2.048MHz – 4.096MHz.

Integer N mode is selected by setting SDM=0.

FRACTIONAL N MODE

Fractional N mode provides a divide resolution of $1/2^{22}$ and is set by K[21:0] (register 46h, see section). The relationship between the required division X, the fractional division K[21:0] and the integer division N[3:0] is:

$$K = 2^{22}(X - N)$$

where 0 < (X – N) < 1 and K is rounded to the nearest whole number.

For example, if the PLL_IN clock is 13MHz and the desired PLL_OUT clock is 98.304MHz then the desired division, X, is 7.5618. So N[3:0] will be 7h and K[21:0] will be 23F488h to produce the desired 98.304MHz clock (see Table 5).

INPUT CLOCK (PLL_IN)	DESIRED PLL OUTPUT (PLL_OUT)	DIVISION REQUIRED (X)	FRACTIONAL DIVISION (K)	INTEGER DIVISION (N)
2.048MHz	98.304MHz	48	0	12x4*
4.096MHz	98.304MHz	24	0	6x4*
12.288MHz	98.304MHz	8	0	8
13MHz	98.304MHz	7.5618	0.5618	7
27MHz (13.5MHz)**	98.304MHz	7.2818	0.2818	7
*Divide by 4 enabled in PLL feedback path for low frequency inputs. (LF = 1) **Divide by 2 enabled at PLL input for frequencies > 14.4MHz > 38MHz (DIVSEL = 1, DIVCTL = 0)				

Table 5 PLL Modes of Operation

PLL REGISTER PAGE ADDRESS MAPPING

The clock division control bits S_{PLL}[6:0] and the PLL fractional N division bits are accessed through register 46h using a sub-page address system. The 3-bit pager address allows 8 blocks of 4-bit data words to be accessed whilst the register address is set to 46h. This means that when register address 46h is selected a further 7 cycles of programming are required to set all of the page data bits. Control bit allocation for these page addresses is described in Table 6.

PAGE ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
111	31:28	S_{PLL}[6:4]	0h	Clock division control bus SPLL[6:0]. Clock divider reads this control word if PLL is enabled. Bits [6:4] and [3:0] have the same functionality as 44h [14:12] and [11:8] respectively
110	27:24	S_{PLL}[3:0]	0h	
101	23:22	Reserved	0h	Reserved bits
	21:20	K[21:0]	0h	Sigma Delta Modulator control word for fractional N division. Division resolution is $1/22^2$
100	19:16		0h	
011	15:12		0h	
010	11:8		0h	
001	7:4		0h	
000	3:0	S_{PLL}[3:0]	0h	

Table 6 Pager Control Bit Allocation

Powerdown for the PLL and internal clocks is via registers 26h and 3Ch (see Table 7).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
26h	13	PR5	1 (Off)	**Internal Clock Disable Control** 1 = Disabled 0 = Enabled
3Ch	9	PLL	1 (Off)	**PLL Disable Control** 1 = Disabled 0 = Enabled
N.B. both PR5 and PLL must be asserted low before PLL is enabled				

Table 7 PLL Powerdown Control

DIGITAL INTERFACES

The WM9714L has two interfaces, a data and control AC'97 interface and a data only PCM interface. The AC'97 interface is available through dedicated pins (SDATAOUT, SDATAIN, SYNC, BITCLK and RESETB) and is the sole control interface with access to all data streams on the device except for the Voice DAC. The PCM interface is available through the GPIO pins (PCMCLK, PCMFS, PCMDAC and PCMADC) and provides access to the Voice DAC. It can also transmit the data from the Stereo ADC. This can be useful, for example, to allow both sides of a phone conversation to be recorded by mixing the transmit and receive paths on one of the ADC channels and transmitting it over the PCM interface.

AC97 INTERFACE

INTERFACE PROTOCOL

The WM9714L uses an AC'97 interface for both data transfer and control. The AC-Link has 5 wires:

- SDATAIN (pin 8) carries data from the WM9714L to the controller
- SDATAOUT (pin 5) carries data from the controller to the WM9714L
- BITCLK (pin 6) is a clock, derived from either MCLKA or MCLKB inputs and supplied to the controller.
- SYNC is a synchronization signal generated by the controller and passed to the WM9714L
- RESETB resets the WM9714L to its default state

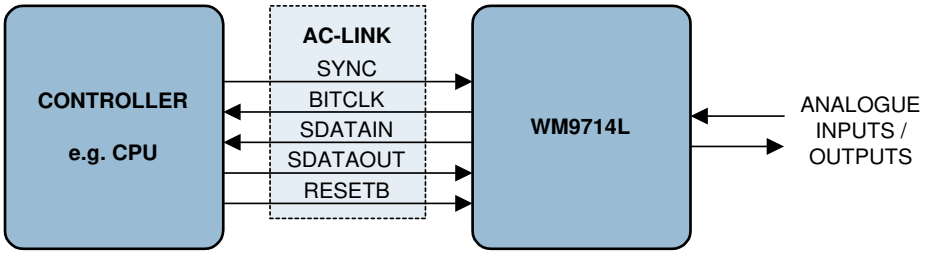


Figure 12 AC-Link Interface (typical case with BITCLK generated by the AC97 CODEC)

The SDATAIN and SDATAOUT signals each carry 13 time-division multiplexed data streams (slots 0 to 12). A complete sequence of slots 0 to 12 is referred to as an AC-Link frame, and contains a total of 256 bits. The frame rate is 48kHz. This makes it possible to simultaneously transmit and receive multiple data streams (e.g. audio, AUXADC, control) at sample rates up to 48kHz.

Detailed information can be found in the AC'97 (Revision 2.2) specification, which can be obtained at www.intel.com/design/chipsets/audio/

Note:

SDATAOUT and SYNC must be held low when RESETB is applied. These signals must be held low for the entire duration of the RESETB pulse and especially during the low-to-high transition of RESETB. If SDATAOUT or SYNC is high during reset, the WM9714L may enter test modes. Information relating to this operation is available in the AC'97 specification and in Application Note WAN 0104.

PCM INTERFACE

OPERATION

WM9714L can implement a PCM voice CODEC function using the dedicated VXDAC and either one or both of the existing hi-fi ADC's. In PCM CODEC mode, VXDAC input and ADC output are interfaced via a PCM style port via GPIO pins.

This interface can support one ADC channel, or stereo/dual ADC channels if required, (two channels of data are sent per PCM frame as back to back words).

In voice-only mode, the AC link is used only for control information, not audio data. Therefore it will generally be shut down (PR4=1), except when control data must be sent.

The PCM interface makes use of 4 of the GPIO interface pins, for clock, frame, and data in/out. If the PCM CODEC function is not enabled then the GPIO pins may be used for other functions.