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WMS7100/1

NONVOLATILE DIGITAL POTENTIOMETERS

WITH UP/DOWN (3-WIRE) INTERFACE,

10KOHM, 50KOHM, 100KOHM RESISTANCE

256 TAPS

WITH OPTIONAL OUTPUT BUFFER

1. GENERAL DESCRIPTION

The WMS710x is a 256 non-volatile linear digital potentiometers available in 10KΩ, 50KΩ and 100KΩ resistance values. The WMS7100/1 can be used as a three-terminal potentiometer or as a two terminal variable resistor in a wide variety of applications.

The output of each potentiometer is determined by the wiper position, which varies in linearly between V_A and V_B terminal according to the content stored in the volatile Tap Register (TR) which is programmed through Up/Down (Increment/Decrement) interface. The channel has one non-volatile memory location (NVMEM0) that can be directly written to by users through the Up/Down interface. Power-on recall is also built in so the content of the NVMEM0 to Tap Register is automatically loaded.

The WMS7100/1 devices pin out the resistor wiper directly. The WMS7101 devices feature an output buffer with 3mA minimum drive capability.

All the WMS7100/1 devices are single channel devices offered in 8-pin PDIP, SOIC and MSOP packages. The WMS7100/1 devices operate over a wide operating voltage ranging from 2.7V to 5.5V.

2. FEATURES

- Drop-in replacements for many popular parts
- Available output buffer for WMS7101 devices
- Single linear-taper channel
- 256 taps
- 10K, 50K and 100K end-to end resistance
- V_{SS} to V_{DD} terminal voltages
- Non-volatile storage of wiper positions with power-on recall
- Data storage and potentiometer control through Up/Down (3-wire) interface
- Endurance 100,000 write cycles
- Data retention 100 years
- Package options:
  - 8-pin PDIP, SOIC or MSOP
- Industrial temperature range: -40° ~ 85°C
- Single supply operation 2.7V to 5.5V

3. BLOCK DIAGRAM

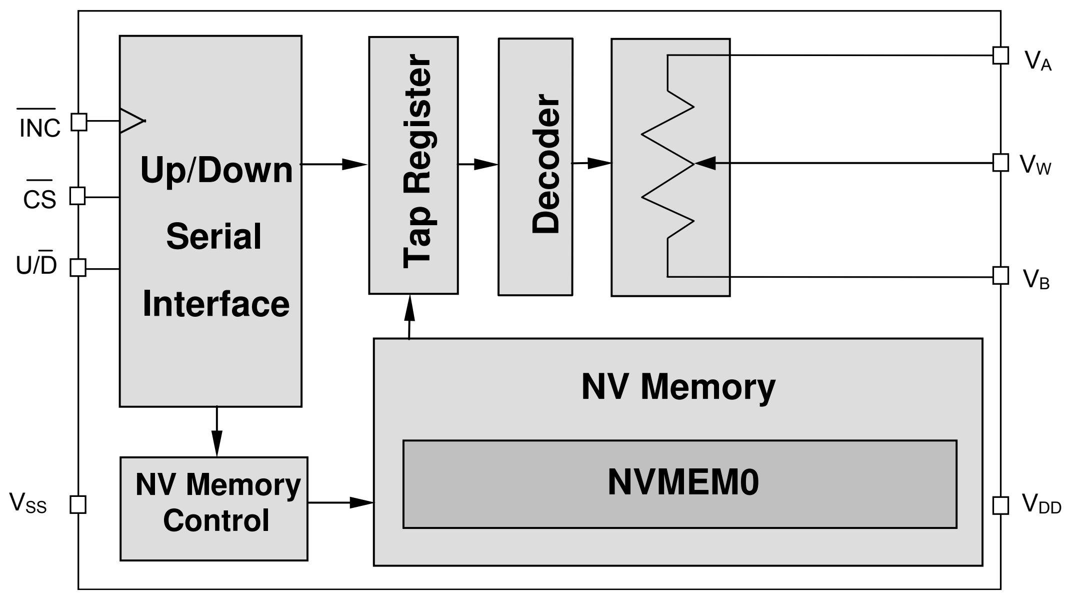

FIGURE 1 – WMS7100 BLOCK DIAGRAM (Rheostat Mode)

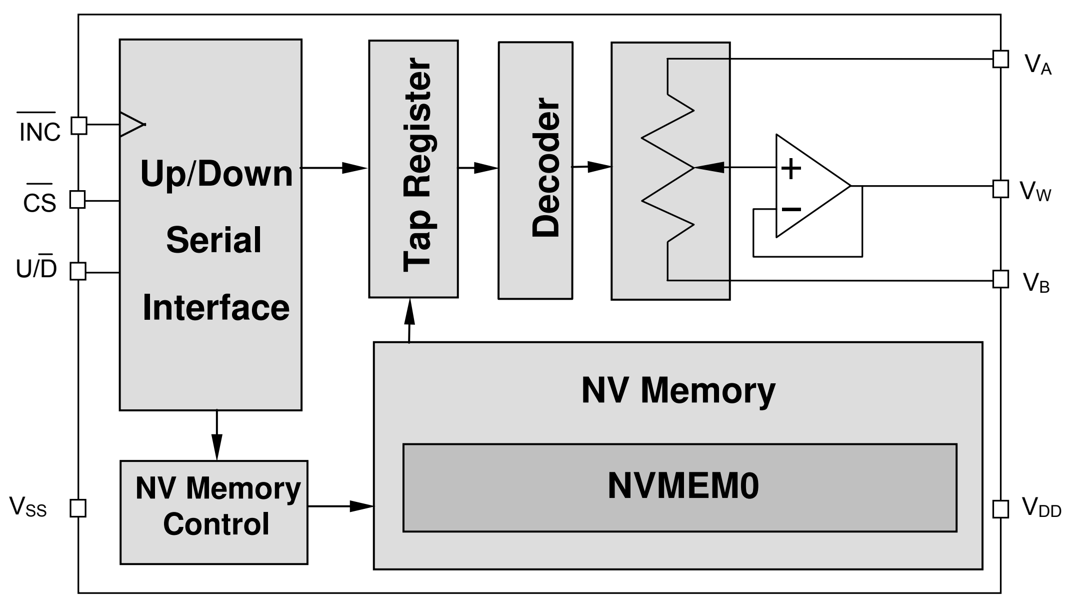

FIGURE 2 – WMS7101 BLOCK DIAGRAM (Divider Mode)

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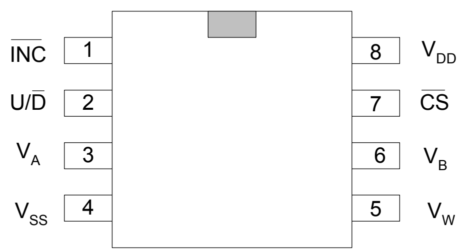
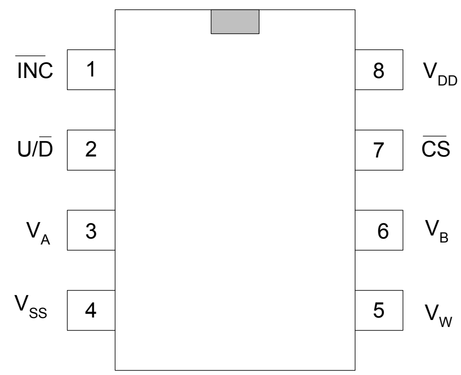
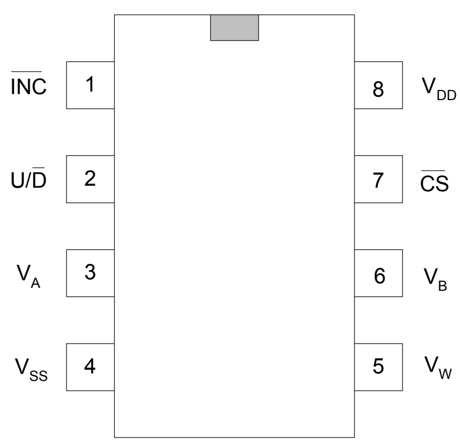
5. PIN CONFIGURATION



8-MSOP



8-SOIC



8-PDIP

6. PIN DESCRIPTION

TABLE 1 – PIN DESCRIPTION

Pin Name	I/O	Description
$\overline{INC}$	I	Increment Control. A High-Low transition of $\overline{INC}$ when $\overline{CS}$ is low will move the wiper up or down for one increment based on the $U/\overline{D}$ input
$U/\overline{D}$	I	Up/Down control Input. High state will cause the wiper to move to the V_B terminal, Low state to the V_A terminal
V_A	-	High terminal of WinPot
V_{SS}	-	Ground pin, logic ground reference
V_{DD}	-	Power Supply
$\overline{CS}$	I	Chip Select. When $\overline{CS}$ is HIGH, the part is deselected and the device will be in the standby mode. $\overline{CS}$ LOW enables the part, placing it in the active power mode
V_B	-	Low terminal of WinPot
V_W	O	Wiper terminal of WinPot (can be buffered), its position on the resistor array is controlled by the inputs on $\overline{INC}$, $U/\overline{D}$, and $\overline{CS}$

7. FUNCTIONAL DESCRIPTION

The WMS7100/1, a nonvolatile digitally programmable potentiometers with 256 taps, with or without output buffer, is designed to operate as both a potentiometer or a variable resistor depending upon the output configuration selected.

The chip can store up to one 8-bit word in a nonvolatile memory (NVMEM0) in order to set the tap register value when the device is powered up.

The WMS7100/1 is controlled by a serial Up-Down (3-wire) interface that allows setting the tap register value as well as storing data in the nonvolatile memory.

7.1. POTENTIOMETER AND RHEOSTAT MODES

The WMS7100/1 can operate as either a rheostat or as a potentiometer (voltage divider). When in the potentiometer configuration there are two possible modes. One is done using WMS7100 Winpot device without the output buffer and the other mode is done with WMS7101 WinPot device with the output buffer.

7.1.1. Rheostat Configuration

The WMS7100/1 acts as a two terminal resistive element in the rheostat configuration where one terminal can be connected to either the end point pins of the resistor (V_A and V_B) and the other terminal is the wiper (V_W) pin. This configuration controls the resistance between the two terminals and the resistance can be adjusted by sending the corresponding tap register setting to the WMS7100/1 or can also be set by loading a pre-set tap register value from nonvolatile memory NVMEM0 upon power up.

7.1.2. Potentiometer Configuration

In potentiometer configuration an input voltage is applied to either one of the end point pins (V_A or V_B). The voltage on the wiper pin will be proportional to the voltage difference between V_A and V_B and the wiper setting. The resistance cannot be directly measured in this configuration.

7.2. NON-VOLATILE MEMORY (NVMEM)

The WMS7100/1 has one NVMEM position available for storing the potentiometer setting. The NVMEM position can be directly written via the Up/Down interface. The potentiometer is loaded with the value stored in the NVMEM0 on power up.

7.3. SERIAL DATA INTERFACE

The Up/Down family has a 3-wire Serial Data Interface consisting of $\overline{CS}$, $\overline{INC}$, U/$\overline{D}$ pins. Only UP/DOWN operations can be performed. The key features of this interface include:

- Increment/Decrement operations on the tap register (TR)
- Direct refresh of tap register (TR) from internal NVMEM
- Nonvolatile storage of the present tap register value into the NVMEM and automatic recall at power up
- For WMS7101 devices, output buffer amplifier

7.4. OPERATION OVERVIEW

The wiper position or the Tap Register(TR) setting can only be changed by the UP/DOWN operation with the combination of $\overline{CS}$, U/$\overline{D}$, and $\overline{INC}$ signals. When $\overline{CS}$ is low, the part will be activated and the TR setting can be changed by toggling $\overline{INC}$, and TR will move up when U/$\overline{D}$ is High and move down when U/$\overline{D}$ is Low. The TR setting will be stored into the user NVMEM automatically each time $\overline{CS}$ goes high while $\overline{INC}$ holds high. Otherwise, if $\overline{INC}$ is low when $\overline{CS}$ goes high, the TR setting will not be stored. The NVMEM content will be automatically loaded into TR at Power On. The user NVMEM can be tested through the voltage measurement on the wiper pin after saving TR setting into the NVMEM and reloading into the TR. When the TR setting is already at LOW, further DOWN operations won't change the setting. Similarly, when TR setting is at HIGH, further UP operations won't change the setting.

When $\overline{CS}$ is held HIGH, the part will be in Standby mode and the TR setting will not be changed. The operating modes of Up/Down are summarized below.

$\overline{CS}$	U/$\overline{D}$	$\overline{INC}$	Operation
Low	High	High to Low	Wiper toward V_A
Low	Low	High to Low	Wiper toward V_B
Low to High	x	High	Store Wiper Position
Low to High	x	Low	No Store, Return to Standby
High	x	x	Standby

Note: x means don't care

8. TIMING DIAGRAMS

Conditions: V_{DD} = +2.7V to 5.5V, $V_A = V_{DD}$, V_B = 0V, T = 25°C

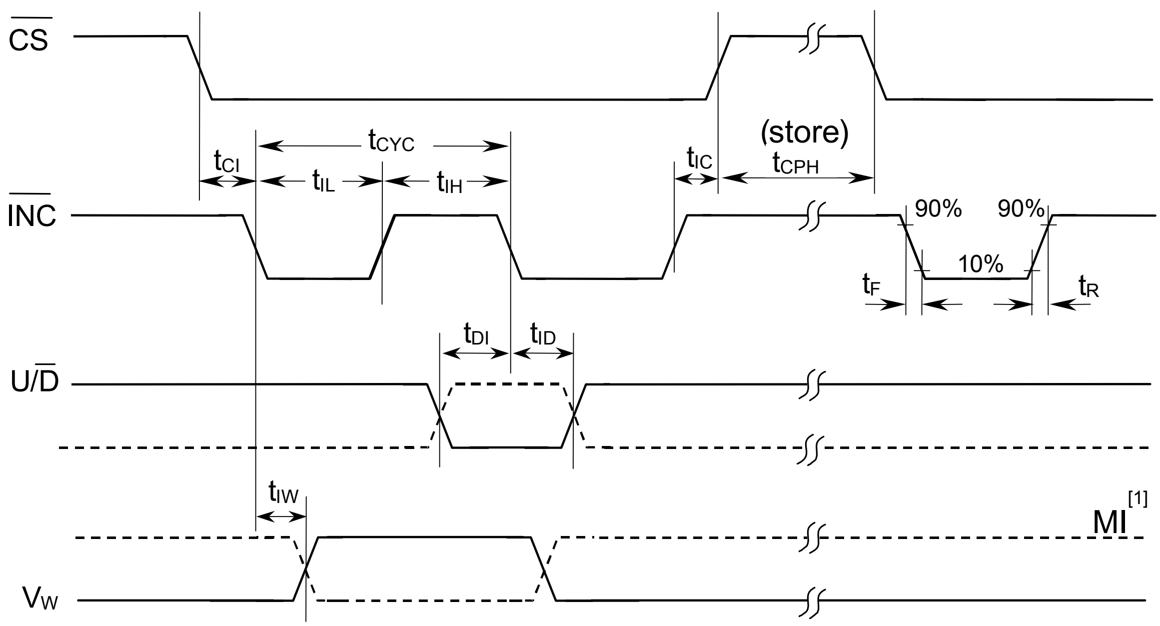


FIGURE 3 –WMS7100/1 TIMING DIAGRAM

Note:

[1] MI in the AC Timing diagram (Figure 3) refers to the minimum incremental change in the wiper output due to a change in the wiper position.

TABLE 10 – TIMING PARAMETERS

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
$\overline{CS}$ to $\overline{INC}$ Setup	t_{CI}	100		ns
U/$\overline{D}$ to $\overline{INC}$ Setup	t_{DI}	50		ns
U/$\overline{D}$ to $\overline{INC}$ Hold	t_{ID}	100		ns
$\overline{INC}$ LOW Period	t_{IL}	250		ns
$\overline{INC}$ HIGH Period	t_{IH}	250		ns
$\overline{INC}$ Inactive to $\overline{CS}$ Inactive	t_{IC}	1		µs
$\overline{CS}$ Deselect Time (NO STORE)	t_{CPH}	100		ns
$\overline{CS}$ Deselect Time (STORE)	t_{CPH}	15 (2.7V)		ms
$\overline{INC}$ to V_W Change	t_{IW}		5	µs
$\overline{INC}$ Cycle Time	t_{CYC}	1		µs
$\overline{INC}$ Input Rise and Fall Time	t_R, t_F		500	µs
Power-Up to Wiper Stable	t_{PU}		1	ms
V_{CC} Power-Up rate	t_R V_{CC}	0.2 (13ms 0-2.7V)	50 (54µs 0-2.7V)	V/ms

9. ABSOLUTE MAXIMUM RATINGS

TABLE 11 – ABSOLUTE MAXIMUM RATINGS (PACKAGED PARTS)[1]

Conditions	Values
Junction temperature	150ºC
Storage temperature	-65º to +150ºC
Voltage applied to any pad	(V_{ss} – 0.3V) to (V_{DD} + 0.3V)
V_{DD} – V_{SS}	-0.3 to 7.0V

TABLE 12 – OPERATING CONDITIONS (PACKAGED PARTS)

Conditions	Values
Commercial operating temperature range	0ºC to +70ºC
Extended operating temperature	-20ºC to +70ºC
Industrial operating temperature	-40ºC to +85ºC
Supply voltage (V_{DD})	+2.7V to +5.5V
Ground voltage (V_{SS})	0V

[1] Stresses above those listed may cause permanent damage to the device. Exposure to the absolute maximum ratings may affect device reliability. Functional operation is not implied at these conditions

10. ELECTRICAL CHARACTERISTICS

TABLE 12 – ELECTRICAL CHARACTERISTICS (Packaged parts)

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONDS
Rheostat Mode						
Nominal Resistance	R	-20		+20	%	T=25ºC, V_W open
Different Non Linearity [2]	DNL	-1		+1	LSB	
Integral Non Linearity [2]	INL	-1		+1	LSB	
Tempo[1]	$\Delta R_{AB}/\Delta T$		300		ppm/°C	
Wiper Resistance [2]	R_W		50		Ω	V_{DD}=5V, I=V_{DD}/R_{Total}
			80		Ω	V_{DD}=2.7V, I=V_{DD}/R_{Total}
Wiper Current	I_W	-1		1	mA	
Divider Mode						
Resolution	N	8			Bits	
Different Non Linearity [2]	DNL	-1	±0.4	+1	LSB	
Integral Non Linearity [2]	INL	-1	±0.2	+1	LSB	
Temperature Coefficient [1]	$\Delta V_w/\Delta T$		+20		ppm/°C	Code = 80h
Full Scale Error	V_{FSE}	-1		0	LSB	Code = Full Scale
Zero Scale Error	V_{ZSE}	0		1	LSB	Code = Zero Scale
Resistor Terminal						
Voltage Range	V_A,V_B,V_W	V_{SS}		V_{DD}	V	
Terminal Capacitance [1]	C_A, C_B		30		pF	
Wiper Capacitance [1]			30		pF	
Dynamic Characteristics [1]						
Bandwidth –3dB	BW_{10K}		1.5		MHz	V_{DD}=5V, V_B=VSS
	BW_{50K}		300		KHz	Code = 80h
	BW_{100K}		200		KHz	
Settling Time to 1 LSB	T_S		80	100	uS	
Analog Output (Buffer enables)						
Amp Output Current	I_{OUT}	3			mA	V_O=1/2 scale
Amp Output Resistance	Rout		1	10	Ω	I_L = 100uA
Total Harmonic Distortion [1]	THD			0.08	%	V_A=2.5V, V_{DD}=5V, f=1kHz, V_{IN}=1V_{RMS}
Digital Inputs/Outputs						
Input High Voltage	V_{IH}	0.7V_{DD}			V	
Input Low Voltage	V_{IL}			0.3V_{DD}	V	

PARAMETERS	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONDS
Output Low Voltage	V_{OL}			0.4	V	I_{OL}=2mA
Input Leakage Current	I_{LI}	-1		+1	uA	$\overline{CS}$ =V_{DD},Vin=Vss ~ V_{DD}
Output Leakage Current	I_{Lo}	-1		+1	uA	$\overline{CS}$ =V_{DD},Vin=V_{SS} ~ V_{DD}
Input Capacitance [1]	C_{IN}		25		pF	V_{DD}=5V, fc = 1Mhz
Output Capacitance [1]	C_{OUT}		25		pF	V_{DD}=5V, fc = 1Mhz
Power Requirements						
Operating Voltage	V_{DD}	2.7		5.5	V	
Operating Current	I_{DDR}		0.5	1	mA	All ops except NVMEM program
Operating Current	I_{DDW}		1	2	mA	During Non-volatile memory program
Standby Current	I_{SA} [3]		0.5	1	mA	Buffer is active, NOP, no load
	I_{SB} [4]		0.1	1	uA	Buffer is inactive, Power Down, No load
Power Supply Rejection Ratio	PSRR			1	LSB/V	V_{DD}=5V±10%, Code=80H

Notes:

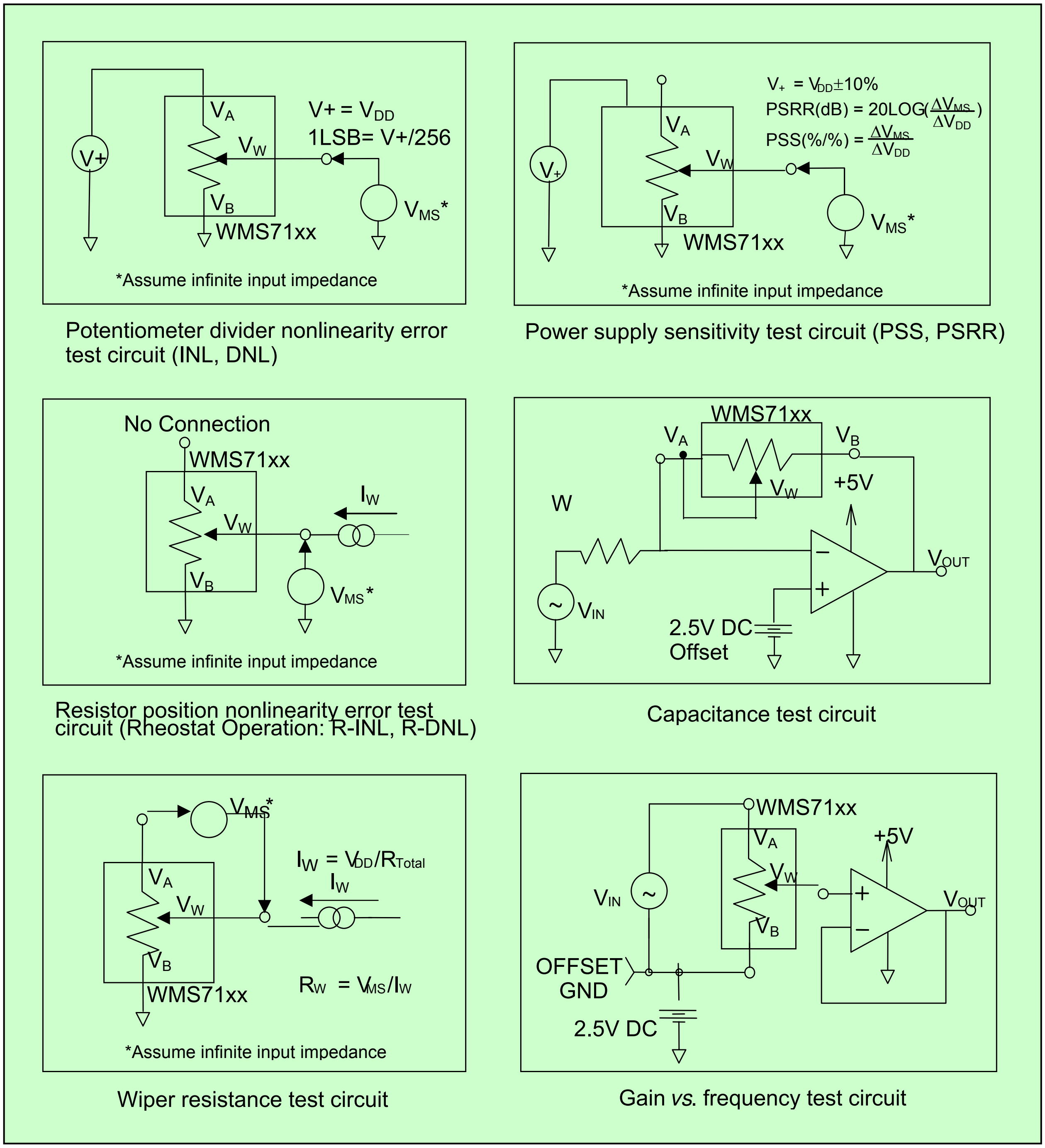
[1] Not subject to production test.

[2] LSB = (V_A - V_B) / (T- 1); DNL = (V_{i+1} - V_i) / LSB; INL = (V_i - i*LSB) / LSB; where i = [0, (T -1)] and T = # of taps of the device.

[3] WMS71x1 only.

[4] WMS71x0 only.

10.1 TEST CIRCUITS



Potentiometer divider nonlinearity error test circuit (INL, DNL)

Power supply sensitivity test circuit (PSS, PSRR)

Resistor position nonlinearity error test circuit (Rheostat Operation: R-INL, R-DNL)

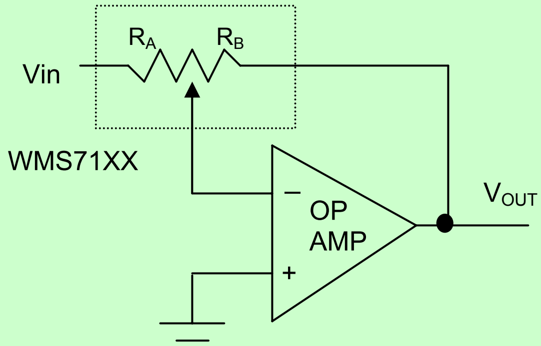
Capacitance test circuit

Wiper resistance test circuit

Gain *vs.* frequency test circuit

FIGURE 4 – TEST CIRCUITS

11. TYPICAL APPLICATION CIRCUITS



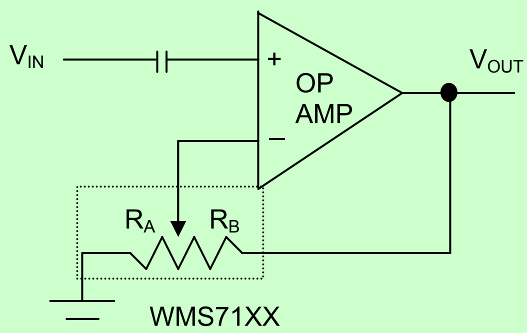
$$V_{OUT} = -V_{IN}\frac{R_B}{R_A}$$

$$R_A = \frac{R_{AB}(256-D)}{256}, \quad R_B = \frac{R_{AB}D}{256}$$

R_{AB} = Total resistance of potentiometer

D = Wiper setting for WMS71XX

FIGURE 5 – PROGRAMMABLE INVERTING GAIN AMPLIFIER USING THE WMS7100/1



$$V_{OUT} = V_{IN}\left(1+\frac{R_B}{R_A}\right)$$

$$R_A = \frac{R_{AB}(256-D)}{256}, \quad R_B = \frac{R_{AB}D}{256}$$

R_{AB} = Total resistance of potentiometer

D = Wiper setting for WMS71XX

FIGURE 6 – PROGRAMMABLE NON-INVERTING GAIN AMPLIFIER USING THE WMS7100/1

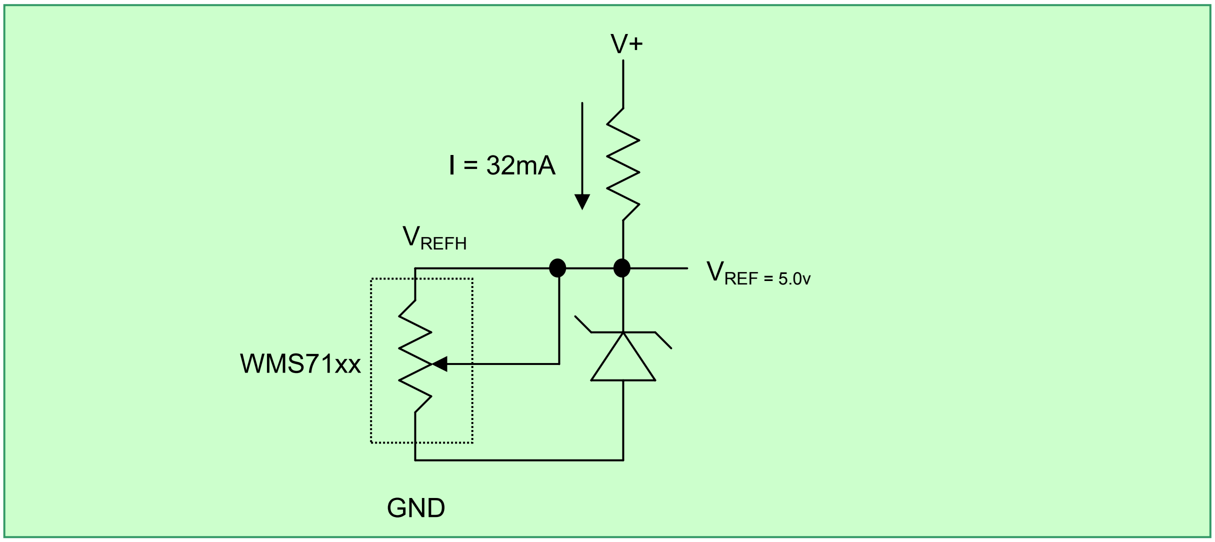


FIGURE 7 – WMS7100/1 TRIMMING VOLTAGE REFERENCE

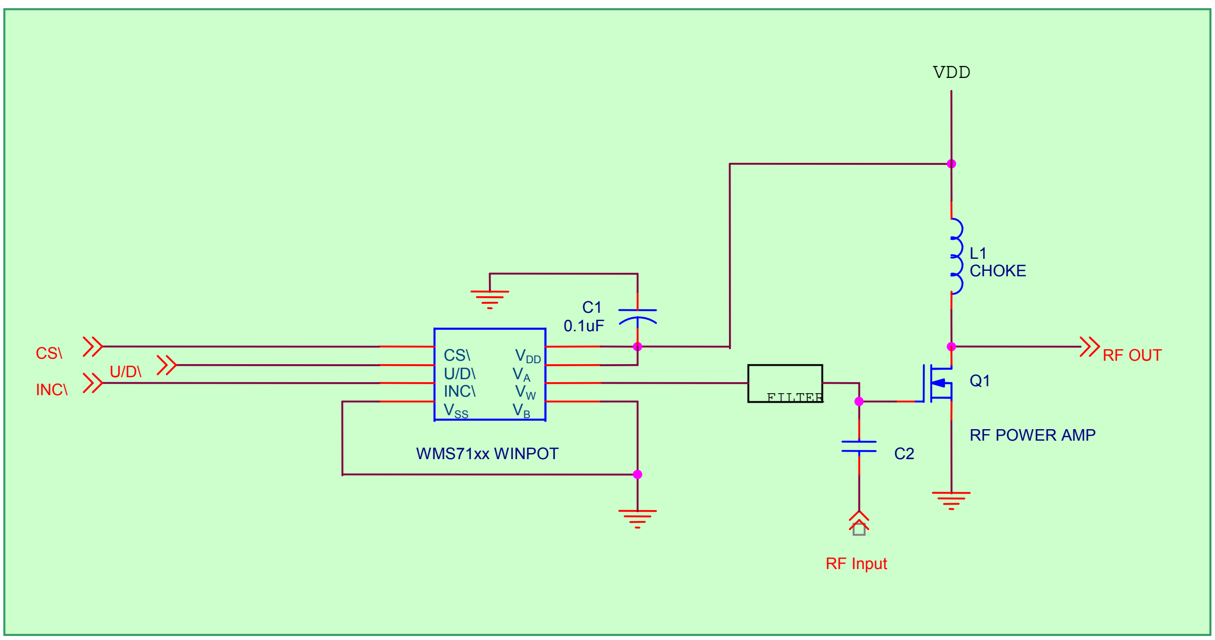


FIGURE 8 – WMS7100/1 RF AMP CONTROL

11.1. LAYOUT CONSIDERATIONS

Use a 0.1μF bypass capacitor as close as possible to the V_{DD} pin. This is recommended for best performance. Often this can be done by placing the surface mount capacitor on the bottom side of the PC board, directly between the V_{DD} and V_{SS} pins. Care should be taken to separate the analog and digital traces. Sensitive traces should not run under the device or close to the bypass capacitors.

A dedicated plane for analog ground helps in reducing ground noise for sensitive analog signals.

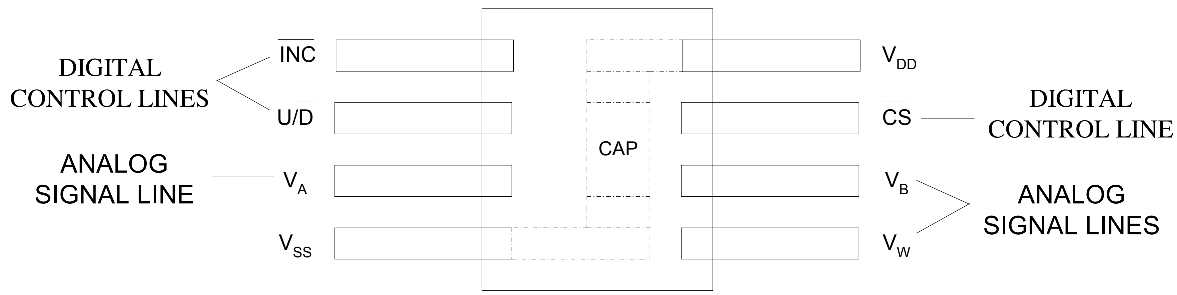
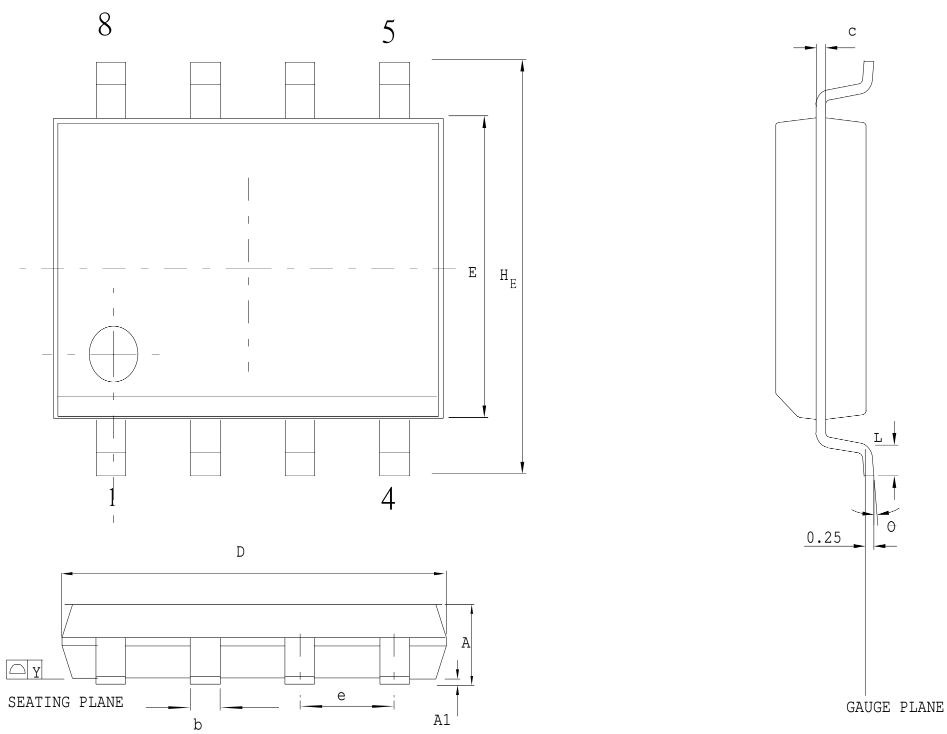


FIGURE 9 – WMS7100/1 LAYOUT

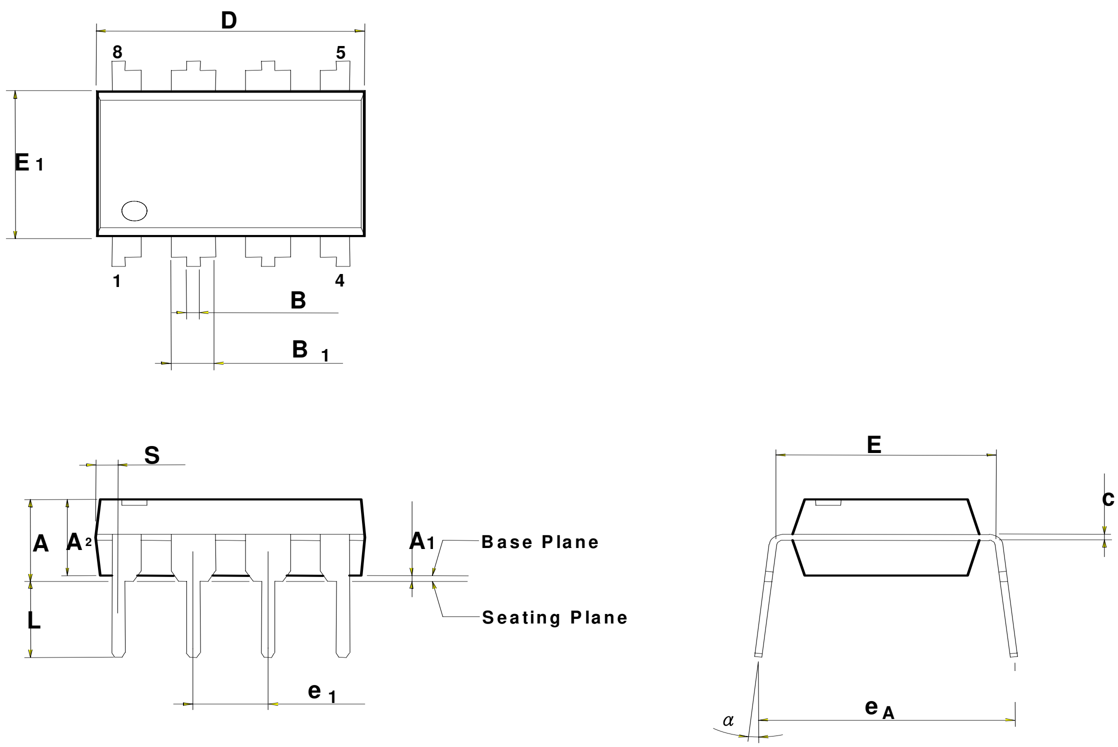
12. PACKAGE DRAWINGS AND DIMENSIONS



Control demensions are in milmeters .

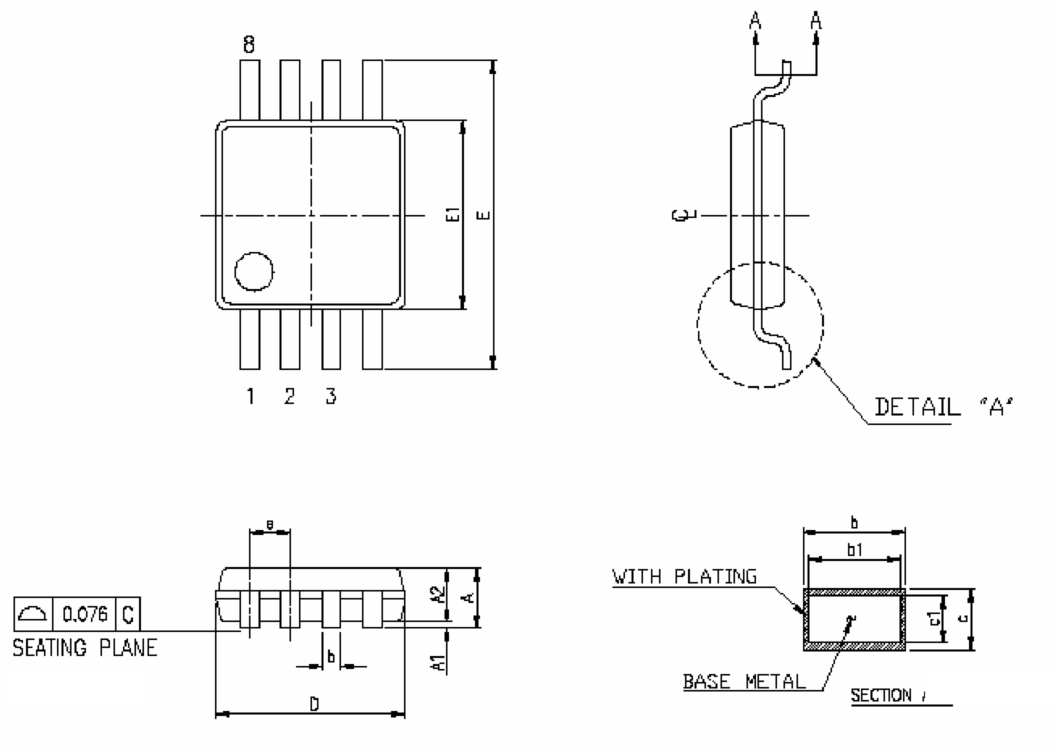
SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
E	3.80	4.00	0.150	0.157
D	4.80	5.00	0.188	0.196
e	1.27 BSC		0.050 BSC	
H_E	5.80	6.20	0.228	0.244
Y	—	0.10	—	0.004
L	0.40	1.27	0.016	0.050
θ	0	10	0	10

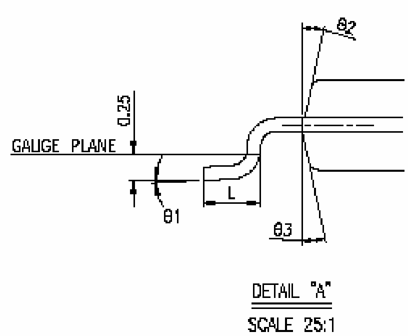
FIGURE 10: 8L 150MIL SOIC



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.175	—	—	4.45
A_1	0.010	—	—	0.25	—	—
A_2	0.125	0.130	0.135	3.18	3.30	3.43
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.058	0.060	0.064	1.47	1.52	1.63
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	0.360	0.380	—	9.14	9.65
E	0.290	0.300	0.310	7.37	7.62	7.87
E_1	0.245	0.250	0.255	6.22	6.35	6.48
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
α	0	—	15	0	—	15
e_A	0.335	0.355	0.375	8.51	9.02	9.53
S	—	—	0.045	—	—	1.14

FIGURE 11: 8L 300MIL PDIP





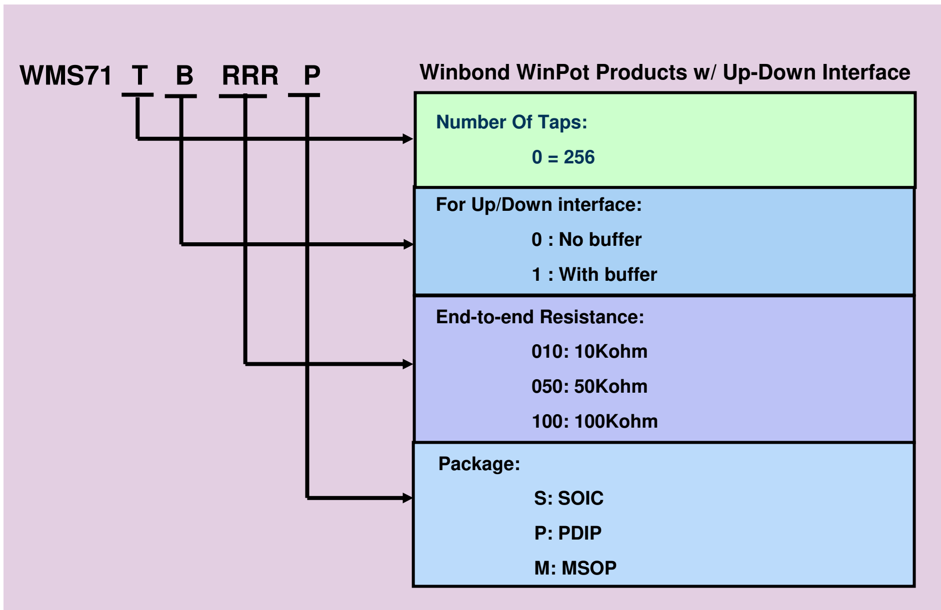
SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	1.10	---	---	0.043
A1	0.05	---	0.15	0.002	---	0.006
A2	0.81	0.86	0.91	0.032	0.034	0.036
c	0.13	---	0.23	0.005	---	0.009
c1	0.13	0.15	0.18	0.005	0.006	0.007
D	2.90	3.00	3.10	0.114	0.118	0.122
E1	2.90	3.00	3.10	0.114	0.118	0.122
E	4.90 BSC			0.193 BSC		
L	0.445	0.55	0.648	0.0175	0.0217	0.0255
θ1	0°		6°	0°		6°

SYMBOL	8L			10L		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.25	---	0.40	0.17	---	0.27
b1	0.25	0.30	0.35	0.17	0.20	0.23
e	0.65 BSC			0.50 BSC		
JEDEC	MO-187AA			MO-187		

FIGURE 12: 8L 3MM MSOP

13. ORDERING INFORMATION

Winbond's WinPot Part Number Description:



Output Buffer	End-to-End Resistance	SOIC	PDIP	MSOP
NO	10K	WMS7100**010S**	WMS7100**010P**	WMS7100**010M**
	50K	WMS7100**050S**	WMS7100**050P**	WMS7100**050M**
	100K	WMS7100**100S**	WMS7100**100P**	WMS7100**100M**
YES	10K	WMS7101**010S**	WMS7101**010P**	WMS7101**010M**
	50K	WMS7101**050S**	WMS7101**050P**	WMS7101**050M**
	100K	WMS7101**100S**	WMS7101**100P**	WMS7101**100M**

Notes:

Part number with white background: Available for sampling and mass production.

Part numbers with shaded background: Call factory for availability.

For the latest product information, access Winbond's worldwide website at http://www.winbond-usa.com

14. VERSION HISTORY

VERSION	DATE	DESCRIPTION
1.0	June 2003	Initial issue
1.1	April 2005	Revise disclaim section