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WS1102

3 x 3 Power Amplifier Module for CDMA/AMPS (824–849 MHz)

AVAGO TECHNOLOGIES

Data Sheet

Description

The WS1102 is a CDMA (Code Division Multiple Access) and AMPS (Advanced Mobile Phone Service) power amplifier module designed for handsets operating in the 824–849 MHz bandwidth. The WS1102 features CoolPAM circuit technology that offers state-of-the-art reliability, temperature stability and ruggedness.

The WS1102 meets stringent CDMA linearity requirements to and beyond 28 dBm output power. The 3 mm x 3 mm form factor 8-pin surface mount package is self contained, incorporating 50 ohm input and output matching networks.

Features

- Good linearity
- Excellent efficiency: 40% at Pout = 28 dBm; 19% at Pout = 16 dBm (without a DC/DC converter)
- 8-pin surface mounting package (3 mm x 3 mm x 1.1 mm)
- Internal 50Ω matching networks for both RF Input and output
- CDMA 95A/B, CDMA2000-1X/EVDO

Applications

- Digital Cellular (CDMA)
- Analog Cellular (AMPS)

Functional Block Diagram

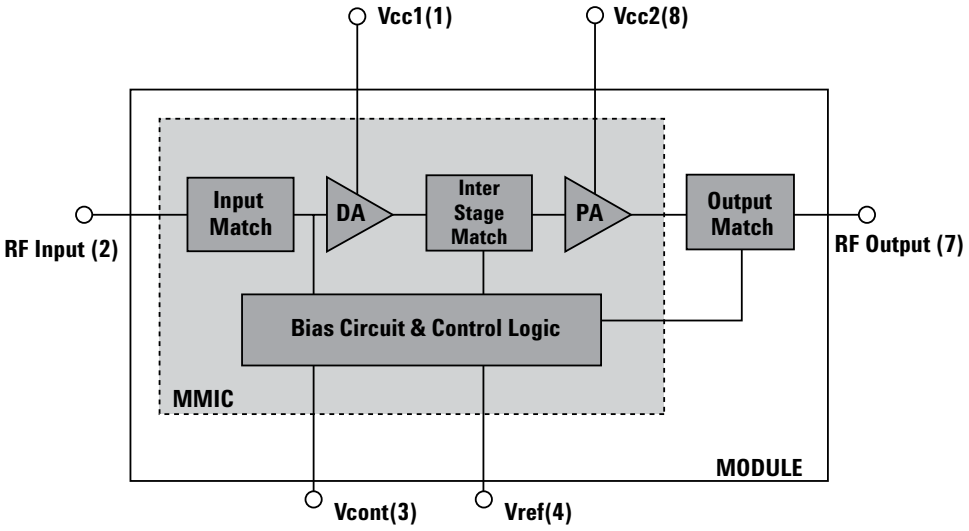


Table 1. Absolute Maximum Ratings[1]

Parameter	Symbol	Min.	Nominal	Max.	Unit
RF Input Power	P_{in}	–	–	10.0	dBm
DC Supply Voltage	V_{cc}	–	3.4	5.0	V
DC Reference Voltage	V_{ref}	–	2.85	3.3	V
Storage Temperature	T_{stg}	-55	–	+125	°C

Table 2. Recommended Operating Conditions

Parameter	Symbol	Min.	Nominal	Max.	Unit
DC Supply Voltage	V_{cc}	3.2	3.4	4.2	V
DC Reference Voltage	V_{ref}	2.75	2.85	2.95	V
Mode Control Voltage					
– High Power Mode	V_{cont}	–	0	–	V
– Low Power Mode	V_{cont}	–	2.85	–	V
Operating Frequency	F_o	824	–	849	MHz
Ambient Temperature	T_a	-30	25	85	°C

Table 3. Power Range Truth Table

Power Mode	Symbol	Vref	Vcont[2]	Range
High Power Mode[3]	PR2	2.85	Low	~28 dBm
Low Power Mode[3]	PR1	2.85	High	~16 dBm
Shut Down Mode[4]	–	0.00	–	–

Notes:
1. No damage assuming only one parameter is set at limit at a time with all other parameters set at or below nominal value.
2. High (1.5V – 3.0V), Low (0.0V – 0.5V).
3. To change between High Power Mode and Low Power Mode, switch Vcont accordingly.
4. In order to shut down the module, turn off V_{ref} accordingly.

Table 4-1. Electrical Characteristics for CDMA Mode (Vcc=3.4V, Vref=2.85V, T=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Gain		Gain_hi	Pout = 28.0 dBm	25.5	28.5		dB
		Gain_low	Pout = 16.0 dBm	15.5	18.5		dB
Power Added Efficiency		PAE_hi	Pout = 28.0 dBm	37	40		%
		PAE_low	Pout = 16.0 dBm	16	19		%
Total Supply Current		Icc_hi	Pout = 28.0 dBm		460	500	mA
		Icc_low	Pout = 16.0 dBm		60	80	mA
Quiescent Current		Iq_hi	High Power Mode	60	85	110	mA
		Iq_low	Low Power Mode	8	14	22	mA
Reference Current		Iref_hi	Pout = 28.0 dBm		3	7	mA
		Iref_low	Pout = 16.0 dBm		4	8	mA
Control Current [1]		Icont	Pout = 16.0 dBm		0.2	1	mA
Total Current in Power-down Mode		Ipd	Vref = 0.0V		0.2	5	µA
ACPR in High Power Mode	0.90 MHz offset	ACPR1_hi	Pout = 28.0 dBm		-50	-47	dBc
	1.98 MHz offset	ACPR2_hi	Pout = 28.0 dBm		-60	-57	dBc
ACPR in Low Power Mode	0.90 MHz offset	ACPR1_low	Pout = 16.0 dBm		-52	-47	dBc
	1.98 MHz offset	ACPR2_low	Pout = 16.0 dBm		-62	-57	dBc
Harmonic Suppression	Second	2f0	Pout = 28.0 dBm		-33	-30	dBc
	Third	3f0	Pout = 28.0 dBm		-55	-40	dBc
Input VSWR		VSWR			2:1	2.5:1	VSWR
Stability (Spurious Output)		S	VSWR 6:1, All phase			-60	dBc
Noise Power in RX Band		RxBN	Pout = 28.0 dBm		-136	-132	dBm/Hz
Ruggedness		Ru	Pout < 28.0 dBm, Pin < 10.0 dBm			10:1	VSWR

Table 4-2. Electrical Characteristics for AMPS Mode (Vcc=3.4V, Vref=2.85V, T=25°C)

Characteristics		Symbol	Condition	Min.	Typ.	Max.	Unit
Gain		Gain_a	Pout = 31.0 dBm	25	28	31	dB
Power Added Efficiency		PAE_a	Pout = 31.0 dBm	50	54		%
Total Supply Current		Icc_a	Pout = 31.0 dBm		685	740	mA
Quiescent Current		Iq_a	High Power Mode	60	85	110	mA
Reference Current		Iref_a	Pout = 31.0 dBm		4	10	mA
Total Supply Current in Power-down Mode		Ipd	Vcc=3.4, Vref=0V, Vcont=0V		0.2	5	µA
Harmonic Suppression	Second	2f0	Pout = 31.0 dBm		-33	-30	dBc
	Third	3f0	Pout = 31.0 dBm		-50	-40	dBc
Input VSWR		VSWR			2:1	2.5:1	VSWR
Stability (Spurious Output)		S	VSWR 6:1, All phase			-60	dBc
Noise Power in RX Band		RxBN	Pout = 31 dBm		-136	-130	dBm/Hz
Ruggedness		Ru	Pout < 31 dBm, Pin<10.0 dBm			10:1	VSWR

Note:
1. Control current when series 6.2okm is used.

Characterization Data (Vcc=3.4V, Vref=2.85V, T=25°C, Fo=837 MHz)

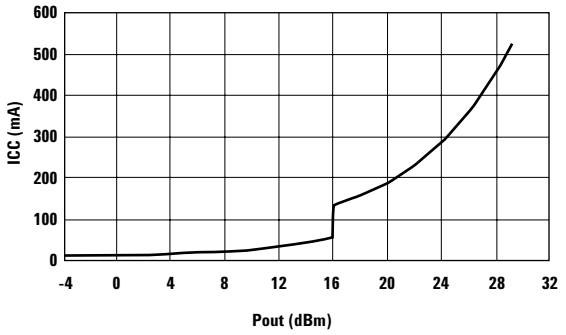


Figure 1. Total Current vs. Output Power.

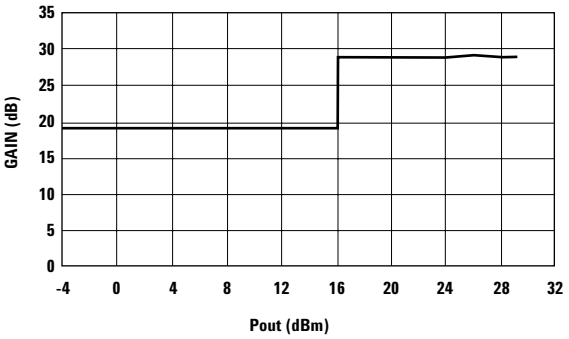


Figure 2. Gain vs. Output Power.

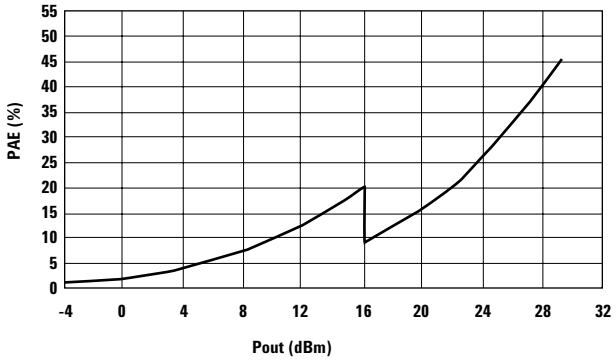


Figure 3. Power Added Efficiency vs. Output Power.

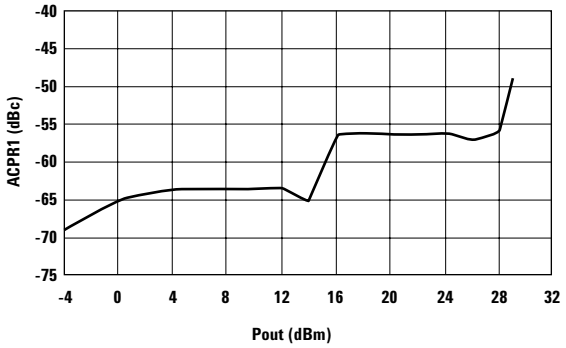


Figure 4. Adjacent Channel Power 1 vs. Output Power.

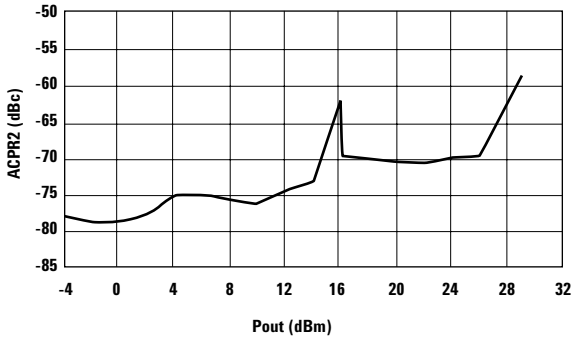


Figure 5. Adjacent Channel Power 2 vs. Output Power.

Evaluation Board Description

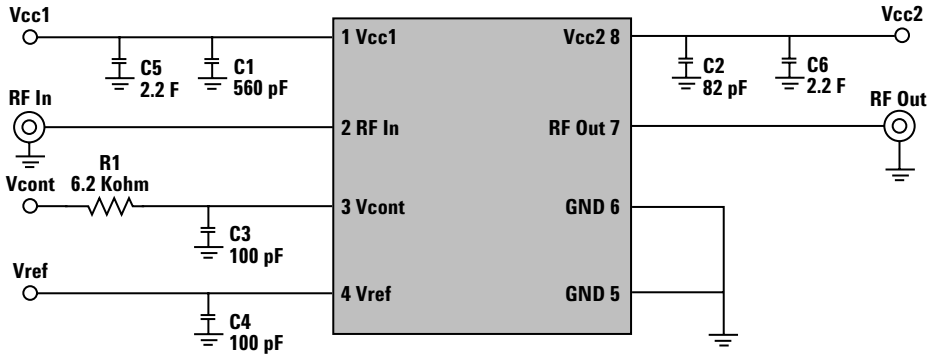


Figure 6. Evaluation Board Schematic.

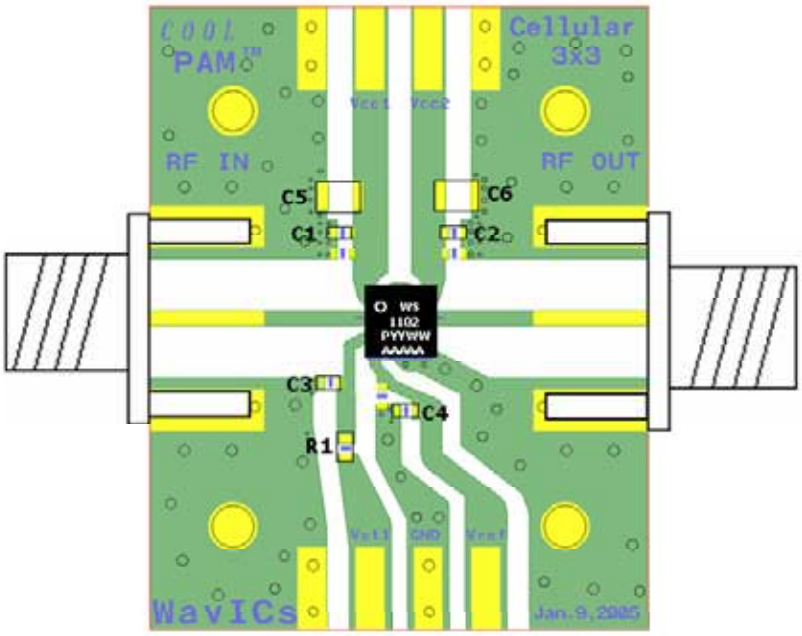
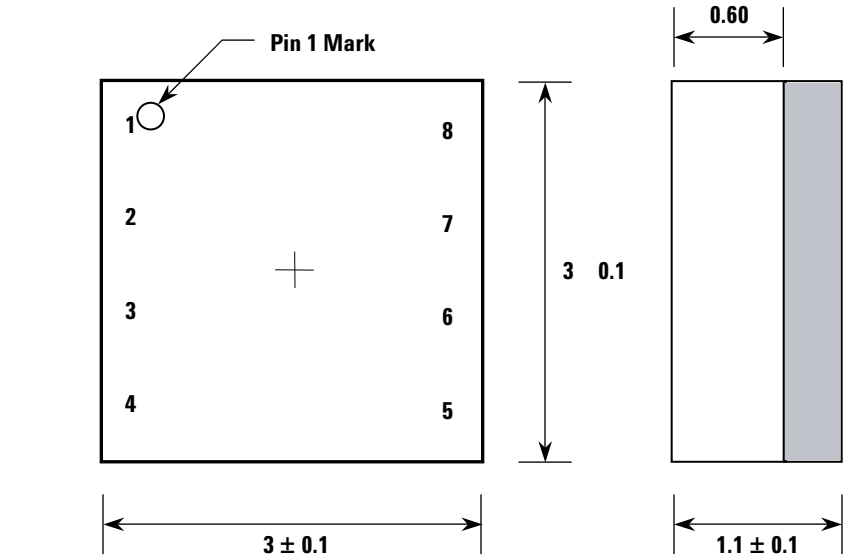
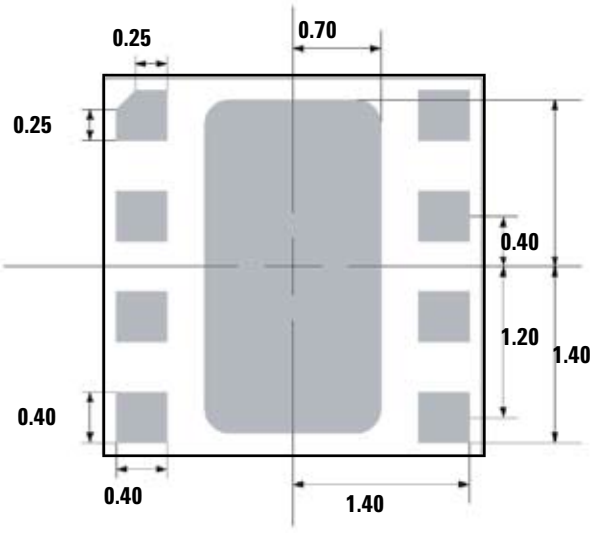


Figure 7. Evaluation Board Assembly Diagram.

Package Dimensions and Pin Descriptions





Pin #	Name	Description
1	Vcc1	Supply Voltage
2	RF In	RF Input
3	Vcont	Control Voltage
4	Vref	Reference Voltage
5	GND	Ground
6	GND	Ground
7	RF Out	RF Output
8	Vcc2	Supply Voltage

PIN DESCRIPTIONS

Figure 8. Package Dimensional Drawing and Pin Descriptions.

Notes:
1. All dimensions are in millimeters.
2. Dimensions Without Tolerance: .XX ‡ ± 0.05mm.

Package Dimensions and Pin Descriptions, continued

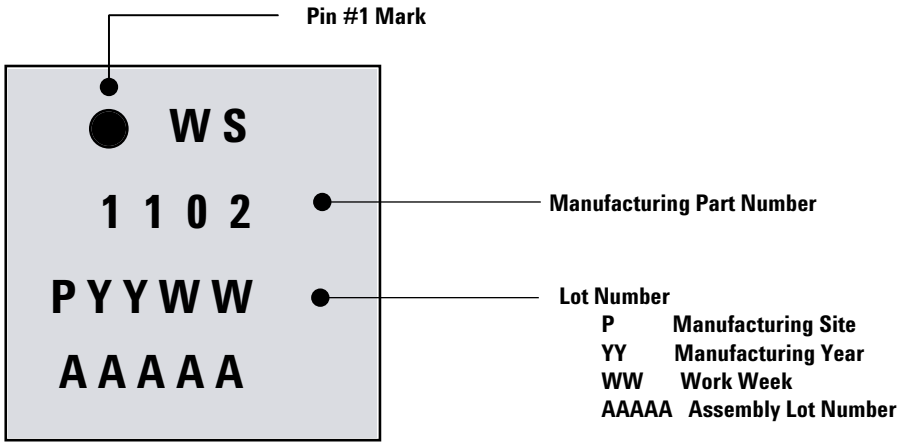


Figure 9. Marking Specifications.

Peripheral Circuit in Handset

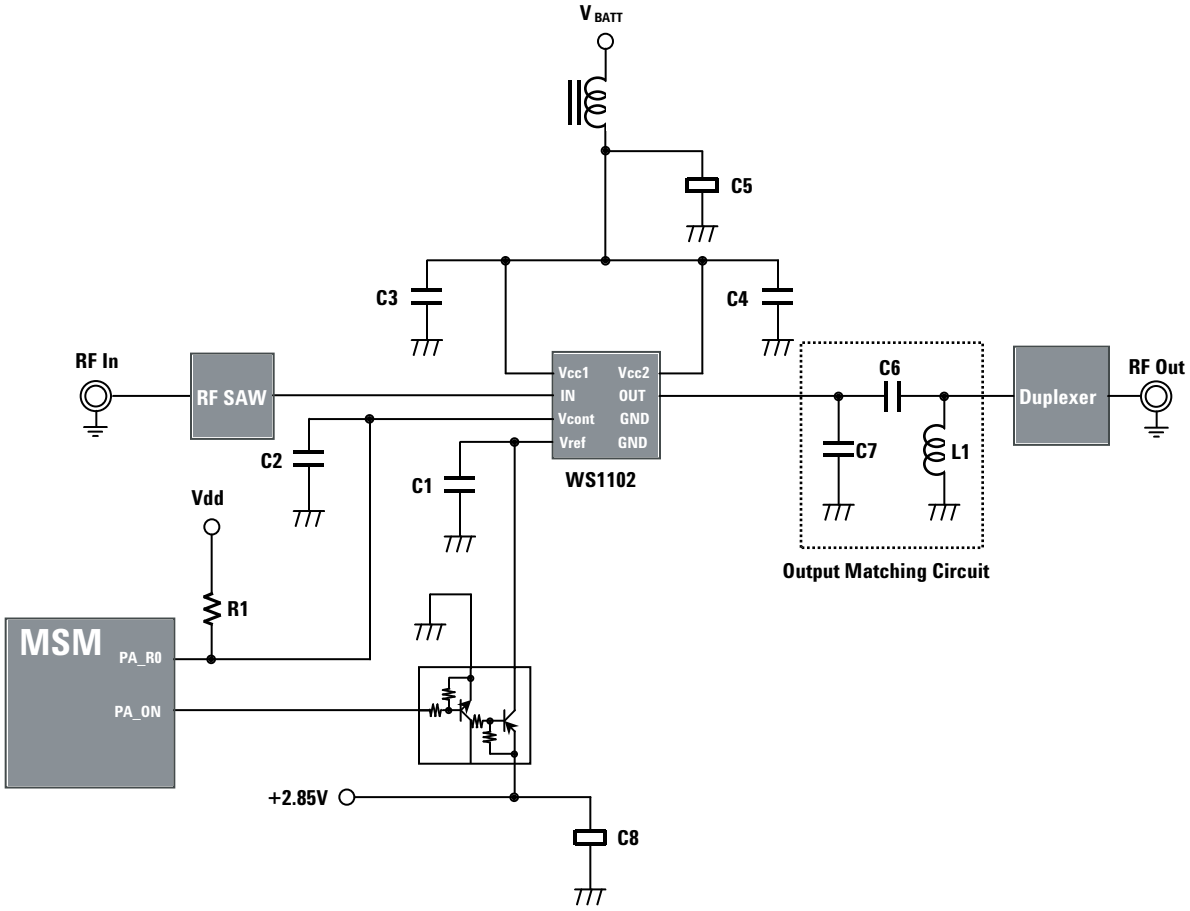


Figure 10. Peripheral circuit.

Notes:
1. Recommended voltage for Vref is 2.85V.
2. Place C1 near to Vref pin.
3. Place C3 and C4 close to pin 1 (Vcc1) and pin 8 (Vcc2). These capacitors can affect the RF performance.
4. Use 50Ω transmission line between PAM and Duplexer and make it as short as possible to reduce conduction loss.
5. π-type circuit topology is good to use for matching circuit between PA and Duplexer.
6. Pull-up resistor (R1) should be used to limit current drain. 6.2 kΩ is recommended for WS1102.

Calibration

Calibration procedure is shown in Figure 11. Two calibration tables, high mode and low mode respectively, are required for CoolPAM, which is due to gain difference in each mode.

For continuous output power at the mode change points, the input power should be adjusted according to gain step during the mode change.

Offset Value (difference between rising point and falling point)

Offset value, which is the difference between the rising point (output power where PA mode changes from low mode to high mode) and falling point (output power where PA mode changes from high mode to low mode), should be adopted to prevent system oscillation. 3 to 5 dB is recommended for Hysteresis.

Average Current and Talk Time

Probability Distribution Function implies that what is important for longer talk time is the efficiency of low or medium power range rather than the efficiency at full power. WS1102 idle current is 14 mA and operating current at 16 dBm is 60 mA at nominal condition. Average current calculated with CDMA PDF is 33 mA in urban area and 54 mA in suburban area. This PA with low current consumption prolongs talk time by no less than 30 minutes compared to other PAs.

Average current = ∫(PDF x Current) dp

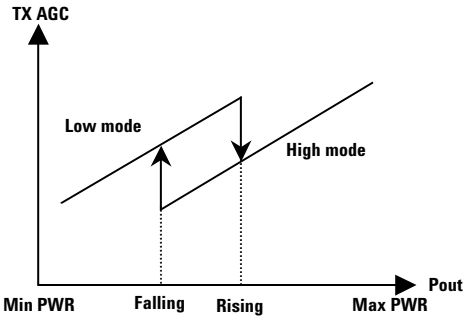


Figure 11. Calibration procedure.

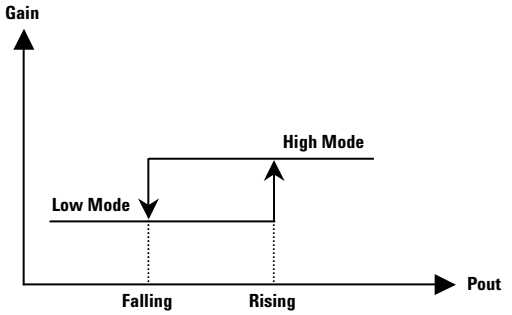


Figure 12. Setting of offset between rising and falling power.

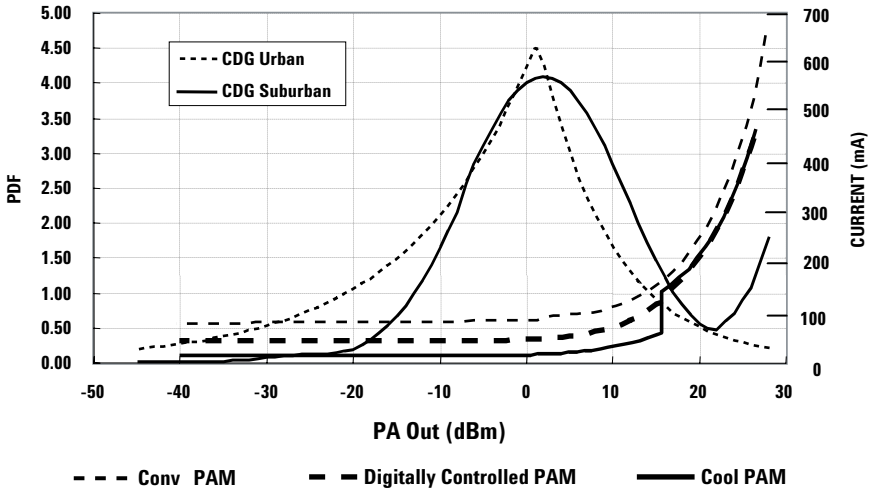


Figure 13. CDMA Power Distribution Function.

PCB Design Guidelines

The recommended WS1102 PCB Land pattern is shown in Figure 14 and Figure 15. The substrate is coated with solder mask between the I/O and conductive paddle to protect the gold pads from short circuit that is caused by solder bleeding/bridging.

Stencil Design Guidelines

A properly designed solder screen or stencil is required to ensure optimum amount of solder paste is deposited onto the PCB pads.

The recommended stencil layout is shown in Figure 16. Reducing the stencil opening can potentially generate more voids. On the other hand, stencil openings larger than 100% will lead to excessive solder paste smear or bridging across the I/O pads or conductive paddle to adjacent I/O pads. Considering the fact that solder paste thickness will directly affect the quality of the solder joint, a good choice is to use laser cut stencil composed of 0.100 mm (4 mils) or 0.127 mm (5mils) thick stainless steel which is capable of producing the required fine stencil outline.

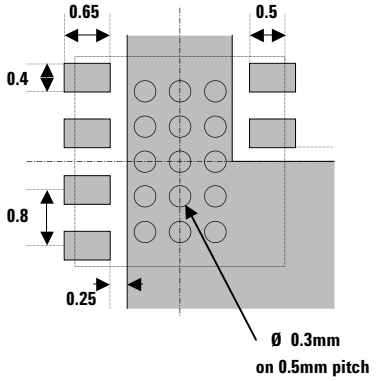


Figure 14. Metallization.

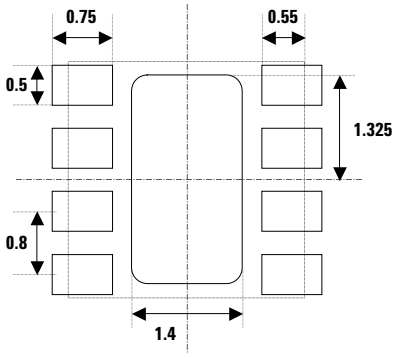


Figure 15. Solder Mask Opening.

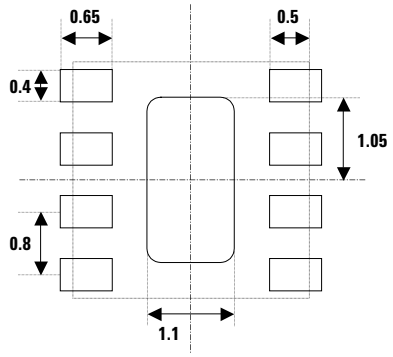
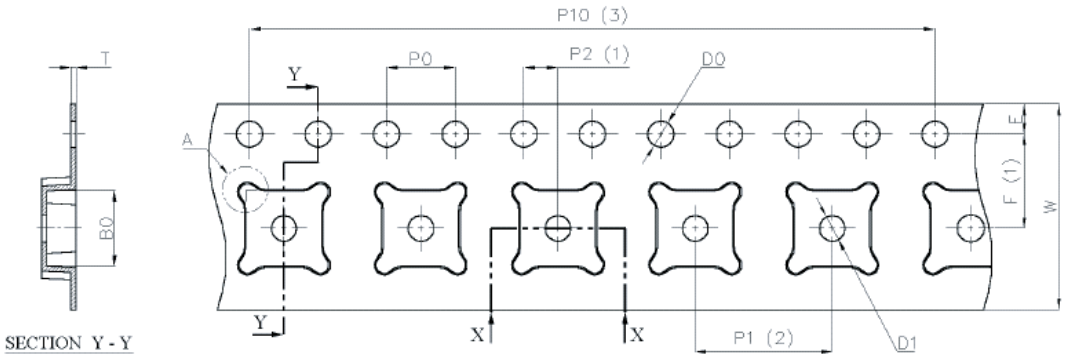


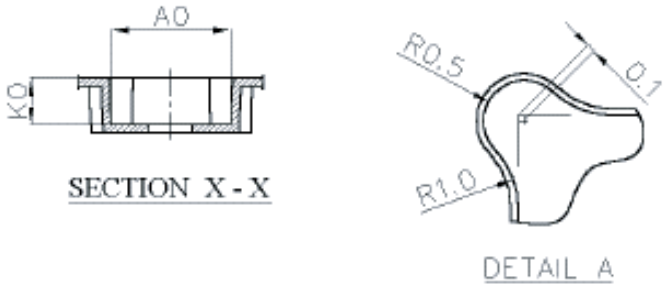
Figure 16. Solder Paste Stencil Aperture.

Ordering Information

Part Number	Number of Devices	Container
WS1102-BLK	100	Bulk
WS1102-TR1	2500	13" Tape and Reel

Tape and Reel Information



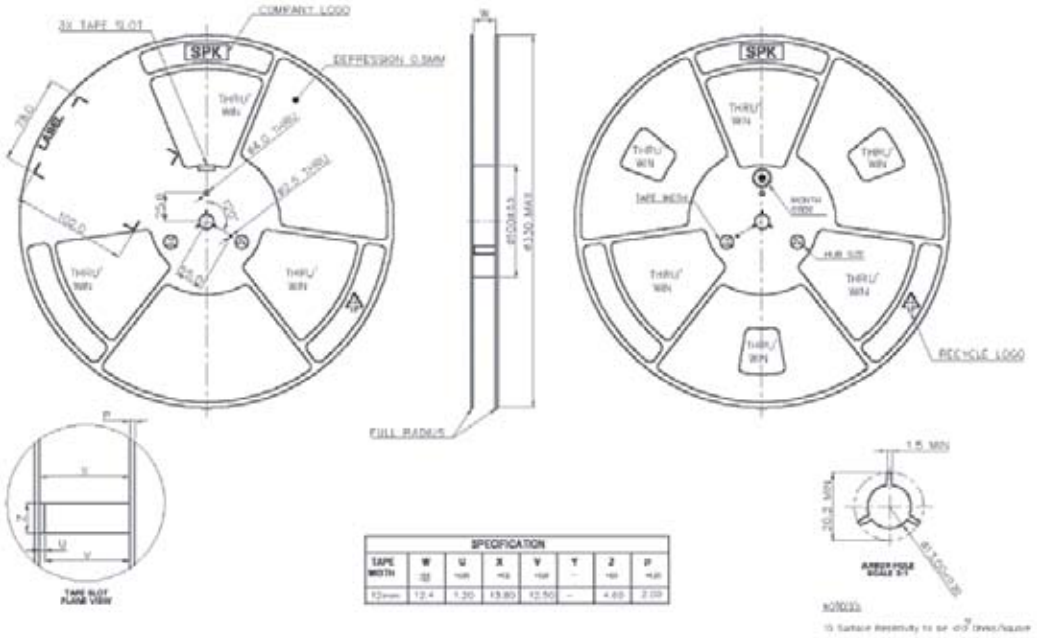


Dimension List

Annote	Milimeter	Annote	Milimeter
A0	3.40 ± 0.10	P2	2.00 ± 0.05
B0	3.40 ± 0.10	P10	40.00 ± 0.20
K0	1.70 ± 0.10	E	1.75 ± 0.10
D0	1.55 ± 0.05	F	5.50 ± 0.05
D1	1.60 ± 0.10	W	12.00 ± 0.30
P0	4.00 ± 0.10	T	0.30 ± 0.05
P1	8.00 ± 0.10		

Figure 17. Tape and Reel Format – 3mm x 3mm.

Tape and Reel Information, continued



all dimensions are in millimeters

Figure 18. Plastic Reel Format 13"/14".

Handling and Storage

ESD (Electrostatic Discharge)

Electrostatic discharge occurs naturally in the environment. With the increase in voltage potential, the outlet of neutralization or discharge will be sought. If the acquired discharge route is through a semiconductor device, destructive damage will result.

ESD countermeasure methods should be developed and used to control potential ESD damage during handling in a factory environment at each manufacturing site.

MSL (Moisture Sensitivity Level)

Plastic encapsulated surface mount package is sensitive to damage induced by absorbed moisture and temperature. Avago Technologies follows JEDEC Standard J-STD 020B. Each component and package type is classified for moisture sensitivity by soaking a known dry package at various temperatures and relative humidity, and times. After soak, the components are subjected to three consecutive simulated reflows.

The out of bag exposure time maximum limits are determined by the classification test described above which corresponds to a MSL classification level 6 to 1 according to the JEDEC standard IPC/JEDEC J-STD-020B and J-STD-033.

WS1102 is MSL3. Thus, according to the J-STD-033 p.11 the maximum Manufacturers Exposure Time (MET) for this part is 168 hours. After this time period, the part would need to be removed from the reel, de-taped and then re-baked.

MSL classification reflow temperature for the WS1102 is targeted at 250°C +0/-5°C. Figure 19 and Table 7 show typical SMT profile for maximum temperature of 250°C +0/-5°C.

Table 5. ESD Classification

Pin#	Name	Description	HBM	MM	Classification
1	Vcc1	Supply Voltage	± 2000V	± 200V	Class 2
2	RF In	RF Input	± 2000V	± 200V	Class 2
3	Vcont	Control Voltage	± 2000V	± 200V	Class 2
4	Vref	Reference Voltage	± 2000V	± 200V	Class 2
5	GND	Ground	± 2000V	± 200V	Class 2
6	GND	Ground	± 2000V	± 200V	Class 2
7	RF Out	RF Output	± 2000V	± 200V	Class 2
8	Vcc2	Supply Voltage	± 2000V	± 200V	Class 2

Note:
1. Module products should be considered extremely ESD sensitive.

Table 6. Moisture Classification Level and Floor Life

MSL Level	Floor Life (out of bag) at factory ambient ≤ 30°C/60% RH or as stated
1	Unlimited at ≤ 30°C/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label

Note:
1. The MSL Level is marked on the MSL Label on each shipping bag.

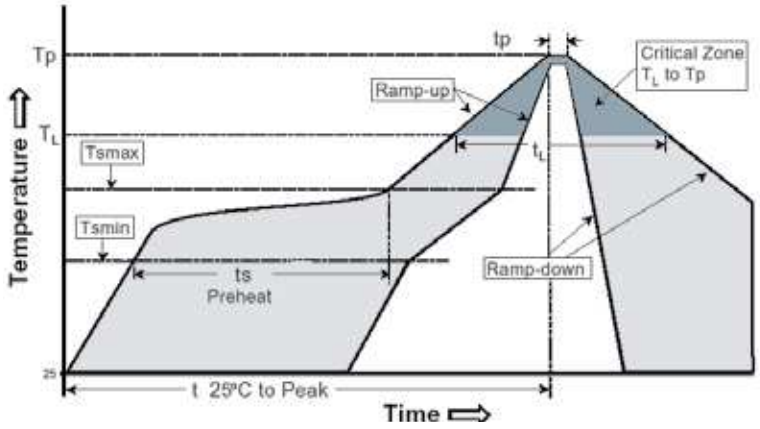


Figure 19. Typical SMT Reflow Profile for Maximum Temperature = 250+0/-5°C.

Table 7. Typical SMT Reflow Profile for Maximum Temperature = 250+0/-5°C

Profile Feature	Sn-Pb Solder	Pb-Free Solder
Average ramp-up rate (T_L to T_P)	3°C/sec max	3°C/sec max
Preheat		
- Temperature Min (Tsmin)	100°C	150°C
- Temperature Max (Tsmax)	150°C	200°C
- Time (min to max) (ts)	60 – 120 sec	60–180 sec
Tsmax to T_L		
- Ramp-up Rate		3°C/sec max
Time maintained above:		
- Temperature (T_L)	183°C	217°C
- Time (T_L)	60–150 sec	60–150 sec
Peak Temperature (T_p)	240 +0/-5°C	250 +0/-5°C
Time within 5°C of actual Peak Temperature (tp)	10–30 sec	20–40 sec
Ramp-down Rate	6°C/sec max	6°C/sec max
Time 25°C to Peak Temperature	6 min max.	8 min max.

Handling and Storage, continued

Storage Conditions
Packages described in this document must be stored in sealed moisture barrier, anti-static bags. Shelf life in a sealed moisture barrier bag is 12 months at <40ºC and 90% relative humidity (RH) J-STD-033 p.7.

Out-of-Bag Time Duration
After unpacking the device must be soldered to the PCB within 168 hours as listed in the J-STD-020B p.11 with factory conditions <30ºC and 60% RH.

Baking
It is not necessary to re-bake the part if both conditions (storage conditions and out-of-bag conditions) have been satisfied. Baking must be done if at least one of the conditions above have not been satisfied. The baking conditions are 125ºC for 12 hours J-STD-033 p.8.

CAUTION: Tape and reel materials typically cannot be baked at the temperature described above. If out-of-bag exposure time is exceeded, parts must be baked for a longer time at low temperatures, or the parts must be de-reeled, de-taped, re-baked and then put back on tape and reel. (See moisture sensitive warning label on each shipping bag for information of baking).

Board Rework

Component Removal, Rework and Remount
If a component is to be removed from the board, it is recommended that localized heating be used and the maximum body temperatures of any surface mount component on the board not exceed 200°C. This method will minimize moisture related component damage. If any component temperature exceeds 200°C, the board must be baked dry per "Baking of Populated Boards" below prior to rework and/or component removal. Component temperatures shall be measured at the top center of the package body. Any SMD packages that have not exceeded their floor life can be exposed to a maximum body temperature as high as their specified maximum reflow temperature.

Removal for Failure Analysis
Not following the requirements may cause moisture/reflow damage that could hinder or completely prevent the determination of the original failure mechanism.

Baking of Populated Boards
Some SMD packages and board materials are not able to withstand long duration bakes at 125°C. Examples of this are some FR-4 materials, which cannot withstand a 24 hr bake at 125°C. Batteries and electrolytic capacitors are also temperature sensitive. With component and board temperature restrictions in mind, choose a bake temperature from Table 4-1 in J-STD 033; then determine the appropriate bake duration based on the component to be removed. For additional considerations see IPC-7711 and IPC-7721.

Derating due to Factory Environmental Conditions
Factory floor life exposures for SMD packages removed from the dry bags will be a function of the ambient environmental conditions. A safe, yet conservative, handling approach is to expose the SMD packages only up to the maximum time limits for each moisture sensitivity level as shown in Table 6. This approach, however, does not work if the factory humidity or temperature are greater than the testing conditions of 30°C/60% RH. A solution for addressing this problem is to derate the exposure times based on the knowledge of moisture diffusion in the component packaging materials (ref. JESD22-A120). Recommended equivalent total floor life exposures can be estimated for a range of humidities and temperatures based on the nominal plastic thickness for each device. Table 8 lists equivalent derated floor lives for humidities ranging from 20-90% RH for three temperatures, 20°C, 25°C, and 30°C. This table is applicable to SMDs molded with novolac, biphenyl or multifunctional epoxy mold compounds. The following assumptions were used in calculating Table 8:

1. Activation Energy for diffusion = 0.35eV (smallest known value).
2. For ≤60% RH, use Diffusivity = 0.121exp (- 0.35eV/kT) mm2/s (this uses smallest known Diffusivity @ 30°C).
3. For >60% RH, use Diffusivity = 1.320exp (- 0.35eV/kT) mm2/s (this uses largest known Diffusivity @ 30°C).

Handling and Storage, continued

Table 8. Recommended Equivalent Total Floor Life (days) @ 20°C, 25°C & 30°C For ICs with Novolac, Biphenyl and Multifunctional Epoxies (Reflow at same temperature at which the component was classified)

Maximum Percent Relative Humidity												
Package Type and Body Thickness	Moisture Sensitivity Level	5%	10%	20%	30%	40%	50%	60%	70%	80%	90%	
Body Thickness ≥3.1 mm including PQFPs >84 pins, PLCCs (square) All MQFPs or All BGAs ≥1 mm	Level 2a	∞	∞	∞	60	41	33	28	10	7	6	30°C
		∞	∞	∞	78	53	42	36	14	10	8	25°C
		∞	∞	∞	103	69	57	47	19	13	10	20°C
	Level 3	∞	∞	10	9	8	7	7	5	4	4	30°C
		∞	∞	13	11	10	9	9	7	6	5	25°C
		∞	∞	17	14	13	12	12	10	8	7	20°C
	Level 4	∞	5	4	4	4	3	3	3	2	2	30°C
		∞	6	5	5	5	5	4	3	3	3	25°C
		∞	8	7	7	7	7	6	5	4	4	20°C
	Level 5	∞	4	3	3	2	2	2	2	1	1	30°C
		∞	5	5	4	4	3	3	2	2	2	25°C
		∞	7	7	6	5	5	4	3	3	3	20°C
	Level 5a	∞	2	1	1	1	1	1	1	1	1	30°C
		∞	3	2	2	2	2	2	1	1	1	25°C
		∞	5	4	3	3	3	2	2	2	2	20°C
Body 2.1 mm ≤ Thickness <3.1 mm including PLCCs (rectangular) 18-32 pins SOICs (wide body) SOICs ≥20 pins, PQFPs ≤80 pins	Level 2a	∞	∞	∞	∞	86	39	28	4	3	2	30°C
		∞	∞	∞	∞	148	51	37	6	4	3	25°C
		∞	∞	∞	∞	∞	69	49	8	5	4	20°C
	Level 3	∞	∞	19	12	9	8	7	3	2	2	30°C
		∞	∞	25	15	12	10	9	5	3	3	25°C
		∞	∞	32	19	15	13	12	7	5	4	20°C
	Level 4	∞	7	5	4	4	3	3	2	2	1	30°C
		∞	9	7	5	5	4	4	3	2	2	25°C
		∞	11	9	7	6	6	5	4	3	3	20°C
	Level 5	∞	4	3	3	2	2	2	1	1	1	30°C
		∞	5	4	3	3	3	3	2	1	1	25°C
		∞	6	5	5	4	4	4	3	3	2	20°C
	Level 5a	∞	2	1	1	1	1	1	1	0.5	0.5	30°C
		∞	2	2	2	2	2	2	1	1	1	25°C
		∞	3	2	2	2	2	2	2	2	1	20°C
Body Thickness <2.1 mm including SOICs <18 pins All TQFPs, TSOPs or all BGAs <1 mm body thickness	Level 2a	∞	∞	∞	∞	∞	∞	28	1	1	1	30°C
		∞	∞	∞	∞	∞	∞	∞	2	1	1	25°C
		∞	∞	∞	∞	∞	∞	∞	2	2	1	20°C
	Level 3	∞	∞	∞	∞	∞	11	7	1	1	1	30°C
		∞	∞	∞	∞	∞	14	10	2	1	1	25°C
		∞	∞	∞	∞	∞	20	13	2	2	1	20°C
	Level 4	∞	∞	∞	9	5	4	3	1	1	1	30°C
		∞	∞	∞	12	7	5	4	2	1	1	25°C
		∞	∞	∞	17	9	7	6	2	2	1	20°C
	Level 5	∞	∞	13	5	3	2	2	1	1	1	30°C
		∞	∞	18	6	4	3	3	2	1	1	25°C
		∞	∞	26	8	6	5	4	2	2	1	20°C
	Level 5a	∞	10	3	2	1	1	1	1	1	0.5	30°C
		∞	13	5	3	2	2	2	1	1	1	25°C
		∞	18	6	4	3	2	2	2	2	1	20°C

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